Data Book
Volume 1

Linear Circuits
Operational Amplifiers

1992

Suggested Retail Price: $17.95

TEXAS INSTRUMENTS

Linear Circuits
Operational Amplifiers

Data Book
Volume 1

1992

Linear Products

Linear Products Quick Reference Guide

	Data Book	Contents	Document No.
•	Optoelectronics and Image Sensors	Optocouplers CCD Image Sensors and Support Phototransistors IR-Emitting Diodes Hybrid Displays	SOYD002A, 1990
•	Speech System Manuals	TSP50C4X Family	SPSS010, 1990
		TSP50C10/11 Synthesizer	SPSS011, 1990
		TSP53C30 Synthesizer	SPSV006, 1991
•	Interface Circuits	Data Transmission and Control Circuits, Peripheral Drivers/Power Actuators, Display Drivers	SLYD006, 1991
•	Telecommunications Circuits	Transmission, Switching, Subscriber, Transient Suppressors	SCTD001B, 1991
•	Linear and Interface Circuits Applications	Op Amps/Comparators, Video Amps, VRegs, Power Supply Design, Timers, Display Drivers, Datran, Peripheral Drivers, Data Acq., Special Functions	SLYA005, 1991
•	Mass Storage ICs Designer's Reference Guide	Disk Drivers: Read/Write, Servo/System Control, Interface/Linear, Digital ASIC, LinASIC™, Applications	SSCA001, 1992
•	Macromodel Data Manual	Level I: Operational Amplifiers, Voltage Comparators, Building Blocks Level II: Selected Operational Amplifiers, Buildilng Blocks	SLOS047B, 1992

January 1992

Linear Circuits
Data Book
1992

Volume 1
Operational Amplifiers

TEXAS
INSTRUMENTS

IMPORTANT NOTICE

Texas Instruments (TI) reserves the right to make changes to or to discontinue any semiconductor product or service identified in this publication without notice. TI advises its customers to obtain the latest version of the relevant information to verify, before placing orders, that the information being relied upon is current.

TI warrants performance of its semiconductor products to current specifications in accordance with TI's standard warranty. Testing and other quality control techniques are utilized to the extent TI deems necessary to support this warranty. Unless mandated by government requirements, specific testing of all parameters of each device is not necessarily performed.

TI assumes no liability for TI applications assistance, customer product design, software performance, or infringement of patents or services described herein. Nor does TI warrant or represent that license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right of TI covering or relating to any combination, machine, or process in which such semiconductor products or services might be or are used.

Texas Instruments products are not intended for use in life-support appliances, devices, or systems. Use of a TI product in such applications without the written consent of the appropriate TI officer is prohibited.

Printed in the U.S.A.

INTRODUCTION

Texas Instruments offers an extensive line of industry-standard and leadership products dedicated to Operational Amplifier functions. The technologies represented in this book include traditional bipolar through BIDFET, BIFET, IMPACT™, LinCMOS™, Advanced LinCMOS™, and Excalibur processes. The IMPACT™, Advanced LinCMOS™, and Excalibur technologies feature a step-function improvement in impedance, speed, power requirements, and threshold stability.

This data book (Volume 1 of 3) provides information on the extensive listing of Texas Instruments Operational Amplifier products.

- Commercial, Industrial, Automotive, and Military Temperature Ranges
- Noncompensated, Single, Dual
- Internally Compensated, Single, Dual, Quad
- Precision, Chopper-Stabilized
- Excalibur: High-Speed, Low-Power, Precision, JFET Input, μPower, High Output, Low Noise
- Precision virtual ground

EXCALIBUR PROCESS DISCUSSION: TLE2425

The TI complementary bipolar process (Excalibur) has several key components, which yield the high performance of the TLE2425 Virtual Ground. Excalibur is a 44-V n-epi bipolar process that includes isolated high-speed PNPs, metal-nitride-poly capacitors, p-channel JFETs, as well as the common bipolar devices. In other bipolar processes, the capacitors have one plate made from the silicon substrate (bottom) and the other from metal. At low levels of operating current, the leakage current from the silicon bottom plate can significantly impact the dc performance of the circuits. The ac performance is also effected by the parasitic substrate capacitance. Use of the poly-nitride-metal capacitor significantly reduces these effects, yielding higher ac performance and stable bias currents. Precision p-channel JFETs are used in the current reference circuit to generate a temperature stable micropower current source. Since this current source is used throughout the circuit, parametric performance stability is improved over the operating temperature range. Single-supply circuits frequently are performance limited by the ac characteristics of the PNP transistors. Using high-speed PNP transistors in the signal path of the amplifier permits the TLE2425 to have a three-to-five times higher bandwidth. This translates into improved load regulation and line regulation over frequency. The capacitors, JFETs, and isolated PNP transistors all work together to provide a high-performance virtual ground in a small package at low cost. This could not be accomplished with other process technologies.

FEATURES IN THIS BOOK

- New Excalibur process devices
- Selected Macromodel programs (Level I)
- Expanded product characterization over supply voltage and temperature
- Extensive graphs showing the characterization
- New space-saving packages, 3-to-20 leads, TSSOP and SOT-89

The alphanumeric listing in this data book includes all devices contained in Volumes 1, 2, and 3. Products in this book are shown in **BOLD** type. Thus, the reader can easily find the particular volume for a given device. Also included are those new products added to this volume as indicated by a dagger(†). The selection guide includes a functional description of each device by providing key parametric information and packaging options. Ordering information and mechanical data are in the last section of the book.

Complete technical data for all TI semiconductor products are available from your nearest TI Field Sales Office, local authorized TI distributor, or by writing directly to:

Texas Instruments Incorporated
LITERATURE RESPONSE CENTER
P.O. BOx 809066
Dallas, Texas 75380-9066

We sincerely feel that this new 1992 Linear Circuits Data Book, Volume 1, will be a significant addition to your technical literature from Texas Instruments.

Contents

†New devices added to this volume.

ALPHANUMERIC INDEX

---

†New devices added to this volume.

†New devices added to this volume.

ALPHANUMERIC INDEX

---

†New devices added to this volume.

noncompensated, single

commercial temperature range

(values specified for T_A = 25°C)

DESCRIPTION	SUPPLY VOLTAGE (V)		V_{IO} (mV)	I_{IB} (nA)	A_{VD} (V/mV)	B_1 (MHz)	SR (V/µs)	TYPE	PACKAGES	PAGE NO.
	MIN	MAX	MAX	MAX	MIN	TYP	TYP			
High Performance	± 5	± 18	7.5	250	15	1	7.5	LM301A	D,P	2–13
High Performance	± 2	± 18	7.5	2	25	1	0.3	LM308	D,P	2–23
High Performance	± 2	± 18	0.5	2	80	1	0.3	LM308A	D,P	2–23
BIFET, Low Noise	± 3.5	± 18	10	0.2	25	3	13	TL070C	D,P	2–371
BIFET, General Purpose	± 3.5	± 18	15	0.4	25	3	13	TL080C	D,P	2–387

industrial temperature range

(values specified for T_A = 25°C)

DESCRIPTION	SUPPLY VOLTAGE (V)		V_{IO} (mV)	I_{IB} (nA)	A_{VD} (V/mV)	B_1 (MHz)	SR (V/µs)	TYPE	PACKAGES	PAGE NO.
	MIN	MAX	MAX	MAX	MIN	TYP	TYP			
High Performance, Bipolar	± 5	± 22	2	75	50	1	0.5	LM201A	D,P	2–13

military temperature range

(values specified for T_A = 25°C)

DESCRIPTION	SUPPLY VOLTAGE (V)		V_{IO} (mV)	I_{IB} (nA)	A_{VD} (V/mV)	B_1 (MHz)	SR (V/µs)	TYPE	PACKAGES	PAGE NO.
	MIN	MAX	MAX	MAX	MIN	TYP	TYP			
High Performance, Bipolar	± 5	± 22	2	75	50	1	0.5	LM101A	FK,JG,U,W	2–13
High Performance, Low Bias Current, Bipolar	± 2	± 20	2	2	50	1	0.3	LM108	JG	2–23
High Performance, Low Bias Current, Bipolar	± 2	± 20	0.5	2	80	1	0.3	LM108A	JG	2–23
General Purpose, Precision Input, Bipolar	± 9	± 18	2	200	Typ 45	1	0.3	uA709AM	J,JG,U,W	2–1301
General Purpose, Bipolar	± 9	± 18	5	500	Typ 45	1	0.3	uA709M	J,JG,U,W	2–1301
General Purpose, Bipolar	± 2	± 22	5	500	50	1	0.5	uA748M	JG,U	2–1319

decompensated, single

commercial temperature range

(values specified for T_A = 25°C)

DESCRIPTION	SUPPLY VOLTAGE (V)		V_{IO} (mV)	I_{IB} (nA)	A_{VD} (V/mV)	GBW‡ (MHz)	SR (V/μs)	TYPE	PACKAGES†	PAGE NO.
	MIN	MAX	MAX	MAX	MIN	TYP	TYP			
Excalibur, Low Noise, High Speed, Precision	± 4	± 22	0.025	90	10000	76	7.5	TLE2037AC	D,P	2–1015
Excalibur, Low Noise, High Speed, Precision	± 4	± 22	0.1	90	5000	76	7.5	TLE2037C	D,P,Y	2–1015
Excalibur, JFET-Input, High-Output Drive, μPower	± 3.5	± 20	1.5	Typ 0.004	30	6.4	10	TLE2161AC	D,P	2–1255
Excalibur, JFET-Input, High-Output Drive, μPower	± 3.5	± 20	0.5	Typ 0.004	30	6.4	10	TLE2161BC	D,P	2–1255
Excalibur, JFET-Input, High-Output Drive, μPower	± 3.5	± 20	3	Typ 0.004	30	6.4	10	TLE2161C	D,P	2–1255

† Y is chip form.

industrial temperature range

(values specified for T_A = 25°C)

DESCRIPTION	SUPPLY VOLTAGE (V)		V_{IO} (mV)	I_{IB} (nA)	A_{VD} (V/mV)	GBW‡ (MHz)	SR (V/μs)	TYPE	PACKAGES	PAGE NO.
	MIN	MAX	MAX	MAX	MIN	TYP	TYP			
Excalibur, Low Noise, High Speed, Precision	± 4	± 22	0.025	90	10000	76	7.5	TLE2037AI	D,P	2–1015
Excalibur, Low Noise, High Speed, Precision	± 4	± 22	0.1	90	5000	76	7.5	TLE2037I	D,P	2–1015
Excalibur, JFET-Input, High-Output Drive, μPower	± 3.5	± 20	1.5	Typ 0.004	30	6.4	10	TLE2161AI	D,P	2–1255
Excalibur, JFET-Input, High-Output Drive, μPower	± 3.5	± 20	0.5	Typ 0.004	30	6.4	10	TLE2161BI	D,P	2–1255
Excalibur, JFET-Input, High-Output Drive, μPower	± 3.5	± 20	3	Typ 0.004	30	6.4	10	TLE2161I	D,P	2–1255

military temperature range

(values specified for T_A = 25°C)

DESCRIPTION	SUPPLY VOLTAGE (V)		V_{IO} (mV)	I_{IB} (nA)	A_{VD} (V/mV)	GBW‡ (MHz)	SR (V/μs)	TYPE	PACKAGES	PAGE NO.
	MIN	MAX	MAX	MAX	MIN	TYP	TYP			
Excalibur, Low Noise, High Speed, Precision	± 4	± 22	0.025	90	10000	76	7.5	TLE2037AM	D,FK,JG,P	2–1015
Excalibur, Low Noise, High Speed, Precision	± 4	± 22	0.1	90	5000	76	7.5	TLE2037M	D,FK,JG,P	2–1015
Excalibur, JFET-Input, High-Output Drive, μPower	± 3.5	± 20	1.5	Typ 0.004	30	6.4	10	TLE2161AM	D,FK,JG,P	2–1255
Excalibur, JFET-Input, High-Output Drive, μPower	± 3.5	± 20	0.5	Typ 0.004	30	6.4	10	TLE2161BM	JG,P	2–1255
Excalibur, JFET-Input, High-Output Drive, μPower	± 3.5	± 20	3	Typ 0.004	30	6.4	10	TLE2161M	D,FK,JG,P	2–1255

‡ Decompensated op amps are not unity-gain stable. Gain bandwidth product is specified with A_{CL} = 5.

internally compensated, single

commercial temperature range

(values specified for $T_A = 25°C$)

DESCRIPTION	SUPPLY VOLTAGE (V)		V_{IO} (mV)	I_{IB} (nA)	A_{VD} (V/mV)	B_1 (MHz)	SR (V/µs)	TYPE	PACKAGES	PAGE NO.
	MIN	MAX	MAX	MAX	MIN	TYP	TYP			
BIFET	± 3.5	± 18	10	0.2	25	3	13	LF351	D,P	2–5
BIFET	± 3.5	± 18	2	0.2	25	3	13	LF411C	D,P	2–9
High Performance	± 2	± 18	7.5	250	25	1	0.5	LM307	D,N,P,W	2–19
High Performance	± 5	± 20	10	250	25	15	70	LM318	D,P	2–35
Low Noise, High Speed, Precision Input	± 2.5	± 22	0.025	35	7000	8	1.7	LT1007AC	P	2–69
Low Noise, High Speed, Precision Input	± 2.5	± 22	0.060	55	5000	8	1.7	LT1007C	P	2–69
Low Noise, High Speed, Noncompensated, $A_{VL} \geq 5$	± 2.5	± 22	0.025	35	7000	60	15	LT1037AC	P	2–69
Low Noise, High Speed, Noncompensated, $A_{VL} \geq 5$	± 2.5	± 22	0.060	55	5000	60	15	LT1037C	P	2–69
Low Noise, High Performance	± 3	± 22	4	1500	25	10	13	NE5534	D,P	2–135
Low Noise, High Performance	± 3	± 22	4	1500	25	10	13	NE5534A	D,P	2–135
Ultra-Low Offset Voltage	± 3	± 22	0.15	7	120	0.6	0.3	OP07C	D,P	2–141
Ultra-Low Offset Voltage	± 3	± 22	0.15	12	120	0.6	0.3	OP07D	D,P	2–141
BIFET, Low Power, Precision	± 3.5	± 18	0.8	0.2	5	1.1	2.9	TL031AC	D,P	2–175
BIFET, Low Power, Precision	± 3.5	± 18	1.5	0.2	5	1.1	2.9	TL031C	D,P	2–175
BIFET, Precision	± 3.5	± 18	0.8	0.2	50	3.1	20	TL051AC	D,P	2–257
BIFET, Precision	± 3.5	± 18	1.5	0.2	50	3.1	20	TL051C	D,P	2–257
BIFET, Low Power	± 3.5	± 18	6	0.2	4	1	3.5	TL061AC	D,P	2–341
BIFET, Low Power	± 3.5	± 18	3	0.2	4	1	3.5	TL061BC	D,P	2–341
BIFET, Low Power	± 3.5	± 18	15	0.2	3	1	3.5	TL061C	D,P	2–341
BIFET, Adjustable, Low Power	± 1.2	± 18	6	0.2	4	1	3.5	TL066AC	D,P	2–357
BIFET, Adjustable, Low Power	± 1.2	± 18	3	0.2	4	1	3.5	TL066BC	D,P	2–357
BIFET, Adjustable, Low Power	± 1.2	± 18	15	0.4	3	1	3.5	TL066C	D,P	2–357
BIFET, Low Noise	± 3.5	± 18	6	0.2	50	3	13	TL071AC	D,P	2–371
BIFET, Low Noise	± 3.5	± 18	3	0.2	50	3	13	TL071BC	D,P	2–371
BIFET, Low Noise	± 3.5	± 18	10	0.2	25	3	13	TL071C	D,P	2–371
BIFET, General Purpose	± 3.5	± 18	6	0.2	50	3	13	TL081AC	D,P	2–387
BIFET, General Purpose	± 3.5	± 18	3	0.2	50	3	13	TL081BC	D,P	2–387
BIFET, General Purpose	± 3.5	± 18	15	0.4	25	3	13	TL081C	D,P	2–387
BIFET, Low V_{IO}	± 3.5	± 18	0.5	0.2	50	3	13	TL087C	D,P	2–401
BIFET, Low V_{IO}	± 3.5	± 18	1	0.2	50	3	13	TL088C	D,P	2–401
High-Slew Rate, Single Supply	± 2	± 22	5	1500	25	4.5	10	TL34071	D,P	2–443

internally compensated, single (continued)

commercial temperature range **(values specified for T_A = 25°C)**

DESCRIPTION	SUPPLY VOLTAGE (V)		V_{IO} (mV)	I_{IB} (nA)	A_{VD} (V/mV)	B_1 (MHz)	SR (V/µs)	TYPE	PACKAGES†	PAGE NO.
	MIN	MAX	MAX	MAX	MIN	TYP	TYP			
LinCMOS, Programmable, Low Bias	1.4	18	5	Typ 0.001	30	0.1	0.04	TLC251AC	D,P	2–449
LinCMOS, Programmable, Medium Bias	1.4	18	5	Typ 0.001	20	0.7	0.6	TLC251AC	D,P	2–449
LinCMOS, Programmable, High Bias	1.4	18	5	Typ 0.001	10	2.3	4.5	TLC251AC	D,P	2–449
LinCMOS, Programmable, Low Bias	1.4	18	2	Typ 0.001	30	0.1	0.04	TLC251BC	D,P	2–449
LinCMOS, Programmable, Medium Bias	1.4	18	2	Typ 0.001	20	0.7	0.6	TLC251BC	D,P	2–449
LinCMOS, Programmable, High Bias	1.4	18	2	Typ 0.001	10	2.3	4.5	TLC251BC	D,P	2–449
LinCMOS, Programmable, Low Bias	1.4	18	10	Typ 0.001	30	0.1	0.04	TLC251C	D,P,Y	2–449
LinCMOS, Programmable, Medium Bias	1.4	18	10	Typ 0.001	20	0.7	0.6	TLC251C	D,P,Y	2–449
LinCMOS, Programmable, High Bias	1.4	18	10	Typ 0.001	10	2.3	4.5	TLC251C	D,P,Y	2–449
LinCMOS, Programmable, Low Bias	3	18	5	Typ 0.007	50	0.11	0.04	TLC271AC	D,P	2–507
LinCMOS, Programmable, Medium Bias	3	18	5	Typ 0.007	25	0.64	0.56	TLC271AC	D,P	2–507
LinCMOS, Programmable, High Bias	3	18	5	Typ 0.007	10	2.2	4.6	TLC271AC	D,P	2–507
LinCMOS, Programmable, Low Bias	3	18	2	Typ 0.007	50	0.11	0.04	TLC271BC	D,P	2–507
LinCMOS, Programmable, Medium Bias	3	18	2	Typ 0.007	25	0.64	0.56	TLC271BC	D,P	2–507
LinCMOS, Programmable, High Bias	3	18	2	Typ 0.007	10	2.2	4.6	TLC271BC	D,P	2–507
LinCMOS, Programmable, Low Bias	3	18	10	Typ 0.007	50	0.11	0.04	TLC271C	D,P	2–507
LinCMOS, Programmable, Medium Bias	3	18	10	Typ 0.007	25	0.64	0.56	TLC271C	D,P	2–507
LinCMOS, Programmable, High Bias	3	18	10	Typ 0.007	10	2.2	4.6	TLC271C	D,P	2–507
LinCMOS, Precision, Low Noise	4.6	16	0.2	Typ 0.001	400	1.9	2.7	TLC2201AC	D,P	2–785
LinCMOS, Precision, Low Noise, 100% Noise Tested	4.6	16	0.2	Typ 0.001	400	1.9	2.7	TLC2201BC	D,P	2–785
LinCMOS, Precision, Low Noise	4.6	16	0.5	Typ 0.001	400	1.9	2.7	TLC2201C	D,P,Y	2–785
LinCMOS, Precision, Chopper-Stabilized	3.8	16	0.001	Typ 0.004	5600	1.9	2.8	TLC2652AC	D,N,P	2–861

† Y is chip form.

internally compensated, single (continued)

commercial temperature range

(values specified for $T_A = 25°C$)

DESCRIPTION	SUPPLY VOLTAGE (V)		V_{IO} (mV)	I_{IB} (nA)	A_{VD} (V/mV)	B_1 (MHz)	SR (V/µs)	TYPE	PACKAGES†	PAGE NO.
	MIN	MAX	MAX	MAX	MIN	TYP	TYP			
LinCMOS, Precision, Chopper-Stabilized	3.8	16	0.003	Typ 0.004	1000	1.9	2.8	TLC2652C	D,N,P,Y	2–861
LinCMOS, Low Noise, Precision, Chopper-Stabilized	4.6	16	0.01	Typ 0.05	5600	1.9	2	TLC2654AC	D,N,P	2–885
LinCMOS, Low Noise, Precision, Chopper-Stabilized	4.6	16	0.02	Typ 0.05	1000	1.9	2	TLC2654C	D,N,P,Y	2–885
Excalibur, High Speed, Low Power, Precision	4	40	0.2	Typ 25	1000	2	0.65	TLE2021AC	D,P	2–909
Excalibur, High Speed, Low Power, Precision	4	40	0.1	Typ 25	1000	2	0.65	TLE2021BC	D,P	2–909
Excalibur, High Speed, Low Power, Precision	4	40	0.5	25	1000	2	0.9	TLE2021C	D,P,Y	2–909
Excalibur, Low Noise, High Speed, Precision	± 4	± 22	0.025	Typ 15	8000	13	2.8	TLE2027AC	D,P	2–991
Excalibur, Low Noise, High Speed, Precision	± 4	± 22	0.1	Typ 15	3500	13	2.8	TLE2027C	D,P,Y	2–991
Excalibur, JFET-Input, High-Output Drive, µPower	± 3.5	± 20	1.5	Typ 0.004	30	2	3.4	TLE2061AC	D,P	2–1039
Excalibur, JFET-Input, High-Output Drive, µPower	± 3.5	± 20	0.5	Typ 0.004	30	2	3.4	TLE2061BC	D,P	2–1039
Excalibur, JFET-Input, High-Output Drive, µPower	± 3.5	± 20	3	Typ 0.004	30	2	3.4	TLE2061C	D,P,Y	2–1039
Excalibur, Low Noise, High Speed, Precision	± 2	± 22	0.5	–700	100	6	45	TLE2141AC	D,P	2–1181
Excalibur, Low Noise, High Speed, Precision	± 2	± 22	0.9	–700	100	6	45	TLE2141C	D,P,Y	2–1181
General Purpose	± 2	± 18	6	500	20	1	0.5	uA741C	D,P	2–1305

† Y is chip form.

internally compensated, single (continued)

industrial temperature range

(values specified for T_A = 25°C)

DESCRIPTION	SUPPLY VOLTAGE (V)		V_{IO} (mV)	I_{IB} (nA)	A_{VD} (V/mV)	B_1 (MHz)	SR (V/µs)	TYPE	PACKAGES	PAGE NO.
	MIN	MAX	MAX	MAX	MIN	TYP	TYP			
Chopper-Stabilized	± 1.9	± 8	0.005	0.03	1000	1.2	4	LTC1052C	D,P	2–117
Low Noise, High Speed	± 3.5	± 22	0.025	40	1000	8	2.8	OP27E	P	2–149
Low Noise, High Speed	± 3.5	± 22	0.1	80	700	8	2.8	OP27G	P	2–149
Low Noise, High Speed, Bipolar, Noncompensated, $A_{VL} \geq 5$	± 4	± 22	0.025	40	1000	40	17	OP37E	P	2–149
Low Noise, High Speed, Bipolar, Noncompensated, $A_{VL} \geq 5$	± 4	± 22	0.1	80	700	40	17	OP37G	P	2–149
BIFET, Low Power, Precision	± 3.5	± 18	0.8	0.2	5	1.1	2.9	TL031AI	D,P	2–175
BIFET, Low Power, Precision	± 3.5	± 18	1.5	0.2	5	1.1	2.9	TL031I	D,P	2–175
BIFET, Precision	± 3.5	± 18	0.8	0.2	50	3.1	20	TL051AI	D,P	2–257
BIFET, Precision	± 3.5	± 18	1.5	0.2	50	3.1	20	TL051I	D,P	2–257
BIFET, Low Power	± 3.5	± 18	6	0.2	4	1	3.5	TL061I	D,P	2–341
BIFET, Adjustable, Low Power	± 1.2	± 18	6	0.2	4	1	3.5	TL066I	D,P	2–357
BIFET, Low Noise	± 3.5	± 18	6	0.2	50	3	13	TL071I	D,P	2–371
BIFET, General Purpose	± 3.5	± 18	6	0.2	50	3	13	TL081I	D,P	2–387
BIFET, Low Offset Voltage	± 3.5	± 18	0.5	0.2	50	3	13	TL087I	D,P	2–401
BIFET, Low Offset Voltage	± 3.5	± 18	1	0.2	50	3	13	TL088I	D,P	2–401
High-Slew Rate, Single Supply	± 2	± 22	5	1500	25	4.5	10	TL33071	D,P	2–442
LinCMOS, Programmable, Low Bias	4	18	5	Typ 0.007	50	0.11	0.04	TLC271AI	D,P	2–507
LinCMOS, Programmable, Medium Bias	4	18	5	Typ 0.007	25	0.64	0.56	TLC271AI	D,P	2–507
LinCMOS, Programmable, High Bias	4	18	5	Typ 0.007	10	2.2	4.6	TLC271AI	D,P	2–507
LinCMOS, Programmable, Low Bias	4	18	2	Typ 0.007	50	0.11	0.04	TLC271BI	D,P	2–507
LinCMOS, Programmable, Medium Bias	4	18	2	Typ 0.007	25	0.64	0.56	TLC271BI	D,P	2–507
LinCMOS, Programmable, High Bias	4	18	2	Typ 0.007	10	2.2	4.6	TLC271BI	D,P	2–507
LinCMOS, Programmable, Low Bias	4	18	10	Typ 0.007	50	0.11	0.04	TLC271I	D,P	2–507
LinCMOS, Programmable, Medium Bias	4	18	10	Typ 0.007	25	0.64	0.56	TLC271I	D,P	2–507
LinCMOS, Programmable, High Bias	4	18	10	Typ 0.007	10	2.2	4.6	TLC271I	D,P	2–507
LinCMOS, Precision, Low Noise	4.6	16	0.2	Typ 0.001	400	1.9	2.7	TLC2201AI	D,P	2–785
LinCMOS, Precision, Low Noise, 100% Noise Tested	4.6	16	0.2	Typ 0.001	400	1.9	2.7	TLC2201BI	D,P	2–785
LinCMOS, Precision, Low Noise	4.6	16	0.5	Typ 0.001	400	1.9	2.7	TLC2201I	D,P	2–785

internally compensated, single (continued)

industrial temperature range

(values specified for T_A = 25°C)

DESCRIPTION	SUPPLY VOLTAGE (V)		V_{IO} (mV)	I_{IB} (nA)	A_{VD} (V/mV)	B_1 (MHz)	SR (V/µs)	TYPE	PACKAGES	PAGE NO.
	MIN	MAX	MAX	MAX	MIN	TYP	TYP			
LinCMOS, Precision, Chopper-Stabilized	3.8	16	0.001	Typ 0.004	5600	1.9	2.8	TLC2652AI	D,N,P	2–861
LinCMOS, Precision, Chopper-Stabilized	3.8	16	0.003	Typ 0.004	1000	1.9	2.8	TLC2652I	D,N,P	2–861
LinCMOS, Low Noise, Precision, Chopper-Stabilized	4.6	16	0.01	Typ 0.05	5600	1.9	2	TLC2654AI	D,N,P	2–885
LinCMOS, Low Noise, Precision, Chopper-Stabilized	4.6	16	0.02	Typ 0.05	1000	1.9	2	TLC2654I	D,N,P	2–885
Excalibur, High Speed, Low Power, Precision	± 2	± 20	0.2	50	300	2	0.65	TLE2021AI	D,P	2–909
Excalibur, High Speed, Precision	4	40	0.5	25	1000	2	0.9	TLE2021I	D,P	2–909
Excalibur, Low Noise, High Speed, Precision	± 4	± 22	0.025	90	10000	13	2.8	TLE2027AI	D,P	2–991
Excalibur, Low Noise, High Speed, Precision	± 4	± 22	0.1	90	5000	13	2.8	TLE2027I	D,P	2–991
Excalibur, JFET-Input, High-Output Drive, µPower	± 3.5	± 20	1.5	Typ 0.004	30	2	3.4	TLE2061AI	D,P	2–1039
Excalibur, JFET-Input, High-Output Drive, µPower	± 3.5	± 20	0.5	Typ 0.004	30	2	3.4	TLE2061BI	D,P	2–1039
Excalibur, JFET-Input, High-Output Drive, µPower	± 3.5	± 20	3	Typ 0.004	30	2	3.4	TLE2061I	D,P	2–1039
Excalibur, Low Noise, High Speed, Precision	± 2	± 22	0.05	–1500	100	6	45	TLE2141AI	D,P	2–1181
Excalibur, Low Noise, High Speed, Precision	± 2	± 22	0.9	–1500	100	6	45	TLE2141I	D,P	2–1181
General Purpose	± 2	± 22	5	500	50	1	0.5	uA741I	D,P	2–1305

OPERATIONAL AMPLIFIERS SELECTION GUIDE

internally compensated, single (continued)

automotive temperature range

(values specified for T_A = 25°C)

DESCRIPTION	SUPPLY VOLTAGE (V)		V_{IO} (mV)	I_{IB} (nA)	A_{VD} (V/mV)	B_1 (MHz)	SR (V/μs)	TYPE	PACKAGES	PAGE NO.
	MIN	MAX	MAX	MAX	MIN	TYP	TYP			
High Performance	± 5	± 22	2	75	50	1	0.5	LM207	D,N,P,W	2–19
High Perormance	± 5	± 20	4	250	50	15	70	LM218	D,P	2–35
Chopper-Stabilized	± 1.9	± 8	0.005	0.03	1000	1.2	4	LTC1052C	J,N,P	2–117
Low Noise, High Speed	± 3.5	± 22	0.025	40	1000	8	2.8	OP27E	P	2–149
Low Noise, High Speed	± 3.5	± 22	0.1	80	700	8	2.8	OP27G	P	2–149
Low Noise, High Speed Noncompensated, $A_{VL} \geq 5$	± 4	± 22	0.025	40	1000	40	17	OP37E	P	2–149
Low Noise, High Speed Noncompensated, $A_{VL} \geq 5$	± 4	± 22	0.1	80	700	40	17	OP37G	P	2–149
BIFET, Low Power, Precision	± 3.5	± 18	0.8	0.2	5	1.1	2.9	TL031AI	D,P	2–175
BIFET, Low Power, Precision	± 3.5	± 18	1.5	0.2	5	1.1	2.9	TL031I	D,P	2–175
BIFET, Precision	± 3.5	± 18	0.8	0.2	50	3.1	20	TL051AI	D,P	2–257
BIFET, Precision	± 3.5	± 18	1.5	0.2	50	3.1	20	TL051I	D,P	2–257
BIFET, Low Power	± 3.5	± 18	6	0.2	4	1	3.5	TL061I	D,P	2–341
BIFET, Adjustable, Low Power	± 1.2	± 18	6	0.2	4	1	3.5	TL066I	D,P	2–357
BIFET, Low Noise	± 3.5	± 18	6	0.2	50	3	13	TL071I	D,P	2–371
BIFET, General Purpose	± 3.5	± 18	6	0.2	50	3	13	TL081I	D,P	2–387
BIFET, Low Offset Voltage	± 3.5	± 18	0.5	0.2	50	3	13	TL087I	D,P	2–401
BIFET, Low Offset Voltage	± 3.5	± 18	1	0.2	50	3	13	TL088I	D,P	2–401
LinCMOS, Programmable, Low Bias	4	18	5	Typ 0.007	50	0.11	0.04	TLC271AI	D,P	2–507
LinCMOS, Programmable, Medium Bias	4	18	5	Typ 0.007	25	0.64	0.56	TLC271AI	D,P	2–507
LinCMOS, Programmable, High Bias	4	18	5	Typ 0.007	10	2.2	4.6	TLC271AI	D,P	2–507
LinCMOS, Programmable, Low Bias	4	18	2	Typ 0.007	50	0.11	0.04	TLC271BI	D,P	2–507
LinCMOS, Programmable, Medium Bias	4	18	2	Typ 0.007	25	0.64	0.56	TLC271BI	D,P	2–507
LinCMOS, Programmable, High Bias	4	18	2	Typ 0.007	10	2.2	4.6	TLC271BI	D,P	2–507
LinCMOS, Programmable, Low Bias	4	18	10	Typ 0.007	50	0.11	0.04	TLC271I	D,P	2–507
LinCMOS, Programmable, Medium Bias	4	18	10	Typ 0.007	25	0.64	0.56	TLC271I	D,P	2–507
LinCMOS, Programmable, High Bias	4	18	10	Typ 0.007	10	2.2	4.6	TLC271I	D,P	2–507
LinCMOS, Low Noise Precision	4.6	16	0.2	Typ 0.001	400	1.9	2.7	TLC2201AI	D,P	2–785

internally compensated, single (continued)

automotive temperature range

(values specified for $T_A = 25°C$)

DESCRIPTION	SUPPLY VOLTAGE (V)		V_{IO} (mV)	I_{IB} (nA)	A_{VD} (V/mV)	B_1 (MHz)	SR (V/μs)	TYPE	PACKAGES	PAGE NO.
	MIN	MAX	MAX	MAX	MIN	TYP	TYP			
LinCMOS, Low Noise, Precision, 100% Noise Tested	4.6	16	0.2	Typ 0.001	400	1.9	2.7	TLC2201BI	D,P	2–785
LinCMOS, Low Noise, Precision	4.6	16	0.5	Typ 0.001	400	1.9	2.7	TLC2201I	D,P	2–785
LinCMOS, Precision, Chopper Stabilized	3.8	16	0.001	Typ 0.004	5600	1.9	2.8	TLC2652AI	D,N,P	2–861
LinCMOS, Precision, Chopper Stabilized	3.8	16	0.003	Typ 0.004	1000	1.9	2.8	TLC2652I	D,N,P	2–861
LinCMOS, Low Noise, Precision, Chopper Stabilized	4.6	16	0.01	Typ 0.05	5600	1.9	2	TLC2654AI	D,N,P	2–885
LinCMOS, Low Noise, Precision, Chopper Stabilized	4.6	16	0.02	Typ 0.05	1000	1.9	2	TLC2654I	D,N,P	2–885
Excalibur, High Speed, Precision	4	40	0.5	25	1000	2	0.9	TLE2021I	D,P	2–909

internally compensated, single (continued)

military temperature range (values specified for T_A = 25°C)

DESCRIPTION	SUPPLY VOLTAGE (V)		V_{IO} (mV)	I_{IB} (nA)	A_{VD} (V/mV)	B_1 (MHz)	SR (V/μs)	TYPE	PACKAGES	PAGE NO.
	MIN	MAX	MAX	MAX	MIN	TYP	TYP			
High Performance	± 5	± 20	2	75	50	1	0.5	LM107	J,JG,U,W	2–19
Low Noise, High Speed, Precision Input	± 2.5	± 22	0.025	35	7000	8	2.5	LT1007AM	JG	2–69
Low Noise, High Speed, Precision Input	± 2.5	± 22	0.060	55	5000	8	2.5	LT1007M	JG,P	2–69
Low Noise, High Speed, Noncompensated, $A_{VL} \geq 5$	± 2.5	± 22	0.025	35	7000	60	15	LT1037AM	JG	2–69
Low Noise, High Speed, Noncompensated, $A_{VL} \geq 5$	± 2.5	± 22	0.060	55	5000	60	15	LT1037M	JG	2–69
Chopper-Stabilized	± 1.9	± 8	0.005	0.03	1000	1.2	4	LTC1052M	J,JG	2–117
Low Noise, High Speed	± 3.5	± 22	0.025	40	1000	8	2.8	OP27A	JG	2–149
Low Noise, High Speed	± 3.5	± 22	0.1	80	700	8	2.8	OP27C	JG	2–149
Low Noise, High Speed, Noncompensated, $A_{VL} \geq 5$	± 4	± 22	0.025	40	1000	40	17	OP37A	JG	2–149
Low Noise, High Speed, Noncompensated, $A_{VL} \geq 5$	± 4	± 22	0.1	80	700	40	17	OP37C	JG	2–149
Low Noise, High Performance	± 3	± 22	2	800	50	10	13	SE5534	FK,JG	2–135
Low Noise, High Performance	± 3	± 22	2	800	50	10	13	SE5534A	FK,JG	2–135
BIFET, Low Power, Precision	± 3.5	± 18	0.8	0.2	5	1.1	2.9	TL031AM	FK,JG	2–175
BIFET, Low Power, Precision	± 3.5	± 18	1.5	0.2	5	1.1	2.9	TL031M	FK,JG	2–175
BIFET, Precision	± 3.5	± 18	0.8	0.2	50	3.1	20	TL051AM	FK,JG	2–257
BIFET, Precision	± 3.5	± 18	1.5	0.2	50	3.1	20	TL051M	FK,JG	2–257
BIFET, Low Power	± 1.5	± 18	6	0.2	4	1	3.5	TL061M	FK,JG,U	2–341
BIFET, Adjustable, Low Power	± 1.2	± 18	6	0.2	4	1	3.5	TL066M	FK,JG	2–357
BIFET, Low Noise	± 3.5	± 18	6	0.2	35	3	13	TL071M	FK,JG	2–371
BIFET, General Purpose	± 3.5	± 18	6	0.2	25	3	13	TL081M	FK,JG	2–387
BIFET, Low V_{IO}	± 3.5	± 18	3	0.4	50	3	13	TL088M	JG,U	2–387
High-Slew Rate, Single Supply	± 2	± 22	5	–1500	25	4.5	10	TL35071	D,P	2–443
LinCMOS, Programmable, Low Bias	4	18	10	Typ 0.007	50	0.11	0.04	TLC271M	FK,JG	2–507
LinCMOS, Programmable, Medium Bias	4	18	10	Typ 0.007	25	0.64	0.56	TLC271M	FK,JG	2–507
LinCMOS, Programmable, High Bias	4	18	10	Typ 0.007	10	2.2	4.6	TLC271M	FK,JG	2–507
LinCMOS, Low Noise, Precision	4.6	16	0.2	Typ 0.001	400	1.9	2.7	TLC2201AM	D,FK,JG,P	2–785

internally compensated, single (continued)

military temperature range (values specified for $T_A = 25°C$)

DESCRIPTION	SUPPLY VOLTAGE V		V_{IO} (mV)	I_{IB} (nA)	A_{VD} (V/mV)	B_1 (MHz)	SR (V/µs)	TYPE	PACKAGES	PAGE NO.
	MIN	MAX	MAX	MAX	MIN	TYP	TYP			
LinCMOS, Low Noise, Precision, 100% Noise Tested	4.6	16	0.2	Typ 0.001	400	1.9	2.7	TLC2201BM	D,FK,JG,P	2–785
LinCMOS, Low Noise, Precision	4.6	16	0.5	Typ 0.001	400	1.9	2.7	TLC2201M	D,FK,JG,P	2–785
LinCMOS, Precision, Chopper Stabilized	3.8	16	0.001	Typ 0.004	5600	1.9	2.8	TLC2652AM	D,FK,J,JG, N,P	2–861
LinCMOS, Precision, Chopper Stabilized	3.8	16	0.003	Typ 0.004	1000	1.9	2.8	TLC2652M	D,FK,J,JG, N,P	2–861
LinCMOS, Low Noise, Precision, Chopper Stabilized	4.6	16	0.01	Typ 0.05	5600	1.9	2	TLC2654AM	D,FK,J,JG, N,P	2–885
LinCMOS, Low Noise, Precision, Chopper Stabilized	4.6	16	0.02	Typ 0.05	1000	2.2	2	TLC2654M	D,FK,J,JG, N,P	2–885
Excalibur, High Speed, Low Power, Precision	± 2	± 20	0.2	50	300	2	0.65	TLE2021AM	D,FK,JG,P	2–909
Excalibur, High Speed, Low Power, Precision	± 2	± 20	0.1	50	300	2	0.65	TLE2021BM	D,FK,JG,P	2–909
Excalibur, High Speed, Precision	4	40	0.5	25	1000	2	0.9	TLE2021M	D,FK,JG,P	2–909
Excalibur, Low Noise, High Speed, Precision	± 4	± 22	0.025	90	10 000	13	2.8	TLE2027AM	D,FK,JG,P	2–991
Excalibur, Low Noise, High Speed, Precision	± 4	± 22	0.1	90	5000	13	2.8	TLE2027M	D,FK,JG,P	2–991
Excalibur, JFET-Input, High-Output Drive, µPower	± 3.5	± 20	1.5	Typ 0.004	30	2	3.4	TLE2061AM	D,FK,JG,P	2–1039
Excalibur, JFET-Input, High-Output Drive, µPower	± 3.5	± 20	0.5	Typ 0.004	30	2	3.4	TLE2061BM	JG,P	2–1039
Excalibur, JFET-Input, High-Output Drive, µPower	± 3.5	± 20	3	Typ 0.004	30	2	3.4	TLE2061M	D,FK,JG,P	2–1039
Excalibur, Low Noise, High Speed, Precision	± 2	± 22	0.5	–1500	100	6	45	TLE2141AM	D,FK,JG,P	2–1181
Excalibur, Low Noise, High Speed, Precision	± 2	± 22	0.9	–1500	100	6	45	TLE2141M	D,FK,JG,P	2–1181
General Purpose	± 2	± 22	5	500	50	1	0.5	uA741M	FK,J,JG,U	2–1305

internally compensated, dual

commercial temperature range (values specified for T_A = 25°C)

DESCRIPTION		SUPPLY VOLTAGE (V)		V_{IO} (mV)	I_{IB} (nA)	A_{VD} (V/mV)	B_1 (MHz)	SR (V/μs)	TYPE	PACKAGES†	PAGE NO.
		MIN	MAX	MAX	MAX	MIN	TYP	TYP			
BIFET, General Purpose		± 3.5	± 18	10	0.2	25	3	13	LF353	D,P	2–7
BIFET, Low Offset		± 3.5	± 18	3	0.2	25	3	13	LF412C	D,P	2–11
High Gain, Low Power, Bipolar	S/S	3	30	7	–250	25	0.6	0.2	LM358	D,P,U,Y	2–51
	D/S	± 1.5	± 15								
High Gain, Low Power, Bipolar	S/S	3	30	3	–100	25	0.6	0.2	LM358A	D,P,U	2–51
	D/S	± 1.5	± 15								
Precision		4	44	0.15	20	1500	0.8	0.4	LT1013AC	P	2–93
Precision	S/S	4	44	0.3	30	1200	0.8	0.4	LT1013C	P	2–93
	D/S	± 2	± 22	0.3	30	500	0.8	0.4	LT1013C	P	2–93
Precision	S/S	4	44	0.8	30	1200	0.8	0.4	LT1013D	D,P	2–93
	D/S	± 2	± 22	0.8	30	500	0.8	0.4	LT1013D	D,P	2–93
General Purpose		± 1.5	± 18	6	500	20	1	0.5	MC1458	D,P,U	2–121
Low Noise		± 3	± 20	4	800	25	10	9	NE5532	P	2–131
Low Noise		± 3	± 20	4	800	25	10	9	NE5532A	P	2–131
High Performance		± 4	± 18	6	500	20	3	1.7	RC4558	D,P,Y	2–163
High Performance		± 4	± 18	6	250	20	4	2	RC4559	D,P	2–169
Low Power		± 2	± 18	5	250	1	0.5	0.5	TL022C	D,P	2–171
BIFET, Low Power, Precision		± 3.5	± 18	0.8	0.2	5	1.1	2.9	TL032AC	D,P	2–202
BIFET, Low Power, Precision		± 3.5	± 18	1.5	0.2	5	1.1	2.9	TL032C	D,P	2–202
BIFET, Precision		± 3.5	± 18	1.5	0.2	50	3	16	TL052AC	D,P	2–283
BIFET, Precision		± 3.5	± 18	4	0.2	50	3	16	TL052C	D,P	2–283
BIFET, Low Power		± 3.5	± 18	6	0.2	4	1	3.5	TL062AC	D,P	2–341
BIFET, Low Power		± 3.5	± 18	3	0.2	4	1	3.5	TL062BC	D,P	2–341
BIFET, Low Power		± 3.5	± 18	15	0.4	3	1	3.5	TL062C	D,P	2–341
BIFET, Low Noise		± 3.5	± 18	6	0.2	50	3	13	TL072AC	D,P	2–371
BIFET, Low Noise		± 3.5	± 18	3	0.2	50	3	13	TL072BC	D,P	2–371
BIFET, Low Noise		± 3.5	± 18	10	0.2	25	3	13	TL072C	D,P	2–371
BIFET, General Purpose		± 3.5	± 18	6	0.2	50	3	13	TL082AC	D,P	2–387
BIFET, General Purpose		± 3.5	± 18	3	0.2	50	3	13	TL082BC	D,P	2–387
BIFET, General Purpose		± 3.5	± 18	15	0.4	25	3	13	TL082C	D,P	2–387
BIFET, General Purpose		± 3.5	± 18	0.5	2	50	3	13	TL287C	D,P	2–401
BIFET, General Purpose		± 3.5	± 18	1	0.2	50	3	13	TL288C	D,P	2–401
High-Slew Rate, Single Supply		± 2	± 22	5	– 2000	50	0.2	8	TL34072	D,P	2–443
High-Slew Rate, Single Supply		± 2	± 22	3	– 2000	50	0.2	8	TL34072A	D,P	2–443
LinCMOS, Rail-to-Rail		4.4	16	2.5	Typ 0.0001	Typ 35	2.25	3.6	TLC2272C	D,P,Y	2–841
LinCMOS, Rail-to-Rail		4.4	16	0.95	Typ 0.0001	Typ 35	2.25	3.6	TLC2272AC	D,P	2–841

† Y is chip form.

internally compensated, dual (continued)

commercial temperature range

(values specified for T_A = 25°C)

DESCRIPTION	SUPPLY VOLTAGE (V)		V_{IO} (mV)	I_{IB} (nA)	A_{VD} (V/mV)	B_1 (MHz)	SR (V/µs)	TYPE	PACKAGES†	PAGE NO.
	MIN	MAX	MAX	MAX	MIN	TYP	TYP			
LinCMOS, High Bias	1.4	18	5	Typ 0.005	10	2.2	5.3	TLC252AC	D,P	2–467
LinCMOS, High Bias	1.4	18	2	Typ 0.005	10	2.2	5.3	TLC252BC	D,P	2–467
LinCMOS, High Bias	1.4	18	10	Typ 0.005	10	2.2	5.3	TLC252C	D,P,Y	2–467
LinCMOS, Low Bias	1.4	18	2	Typ 0.005	30	0.1	0.05	TLC25L2BC	D,P	2–467
LinCMOS, Low Bias	1.4	18	10	Typ 0.005	30	0.1	0.05	TLC25L2C	D,P,Y	2–467
LinCMOS, Medium Bias	1.4	18	5	Typ 0.005	20	0.6	0.6	TLC25M2AC	D,P	2–467
LinCMOS, Medium Bias	1.4	18	2	Typ 0.005	20	0.6	0.6	TLC25M2BC	D,P	2–467
LinCMOS, Medium Bias	1.4	18	10	Typ 0.005	20	0.6	0.6	TLC25M2C	D,P,Y	2–467
LinCMOS, High Bias	3	18	5	Typ 0.005	10	2.2	5.3	TLC272AC	D,P	2–565
LinCMOS, High Bias	3	18	2	Typ 0.005	10	2.2	5.3	TLC272BC	D,P	2–565
LinCMOS, High Bias	3	18	10	Typ 0.005	10	2.2	5.3	TLC272C	D,P	2–565
LinCMOS, High Bias	3	18	0.5	Typ 0.005	10	2.2	5.3	TLC277C	D,P	2–565
LinCMOS, Low Bias	3	18	5	Typ 0.005	50	0.1	0.05	TLC27L2AC	D,P	2–629
LinCMOS, Low Bias	3	18	2	Typ 0.005	50	0.1	0.05	TLC27L2BC	D,P	2–629
LinCMOS, Low Bias	3	18	10	Typ 0.005	50	0.1	0.05	TLC27L2C	D,P	2–629
LinCMOS, Low Bias	3	18	0.5	Typ 0.005	50	0.1	0.05	TLC27L7C	D,P	2–629
LinCMOS, Medium Bias	3	18	5	Typ 0.005	25	0.6	0.6	TLC27M2AC	D,P	2–693
LinCMOS, Medium Bias	3	18	2	Typ 0.005	25	0.6	0.6	TLC27M2BC	D,P	2–693
LinCMOS, Medium Bias	3	18	10	Typ 0.005	25	0.6	0.6	TLC27M2C	D,P	2–693
LinCMOS, Medium Bias	3	18	0.5	Typ 0.005	25	0.6	0.6	TLC27M7C	D,P	2–693
LinCMOS, µPower, Precision	1.4	18	0.6	Typ 0.007	500	0.11	0.05	TLC1078C	D,P	2–757

† Y is chip form.

internally compensated, dual (continued)

commercial temperature range **(values specified for T_A = 25°C)**

DESCRIPTION	SUPPLY VOLTAGE (V)		V_{IO} (mV)	I_{IB} (nA)	A_{VD} (V/mV)	B_1 (MHz)	SR (V/µs)	TYPE	PACKAGES†	PAGE NO.
	MIN	MAX	MAX	TYP	MIN	TYP	TYP			
LinCMOS, Low Noise, Precision	4.6	16	0.5	Typ 0.005	400	1.9	1.8	TLC2202AC	D,P	2–813
LinCMOS, Low Noise, Precision	4.6	16	0.5	Typ 0.005	400	1.9	1.8	TLC2202BC	D,P	2–813
LinCMOS, Low Noise, Precision	4.6	16	1	Typ 0.005	400	1.9	1.8	TLC2202C	D,P	2–813
Excalibur, High Speed, Low Power, Precision	4	40	0.3	Typ 33	1000	2.8	0.65	TLE2022AC	D,P	2–935
Excalibur, High Speed, Low Power, Precision	4	40	0.15	Typ 30	1500	2.8	0.65	TLE2022BC	D,P	2–935
Excalibur, High Speed, Low Power, Precision	4	40	0.5	35	800	2.8	0.65	TLE2022C	D,P,Y	2–935
Excalibur, JFET-Input, High-Output Drive, µPower	± 3.5	± 20	2	Typ 0.004	30	2	3.4	TLE2062AC	D,P	2–1075
Excalibur, JFET-Input, High-Output Drive, µPower	± 3.5	± 20	1	Typ 0.004	30	2	3.4	TLE2062BC	D,P	2–1075
Excalibur, JFET-Input, High-Output Drive, µPower	± 3.5	± 20	4	Typ 0.004	30	2	3.4	TLE2062C	D,P,Y	2–1075
Excalibur, Low Noise, High Speed, Precision	± 2	± 22	1.2	− 700	100	6	45	TLE2142AC	D,P	2–1199
Excalibur, Low Noise, High Speed, Precision	± 2	± 22	0.75	− 700	100	6	45	TLE2142C	D,P,Y	2–1199
Excalibur, Low Noise, High Speed, Precision	± 4	± 22	0.1	Typ 15	3500	13	2.8	TLE2227C	D,P,Y	2–1289
General Purpose	± 5	± 22	6	500	25	1	0.5	uA747C	D,N	2–1313

† Y is chip form.

decompensated, dual

commercial temperature range **(values specified for T_A = 25°C)**

DESCRIPTION	SUPPLY VOLTAGE (V)		V_{IO} (mV)	I_{IB} (nA)	A_{VD} (V/mV)	GBW‡ (MHz)	SR (V/µs)	TYPE	PACKAGES	PAGE NO.
	MIN	MAX	MAX	TYP	MIN	TYP	TYP			
Excalibur, Low Noise, High Speed, Precision	± 4	± 22	0.1	Typ 15	5000	76	7.5	TLE2237C	D,P	2–1295

‡ Decompensated op amps are not unity-gain stable. Gain bandwidth product is specified with A_{CL} = 5.

internally compensated, dual

industrial temperature range

(values specified for T_A = 25°C)

DESCRIPTION		SUPPLY VOLTAGE (V)		V_{IO} (mV)	I_{IB} (nA)	A_{VD} (V/mV)	B_1 (MHz)	SR (V/µs)	TYPE	PACKAGES	PAGE NO.
		MIN	MAX	MAX	MAX	MIN	TYP	TYP			
High Performance, Bipolar		4	44	0.15	20	1500	0.8	0.4	LT1013AI	P	2–93
High Performance, Bipolar	S/S	4	44	0.3	30	1200	0.8	0.4	LT1013I	P	2–93
	D/S	± 2	± 22	0.3	30	500	0.8	0.4	LT1013I	P	2–93
High Performance, Bipolar	S/S	4	44	0.8	30	1200	0.8	0.4	LT1013DI	D,P	2–93
	D/S	± 2	± 22	0.8	30	500	0.8	0.4	LT1013DI	D,P	2–93
BIFET, Low Power, Precision		± 3.5	± 18	0.8	0.2	5	1.1	2.9	TL032AI	D,P	2–203
BIFET, Low Power, Precision		± 3.5	± 18	1.5	0.2	5	1.1	2.9	TL032I	D,P	2–203
BIFET, Precision		± 3.5	± 18	0.8	0.2	50	3	16	TL052AI	D,P	2–283
BIFET, Precision		± 3.5	± 18	1.5	0.2	50	3	16	TL052I	D,P	2–283
BIFET, Low Power		± 3.5	± 18	6	0.2	4	1	3.5	TL062I	D,P	2–341
BIFET, Low Noise		± 3.5	± 18	6	0.2	50	3	13	TL072I	D,P	2–371
BIFET, General Purpose		± 3.5	± 18	6	0.2	50	3	13	TL082I	D,P	2–387
BIFET, General Purpose		± 3.5	± 18	0.5	0.2	50	3	13	TL287I	D,P	2–401
BIFET, General Purpose		± 3.5	± 18	1	0.2	50	3	13	TL288I	D,P	2–401
High-Slew Rate, Single Supply		± 2	± 22	5	–2000	50	0.2	8	TL33072	D,P	2–443
High-Slew Rate, Single Supply		± 2	± 22	3	–2000	50	0.2	8	TL33072A	D,P	2–443
LinCMOS, High Bias		4	18	5	Typ 0.005	10	2.2	5.3	TLC272AI	D,P	2–565
LinCMOS, High Bias		4	18	2	Typ 0.005	10	2.2	5.3	TLC272BI	D,P	2–565
LinCMOS, High Bias		4	18	10	Typ 0.005	10	2.2	5.3	TLC272I	D,P	2–565
LinCMOS, High Bias		4	18	0.5	Typ 0.005	10	2.2	5.3	TLC277I	D,P	2–565
LinCMOS, µPower, Precision		4	18	0.6	Typ 0.007	500	0.11	0.05	TLC1078I	D,P	2–757
LinCMOS, Low Noise, Precision		4.6	16	0.5	Typ 0.005	400	1.9	1.8	TLC2202AI	D,P	2–813
LinCMOS, Low Noise, Precision		4.6	16	0.5	Typ 0.005	400	1.9	1.8	TLC2202BI	D,P	2–813
LinCMOS, Low Noise, Precision		4.6	16	1	Typ 0.005	400	1.9	1.8	TLC2202I	D,P	2–813
LinCMOS, Low Bias		4	18	5	Typ 0.005	50	0.1	0.05	TLC27L2AI	D,P	2–629
LinCMOS, Low Bias		4	18	2	Typ 0.005	50	0.1	0.05	TLC27L2BI	D,P	2–629
LinCMOS, Low Bias		4	18	10	Typ 0.005	50	0.1	0.05	TLC27L2I	D,P	2–629
LinCMOS, Low Bias		4	18	0.5	Typ 0.005	50	0.1	0.05	TLC27L7I	D,P	2–629
LinCMOS, Medium Bias		4	18	5	Typ 0.005	25	0.6	0.6	TLC27M2AI	D,P	2–693
LinCMOS, Medium Bias		4	18	2	Typ 0.005	25	0.6	0.6	TLC27M2BI	D,P	2–693
LinCMOS, Medium Bias		4	18	10	Typ 0.005	25	0.6	0.6	TLC27M2I	D,P	2–693

internally compensated, dual (continued)

industrial temperature range

(values specified for $T_A = 25°C$)

DESCRIPTION	SUPPLY VOLTAGE (V)		V_{IO} (mV)	I_{IB} (nA)	A_{VD} (V/mV)	B_1 (MHz)	SR (V/μs)	TYPE	PACKAGES	PAGE NO.
	MIN	MAX	MAX	MAX	MIN	TYP	TYP			
LinCMOS, Medium Bias	4	18	0.5	Typ 0.005	25	0.6	0.6	TLC27M7I	D,P	2–693
Excalibur, High Speed, Low Power, Precision	± 2	± 20	0.3	55	1000	2.8	0.65	TLE2022AI	D,P	2–935
Excalibur, High Speed, Precision	4	40	0.5	25	1000	2	0.9	TLE2022I	D,P	2–935
Excalibur, JFET-Input, High-Output Drive, μPower	± 3.5	± 20	2	Typ 0.004	30	2	3.4	TLE2062AI	D,P	2–1075
Excalibur, JFET-Input, High-Output Drive, μPower	± 3.5	± 20	1	Typ 0.004	30	2	3.4	TLE2062BI	D,P	2–1075
Excalibur, JFET-Input, High-Output Drive, μPower	± 3.5	± 20	4	Typ 0.004	30	2	3.4	TLE2062I	D,P	2–1075
Excalibur, Low Noise, High Speed, Precision	± 2	± 22	1.2	–1500	100	6	45	TLE2142AI	D,P	2–1199
Excalibur, Low Noise, High Speed, Precision	± 2	± 22	0.75	–1500	100	6	45	TLE2142I	D,P	2–1199

extended temperature range

(values specified for $T_A = 25°C$)

DESCRIPTION	SUPPLY VOLTAGE (V)		V_{IO} (mV)	I_{IB} (nA)	A_{VD} (V/mV)	B_1 (MHz)	SR (V/μs)	TYPE	PACKAGES†	PAGE NO.
	MIN	MAX	MAX	MAX	MIN	TYP	TYP			
General Purpose, Bipolar	± 2	± 16	7	–100	25	0.4	Min 0.15	TL2828Z	D,P,Y	2–421

† Y is chip form.

internally compensated, dual (continued)

automotive temperature range **(values specified for T_A = 25°C)**

DESCRIPTION		SUPPLY VOLTAGE (V)		V_{IO} (mV)	I_{IB} (nA)	A_{VD} (V/mV)	B_1 (MHz)	SR (V/µs)	TYPE	PACKAGES	PAGE NO.
		MIN	MAX	MAX	MAX	MIN	TYP	TYP			
High Gain, Low Power, Bipolar	S/S	3	30	5	− 150	50	0.6	0.2	LM258	D,P,U	2–51
	D/S	± 1.5	± 15								
High Gain, Low Power, Bipolar	S/S	3	30	3	− 80	50	0.6	0.2	LM258A	D,P,U	2–51
	D/S	± 1.5	± 15								
High Gain, Low Power, Bipolar	S/S	3	26	7	− 250	Typ 100	0.6	0.2	LM2904	D,P,U	2–51
	D/S	± 1.5	± 13								
High Performance		± 4	± 18	6	− 500	20	3	1.7	RV4558	D,P	2–163
BIFET, Low Power, Precision		± 3.5	± 18	0.8	0.2	5	1.1	2.9	TL032AI	D,P	2–203
BIFET, Low Power, Precision		± 3.5	± 18	1.5	0.2	5	1.1	2.9	TL032I	D,P	2–203
BIFET, Precision		± 3.5	± 18	0.8	0.2	50	3	16	TL052AI	D,P	2–283
BIFET, Precision		± 3.5	± 18	1.5	0.2	50	3	16	TL052I	D,P	2–283
BIFET, Low Power		± 3.5	± 18	6	0.2	4	1	3.5	TL062I	D,P	2–341
BIFET, Low Noise		± 3.5	± 18	6	0.2	50	3	13	TL072I	D,P	2–371
BIFET, General Purpose		± 3.5	± 18	6	0.2	50	3	13	TL082I	D,P	2–387
BIFET, General Purpose		± 3.5	± 18	0.5	0.2	50	3	13	TL287I	D,P	2–401
BIFET, General Purpose		± 3.5	± 18	1	0.2	50	3	13	TL288I	D,P	2–401
LinCMOS, High Bias		4	18	5	Typ 0.005	10	2.2	5.3	TLC272AI	D,P	2–565
LinCMOS, High Bias		4	18	2	Typ 0.005	10	2.2	5.3	TLC272BI	D,P	2–565
LinCMOS, High Bias		4	18	10	Typ 0.005	10	2.2	5.3	TLC272I	D,P	2–565
LinCMOS, High Bias		4	18	0.5	Typ 0.005	10	2.2	5.3	TLC277I	D,P	2–565
LinCMOS, Low Bias		4	18	5	Typ 0.005	50	0.1	0.05	TLC27L2AI	D,P	2–629
LinCMOS, Low Bias		4	18	2	Typ 0.005	50	0.1	0.05	TLC27L2BI	D,P	2–629
LinCMOS, Low Bias		4	18	10	Typ 0.005	50	0.1	0.05	TLC27L2I	D,P	2–629
LinCMOS, Low Bias		4	18	0.5	Typ 0.005	50	0.1	0.05	TLC27L7I	D,P	2–629
LinCMOS, Medium Bias		4	18	5	Typ 0.005	25	0.6	0.6	TLC27M2AI	D,P	2–693
LinCMOS, Medium Bias		4	18	2	Typ 0.005	25	0.6	0.6	TLC27M2BI	D,P	2–693
LinCMOS, Medium Bias		4	18	10	Typ 0.005	25	0.6	0.6	TLC27M2I	D,P	2–693
LinCMOS, Medium Bias		4	18	0.5	Typ 0.005	25	0.6	0.6	TLC27M7I	D,P	2–693

internally compensated, dual (continued)

automotive temperature range

(values specified for $T_A = 25°C$)

DESCRIPTION	SUPPLY VOLTAGE (V)		V_{IO} (mV)	I_{IB} (nA)	A_{VD} (V/mV)	B_1 (MHz)	SR (V/µs)	TYPE	PACKAGES	PAGE NO.
	MIN	MAX	MAX	MAX	MIN	TYP	TYP			
LinCMOS, µPower, Precision	4	18	0.6	Typ 0.007	500	0.11	0.05	TLC1078I	D,P	2–757
Excalibur, High Speed, Precision	4	40	0.5	25	1000	2	0.9	TLE2022I	D,P	2–935

internally compensated, dual (continued)

military temperature range **(values specified for T_A = 25°C)**

DESCRIPTION		SUPPLY VOLTAGE (V)		V_{IO} (mV)	I_{IB} (nA)	A_{VD} (V/mV)	B_1 (MHz)	SR (V/µs)	TYPE	PACKAGES	PAGE NO.
		MIN	MAX	MAX	MAX	MIN	TYP	TYP			
High Gain, Low Power, Bipolar	S/S	3	30	3	– 80	50	0.6	0.2	LM158	FK,JG,U	2–51
	D/S	± 1.5	± 15	5	– 150	50	0.6	0.2			
General Purpose		± 2	± 22	5	500	50	1	0.5	MC1558	FK,JG,U	2–121
Precision		± 5	± 22	0.15	– 20	1200	0.8	0.4	LT1013AM	D,FK,JG,P	2–93
Precision		± 5	± 22	0.3	– 30	1200	0.8	0.4	LT1013M	D,FK,JG,P	2–93
High Performance		± 4	± 22	5	500	50	3.5	1.7	RM4558	JG	2–163
Low Power		± 2	± 22	5	100	1	0.5	0.5	TL022M	U	2–171
BIFET, Low Power, Precision		± 3.5	± 18	0.8	0.2	5	1.1	2.9	TL032AM	FK,JG	2–203
BIFET, Low Power, Precision		± 3.5	± 18	1.5	0.2	5	1.1	2.9	TL032M	FK,JG	2–203
BIFET, Precision		± 3.5	± 18	0.8	0.2	50	3	16	TL052AM	FK,JG	2–283
BIFET, Precision		± 3.5	± 18	1.5	0.2	50	3	16	TL052M	FK,JG	2–283
BIFET, Low Power		± 3.5	± 18	6	0.2	4	1	3.5	TL062M	FK,JG,U	2–341
BIFET, Low Noise		± 3.5	± 18	6	0.2	35	3	13	TL072M	FK,JG	2–371
BIFET, General Purpose		± 3.5	± 18	16	0.2	25	3	13	TL082M	FK,JG	2–387
BIFET, General Purpose		± 3.5	± 18	3	0.4	50	3	13	TL287M	JG,U	2–401
BIFET, General Purpose		± 3.5	± 18	3	0.4	50	3	13	TL288M	JG,U	2–401
High-Slew Rate, Single Supply		± 2	± 22	5	– 2000	50	0.2	8	TL35072	D,P	2–443
High-Slew Rate, Single Supply		± 2	± 22	3	– 2000	50	0.2	8	TL35072A	D,P	2–443
LinCMOS, High Bias		4	18	10	Typ 0.005	10	2.2	5.3	TLC272M	FK,JG	2–565
LinCMOS, High Bias		4	18	0.5	Typ 0.005	10	2.2	5.3	TLC277M	FK,JG	2–565
LinCMOS, µPower, Precision		4	18	0.6	Typ 0.007	500	0.11	0.5	TLC1078M	FK,JG	2–757
LinCMOS, Low Noise, Precision		± 2.3	± 8	0.5	Typ 0.001	400	1.9	2.7	TLC2202AM	D,FK,JG,P	2–813
LinCMOS, Low Noise, Precision		± 2.3	± 8	0.5	Typ 0.001	400	1.9	2.7	TLC2202BM	D,FK,JG,P	2–813
LinCMOS, Low Noise, Precision		± 2.3	± 8	1	Typ 0.001	400	1.9	2.7	TLC2202M	D,FK,JG,P	2–813
LinCMOS, Low Bias		4	18	10	Typ 0.005	50	0.1	0.05	TLC27L2M	FK,JG	2–629
LinCMOS, Low Bias		4	18	0.5	Typ 0.005	50	0.1	0.05	TLC27L7M	FK,JG	2–629
LinCMOS, Medium Bias		4	18	10	Typ 0.005	25	0.6	0.6	TLC27M2M	FK,JG	2–693
LinCMOS, Medium Bias		4	18	0.5	Typ 0.005	25	0.6	0.6	TLC27M7M	FK,JG	2–693

internally compensated, dual (continued)

military temperature range **(values specified for T_A = 25°C)**

DESCRIPTION		SUPPLY VOLTAGE (V)		V_{IO} (mV)	I_{IB} (nA)	A_{VD} (V/mV)	B_1 (MHz)	SR (V/µs)	TYPE	PACKAGES	PAGE NO.
		MIN	MAX	MAX	MAX	MIN	TYP	TYP			
Precision	S/S	4	44	0.3	50	1200	0.8	0.2	LT1013M	JG	2–93
	D/S	± 2	± 22	0.3	50	500	0.8	0.2	LT1013M	JG	2–93
Excalibur, High Speed, Low Power, Precision		± 2	± 20	0.3	55	1000	2.8	0.65	TLE2022AM	D,FK,JG,P	2–935
Excalibur, High Speed, Low Power, Precision		± 2	± 20	0.15	50	1500	2.8	0.65	TLE2022BM	JG	2–935
Excalibur, High Speed, Precision		4	40	0.5	25	1000	2	0.9	TLE2022M	FK,JG	2–935
Excalibur, JFET-Input, High-Output Drive, µPower		± 3.5	± 20	2	Typ 0.004	30	2	3.4	TLE2062AM	D,FK,JG,P	2–1075
Excalibur, JFET-Input, High-Output Drive, µPower		± 3.5	± 20	1	Typ 0.004	30	2	3.4	TLE2062BM	JG,P	2–1075
Excalibur, JFET-Input, High-Output Drive, µPower		± 3.5	± 20	4	Typ 0.004	30	2	3.4	TLE2062M	D,FK,JG,P	2–1075
Excalibur, Low Noise, High Speed, Precision		± 2	± 22	1.2	– 1500	100	6	45	TLE2142AM	D,FK,JG,P	2–1199
Excalibur, Low Noise,High Speed, Precision		± 2	± 22	0.75	– 1500	100	6	45	TLE2142M	D,FK,JG,P	2–1199

internally compensated, quad

commercial temperature range **(values specified for T_A = 25°C)**

DESCRIPTION		SUPPLY VOLTAGE (V)		V_{IO} (mV)	I_{IB} (nA)	A_{VD} (V/mV)	B_1 (MHz)	SR (V/μs)	TYPE	PACKAGES†	PAGE NO.
		MIN	MAX	MAX	MAX	MIN	TYP	TYP			
BIFET, General Purpose		± 3.5	± 18	10	0.2	25	3	13	LF347	D,N	2–3
General Purpose		3	30	7	– 250	25	0.6	0.3	LM324	D,N,W,Y	2–39
General Purpose		3	30	3	– 100	25	0.6	0.3	LM324A	N,W	2–39
General Purpose		± 4	± 18	6	200	25	1	0.5	LM348	D,N	2–47
Norton Amplifier, Bipolar	S/S	4	32	—	200	1.2	2.5	0.5	LM3900	D,N	2–61
	D/S	± 2	± 16								
Low Power, Bipolar	S/S	3	36	10	– 500	20	1	0.6	MC3403	D,N	2–125
	D/S	± 1.5	± 18								
Quad uA741, High Performance		± 4	± 18	6	500	20	3	1.7	RC4136	D,N	2–159
BIFET, Low Power, Precision		± 3.5	± 18	1.5	0.2	5	1.1	2.9	TL034AC	D,N	2–229
BIFET, Low Power, Precision		± 3.5	± 18	4	0.2	5	1.1	2.9	TL034C	D,N	2–229
General Purpose		± 2	± 18	5	250	60	0.5	0.5	TL044C	N.W	2–253
BIFET, Precision		± 3.5	± 18	1.5	0.2	50	2.7	16	TL054AC	D,N	2–311
BIFET, Precision		± 3.5	± 18	4	0.2	50	2.7	16	TL054C	D,N	2–311
BIFET, Low Power		± 3.5	± 18	6	0.2	4	1	3.5	TL064AC	D,N	2–341
BIFET, Low Power		± 3.5	± 18	3	0.2	4	1	3.5	TL064BC	D,N	2–341
BIFET, Low Power		± 3.5	± 18	15	0.4	3	1	3.5	TL064C	D,N	2–341
BIFET, Low Noise		± 3.5	± 18	6	0.2	50	3	13	TL074AC	D,N	2–371
BIFET, Low Noise		± 3.5	± 18	3	0.2	50	3	13	TL074BC	D,N	2–371
BIFET, Low Noise		± 3.5	± 18	10	0.2	50	3	13	TL074C	D,N	2–371
BIFET, General Purpose		± 3.5	± 18	6	0.2	50	3	13	TL084AC	D,N	2–387
BIFET, General Purpose		± 3.5	± 18	3	0.2	50	3	13	TL084BC	D,N	2–387
BIFET, General Purpose		± 3.5	± 18	15	0.4	25	3	13	TL084C	D,N	2–387
High-Slew Rate		± 2	± 22	5	– 2000	50	0.2	8	TL34074	DW,N	2–443
High-Slew Rate		± 2	± 22	3	– 2000	50	0.2	8	TL34074A	DW,N	2–443
LinCMOS, High Bias		1.4	18	5	Typ 0.005	10	2.2	5.3	TLC254AC	D,N	2–487
LinCMOS, High Bias		1.4	18	2	Typ 0.005	10	2.2	5.3	TLC254BC	D,N	2–487
LinCMOS, High Bias		1.4	18	10	Typ 0.005	10	2.2	5.3	TLC254C	D,N,Y	2–487
LinCMOS, Low Bias		1.4	18	5	Typ 0.005	30	0.1	0.05	TLC25L4AC	D,N	2–487
LinCMOS, Low Bias		1.4	18	2	Typ 0.005	30	0.1	0.05	TLC25L4BC	D,N	2–487
LinCMOS, Low Bias		1.4	18	10	Typ 0.005	30	0.1	0.05	TLC25L4C	D,N,Y	2–487
LinCMOS, Medium Bias		1.4	18	5	Typ 0.005	20	0.6	0.6	TLC25M4AC	D,N	2–487

† Y is chip form.

internally compensated, quad (continued)

commercial temperature range

(values specified for T_A = 25°C)

DESCRIPTION	SUPPLY VOLTAGE (V)		V_{IO} (mV)	I_{IB} (nA)	A_{VD} (V/mV)	B_1 (MHz)	SR (V/μs)	TYPE	PACKAGES†	PAGE NO.
	MIN	MAX	MAX	MAX	MIN	TYP	TYP			
LinCMOS, Medium Bias	1.4	18	2	Typ 0.005	20	0.6	0.6	TLC25M4BC	D,N	2–487
LinCMOS, Medium Bias	1.4	18	10	Typ 0.005	20	0.6	0.6	TLC25M4C	D,N,Y	2–487
LinCMOS, High Bias	3	18	5	Typ 0.005	10	2.2	5.3	TLC274AC	D,N	2–597
LinCMOS, High Bias	3	18	2	Typ 0.005	10	2.2	5.3	TLC274BC	D,N	2–597
LinCMOS, High Bias	3	18	10	Typ 0.005	10	2.2	5.3	TLC274C	D,N	2–597
LinCMOS, High Bias	3	18	0.9	Typ 0.005	10	2.2	5.3	TLC279C	D,N	2–597
LinCMOS, Low Bias	3	18	5	Typ 0.005	50	0.1	0.05	TLC27L4AC	D,N	2–661
LinCMOS, Low Bias	3	18	2	Typ 0.005	50	0.1	0.05	TLC27L4BC	D,N	2–661
LinCMOS, Low Bias	3	18	10	Typ 0.005	50	0.1	0.05	TLC27L4C	D,N	2–661
LinCMOS, Low Bias	3	18	0.9	Typ 0.005	50	0.1	0.05	TLC27L9C	D,N	2–661
LinCMOS, Medium Bias	3	18	5	Typ 0.005	25	0.6	0.6	TLC27M4AC	D,N	2–725
LinCMOS, Medium Bias	3	18	2	Typ 0.005	25	0.6	0.6	TLC27M4BC	D,N	2–725
LinCMOS, Medium Bias	3	18	10	Typ 0.005	25	0.6	0.6	TLC27M4C	D,N	2–725
LinCMOS, Medium Bias	3	18	0.9	Typ 0.005	25	0.7	0.6	TLC27M9C	D,N	2–725
LinCMOS, μPower, Precision	1.4	18	1.15	Typ 0.007	500	0.11	0.05	TLC1079C	D,N	2–771
Excalibur, High Speed, Low Power, Precision	4	40	0.75	Typ 45	800	2.8	0.7	TLE2024AC	DW,N	2–963
Excalibur, High Speed, Low Power, Precision	4	40	0.5	Typ 40	1000	2.8	0.7	TLE2024BC	DW,N	2–963
Excalibur, High Speed, Precision	± 2	± 22	0.9	– 700	100	6	4.5	TLE2024C	DW,N,Y	2–963
Excalibur, JFET-Input, High-Output Drive, μPower	± 3.5	± 20	4	Typ 0.004	30	2	3.4	TLE2064AC	D,N	2–1111
Excalibur, JFET-Input, High-Output Drive, μPower	± 3.5	± 20	2	Typ 0.004	30	2	3.4	TLE2064BC	D,N	2–1111
Excalibur, JFET-Input, High-Output Drive, μPower	± 3.5	± 20	6	Typ 0.004	30	2	3.4	TLE2064C	D,N,Y	2–1111

† Y is chip form.

internally compensated, quad (continued)

industrial temperature range

(values specified for T_A = 25°C)

DESCRIPTION		SUPPLY VOLTAGE (V)		V_{IO} (mV)	I_{IB} (nA)	A_{VD} (V/mV)	B_1 (MHz)	SR (V/μs)	TYPE	PACKAGES	PAGE NO.
		MIN	MAX	MAX	MAX	MIN	TYP	TYP			
General Purpose, Bipolar		3	30	5	– 150	50	0.6	0.3	LM224	D,N,W	2–39
General Purpose, Bipolar		3	30	3	– 80	50	0.6	0.3	LM224A	N,W	2–39
General Purpose, Bipolar		± 4	± 18	6	200	25	1	0.5	LM248	D,N	2–47
High Gain, Low Power, Bipolar	S/S	3	32	5	– 150	50	0.6	0.2	LM258	D,P	2–51
	D/S	± 1.5	± 22								
High Gain, Low Power, Bipolar	S/S	3	32	3	– 80	50	0.6	0.2	LM258A	D,P	2–51
	D/S	± 1.5	± 22								
Norton Amplifier, Bipolar	S/S	4	32	—	200	1.2	2.5	0.5	LM2900	D,N	2–39
	D/S	± 2	± 16								
BIFET, Low Power		± 3.5	± 18	1.5	0.2	5	1.1	2.9	TL034AI	D,N	2–229
BIFET, Low Power		± 3.5	± 18	4	0.2	5	1.1	2.9	TTL034I	D,N	2–229
BIFET, Precision		± 3.5	± 18	1.5	0.2	50	2.7	16	TL054AI	D,N	2–311
BIFET, Precision		± 3.5	± 18	4	0.2	50	2.7	16	TL054I	D,N	2–311
BIFET, Low Power, Precision		± 3.5	± 18	6	0.2	4	1	3.5	TL064I	D,N	2–341
BIFET, Low Noise, Precision		± 3.5	± 18	6	0.2	50	3	13	TL074I	D,N	2–371
BIFET, General Purpose		± 3.5	± 18	6	0.2	50	3	13	TL084I	D,N	2–387
High-Slew Rate		± 2	± 22	3	– 2000	50	0.2	8	TL33074A	DW,N	2–443
High-Slew Rate		± 2	± 22	5	– 2000	50	0.2	8	TL33074	DW,N	2–443
LinCMOS, High Bias		4	18	5	Typ 0.001	10	2.2	5.3	TLC274AI	D,N	2–597
LinCMOS, High Bias		4	18	2	Typ 0.001	10	2.2	5.3	TLC274BI	D,N	2–597
LinCMOS, High Bias		4	18	10	Typ 0.001	10	2.2	5.3	TLC274I	D,N	2–597
LinCMOS, High Bias		4	18	0.9	Typ 0.005	10	2.2	5.3	TLC279I	D,N	2–597
LinCMOS, Low Bias		4	18	5	Typ 0.005	50	0.1	0.05	TLC27L4AI	D,N	2–661
LinCMOS, Low Bias		4	18	2	Typ 0.005	50	0.1	0.05	TLC27L4BI	D,N	2–661
LinCMOS, Low Bias		4	18	10	Typ 0.005	50	0.1	0.05	TLC27L4I	D,N	2–661
LinCMOS, Low Bias		4	18	0.9	Typ 0.005	50	0.1	0.05	TLC27L9I	D,N	2–661
LinCMOS, Medium Bias		4	18	5	Typ 0.005	25	0.6	0.6	TLC27M4AI	D,N	2–725
LinCMOS, Medium Bias		4	18	2	Typ 0.005	25	0.6	0.6	TLC27M4BI	D,N	2–725
LinCMOS, Medium Bias		4	18	10	Typ 0.005	25	0.6	0.6	TLC27M4I	D,N	2–725
LinCMOS, Medium Bias		4	18	0.9	Typ 0.005	25	0.6	0.6	TLC27M9I	D,N	2–725

internally compensated, quad (continued)

industrial temperature range **(values specified for T_A = 25°C)**

DESCRIPTION	SUPPLY VOLTAGE (V)		V_{IO} (mV)	I_{IB} (nA)	A_{VD} (V/mV)	B_1 (MHz)	SR (V/µs)	TYPE	PACKAGES	PAGE NO.
	MIN	MAX	MAX	MAX	MIN	TYP	TYP			
LinCMOS, µPower, Precision	4	18	1.15	Typ 0.007	500	0.11	0.05	TLC1079I	D,P	2–771
Excalibur, High Speed, Low Power, Precision	± 2	± 20	0.75	55	800	2.8	0.7	TLE2024AI	DW,N	2–963
Excalibur, High Speed, Low Power, Precision	± 2	± 20	0.5	50	1000	2.8	0.7	TLE2024BI	DW,N	2–963
Excalibur, High Speed, Precision	4	40	0.5	25	1000	2	0.9	TLE2024I	DW,N	2–963
Excalibur, JFET-Input, High-Output Drive, µPower	± 3.5	± 20	4	Typ 0.004	30	2	3.4	TLE2064AI	D,N	2–1111
Excalibur, JFET-Input, High-Output Drive, µPower	± 3.5	± 20	2	Typ 0.004	30	2	3.4	TLE2064BI	N	2–1111
Excalibur, JFET-Input, High-Output Drive, µPower	± 3.5	± 20	6	Typ 0.004	30	2	3.4	TLE2064I	D,N	2–1111

internally compensated, quad (continued)

automotive temperature range

(values specified for T_A = 25°C)

DESCRIPTION		SUPPLY VOLTAGE (V)		V_{IO} (mV)	I_{IB} (nA)	A_{VD} (V/mV)	B_1 (MHz)	SR (V/μs)	TYPE	PACKAGES	PAGE NO.
		MIN	MAX	MAX	MAX	MIN	TYP	TYP			
Norton Amplifier, Bipolar	S/S	4.5	32	—	200	1.2	2.5	0.5	LM2900	N	2–61
	D/S	± 2.2	± 16								
Extended Temperature Range LM324		3	26	7	– 250	Typ 100	0.6	0.3	LM2902 LM2902Q	D,N	2–39
Low Power, Bipolar	S/S	3	36	8	– 500	20	1	0.6	MC3303	D,N	2–125
	D/S	± 1.5	± 18								
Quad uA741		± 4.5	± 18	6	500	20	3	1.7	RM4136	D,N,W	2–159
BIFET, Low Power, Precision		± 3.5	± 18	1.5	0.2	5	1.1	2.9	TL034AI	D,N	2–229
BIFET, Low Power, Precision		± 3.5	± 18	4	0.2	5	1.1	2.9	TL034I	D,N	2–229
BIFET, Precision		± 3.5	± 18	1.5	0.2	50	2.7	16	TL054AI	D,N	2–311
BIFET, Precision		± 3.5	± 18	4	0.2	50	2.7	16	TL054I	D,N	2–311
BIFET, Low Power, Precision		± 3.5	± 18	6	0.2	4	1	3.5	TL064I	D,N	2–341
BIFET, Low Noise, Precision		± 3.5	± 18	6	0.2	50	3	13	TL074I	D,N	2–371
BIFET, General Purpose		± 3.5	± 18	6	0.2	50	3	13	TL084I	D,N	2–387
LinCMOS, High Bias		4	18	5	Typ 0.001	10	2.2	5.3	TLC274AI	D,N	2–597
LinCMOS, High Bias		4	18	2	Typ 0.001	10	2.2	5.3	TLC274BI	D,N	2–597
LinCMOS, High Bias		4	18	10	Typ 0.001	10	2.2	5.3	TLC274I	D,N	2–597
LinCMOS, High Bias		4	18	1.2	Typ 0.005	10	2.2	5.3	TLC279I	D,N	2–597
LinCMOS, Low Bias		4	18	5	Typ 0.005	50	0.1	0.05	TLC27L4AI	D,N	2–661
LinCMOS, Low Bias		4	18	2	Typ 0.005	50	0.1	0.05	TLC27L4BI	D,N	2–661
LinCMOS, Low Bias		4	18	10	Typ 0.005	50	0.1	0.05	TLC27L4I	D,N	2–661
LinCMOS, Low Bias		4	18	0.9	Typ 0.005	50	0.1	0.05	TLC27L9I	D,N	2–661
LinCMOS, Medium Bias		4	18	5	Typ 0.005	25	0.6	0.6	TLC27M4AI	D,N	2–725
LinCMOS, Medium Bias		4	18	2	Typ 0.005	25	0.6	0.6	TLC27M4BI	D,N	2–725
LinCMOS, Medium Bias		4	18	10	Typ 0.005	25	0.6	0.6	TLC27M4I	D,N	2–725
LinCMOS, Medium Bias		4	18	0.9	Typ 0.005	25	0.6	0.6	TLC27M9I	D,N	2–725
LinCMOS, μPower, Precision		4	18	1.15	Typ 0.007	500	0.11	0.05	TLC1079I	D,N	2–771
Excalibur, High Speed, Precision		4	40	0.5	25	1000	2	0.9	TLE2024I	DW,N	2–963

internally compensated, quad (continued)

extended temperature range **(values specified for T_A = 25°C)**

DESCRIPTION	SUPPLY VOLTAGE (V)		V_{IO} (mV)	I_{IB} (nA)	A_{VD} (V/mV)	B_1 (MHz)	SR (V/μs)	TYPE	PACKAGES†	PAGE NO.
	MIN	MAX	MAX	MAX	MIN	TYP	TYP			
High Temperature (– 40°C to 150°C)	± 2	± 16	7	– 100	25	0.4	Min 0.2	TL2829Z	D,N,Y	2–429

† Y is chip form.

internally compensated, quad

military temperature range **(values specified for T_A = 25°C)**

DESCRIPTION	SUPPLY VOLTAGE (V)		V_{IO} (mV)	I_{IB} (nA)	A_{VD} (V/mV)	B_1 (MHz)	SR (V/μs)	TYPE	PACKAGES	PAGE NO.
	MIN	MAX	MAX	MAX	MIN	TYP	TYP			
General Purpose	3	30	5	– 150	50	0.6	0.13	LM124	FK,J,W	2–39
General Purpose	± 4	± 22	5	100	50	1	0.5	LM148	FK,J	2–47
Quad uA741, High Performance	± 4	± 22	4	400	50	3.5	1.7	RM4136	FK,J,W	2–159
BIFET, Low Power, Precision	± 3.5	± 18	1.5	0.2	5	1.1	2.9	TL034AM	FK,J	2–229
BIFET, Low Power, Precision	± 3.5	± 18	4	0.2	5	1.1	2.9	TL034M	FK,J	2–229
Low Power	± 2	± 22	5	100	72	0.5	0.5	TL044M	FK,J,W	2–253
BIFET, Precision	± 3.5	± 18	1.5	0.2	50	2.7	16	TL054AM	FK,J	2–311
BIFET, Precision	± 3.5	± 18	4	0.2	50	2.7	16	TL054M	FK,J	2–311
BIFET, Low Power	± 3.5	± 18	9	0.2	4	1	3.5	TL064M	FK,J,W	2–341
BIFET, Low Noise	± 3.5	± 18	9	0.2	35	3	13	TL074M	FK,J,W	2–371
BIFET, General Purpose	± 3.5	± 18	9	0.2	25	3	13	TL084M	FK,J,W	2–387
High-Slew Rate	± 2	± 22	5	– 2000	50	0.2	8	TL35074	DW,N	2–443
High-Slew Rate	± 2	± 22	3	– 2000	50	0.2	8	TL35074A	DW,N	2–443
LinCMOS, High Bias	4	18	10	Typ 0.005	10	2.2	5.3	TLC274AM	FK,J	2–597
LinCMOS, High Bias	4	18	1.2	Typ 0.005	10	2.2	5.3	TLC279M	FK,J	2–597
LinCMOS, Low Bias	4	18	10	Typ 0.005	50	0.1	0.05	TLC27L4M	FK,J	2–661
LinCMOS, Low Bias	4	18	0.9	Typ 0.005	50	0.1	0.05	TLC27L9M	FK,J	2–661
LinCMOS, Medium Bias	4	18	10	Typ 0.005	20	0.6	0.6	TLC27M4M	FK,J	2–725
LinCMOS, Medium Bias	4	18	0.9	Typ 0.005	20	0.6	0.6	TLC27M9M	FK,J	2–725
LinCMOS, μPower, Precision	4	18	1.15	Typ 0.007	500	0.11	0.05	TLC1079M	D,J,P	2–771

internally compensated, quad (continued)

military temperature range

(values specified for T_A = 25°C)

DESCRIPTION	SUPPLY VOLTAGE (V)		V_{IO} (mV)	I_{IB} (nA)	A_{VD} (V/mV)	B_1 (MHz)	SR (V/µs)	TYPE	PACKAGES	PAGE NO.
	MIN	MAX	MAX	MAX	MIN	TYP	TYP			
Excalibur, High Speed, Low Power, Precision	± 2	± 20	0.75	55	800	2.8	0.7	TLE2024AM	DW,FK,J,N	2–963
Excalibur, High Speed, Low Power, Precision	± 2	± 20	0.5	50	1000	2.8	0.7	TLE2024BM	DW,J,N	2–963
Excalibur, High Speed, Precision	4	40	0.5	25	1000	2	0.9	TLE2024M	DW,FK,J,N	2–963
Excalibur, JFET-Input, High-Output Drive, µPower	± 3.5	± 20	4	Typ 0.004	30	2	3.4	TLE2064AM	D,FK,J,N	2–1111
Excalibur, JFET-Input, High-Output Drive, µPower	± 3.5	± 20	2	Typ 0.004	30	2	3.4	TLE2064BM	J,N	2–1111
Excalibur, JFET-Input, High-Output Drive, µPower	± 3.5	± 20	6	Typ 0.004	30	2	3.4	TLE2064M	D,FK,J,N	2–1111

Replacements are based on similarity of electrical and mechanical characteristics shown in currently published data. Interchangeability in particular applications is not guaranteed. Before using a device as a substitute, the user should compare the specifications of the substitute device with the specifications of the original.

Texas Instruments makes no warranty as to the information furnished and the buyer assumes all risk in the use thereof. No liability is assumed for damages resulting from the use of the information contained herein.

Manufacturers are arranged in alphabetical order.

ADVANCED LINEAR DEVICES	SUGGESTED TI REPLACEMENT	PAGE NO.
ALD1701 or ALD1702 or ALD1703	TLC271	2–507

ANALOG DEVICES	SUGGESTED TI REPLACEMENT	PAGE NO.
AD510 or AD517	OP-07	2–141
AD712J	TLE2082A	2–1147

FAIRCHILD	DIRECT TI REPLACEMENT	SUGGESTED TI REPLACEMENT	PAGE NO.
uA714		OP-07C	2–141
uA714L		OP-07D	2–141
uA741	uA741		2–1305
uA747	uA747		2–1313
uA748	uA748		2–1319
uA771		TL071	2–371
uA771A		TL071B or TL081B	2–371 / 2–387
uA771B		TL071A or TL081A	2–371 / 2–387
uA771L		TL081	2–387
uA772		TL072	2–371
uA772A		TL072B	2–371
uA772B		TL072A or TL082A	2–371 / 2–387
uA772L		TL082	2–387
uA774		TL074	2–371
uA774B		TL074A or TL074B	2–371
uA774L		TL084	2–387

BURR BROWN	SUGGESTED TI REPLACEMENT	PAGE NO.
OPA111	TLC2201	2–785
OPA211	TLC2202	2–813

OPERATIONAL AMPLIFIERS CROSS-REFERENCE GUIDE

GENERAL ELECTRIC	SUGGESTED TI REPLACEMENT	PAGE NO.
ICL7611, or ICL7612, or ICL7613	TLC271	2–507
ICL7621	TLC272	2–565
ICL7641	TLC274 or TLC27L9	2–597 / 2–661
ICL7642	TLC27M9	2–725

HARRIS	SUGGESTED TI REPLACEMENT	PAGE NO.
HA2515	LM318	2–35
HA5127	TLE2027	2–991
HA5135-5	OP-07C	2–141
HA5137	TLE2037	2–1015

INTERSIL	SUGGESTED TI REPLACEMENT	PAGE NO.
ICL7611, or ICL7612 or ICL7613	TLC271	2–507
ICL7621	TLC272	2–565
ICL7641	TLC274 or TLC27L9	2–597 / 2–661
ICL7642	TLC27M9	2–725
ICL7652	TLC2652 or TLC2654	2–861 / 2–885

LINEAR TECHNOLOGY	DIRECT TI REPLACEMENT	SUGGESTED TI REPLACEMENT	PAGE NO.
LT1001		OP-07C, OP-07D,	2–141 / 2–149
LT1007	LT1007	TLE2027	2–69 / 2–991
LT1007A	LT1007A		2–69
LT1037	LT1037	TLE2037	2–69 / 2–1015
LT1037A	LT1037A		2–69
LTC1052		TLC2652 or TLC2654	2–861 / 2–885

MAXIM	SUGGESTED TI REPLACEMENT	PAGE NO.
ICL7611, or ICL7612 or ICL7613	TLC271	2–565
ICL7621	TLC272	2–565
ICL7641	TLC274 or TLC27L9	2–597 / 2–661
ICL7642	TLC27M9	2–725
ICL7652	TLC2652 or TLC2654	2–861 / 2–885

MOTOROLA	DIRECT TI REPLACEMENT	SUGGESTED TI REPLACEMENT	PAGE NO.
MC748	uA748		2–1319
MC1458	MC1458		2–121
MC1558	MC1558		2–121
MC1709	uA709		2–1301
MC1741	uA741		2–1305
MC1747	uA747		2–1313
MC3303	MC3303		2–125
MC3403	MC3403	RC4136	2–125 / 2–159
MC4558	RC4558		2–163
MC4741	LM348		2–47
MC34001		TL071 or LF351	2–371 / 2–5
MC34002		TL072 or LF353	2–371 / 2–7
MC34004		TL074 or LF347	2–371 / 2–3
MC34004B		TL074A or LF347B	2–371 / 2–3
MC34071	TL34071	TLE2141	2–443 / 2–1181
MC34072	TL34072	TLE2142	2–443 / 2–1199
MC34181		TLE2061	2–1039
MC34182		TLE2062	2–1075
MC34184		TLE2064	2–1111

NATIONAL	DIRECT TI REPLACEMENT	SUGGESTED TI REPLACEMENT	PAGE NO.
LF347	LF347	TL074 or TL084	2–3 / 2–371 / 2–387
LF347B	LF347B	TL074A, TL074B, or TL084A	2–3 / 2–371 / 2–387
LF351	LF351	TL071 or TL081A	2–5 / 2–387
LF353	LF353	TL072, TL072A, or TL082A	2–7 / 2–371 / 2–387
LF411	LF411	TL081A	2–9 / 2–387
LF411A		TL071A, TL071B, TL081A, or TL081B	2–371 2–387
LF412	LF412	TL072A, TL082A, or TL082B	2–9 / 2–387
LF412-1A		TLE2082	2–1147
LF441		TL061 or TLE2061	2–341 / 2–1039
LF441A		TL061A or TL061B	2–341
LF442		TL062 or TLE2062	2–341 / 2–1111
LF442A		TL062B	2–341
LF444		TL064 or TLE2064	2–341 / 2–1111
LF444A		TL064A	2–341
LH0044		OP-07C	2–141
LH0044B		OP-07D	2–141
LM201A	LM201A		2–13
LM207	LM207		2–19
LM218	LM218		2–35

(Continued)

NATIONAL	DIRECT TI REPLACEMENT	SUGGESTED TI REPLACEMENT	PAGE NO.
LM224	LM224		2–39
LM248	LM248		2–47
LM258	LM258		2–51
LM301A	LM301A		2–13
LM307	LM307		2–19
LM318	LM318		2–35
LM324	LM324	TLE2024	2–39 / 2–963
LM348	LM348		2–47
LM358	LM358	TLE2022	2–51 / 2–935
LM709	uA709		2–1301
LM741	uA741		2–1305
LM883		RC4558	2–163
LM1458	MC1458		2–121
LM2900	LM2900		2–61
LM2902	LM2902		2–39
LM2904	LM2904		2–51
LM3900	LM3900		2–61
LMC660		TLC274	2–597
UMC662		TLC2202	2–813

NEC	SUGGESTED TI REPLACEMENT	PAGE NO.
uPC159	LM318	2–35
uPC251	MC1458	2–121
uPC354	OP-07	2–141
uPC801	TL071, TL081A, or LF351	2–371 / 2–387 / 2–5

PMI	DIRECT TI REPLACEMENT	SUGGESTED TI REPLACEMENT	PAGE NO.
OP-02		uA741	2–1305
OP-04		uA747	2–1313
OP-07C	OP-07C		2–141
OP-07D	OP-07D		2–141
OP-07F		RC4136	2–159
OP-14C or OP-14E		MC1458	2–121
OP-14J		MC1558	2–121
OP-15F		TL071, TL081A, or LF351	2–371 / 2–387 / 2–3

(Continued)

PMI	DIRECT TI REPLACEMENT	SUGGESTED TI REPLACEMENT	PAGE NO.
OP-27E	OP-27E		2–149
OP-27G	OP-27G		2–149
OP-37E	OP-37E		2–149
OP-37G	OP-37G		2–149
OP-215F		TL072, TL082A, LF353, or TLE2082	2–371 / 2–387
OP-215G		TLE2082A	2–1147
OP-21		TLE2021	2–909
OP-27		TLE2027	2–991
OP-37		TLE2037	2–1015
OP-221		TLE2022	2–935
OP-421		TLE2024	2–963

RAYTHEON	DIRECT TI REPLACEMENT	SUGGESTED TI REPLACEMENT	PAGE NO.
RC4136	RC4136		2–159
RC4156		LM348	2–47
RC4157		LM348	2–47
RC4558	RC4558		2–163
RC4559	RC4559		2–169

RCA	SUGGESTED TI REPLACEMENT	PAGE NO.
CA081A	TL081	2–387
CA081A	TL081A	2–387
CA082	TL082	2–387
CA082A	TL082A	2–387
CA084	TL084	2–387

SIGNETICS	DIRECT TI REPLACEMENT	SUGGESTED TI REPLACEMENT	PAGE NO.
NE532		LM358 or TL022	2–51 / 2–171
NE5532	NE5532		2–131
NE5532A	NE5532A		2–131
NE5534	NE5534	TLE2037	2–135 / 2–1015
NE5534A	NE5534A	TLE2037A	2–135 / 2–1015
SE5534	SE5534		2–135
SE5534A	SE5534A		2–135

SGS-THOMSON	SUGGESTED TI REPLACEMENT	PAGE NO.
TS271	TLC271	2–507
TS271A	TLC271A	2–507
TS271B	TLC271B	2–507
TS272	TLC272	2–565
TS272A	TLC272A	2–565
TS272B	TLC272B	2–565
TS274	TLC274	2–597
TS274A	TLC274A	2–597
TS274B	TLC274B	2–597
TS27L2	TLC27L2	2–629
TS27L2A	TLC27L2A	2–629
TS27L2B	TLC27L2B	2–629
TS27L4	TLC27L4	2–661
TS27L4A	TLC27L4A	2–661
TS27L4B	TLC27L4B	2–661
TS27M2	TLC27M2	2–693
TS27M2A	TLC27M2A	2–693
TS27M2B	TLC27M2B	2–693
TS27M4	TLC27M4	2–725
TS27M4A	TLC27M4A	2–725
TS27M4B	TLC27M4B	2–725

Input Offset Voltage (V_{IO})

The d-c voltage that must be applied between the input terminals to force the quiescent d-c output voltage to zero or other level, if specified.

Average Temperature Coefficient of Input Offset Voltage (αV_{IO})

The ratio of the change in input offset voltage to the change in free-air temperature. This is an average value for the specified temperature range.

$$\alpha V_{IO} = \left[\frac{(V_{IO} \text{ @ } T_{A(1)}) - (V_{IO} \text{ @ } T_{A(2)})}{T_{A(1)} - T_{A(2)}} \right] \text{ where } T_{A(1)} \text{ and } T_{A(2)} \text{ are the specified temperature extremes.}$$

Input Offset Current (I_{IO})

The difference between the currents into the two input terminals with the output at zero volts.

Average Temperature Coefficient of Input Offset Current (αI_{IO})

The ratio of the change in input offset current to the change in free-air temperature. This is an average value for the specified temperature range.

$$\alpha I_{IO} = \left[\frac{(I_{IO} \text{ @ } T_{A(1)}) - (I_{IO} \text{ @ } T_{A(2)})}{T_{A(1)} - T_{A(2)}} \right] \text{ where } T_{A(1)} \text{ and } T_{A(2)} \text{ are the specified temperature extremes.}$$

Input Bias Current (I_{IB})

The average of the currents into the two input terminals with the output at zero volts.

Common-Mode Input Voltage (V_{IC})

The average of the two input voltages.

Common-Mode Input Voltage Range (V_{ICR})

The range of common-mode input voltage that if exceeded will cause the amplifier to cease functioning properly.

Differential Input Voltage (V_{ID})

The voltage at the noninverting input with respect to the inverting input.

Maximum Peak Output Voltage Swing (V_{OM})

The maximum positive or negative peak output voltage that can be obtained without waveform clipping when the quiescent d-c output voltage is zero.

Maximum Peak-to-Peak Output Voltage Swing (V_{OPP})

The maximum peak-to-peak output voltage that can be obtained without waveform clipping when the quiescent d-c output voltage is zero.

Large-Signal Voltage Amplification (A_V)

The ratio of the peak-to-peak output voltage swing to the change in input voltage required to drive the output.

Differential Voltage Amplification (A_{VD})

The ratio of the change in output voltage to the change in differential input voltage producing it.

Maximum-Output-Swing Bandwidth (B_{OM})

The range of frequencies within which the maximum output voltage swing is above a specified value.

Unity-Gain Bandwidth (B_1)

The range of frequencies within which the open-loop voltage amplification is greater than unity.

Phase Margin (ϕ_m)

The absolute value of the open-loop phase shift between the output and the inverting input at the frequency at which the modulus of the open-loop amplification is unity.

Gain Margin (A_m)

The reciprocal of the open-loop voltage amplification at the lowest frequency at which the open-loop phase shift is such that the output is in phase with the inverting input.

Input Resistance (r_i)

The resistance between the input terminals with either input grounded.

Differential Input Resistance (r_{id})

The small-signal resistance between the two ungrounded input terminals.

Output Resistance (r_o)

The resistance between the output terminal and ground.

Input Capacitance (C_i)

The capacitance between the input terminals with either input grounded.

Common-Mode Input Impedance (z_{ic})

The parallel sum of the small-signal impedance between each input terminal and ground.

Output Impedance (z_o)

The small-signal impedance between the output terminal and ground.

Common-Mode Rejection Ratio (k_{CMR}, CMRR)

The ratio of differential voltage amplification to common-mode voltage amplification.
NOTE: This is measured by determining the ratio of a change in input common-mode voltage to the resulting change in input offset voltage.

Supply Voltage Sensitivity (k_{SVS}, $\Delta V_{IO}/\Delta V_{CC}$)

The absolute value of the ratio of the change in input offset voltage to the change in supply voltages producing it.
NOTES: 1. Unless otherwise noted, both supply voltages are varied symmetrically.
2. This is the reciprocal of supply voltage rejection ratio.

Supply Voltage Rejection Ratio (k_{SVR}, $\Delta V_{CC}/\Delta V_{IO}$)

The absolute value of the ratio of the change in supply voltages to the change in input offset voltage.
NOTES: 1. Unless otherwise noted, both supply voltages are varied symmetrically.
2. This is the reciprocal of supply voltage sensitivity.

Equivalent Input Noise Voltage (V_n)

The voltage of an ideal voltage source (having an internal impedance equal to zero) in series with the input terminals of the device that represents the part of the internally generated noise that can properly be represented by a voltage source.

Equivalent Input Noise Current (I_n)

The current of an ideal current source (having an internal impedance equal to infinity) in parallel with the input terminals of the device that represents the part of the internally generated noise that can properly be represented by a current source.

Average Noise Figure ($\overline{F}$)

The ratio of (1) the total output noise power within a designated output frequency band when the noise temperature of the input termination(s) is at the reference noise temperature, T_O, at all frequencies to (2) that part of (1) caused by the noise temperature of the designated signal-input termination within a designated signal-input frequency band.

Short-Circuit Output Current (I_{OS})

The maximum output current available from the amplifier with the output shorted to ground, to either supply, or to a specified point.

Supply Current (I_{CC})

The current into the V_{CC} or V_{CC+} terminal of an integrated circuit.

Total Power Dissipation (P_D)

The total d-c power supplied to the device less any power delivered from the device to a load.
NOTE: At no load: $P_D = V_{CC+} \cdot I_{CC+} + V_{CC-} \cdot I_{CC-}$.

Crosstalk Attenuation (V_{o1}/V_{o2})

The ratio of the change in output voltage of a driven channel to the resulting change in output voltage of another channel.

Rise Time (t_r)

The time required for an output voltage step to change from 10% to 90% of its final value.

Total Response Time (Settling Time) (t_{tot})

The time between a step-function change of the input signal level and the instant at which the magnitude of the output signal reaches for the last time a specified level range ($\pm\epsilon$) containing the final output signal level.

Overshoot Factor

The ratio of (1) the largest deviation of the output signal value from its final steady-state value after a step-function change of the input signal, to (2) the absolute value of the difference between the steady-state output signal values before and after the step-function change of the input signal.

Slew Rate (SR)

The average time rate of change of the closed-loop amplifier output voltage for a step-signal input.

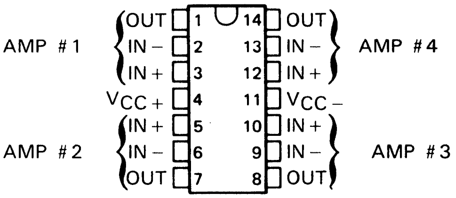
General Information	1
Operational Amplifiers	2
Mechanical Data	3

LF347, LF347B
WIDE-BANDWIDTH QUAD JFET-INPUT OPERATIONAL AMPLIFIERS

D2997, MARCH 1987—REVISED SEPTEMBER 1990

- **Low Input Bias Current**
  Typically 50 pA
- **Low Input Noise Current**
  Typically 0.01 pA/√Hz
- **Low Total Harmonic Distortion**
- **Low Supply Current . . . Typically 8 mA**
- **Wide Gain Bandwidth . . . Typically 3 MHz**
- **High Slew Rate . . . Typically 13 V/μs**
- **Pin Compatible with the LM348**

D OR N PACKAGE
(TOP VIEW)



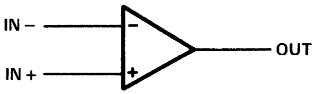
description

These devices are low-cost, high-speed, JFET-input operational amplifiers. They require low supply current yet maintain a large gain-bandwidth product and a fast slew rate. In addition, their matched high-voltage JFET inputs provide very low input bias and offset current.

The LF347 and LF347B can be used in applications such as high-speed integrators, digital-to-analog converters, sample-and-hold circuits, and many other circuits.

The LF347 and LF347B are characterized for operation from 0°C to 70°C.

symbol (each amplifier)



AVAILABLE OPTIONS

T_A	V_{IO} MAX AT 25°C	PACKAGE	
		SMALL-OUTLINE (D)	PLASTIC DIP (N)
0°C to 70°C	10 mV	LF347D	LF347N
	5 mV	LF347BD	LF347BN

D packages are available taped and reeled. Add "R" suffix to the device type, (e.g. LF347DR).

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC+}	18 V
Supply voltage, V_{CC-}	−18 V
Differential input voltage, V_{ID}	±30 V
Input voltage (see Note 1)	±15 V
Duration of output short circuit	Unlimited
Continuous total power dissipation	See Dissipation Rating Table
Operating temperature range	0°C to 70°C
Storage temperature range	−65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C

NOTE 1: Unless otherwise specified, the absolute maximum negative input voltage is equal to the negative power supply voltage.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR	DERATE ABOVE T_A	$T_A = 70°C$ POWER RATING
D	680 mW	7.6 mW/°C	61°C	608 mW
N	680 mW	N/A	N/A	680 mW

recommended operating conditions

	MIN	MAX	UNIT
Supply voltage, V_{CC+}	3.5	18	V
Supply voltage, V_{CC-}	−3.5	−18	V

electrical characteristics over operating free-air temperature range, $V_{CC+} = 15$ V, $V_{CC-} = -15$ V (unless otherwise specified)

PARAMETER		TEST CONDITIONS		LF347			LF347B			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	$V_{IC} = 0$, $R_S = 10$ kΩ	$T_A = 25°C$		5	10		3	5	mV
			Full range			13			7	
$\alpha_{V_{IO}}$	Average temperature coefficient of input offset voltage	$V_{IC} = 0$, RS = 10 kΩ			18			18		μV/°C
I_{IO}	Input offset current†	$V_{IC} = 0$	$T_J = 25°C$		25	100		25	100	pA
			$T_J = 70°C$			4			4	nA
I_{IB}	Input bias current†	$V_{IC} = 0$	$T_J = 25°C$		50	200		50	200	pA
			$T_J = 70°C$			8			8	nA
V_{ICR}	Common-mode input voltage range			±11	−12 to 15		±11	−12 to 15		V
V_{OM}	Maximum peak output voltage swing	$R_L = 10$ kΩ		±12	±13.5		±12	±13.5		V
A_{VD}	Large-signal differential voltage	$V_O = \pm 10$ V, $R_L = 2$ kΩ	$T_A = 25°C$	25	100		50	100		V/mV
			Full range	15			25			
r_i	Input resistance	$T_J = 25°C$			10^{12}			10^{12}		Ω
CMRR	Common-mode rejection ratio	$R_S \leq 10$ kΩ		70	100		80	100		dB
k_{SVR}	Supply voltage rejection ratio	See Note 2		70	100		80	100		dB
I_{CC}	Supply current				8	11		8	11	mA

operating characteristics, $V_{CC+} = 15$ V, $V_{CC-} = -15$ V, $T_A = 25°C$

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{O1}/V_{O2}	Crosstalk attenuation	f = 1 kHz		120		dB
SR	Slew rate		8	13		V/μs
B_1	Unity-gain bandwidth			3		MHz
V_n	Equivalent input noise voltage	f = 1 kHz, $R_S = 100$ Ω		18		nV/√Hz
I_n	Equivalent input noise current	f = 1 kHz		0.01		pA/√Hz

† Input bias currents of a FET-input operational amplifier are normal junction reverse currents, which are temperature sensitive. Pulse techniques must be used that will maintain the junction temperatures as close to the ambient temperature as possible.

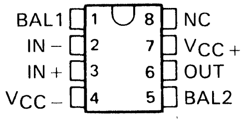
NOTE 2: Supply voltage rejection ratio is measured for both supply magnitudes increasing or decreasing simultaneously.

LF351
WIDE-BANDWIDTH DUAL JFET-INPUT OPERATIONAL AMPLIFIER

D2997, MARCH 1987—REVISED SEPTEMBER 1990

- **Low Input Bias Current**
  Typically 50 pA
- **Low Input Noise Voltage**
  Typically 18 nV/$\sqrt{\text{Hz}}$
- **Low Input Noise Current**
  Typically 0.01 pA/$\sqrt{\text{Hz}}$
- **Low Supply Current . . . Typically 1.8 mA**
- **High Input Impedance**
  Typically 10^{12} Ω
- **Low Total Harmonic Distortion**
- **Internally Trimmed Offset Voltage**
  Typically 10 mV
- **High Slew Rate . . . Typically 13 V/μs**
- **Wide Gain Bandwidth . . . Typically 3 MHz**
- **Pin Compatible with Standard 741**

D OR P PACKAGE
(TOP VIEW)



NC—No internal connection

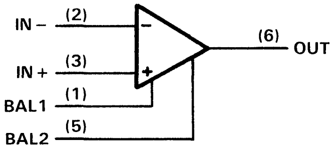
description

This device is a low-cost, high-speed, JFET-input operational amplifier with an internally trimmed input offset voltage. It requires low supply current yet maintains a large gain-bandwidth product and a fast slew rate. In addition, the matched high-voltage JFET input provides very low input bias and offset currents. It uses the same offset voltage adjustment circuits as the 741.

The LF351 can be used in applications such as high-speed integrators, digital-to-analog converters, sample-and-hold circuits, and many other circuits.

The LF351 is characterized for operation from 0°C to 70°C.

symbol (each amplifier)



AVAILABLE OPTIONS

SYMBOLIZATION		OPERATING TEMPERATURE RANGE	V_{IO} MAX at 25°C
DEVICE	PACKAGE SUFFIX		
LF351	D, P	−0°C to 70°C	10 mV

The D packages are available taped and reeled. Add the suffix R to the device type, (ie., LF351DR).

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC+}	18 V
Supply voltage, V_{CC-}	−18 V
Differential input voltage, V_{ID}	±30 V
Input voltage (see Note 1)	±15 V
Duration of output short circuit	Unlimited
Continuous total power dissipation	500 mW
Operating temperature range	0 °C to 70 °C
Storage temperature range	−65 °C to 150 °C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260 °C

NOTE 1: Unless otherwise specified, the absolute maximum negative input voltage is equal to the negative power supply voltage.

recommended operating conditions

	MIN	MAX	UNIT
Supply voltage, V_{CC+}	3.5	18	V
Supply voltage, V_{CC-}	−3.5	−18	V

electrical characteristics over operating free-air temperature range, $V_{CC+} = 15$ V, $V_{CC-} = -15$ V (unless otherwise specified)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	$V_{IC} = 0$, $R_S = 10$ kΩ	$T_A = 25$°C		5	10	mV
			Full range			13	
α_{VIO}	Average temperature coefficient of input offset voltage	$V_{IC} = 0$, $R_S = 10$ kΩ			10		µV/°C
I_{IO}	Input offset current†	$V_{IC} = 0$	$T_J = 25$°C		25	100	pA
			$T_J = 70$°C			4	nA
I_{IB}	Input bias current†	$V_{IC} = 0$	$T_J = 25$°C		50	200	pA
			$T_J = 70$°C			8	nA
V_{ICR}	Common-mode input voltage range			±11	−12 to 15		V
V_{OM}	Maximum peak output voltage swing	$R_L = 10$ kΩ		±12	±13.5		V
A_{VD}	Large-signal differential voltage	$V_O = \pm 10$ V, $R_L = 2$ kΩ	$T_A = 25$°C	25	200		V/mV
			Full range	15	200		
r_i	Input resistance	$T_J = 25$°C			10^{12}		Ω
CMRR	Common-mode rejection ratio	$R_S \leq 10$ kΩ		70	100		dB
k_{SVR}	Supply voltage rejection ratio	See Note 2		70	100		dB
I_{CC}	Supply current				1.8	3.4	mA

operating characteristics, $V_{CC+} = 15$ V, $V_{CC-} = -15$ V, $T_A = 25$°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SR	Slew rate		8	13		V/µs
B_1	Unity-gain bandwidth			3		MHz
V_n	Equivalent input noise voltage	f = 1 kHz, $R_S = 100$ Ω		18		nV/√Hz
I_n	Equivalent input noise current	f = 1 kHz		0.01		pA/√Hz

† Input bias currents of a FET-input operational amplifier are normal junction reverse currents, which are temperature sensitive. Pulse techniques must be used that will maintain the junction temperatures as close to the ambient temperature as possible.

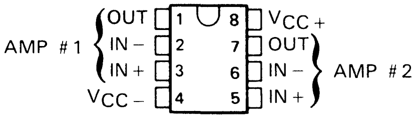
NOTE 2: Supply voltage rejection ratio is measured for both supply magnitudes increasing or decreasing simultaneously.

LF353
WIDE-BANDWIDTH DUAL JFET-INPUT OPERATIONAL AMPLIFIER

D2997, MARCH 1987—REVISED SEPTEMBER 1990

- **Low Input Bias Current**
  Typically 50 pA
- **Low Input Noise Current**
  Typically 0.01 pA/$\sqrt{\text{Hz}}$
- **Low Input Noise Voltage**
  Typically 18 nV/$\sqrt{\text{Hz}}$
- **Low Supply Current . . . Typically 3.6 mA**
- **High Input Impedance**
  Typically 10^{12} Ω
- **Internally Trimmed Offset Voltage**
- **Wide Gain Bandwidth . . . Typically 3 MHz**
- **High Slew Rate . . . Typically 13 V/μs**

D OR P PACKAGE
(TOP VIEW)



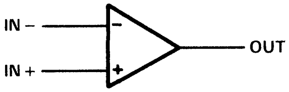
description

This device is a low-cost, high-speed, JFET-input operational amplifier with very low input offset voltage. It requires low supply current yet maintains a large gain-bandwidth product and a fast slew rate. In addition, the matched high-voltage JFET input provides very low input bias and offset currents.

The LF353 can be used in applications such as high-speed integrators, digital-to-analog converters, sample-and-hold circuits, and many other circuits.

The LF353 is characterized for operation from 0°C to 70°C.

symbol (each amplifier)



AVAILABLE OPTIONS

SYMBOLIZATION		OPERATING TEMPERATURE RANGE	V_{IO} MAX at 25°C
DEVICE	PACKAGE SUFFIX		
LF353	D, P	0°C to 70°C	10 mV

The D packages are available taped and reeled. Add the suffix R to the device type, (i.e. LP353DR).

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC+}	18 V
Supply voltage, V_{CC-}	−18 V
Differential input voltage, V_{ID}	±30 V
Input voltage (see Note 1)	±15 V
Duration of output short circuit	Unlimited
Continuous total power dissipation	500 mW
Operating temperature range	0°C to 70°C
Storage temperature range	−65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C

NOTE 1: Unless otherwise specified, the absolute maximum negative input voltage is equal to the negative power supply voltage.

recommended operating conditions

	MIN	MAX	UNIT
Supply voltage, V_{CC+}	3.5	18	V
Supply voltage, V_{CC-}	−3.5	−18	V

electrical characteristics over operating free-air temperature range, $V_{CC+} = 15$ V, $V_{CC-} = -15$ V (unless otherwise specified)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	$V_{IC} = 0$, $R_S = 10$ kΩ	$T_A = 25$°C		5	10	mV
			Full range			13	
α_{VIO}	Average temperature coefficient of input offset voltage	$V_{IC} = 0$, $R_S = 10$ kΩ			10		μV/°C
I_{IO}	Input offset current†	$V_{IC} = 0$	$T_J = 25$°C		25	100	pA
			$T_J = 70$°C			4	nA
I_{IB}	Input bias current†	$V_{IC} = 0$	$T_J = 25$°C		50	200	pA
			$T_J = 70$°C			8	nA
V_{ICR}	Common-mode input voltage range			±11	−12 to 15		V
V_{OM}	Maximum peak output voltage swing	$R_L = 10$ kΩ		±12	±13.5		V
A_{VD}	Large-signal differential voltage	$V_O = \pm 10$ V, $R_L = 2$ kΩ	$T_A = 25$°C	25	100		V/mV
			Full range	15			
r_i	Input resistance	$T_J = 25$°C			10^{12}		Ω
CMRR	Common-mode rejection ratio	$R_S \leq 10$ kΩ		70	100		dB
k_{SVR}	Supply voltage rejection ratio	See Note 2		70	100		dB
I_{CC}	Supply current				3.6	6.5	mA

operating characteristics, $V_{CC+} = 15$ V, $V_{CC-} = -15$ V, $T_A = 25$°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{O1}/V_{O2}	Crosstalk attenuation	f = 1 kHz		120		dB
SR	Slew rate		8	13		V/μs
B_1	Unity-gain bandwidth			3		MHz
V_n	Equivalent input noise voltage	f = 1 kHz, $R_S = 100$ Ω		18		nV/√Hz
I_n	Equivalent input noise current	f = 1 kHz		0.01		pA/√Hz

† Input bias currents of a FET-input operational amplifier are normal junction reverse currents, which are temperature sensitive. Pulse techniques must be used that will maintain the junction temperatures as close to the ambient temperature as possible.

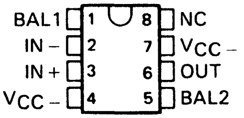
NOTE 2: Supply voltage rejection ratio is measured for both supply magnitudes increasing or decreasing simultaneously.

LF411C
JFET-INPUT OPERATIONAL AMPLIFIER

D2997, MARCH 1987—REVISED SEPTEMBER 1990

- **Low Input Bias Current**
  Typically 50 pA
- **Low Input Noise Current**
  Typically 0.01 pA/$\sqrt{Hz}$
- **Low Supply Current . . . Typically 2.0 mA**
- **High Input Impedance**
  Typically 10^{12} Ω
- **Low Total Harmonic Distortion**
- **Low 1/f Noise Corner . . . Typically 50 Hz**

D OR P PACKAGE
(TOP VIEW)



NC—No internal connection

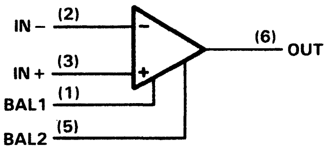
description

This device is a low-cost, high-speed, JFET-input operational amplifier with very low input offset voltage and a maximum input offset voltage drift. It requires low supply current yet maintains a large gain-bandwidth product and a fast slew rate. In addition, the matched high-voltage JFET input provides very low input bias and offset currents.

The LF411C can be used in applications such as high-speed integrators, digital-to-analog converters, sample-and-hold circuits, and many other circuits.

The LF411C is characterized for operation from 0°C to 70°C.

symbol



AVAILABLE OPTIONS

T_A	V_{IO} MAX AT 25°C	PACKAGE	
		SMALL-OUTLINE (D)	PLASTIC DIP (P)
0°C to 70°C	2 mV	LF411CD	LF411CP

D package is available taped and reeled. Add "R" suffix to device type. (e.g. LF411CDR)

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC+}	18 V
Supply voltage, V_{CC-}	−18 V
Differential input voltage, V_{ID}	±30 V
Input voltage (see Note 1)	±15 V
Duration of output short circuit	Unlimited
Continuous total power dissipation	500 mW
Operating temperature range	0°C to 70°C
Storage temperature range	−65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C

NOTE 1: Unless otherwise specified, the absolute maximum negative input voltage is equal to the negative power supply voltage.

recommended operating conditions

	MIN	MAX	UNIT
Supply voltage, V_{CC+}	3.5	18	V
Supply voltage, V_{CC-}	−3.5	−18	V

electrical characteristics over operating free-air temperature range, $V_{CC+} = 15$ V, $V_{CC-} = -15$ V (unless otherwise specified)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	$V_{IC} = 0$, $R_S = 10$ kΩ, $T_A = 25$°C			0.8	2	mV
α_{VIO}	Average temperature coefficient of input offset voltage	$V_{IC} = 0$, $R_S = 10$ kΩ			10	20†	μV/°C
I_{IO}	Input offset current‡	$V_{IC} = 0$	$T_J = 25$°C		25	100	pA
			$T_J = 70$°C			2	nA
I_{IB}	Input bias current‡	$V_{IC} = 0$	$T_J = 25$°C		50	200	pA
			$T_J = 70$°C			4	nA
V_{ICR}	Common-mode input voltage range			±11	−11.5 to 14.5		V
V_{OM}	Maximum peak output voltage swing	$R_L = 10$ kΩ		±12	±13.5		V
A_{VD}	Large-signal differential voltage	$V_O = \pm 10$ V, $R_L = 2$ kΩ	$T_A = 25$°C	25	200		V/mV
			Full range	15	200		
r_i	Input resistance	$T_J = 25$°C			10^{12}		Ω
CMRR	Common-mode rejection ratio	$R_S \leq 10$ kΩ		70	100		dB
k_{SVR}	Supply voltage rejection ratio	See Note 2		70	100		dB
I_{CC}	Supply current				2	3.4	mA

operating characteristics, $V_{CC+} = 15$ V, $V_{CC-} = -15$ V, $T_A = 25$°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SR	Slew rate		8	13		V/μs
B_1	Unity-gain bandwidth		2.7	3		MHz
V_n	Equivalent input noise voltage	f = 1 kHz, $R_S = 100$ Ω		18		nV/√Hz
I_n	Equivalent input noise current	f = 1 kHz		0.01		pA/√Hz

† At least 90% of the devices meet this limit for α_{VIO}.

‡ Input bias currents of a FET-input operational amplifier are normal junction reverse currents, which are temperature sensitive. Pulse techniques must be used that will maintain the junction temperatures as close to the ambient temperature as possible.

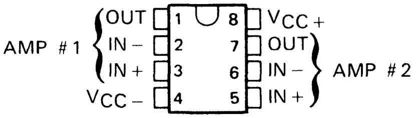
NOTE 2: Supply voltage rejection ratio is measured for both supply magnitudes increasing or decreasing simultaneously.

LF412C
DUAL JFET-INPUT OPERATIONAL AMPLIFIER

D2997, MARCH 1987–REVISED SEPTEMBER 1990

- **Low Input Bias Current**
  Typically 50 pA
- **Low Input Noise Current**
  Typically 0.01 pA/$\sqrt{\text{Hz}}$
- **Low Supply Current . . . Typically 4.5 mA**
- **High Input Impedance**
  Typically 10^{12} Ω
- **Internally Trimmed Offset Voltage**
- **Wide Gain Bandwidth . . . Typically 3 MHz**
- **High Slew Rate . . . Typically 13 V/μs**

D OR P PACKAGE
(TOP VIEW)



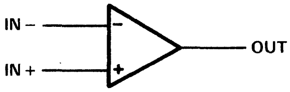
description

This device is a low-cost, high-speed, JFET-input operational amplifier with very low input offset voltage and a specified maximum input offset voltage drift. It requires low supply current yet maintains a large gain bandwidth product and a fast slew rate. In addition, the matched high-voltage JFET input provides very low input bias and offset currents.

The LF412C can be used in applications such as high-speed integrators, digital-to-analog converters, sample-and-hold circuits, and many other circuits.

The LF412C is characterized for operation from 0°C to 70°C.

symbol (each amplifier)



AVAILABLE OPTIONS

SYMBOLIZATION		OPERATING TEMPERATURE RANGE	V_{IO} MAX at 25°C
DEVICE	PACKAGE SUFFIX		
LF412C	D, P	0°C to 70°C	3 mV

The D packages are available taped and reeled. Add the suffix R to the device type, (i.e. LF412CDR).

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC+}	18 V
Supply voltage, V_{CC-}	−18 V
Differential input voltage, V_{ID}	±30 V
Input voltage (see Note 1)	±15 V
Duration of output short-circuit	Unlimited
Continuous total power dissipation	500 mW
Operating temperature range	0°C to 70°C
Storage temperature range	−65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C

NOTE 1: Unless otherwise specified, the absolute maximum negative input voltage is equal to the negative power supply voltage.

recommended oprating conditions

	MIN	MAX	UNIT
Supply voltage, V_{CC+}	3.5	18	V
Supply voltage, V_{CC-}	−3.5	−18	V

electrical characteristics over operating free-air temperature range, $V_{CC+} = 15$ V, $V_{CC-} = -15$ V (unless otherwise specified)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	$V_{IC} = 0$, $R_S = 10$ kΩ, $T_A = 25$°C			1	3	mV
α_{VIO}	Average temperature coefficient of input offset voltage	$V_{IC} = 0$, $R_S = 10$ kΩ			10	20†	μV/°C
I_{IO}	Input offset current‡	$V_{IC} = 0$	$T_J = 25$°C		25	100	pA
			$T_J = 70$°C			2	nA
I_{IB}	Input bias current‡	$V_{IC} = 0$	$T_J = 25$°C		50	200	pA
			$T_J = 70$°C			4	nA
V_{ICR}	Common-mode input voltage range			±11	−11.5 to 14.5		V
V_{OM}	Maximum peak output voltage swing	$R_L = 10$ kΩ		±12	±13.5		V
A_{VD}	Large-signal differential voltage	$V_O = \pm 10$ V, $R_L = 2$ kΩ	$T_A = 25$°C	25	200		V/mV
			Full range	15	200		
r_i	Input resistance	$T_J = 25$°C			10^{12}		Ω
CMRR	Common-mode rejection ratio	$R_S \leq 10$ kΩ		70	100		dB
k_{SVR}	Supply voltage rejection ratio	See Note 2		70	100		dB
I_{CC}	Supply current				4.5	6.8	mA

operating characteristics, $V_{CC+} = 15$ V, $V_{CC-} = -15$ V, $T_A = 25$°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{O1}/V_{O2}	Crosstalk attenuation	f = 1 kHz		120		dB
SR	Slew rate		8	13		V/μs
B_1	Unity-gain bandwidth		2.7	3		MHz
V_n	Equivalent input noise voltage	f = 1 kHz, $R_S = 100$ Ω		18		nV/√Hz
I_n	Equivalent input noise current	f = 1 kHz		0.01		pA/√Hz

† At least 90% of the devices meet this limit for α_{VIO}.

‡ Input bias currents of a FET-input operational amplifier are normal junction reverse currents, which are temperature sensitive. Pulse techniques must be used that will maintain the junction temperatures as close to the ambient temperature as possible.

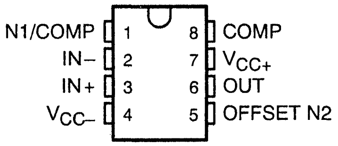
NOTE 2: Supply voltage rejection ratio is measured for both supply magnitudes increasing or decreasing simultaneously.

LM101A, LM201A, LM301A
HIGH-PERFORMANCE OPERATIONAL AMPLIFIERS

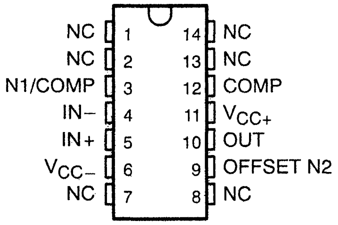
D961, OCTOBER 1979 – REVISED SEPTEMBER 1990

- **Low Input Currents**
- **Low Input Offset Parameters**
- **Frequency and Transient Response Characteristics Adjustable**
- **Short-Circuit Protection**
- **Offset-Voltage Null Capability**
- **No Latch-Up**
- **Wide Common-Mode and Differential Voltage Ranges**
- **Same Pin Assignments as uA709**
- **Designed to be Interchangeable with National Semiconductor LM101A and LM301A**

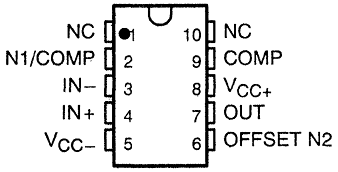
D, JG, OR P PACKAGE
(TOP VIEW)



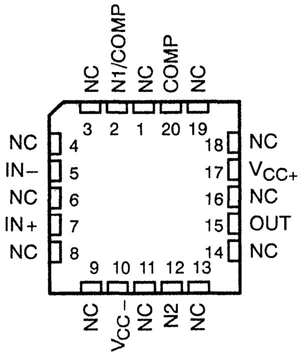
LM101A
W FLAT PACKAGE
(TOP VIEW)



LM101A
U FLAT PACKAGE
(TOP VIEW)



LM101A
FK CHIP-CARRIER PACKAGE
(TOP VIEW)



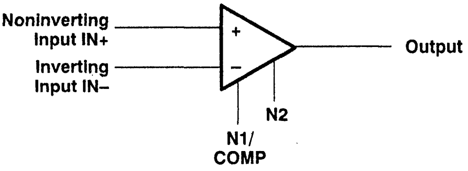
NC – No internal connection

description

The LM101A, LM201A, and LM301A are high-performance operational amplifiers featuring very low input bias current and input offset voltage and current to improve the accuracy of high-impedance circuits using these devices. The high common-mode input voltage range and the absence of latch-up make these amplifiers ideal for voltage-follower applications. The devices are protected to withstand short circuits at the output. The external compensation of these amplifiers allows the changing of the frequency response (when the closed-loop gain is greater then unity) for applications requiring wider bandwidth or higher slew rate. A potentiometer may be connected between the offset-null inputs (N1 and N2), as shown in Figure 7, to null out the offset voltage.

The LM101A is characterized for operation over the full military temperature range of −55°C to 125°C, the LM201A is characterized for operation from −25°C to 85°C, and the LM301A is characterized for operation from 0°C to 70°C.

symbol



AVAILABLE OPTIONS

T_A	V_{IO} MAX at 25°C	PACKAGE					
		SMALL OUTLINE (D)	CHIP CARRIER (FK)	CERAMIC DIP (JG)	PLASTIC DIP (P)	FLAT PACK (U)	FLAT PACK (W)
0°C to 70°C	7.5 mV	LM301AD	–	–	LM301AP	–	–
−25°C to 85°C	2 mV	LM201AD	–	–	LM201AP	–	–
−55°C to 125°C	2 mV	LM101AD	LM101AFK	LM101AJG	LM101AP	LM101AU	LM101AW

The D package is available taped and reeled. Add the suffix R to the device type, (i.e., LM301ADR).

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

		LM101A	LM201A	LM301A	UNIT
Supply voltage V_{CC+} (see Note 1)		22	22	18	V
Supply voltage V_{CC-} (see Note 1)		−22	−22	−18	V
Differential input voltage (see Note 2)		±30	±30	±30	V
Input voltage (either input, see Notes 1 and 3)		±15	±15	±15	V
Voltage between either offset null terminal (N1/N2) and V_{CC-}		−0.5 to 2	−0.5 to 2	−0.5 to 2	V
Duration of output short-circuit (see Note 4)		unlimited	unlimited	unlimited	
Continuous total power dissipation		See Dissipation Rating Table			
Operating free-air temperature range		−55 to 125	−25 to 85	0 to 70	°C
Storage temperature range		−65 to 150	−65 to 150	−65 to 150	°C
Case temperature for 60 seconds: FK package		260			°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds	JG, U, or W package	300			°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	D or P package	260	260	260	°C

NOTES: 1. All voltage values, unless otherwise noted, are with respect to the midpoint between V_{CC+} and V_{CC-}.
2. Differential voltages are at the noninverting input terminal with respect to the inverting input terminal.
3. The magnitude of the input voltage must never exceed the magnitude of the supply voltage or 15 V, whichever is less.
4. The output may be shorted to ground or either power supply. For the LM101A only, the unlimited duration of the short-circuit applies at (or above) 125°C case temperature or 75°C free-air temperature. For the LM201A only, the unlimited duration of the short-circuit applies at (or below) 85°C case temperatuare or 75°C free-air temperature.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR	DERATE ABOVE T_A	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING	$T_A = 125°C$ POWER RATING
D	500 mW	5.8 mW/°C	64°C	464 mW	377 mW	145 mW
FK	500 mW	11.0 mW/°C	105°C	500 mW	500 mW	275 mW
JG	500 mW	8.4 mW/°C	90°C	500 mW	500 mW	210 mW
P	500 mW	8.0 mW/°C	87°C	500 mW	500 mW	200 mW
U	500 mW	5.4 mW/°C	57°C	432 mW	351 mW	135 mW
W	500 mW	8.0 mW/°C	87°C	500 mW	500 mW	200 mW

recommended operating conditions

	MIN	MAX	UNIT
Supply voltage, V_{CC+}	5	18	V
Supply voltage, V_{CC-}	−5	−18	

electrical characteristics at specified free-air temperature, C_C = 30 pF (see Note 5)

PARAMETER		TEST CONDITIONS†		LM101A, LM201A			LM301A			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_O = 0	25°C		0.6	2		2	7.5	mV
			Full range			3			10	
α_{VIO}	Average temperature coefficient of input offset voltage	V_O = 0	Full range		3	15		6	30	µV/°C
I_{IO}	Input offset current		25°C		1.5	10		3	50	nA
			Full range			20			70	
α_{IIO}	Average temperature coefficient of input offset current	T_A = −55°C to 25°C			0.02	0.2				nA/°C
		T_A = 25°C to MAX			0.01	0.1				
		T_A = 0°C to 25°C						0.02	0.6	
		T_A = 25°C to 70°C						0.01	0.3	
I_{IB}	Input bias current		25°C		30	75		70	250	nA
			Full range			100			300	
V_{ICR}	Common-mode input voltage range	See Note 6	Full range	±15			±12			V
V_{OPP}	Maximum peak-to-peak output voltage swing	$V_{CC\pm}$ = ±15 V, R_L = 10 kΩ	25°C	24	28		24	28		V
			Full range	24			24			
		$V_{CC\pm}$ = ±15 V, R_L = 2 kΩ	25°C	20	26		20	26		
			Full range	20			20			
A_{VD}	Large-signal differential voltage amplification	$V_{CC\pm}$ = ±15 V, V_O = ±10 V, $R_L \geq$ 2 kΩ	25°C	50	200		25	200		V/mV
			Full range	25			15			
r_i	Input resistance		25°C	1.5	4		0.5	2		MΩ
CMRR	Common-mode rejection ratio	$V_{IC} = V_{ICR}$ min	25°C	80	98		70	90		dB
			Full range	80			70			
k_{SVR}	Supply voltage rejection ratio ($\Delta V_{CC}/\Delta V_{IO}$)		25°C	80	98		70	96		dB
			Full range	80			70			
I_{CC}	Supply current	No load, V_O = 0, See Note 6	25°C		1.8	3		1.8	3	mA
			MAX		1.2	2.5				

† All characteristics are measured under open-loop conditions with zero common-mode input voltage unless otherwise specified. Full range for LM101A is −55°C to 125°C, for LM201A is −25°C to 85°C, and for LM301A is 0°C to 70°C.

NOTES: 5. Unless otherwise noted, $V_{CC\pm}$ = ±5 V to ±20 V for LM101A and LM201A, and $V_{CC\pm}$ = ±5 V to ±15 V for LM301A. All typical values are at $V_{CC\pm}$ = ±15 V.

6. For LM101A and LM201A, $V_{CC\pm}$ = ±20 V. For LM301A, $V_{CC\pm}$ = ±15 V.

TYPICAL CHARACTERISTICS

INPUT OFFSET CURRENT
vs
FREE-AIR TEMPERATURE

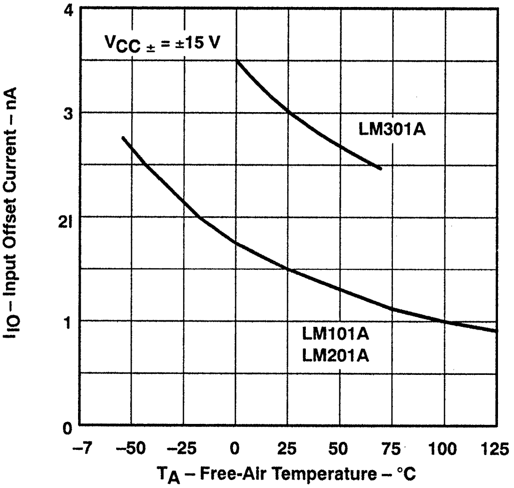


Figure 1

INPUT BIAS CURRENT
vs
FREE-AIR TEMPERATURE

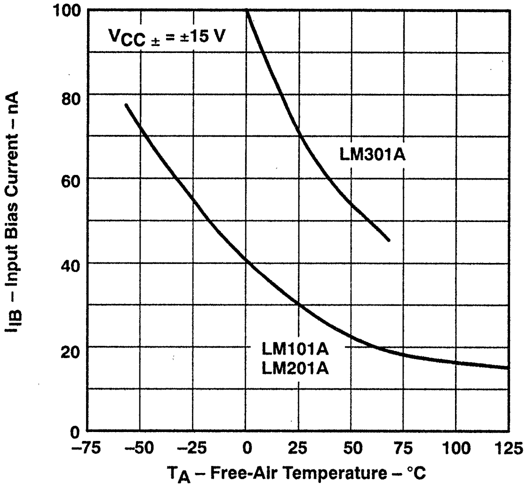


Figure 2

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE
(WITH SINGLE-POLE COMPENSATION)
vs
FREQUENCY

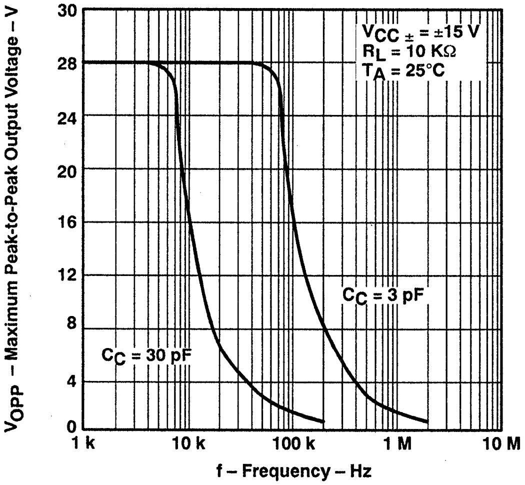


Figure 3

OPEN-LOOP LARGE-SIGNAL DIFFERENTIAL
VOLTAGE AMPLIFICATION
vs
SUPPLY VOLTAGE

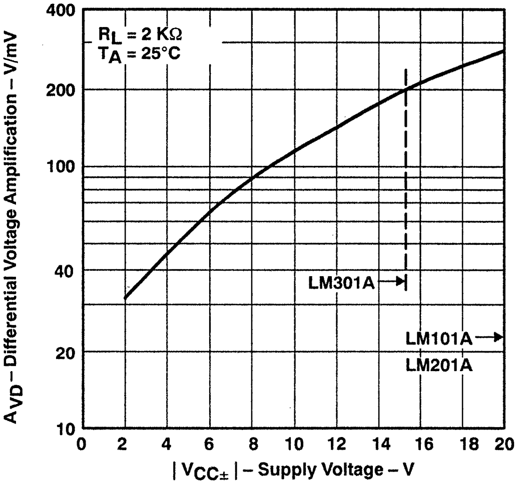


Figure 4

TYPICAL CHARACTERISTICS

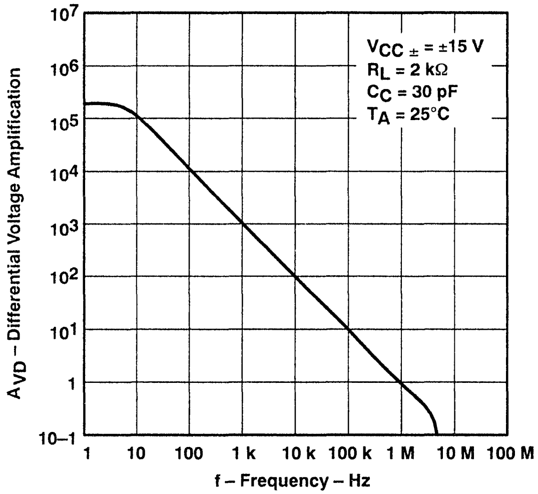


Figure 5

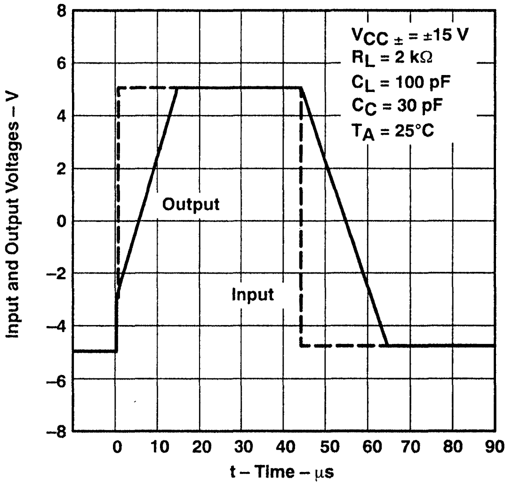
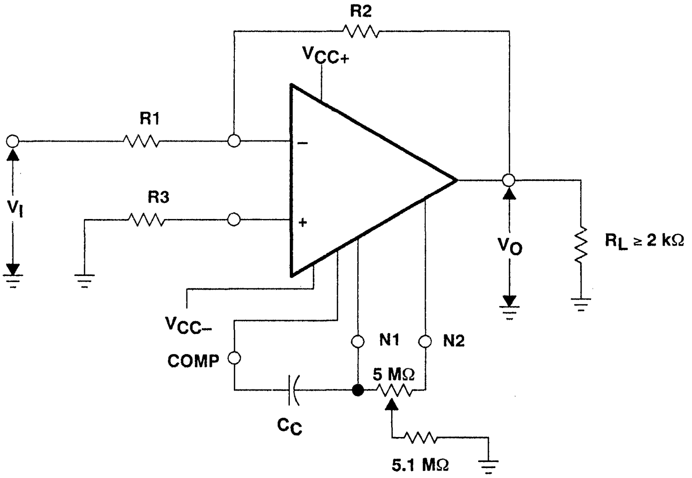


Figure 6

TYPICAL APPLICATION DATA



$$\frac{V_O}{V_I} = -\frac{R2}{R1}$$

$$C_C \geq \frac{R1 \cdot 30\ \text{pF}}{R1 + R2}$$

$$R3 = \frac{R1 \cdot R2}{R1 + R2}$$

Figure 7. Inverting Circuit with Adjustable Gain, Single-Pole Compensation, and Offset Adjustment

LM107, LM207, LM307
HIGH-PERFORMANCE OPERATIONAL AMPLIFIERS

D962, DECEMBER 1970—REVISED SEPTEMBER 1990

- **Low Input Currents**
- **No Frequency Compensation Required**
- **Low Input Offset Parameters**
- **Short-Circuit Protection**
- **No Latch-Up**
- **Wide Common-Mode and Differential Voltage Ranges**

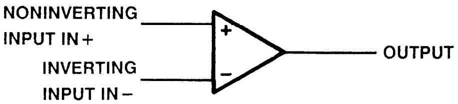
description

The LM107, LM207, and LM307 are high-performance operational amplifiers featuring very low input bias current and input offset voltage and current to improve the accuracy of high-impedance circuits using these devices.

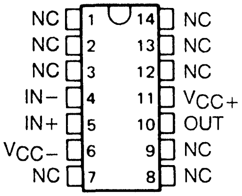
The high common-mode input voltage range and the absence of latch-up make these amplifiers ideal for voltage follower applications. The devices are short-circuit protected and the internal frequency compensation ensures stability without external components.

The LM107 is characterized for operation over the full military temperature range of −55°C to 125°C, the LM207 is characterized for operation from −25°C to 85°C, and the LM307 is characterized for operation from 0°C to 70°C.

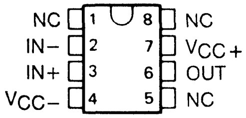
symbol



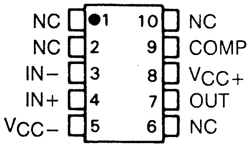
LM107 . . . J OR W PACKAGE
(TOP VIEW)



LM107 . . . JG PACKAGE
LM207, LM307 . . . D OR P PACKAGE
(TOP VIEW)



LM107 . . . U FLAT PACKAGE
(TOP VIEW)



NC—No internal connection

AVAILABLE OPTIONS

T_A	V_{IO} MAX AT 25°C	PACKAGE					
		SMALL OUTLINE (D)	CERAMIC (J)	CERAMIC DIP (JG)	PLASTIC DIP (P)	FLAT PACK (U)	FLAT PACK (W)
0°C to 70°C	7.5 mV	LM307D	—	—	LM307P	—	—
−25°C to 85°C	2 mV	LM207D	—	—	LM207P	—	—
−55°C to 125°C	2 mV	—	LM107J	LM107JG	—	LM107U	LM107W

The D package is available taped and reeled. Add the suffix R to the device type, (e.g., LM307DR).

TEXAS INSTRUMENTS
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

	LM107	LM207	LM307	UNIT
Supply voltage V_{CC+} (see Note 1)	22	22	18	V
Supply voltage V_{CC-} (see Note 1)	−22	−22	−18	V
Differential input voltage (see Note 2)	±30	±30	±30	V
Input voltage (either input, see Notes 1 and 3)	±15	±15	±15	V
Duration of output short-circuit (see Note 4)	unlimited	unlimited	unlimited	
Continuous total dissipation	See Dissipation Rating Table			
Operating free-air temperature range	−55 to 125	−25 to 85	0 to 70	°C
Storage temperature range	−65 to 150	−65 to 150	−65 to 150	°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: J, JG, U, or W package	300			°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D or P package		260	260	°C

NOTES:
1. All voltage values, unless otherwise noted, are with respect to the midpoint between V_{CC+} and V_{CC-}.
2. Differential voltages are at the noninverting input terminal with respect to the inverting input terminal.
3. The magnitude of the input voltage must never exceed the magnitude of the supply voltage or 15 volts, whichever is less.
4. The output may be shorted to ground or either power supply. For the LM107 only, the unlimited duration of the short-circuit applies at (or below) 125°C case temperature or 75°C free-air temperature. For the LM207 only, the unlimited duration of the short-circuit applies at (or below) 85°C case temperature or 75°C free air temperature.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR	DERATE ABOVE T_A	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING	$T_A = 125°C$ POWER RATING
D	500 mW	5.8 mW/°C	64°C	464 mW	377 mW	–
J	500 mW	11.0 mW/°C	105°C	500 mW	500 mW	275 mW
JG	500 mW	8.4 mW/°C	90°C	500 mW	500 mW	210 mW
P	500 mW	N/A	N/A	500 mW	500 mW	–
U	500 mW	5.4 mW/°C	57°C	432 mW	351 mW	135 mW
W	500 mW	8.0 mW/°C	87°C	500 mW	500 mW	200 mW

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC+}	2		18	V
Supply voltage, V_{CC-}	−2		−18	V

electrical characteristics at specified free-air temperature (see Note 5)

PARAMETER		TEST CONDITIONS†		LM107, LM207			LM307			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	$V_O = 0$	25°C		0.6	2		2	7.5	mV
			Full range			3			10	
α_{VIO}	Average temperature coefficeint of input offset voltage	$V_O = 0$	Full range		3	15		6	30	μV/°C
I_{IO}	Input offset current	$V_O = 0$	25°C		1.5	10		3	50	nA
			Full range			20			70	
α_{IIO}	Average temperature coefficeint of input offset current	T_A = −55°C to 25°C			0.02	0.2				nA/°C
		T_A = 25°C to MAX			0.01	0.1				
		T_A = 0°C to 25°C						0.002	0.6	
		T_A = 25°C to 70°C						0.001	0.3	
I_{IB}	Input bias current		25°C		30	75		70	250	nA
			Full range			100			300	
V_{ICR}	Common-mode input voltage range	See Note 6	Full range	±15			±12			V
V_{OPP}	Maximum peak-to-peak output voltage swing	$V_{CC\pm} = \pm 15$ V, $R_L = 10$ kΩ	25°C	24	28		24	28		V
			Full range	24			24			
		$V_{CC\pm} = \pm 15$ V, $R_L = 2$ kΩ	25°C	20	26		20	26		
			Full range	20			20			
A_{VD}	Large-signal differential voltage amplification	$V_{CC\pm} = \pm 15$ V, $V_O = \pm 10$ V, $R_L \geq 2$ kΩ	25°C	50	200		25	200		V/mV
			Full range	25			15			
r_i	Input resistance		25°C	1.5	4		0.5	2		MΩ
CMRR	Common-mode rejection ratio	$V_{IC} = V_{ICR}$ min	25°C	80	98		70	90		dB
			Full range	80			70			
k_{SVR}	Supply voltage rejection ratio $(\Delta V_{CC}/\Delta V_{IO})$		25°C	80	98		70	96		dB
			Full range	80			70			
I_{CC}	Supply current	No load, $V_O = 0$, See Note 6	25°C		1.8	3		1.8	3	mA
			MAX		1.2	2.5				

†All characteristics are measured under open-loop conditions with zero common-mode input voltage unless otherwise specified. Full range for LM107 is −55°C to 125°C, for LM207 is −25°C to 85°C, and for LM307 is 0°C to 70°C.

NOTES: 5. Unless otherwise note $V_{CC\pm} = \pm 5$ V to ±20 V for LM107 and LM207, and $V_{CC\pm} = 5$ V to ±15 V for LM307. All typical values are at $V_{CC\pm} = \pm 15$ V.

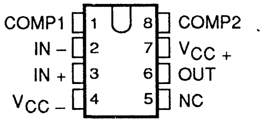
6. For LM107 and LM207, $V_{CC\pm} = \pm 20$ V. For LM307, $V_{CC\pm} = \pm 15$V.

LM108, LM108A, LM208, LM208A, LM308, LM308A OPERATIONAL AMPLIFIERS

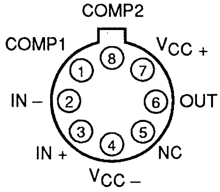
D2808, OCTOBER 1983 – REVISED FEBRUARY 1991

- **Input Offset Current . . . 200 pA Max at 25°C for LM108, LM108A, LM208, LM208A**
- **Input Bias Current . . . 2 nA Max at 25°C for LM108, LM108A, LM208, LM208A**
- **Supply Current . . . 600 µA Max at 25°C for LM108, LM108A, LM208, LM208A**
- **Input Offset Voltage . . . 500 µV Max at 25°C for LM108A, LM208A, LM308A**
- **Offset Voltage Temperature Coefficient . . . 5 µV/°C Max for LM108A, LM208A, LM308A**
- **Supply Voltage Range . . . ±2 V to ±18 V**
- **Applications:**
  - **Integrators**
  - **Transducer Amplifiers**
  - **Analog Memories**
  - **Light Meters**
- **Designed To Be Interchangeable With National LM108 Series and Linear Technology LM108 Series**

D, JG, OR P PACKAGE
(TOP VIEW)

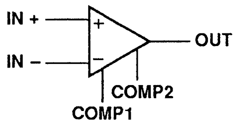


L PACKAGE
(TOP VIEW)



NC – No internal connection
Pin 4 (L package) is in electrical contact with the case.

symbol



description

The LM108 series of precision operational amplifiers is particularly well-suited for high-source-impedance applications requiring low input offset and bias currents as well as low power dissipation. Unlike FET input amplifiers, the input offset and bias currents of the LM108 series do not vary significantly with temperature. Advanced design, processing, and testing techniques make this series a superior choice over previous devices. For applications requiring higher performance, see the LT1008 and LT1012.

The LM108 and LM108A are characterized for operation over the full military temperature range of −55°C to 125°C. The LM208 and LM208A are characterized for operation from −40°C to 105°C. The LM308 and LM308A are characterized for operation from 0°C to 70°C.

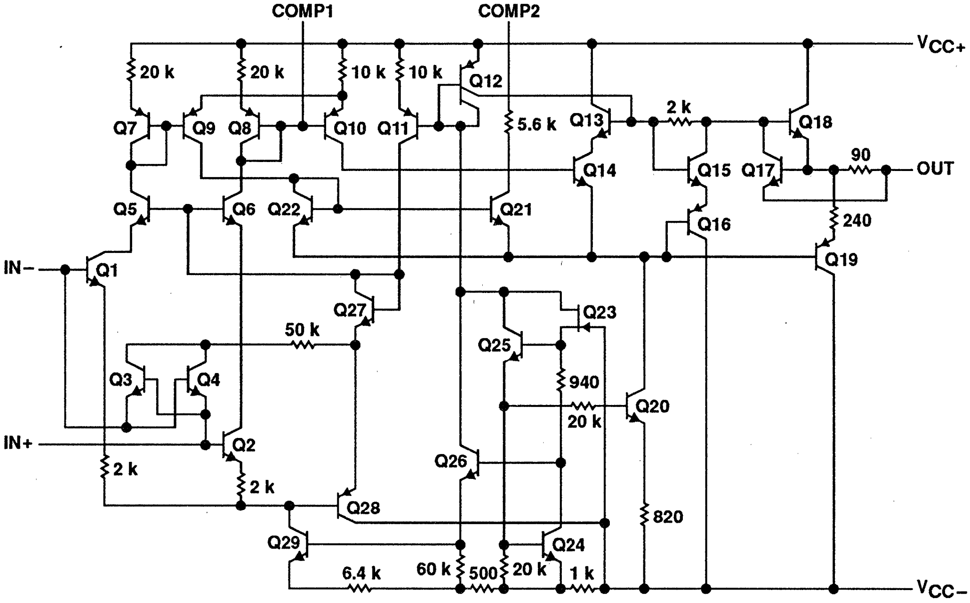
AVAILABLE OPTIONS

T_A	V_{IO} max AT 25°C	PACKAGE			
		SMALL OUTLINE (D)	CERAMIC DIP (JG)	METAL CAN (L)	PLASTIC DIP (P)
0°C to 70°C	0.5 mV	LM308AD	———	———	LM308AP
	7.5 mV	LM308D	———	———	LM308P
– 40°C to 105°C	0.5 mV	LM208AD	———	———	LM208AP
	2 mV	LM208D	———	———	LM208P
– 55°C to 125°C	0.5 mV	LM108AD	LM108AJG	LM108AL	LM108AP
	2 mV	LM108D	LM108JG	LM108L	LM108P

The D package is available taped and reeled. Add the suffix R to the device type (e.g., LM308ADR).

TEXAS INSTRUMENTS

schematic



All resistor values shown are nominal and in ohms.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC+} (see Note 1):	LM108, LM108A, LM208, LM208A	20 V
	LM308, LM308A	18 V
Supply voltage, V_{CC-} (see Note 1):	LM108, LM108A, LM208, LM208A	−20 V
	LM308, LM308A	−18 V
Input voltage range, V_I (see Note 2)		±15 V
Differential input current (see Notes 3 and 4)		±10 mA
Duration of output short-circuit at (or below) 25°C (see Note 5)		unlimited
Operating free-air temperature range, T_A:	LM108, LM108A	−55°C to 125°C
	LM208, LM208A	−40°C to 105°C
	LM308, LM308A	0°C to 70°C
Storage temperature range		−65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D or P package		260°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: JG or L package		300°C

NOTES: 1. All voltage values, unless otherwise noted, are with respect to the midpoint between V_{CC+} and V_{CC-}.
2. The magnitude of the input voltage must never exceed the magnitude of the supply voltage or 15 V, whichever is less.
3. The inputs are shunted with two opposite-facing base-emitter diodes for over-voltage protection. Therefore, excessive current will flow if a differential input voltage in excess of approximately 1 V is applied between the inputs unless some limiting resistance is used.
4. Differential voltages are at the noninverting input terminal with respect to the inverting input terminal.
5. The output may be shorted to ground or either power supply.

recommended operating conditions

	LM108, LM108A			LM208, LM208A			LM308, LM308A			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC+}	5		20	5		20	5		20	V
Supply voltage, V_{CC-}	-5		-20	-5		-20	-5		-20	V
Operating free-air temperature, T_A	−55		125	−40		85	0		70	°C

electrical characteristics at specified free-air temperature, $V_{CC\pm} = \pm 5$ V to ± 20 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A†	LM108A, LM208A			LM108, LM208			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	$R_S = 50\ \Omega$	25°C		0.3	0.5		0.7	2	mV
			Full range			1			3	
α_{VIO}	Temperature coefficient of input offset voltage		Full range		1	5*		3	15*	µV/°C
I_{IO}	Input offset current		25°C		0.05	0.2		0.05	0.2	nA
			Full range			0.4			0.4	
α_{IIO}	Temperature coefficient of input offset current		Full range		0.5	2.5*		0.5	2.5*	pA/°C
I_{IB}	Input bias current		25°C		0.5	2		0.5	2	nA
			Full range			3			3	
V_{ICR}	Common-mode input voltage range	$V_{CC\pm} = \pm 15$ V	Full range	±13.5			±13.5			V
V_{OM}	Maximum peak output voltage swing	$V_{CC\pm} = \pm 15$ V, $R_L = 10\ k\Omega$	Full range	±13			±13			V
A_{VD}	Large-signal differential voltage amplification	$V_{CC\pm} = \pm 15$ V, $V_O = \pm 10$ V, $R_L \geq 10\ k\Omega$	25°C	80	300		50	300		V/mV
			Full range	40			25			
r_i	Input resistance		25°C	30*	70		30*	70		MΩ
CMRR	Common-mode rejection ratio		Full range	96			85			dB
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm} / \Delta V_{IO}$)		Full range	96			80			dB
I_{CC}	Supply current		25°C		0.3	0.6		0.3	0.6	mA
			105°C, 125°C			0.4			0.4	

*On products compliant to MIL-STD-883, Class B, these parameters are not production tested.

†Full range is −40°C to 105°C for the LM208 and LM208A and −55°C to 125°C for the LM108 and LM108A.

electrical characteristics at specified free-air temperature, $V_{CC\pm}$ = ±5 V to ±15 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A†	LM308A			LM308			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	R_S = 50 Ω	25°C		0.3	0.5		2	7.5	mV
			Full range			0.73			10	
α_{VIO}	Temperature coefficient of input offset voltage		Full range		2	5		6	30	μV/°C
I_{IO}	Input offset current		25°C		0.2	1		0.2	1	nA
			Full range			1.5			1.5	
α_{IIO}	Temperature coefficient of input offset current		Full range		2	10		2	10	pA/°C
I_{IB}	Input bias current		25°C		1.5	7		1.5	7	nA
			Full range			10			10	
V_{ICR}	Common-mode input voltage range	$V_{CC\pm}$ = ±15 V	Full range	±14			±14			V
V_{OM}	Maximum peak output voltage swing	$V_{CC\pm}$ = ±15 V, R_L = 10 kΩ	Full range	±13			±13			V
A_{VD}	Large-signal differential voltage amplification	$V_{CC\pm}$ = ±15 V, V_O = ±10 V, R_L ≥ 10 kΩ	25°C	80	300		25	300		V/mV
			Full range	60			15			
r_i	Input resistance		25°C	10	40		10	40		MΩ
CMRR	Common-mode rejection ratio		Full range	96			80			dB
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm} / \Delta V_{IO}$)		Full range	96			80			dB
I_{CC}	Supply current		25°C		0.3	0.8		0.3	0.8	mA

†Full range is 0°C to 70°C.

TYPICAL CHARACTERISTICS[†]

EQUIVALENT INPUT OFFSET VOLTAGE vs MATCHED SOURCE RESISTANCE

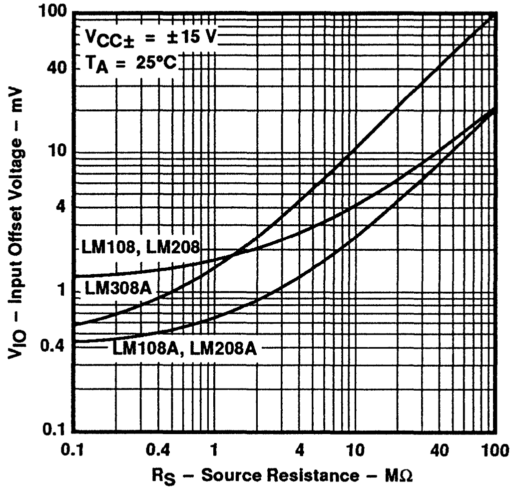


Figure 1

TEMPERATURE COEFFICIENT OF EQUIVALENT INPUT OFFSET VOLTAGE vs MATCHED SOURCE RESISTANCE

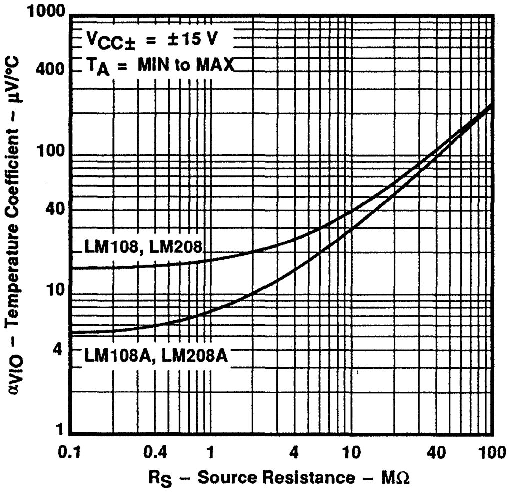


Figure 2

LM108, LM108A, LM208, LM208A INPUT BIAS and OFFSET CURRENTS vs FREE-AIR TEMPERATURE

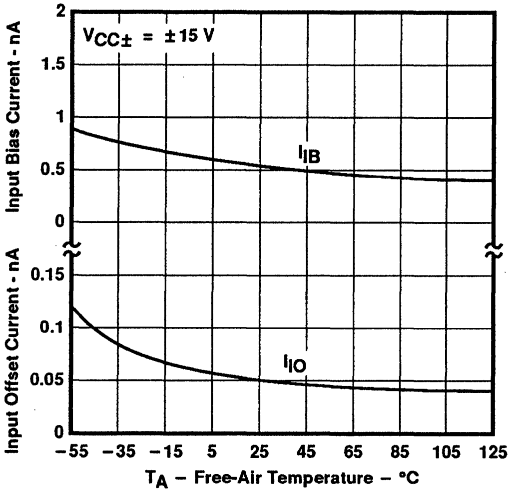


Figure 3

SUPPLY CURRENT vs SUPPLY VOLTAGE

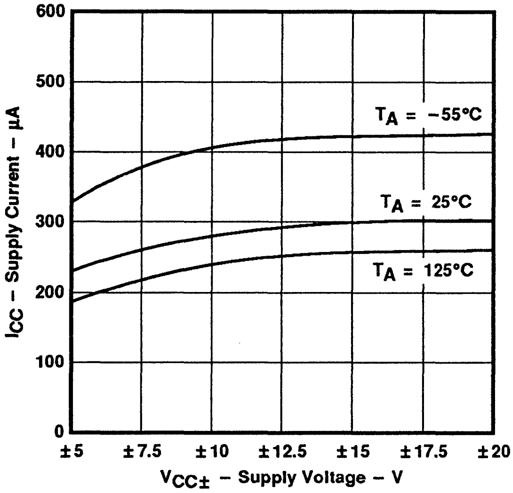


Figure 4

[†] Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

MAXIMUM PEAK OUTPUT VOLTAGE SWING
vs
FREQUENCY

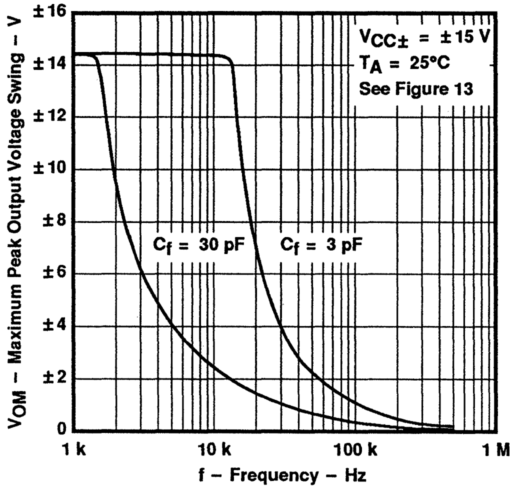


Figure 5

MAXIMUM PEAK OUTPUT VOLTAGE SWING
vs
OUTPUT CURRENT

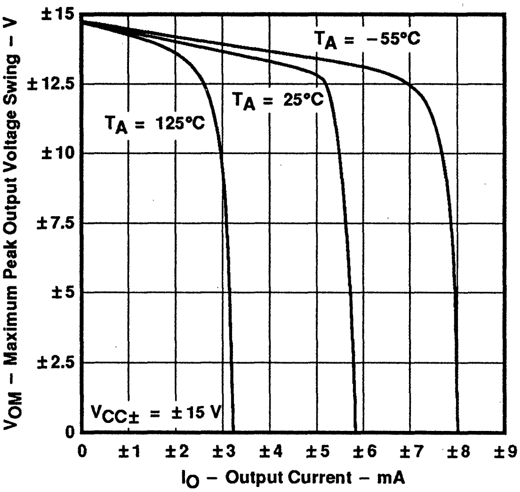


Figure 6

DIFFERENTIAL VOLTAGE AMPLIFICATION
vs
SUPPLY VOLTAGE

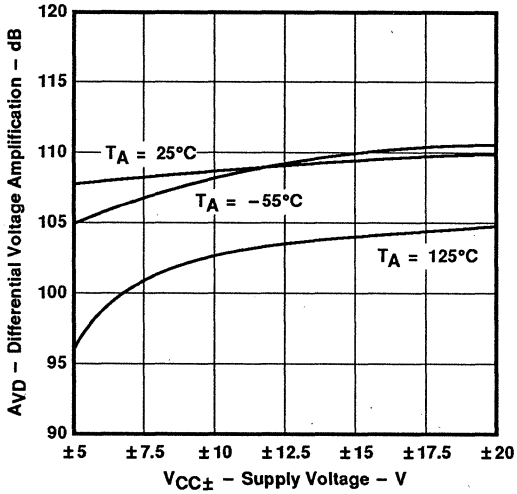


Figure 7

DIFFERENTIAL VOLTAGE AMPLIFICATION
and PHASE DELAY
vs
FREQUENCY

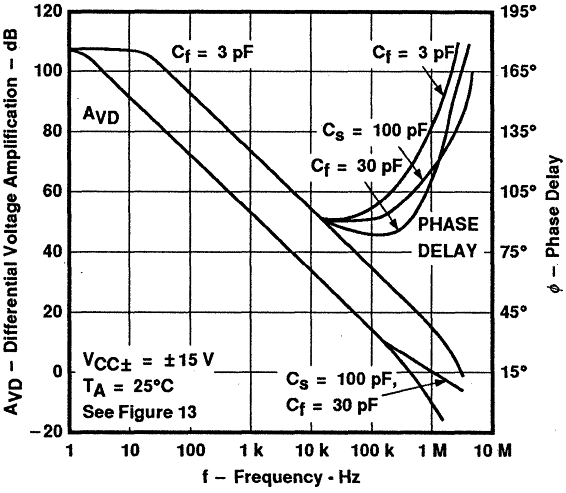


Figure 8

---

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS

SUPPLY VOLTAGE REJECTION RATIO
vs
FREQUENCY

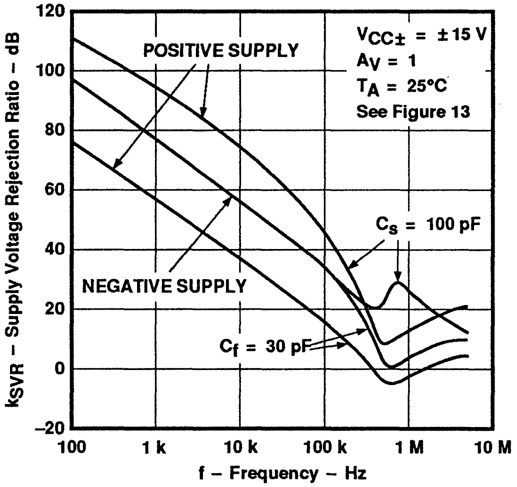


Figure 9

CLOSED-LOOP OUTPUT IMPEDANCE
vs
FREQUENCY

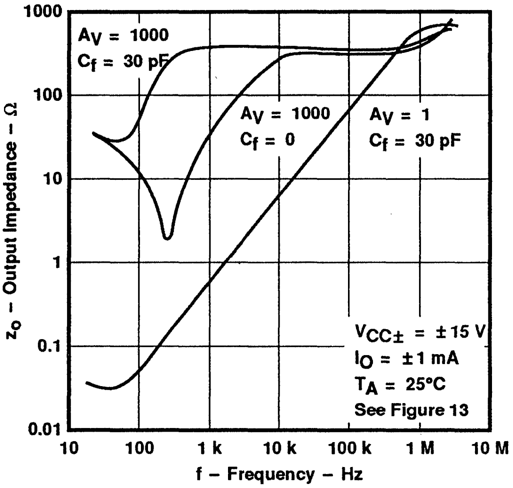


Figure 10

EQUIVALENT INPUT NOISE VOLTAGE
vs
FREQUENCY

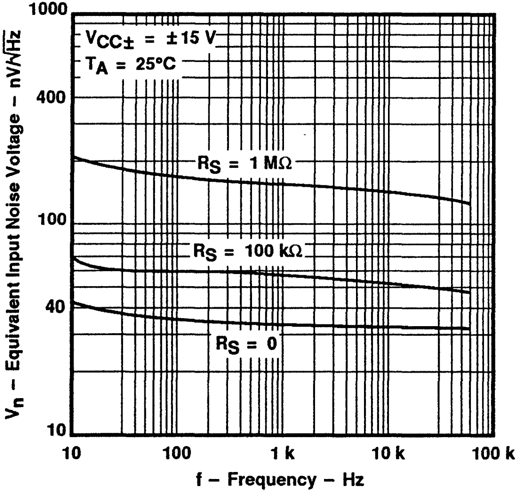


Figure 11

VOLTAGE FOLLOWER
PULSE RESPONSE

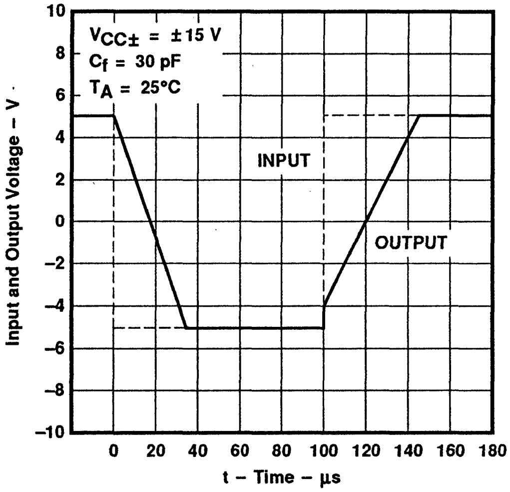
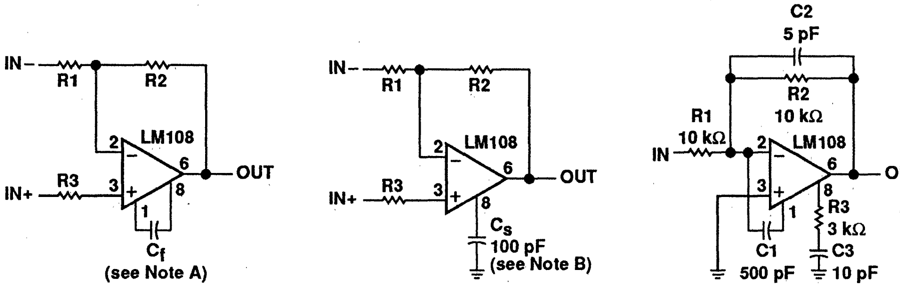


Figure 12

APPLICATION INFORMATION

frequency compensation

Figure 13 shows the frequency compensation circuits for standard compensation, alternate compensation, and feed-forward compensation. The alternate compensation circuit improves supply voltage rejection by a factor of ten.



(a) STANDARD (b) ALTERNATE (c) FEED-FORWARD

NOTES: A. $C_f \geq R1C_O/(R1 + R2)$, C_O = 30 pF, bandwidth and slew rate are proportional to $1/C_f$.
B. Bandwidth and slew rate are proportional to $1/C_S$.

Figure 13. Frequency Compensation Circuits

input guarding

Input guarding is used to reduce surface leakage (see Figure 14). Both sides of the board must be guarded. Bulk leakage reduction is less than surface leakage reduction and depends on the guard-ring width. The guard ring is connected to a low-impedance point at the same potential as the sensitive input leads. Connections for various op-amp configurations are shown in Figure 15.

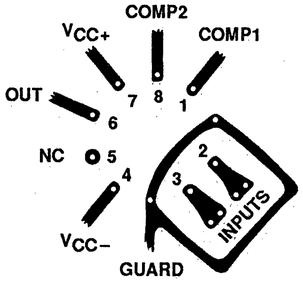
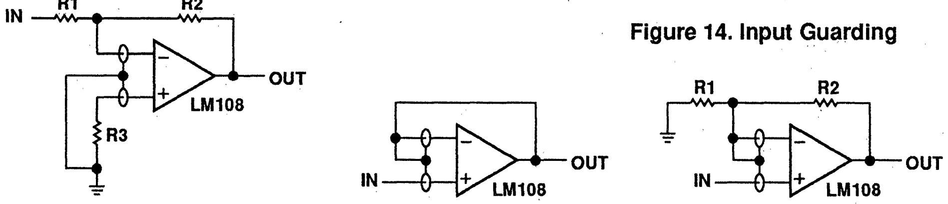


Figure 14. Input Guarding



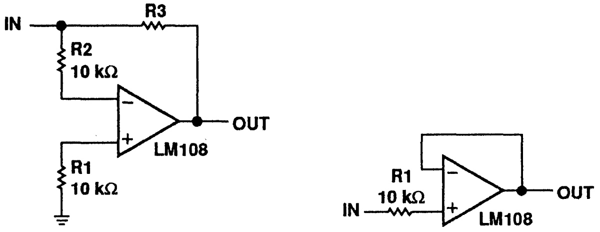
(a) INVERTING (b) FOLLOWER (c) NONINVERTING

Figure 15. Guard Ring Connections for Various Op Amp Configurations

APPLICATION INFORMATION

input protection

Current is limited by R2 even when the input is connected to a voltage source outside the common-mode range [see Figure 16(a)]. If one supply reverses, current is controlled by R1. These resistors do not affect normal operation. The input resistor controls the current when the input exceeds the supply voltages, when the power for the op amp is turned off, or when the output is shorted [see Figure 16(b)].

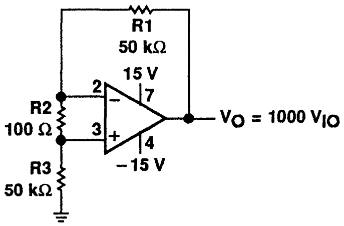


(a) CURRENT LIMITED BY R1 OR R2 (b) CURRENT LIMITED BY R1

Figure 16. Input Protection

input offset voltage testing

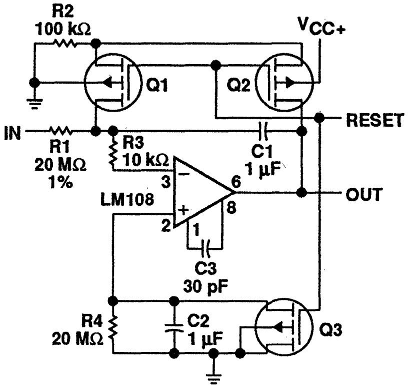
The test circuit for input offset voltage is shown in Figure 17. This circuit is also used as the burn-in configuration with supply voltages equal to ±20 V, R1 = R3 = 10 kΩ, R2 = 200 Ω, AV = 100.



NOTE A: Resistors must have low thermoelectric potential.

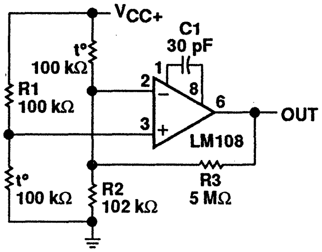
Figure 17. Test Circuit for Input Offset Voltage

APPLICATION INFORMATION



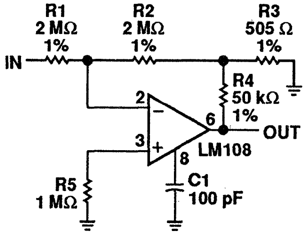
NOTE A: Q1 and Q3 should not have internal gate-protection diodes.

Figure 18. Low-Drift Integrator With Reset



NOTE A: R1 = R2R3/(R2 + R3).

Figure 19. Amplifier for Bridge Transducers



NOTE A: R2 > R1, R2 >> R3,
A_V = R2(R3 + R4)/R1R3.

Figure 20. Inverting Amplifier With High Input Resistance

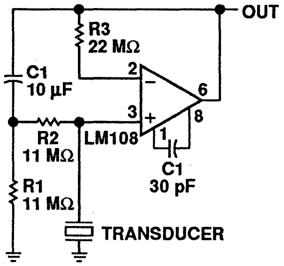
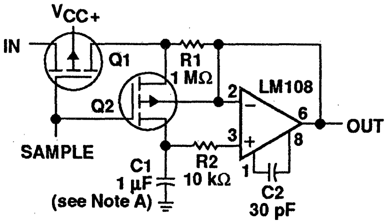
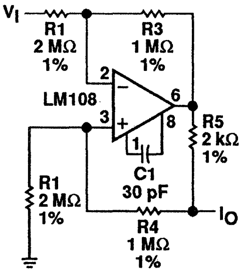


Figure 21. Amplifier for Piezoelectric Transducers



NOTES: A Teflon, polyethylene, or polycarbonate dielectric capacitor.
B. Worst-case drift is less than 2.5 mV/s.

Figure 22. Sample-and-Hold Amplifier



NOTE A: I_O = (R3)V_I/R1R5
R3 = R4 + R5
R1 = R2

Figure 23. Bilateral Current Source

APPLICATION INFORMATION

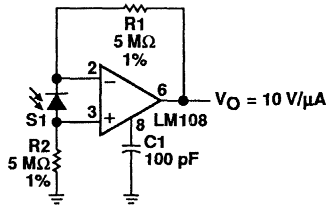
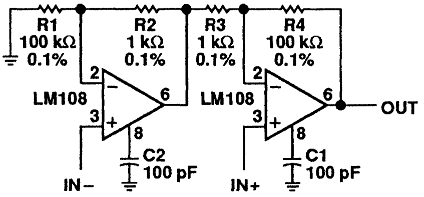
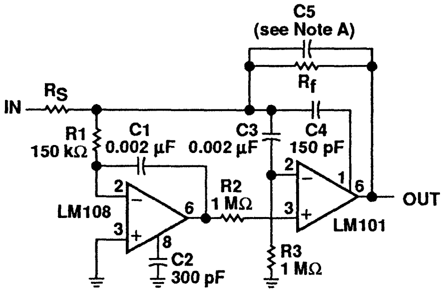


Figure 24. Amplifier for Photodiode Sensor



NOTE A: R1 = R4, R2 = R3, A_V = 1 + R1/R2

Figure 25. Differential-Input Instrumentation Amplifier



NOTES: A. C5 = $6 \times 10^{-8}/R_f$
B. Power bandwidth = 250 kHz
C. Small-signal bandwidth = 3.5 MHz
D. Slew Rate = 10 V/μs
E. The LM101 increases speed, raises high- and low-frequency gain, increases output drive capability, and eliminates thermal feedback.

Figure 26. Fast Summing Amplifier

LM118, LM218, LM318
HIGH-PERFORMANCE OPERATIONAL AMPLIFIERS

D2219, JUNE 1976—REVISED SEPTEMBER 1990

- **Small-Signal Bandwidth . . . 15 MHz Typ**
- **Slew Rate . . . 50 V/μs Min**
- **Bias Current . . . 250 nA Max (LM118, LM218)**
- **Supply Voltage Range . . . ±5 V to ±20 V**
- **Internal Frequency Compensation**
- **Input and Output Overload Protection**
- **Same Pin Assignments as General-Purpose Operational Amplifiers**

description

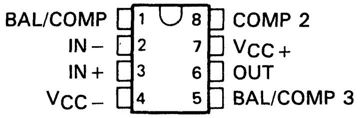
The LM118, LM218, and LM318 are precision, high-speed operational amplifiers designed for applications requiring wide bandwidth and high slew rate. They feature a factor-of-ten increase in speed over general-purpose devices without sacrificing dc performance.

These operational amplifiers have internal unity-gain frequency compensation. This considerably simplifies their application, since no external components are necessary for operation. However, unlike most internally compensated amplifiers, external frequency compensation may be added for optimum performance. For inverting applications, feed-forward compensation boosts the slew rate to over 150 V/μs and almost double the bandwidth. Overcompensation can be used with the amplifier for greater stability when maximum bandwidth is not needed. Further, a single capacitor may be added to reduce the settling time for 0.1% error band to under 1 μs.

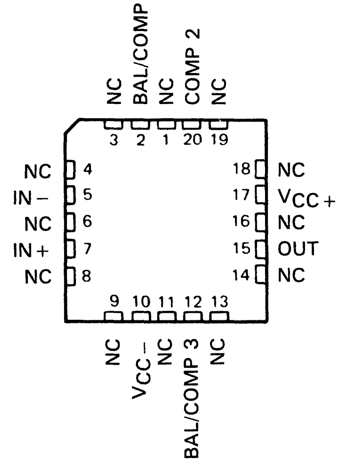
The high speed and fast settling time of these operational amplifiers make them useful in A/D converters, oscillators, active filters, sample and hold circuits, and general-purpose amplifiers.

The LM118 is characterized for operation from −55°C to 125°C. The LM218 is characterized for operation from −25°C to 85°C, and the LM318 is characterized for operation from 0°C to 70°C.

D, JG, OR P PACKAGE
(TOP VIEW)

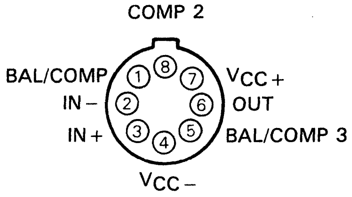


FK PACKAGE
(TOP VIEW)



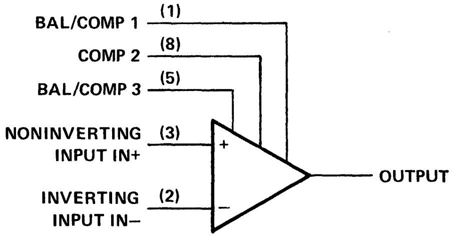
NC—No internal connection

L PACKAGE
(TOP VIEW)



Pin 4 of the L package is in electrical contact with the case.

symbol



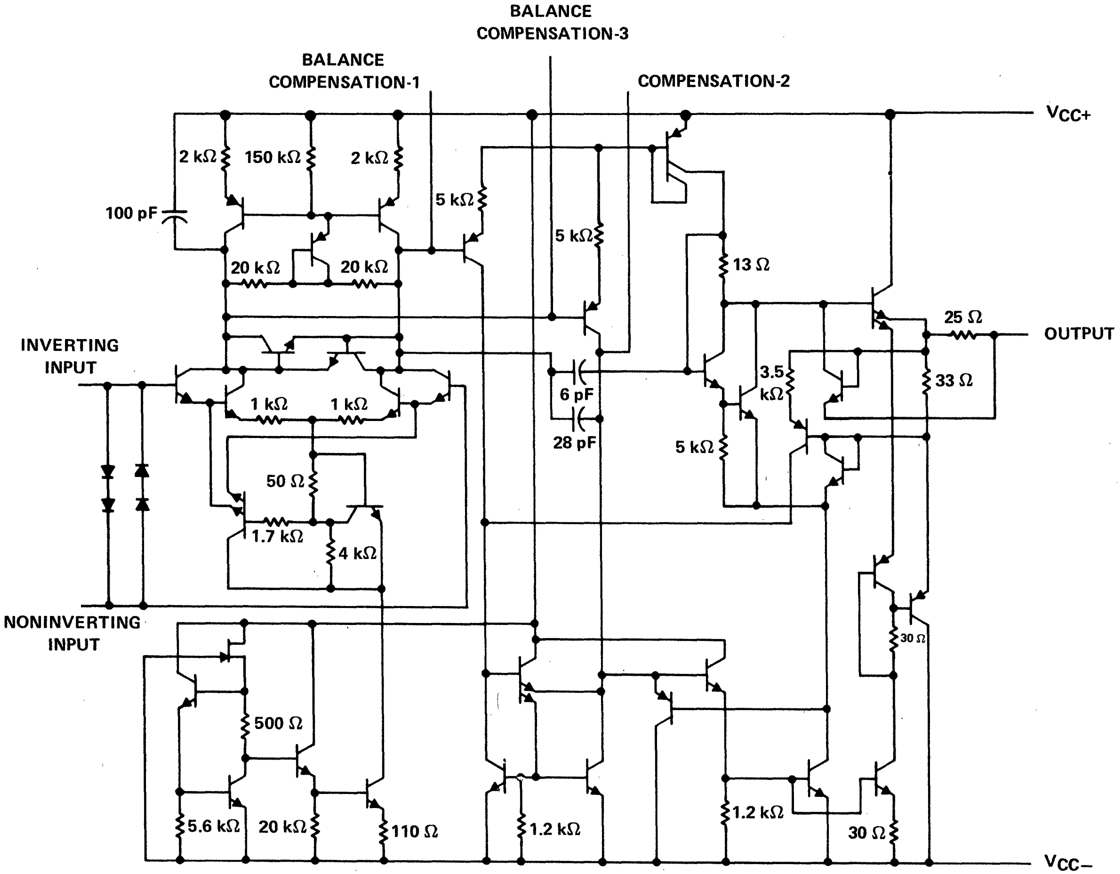
TEXAS INSTRUMENTS
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

AVAILABLE OPTIONS

T_A	V_{IO} MAX AT 25°C	PACKAGE				
		SMALL OUTLINE (D)	CHIP CARRIER (FK)	CERAMIC DIP (JG)	METAL CAN (L)	PLASTIC DIP (P)
0°C to 70°C	10 mV	LM318D	—	—	—	LM318P
−25°C to 85°C	4 mV	LM218D	—	—	—	LM218P
−55°C to 125°C	4 mV	LM118D	LM118FK	LM118JG	LM118L	LM118P

The D package is available taped and reeled. Add the suffix R (e.g., LM318DR).

schematic



Component values shown are nominal.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

		LM118	LM218	LM318	UNIT
Supply voltage, V_{CC+} (see Note 1)		20	20	20	V
Supply voltage, V_{CC-} (see Note 1)		−20	−20	−20	V
Input voltage (either input, see Notes 1 and 2)		±15	±15	±15	V
Differential input current (see Note 3)		±10	±10	±10	mA
Duration of output short-circuit (see Note 4)		unlimited	unlimited	unlimited	
Continuous total power dissipation		See Dissipation Rating Table			
Operating free-air temperature range		−55 to 125	−25 to 85	0 to 70	°C
Storage temperature range		−65 to 150	−65 to 150	−65 to 150	°C
Case temperature for 60 seconds	FK package	260			°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	D or P package	260	260	260	°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds	JG or L package	300			°C

NOTES: 1. All voltage values, unless otherwise noted, are with respect to the midpoint between V_{CC+} and V_{CC-}.
2. The magnitude of the input voltage must never exceed the magnitude of the supply voltage or 15 V, whichever is less.
3. The inputs are shunted with two opposite-facing base-emitter diodes for overvoltage protection. Therefore, excessive current will flow if a differential input voltage in excess of approximately 1 V is applied between the inputs unless some limiting resistance is used.
4. The output may be shorted to ground or either power supply. For the LM118 and LM218 only, the unlimited duration of the short-circuit applies at (or below) 85°C case temperature or 75°C free-air temperature.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR	DERATE ABOVE T_A	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING	$T_A = 125°C$ POWER RATING
D	500 mW	5.8 mW/°C	64°C	464 mW	377 mW	145 mW
FK	500 mW	11.0 mW/°C	105°C	500 mW	500 mW	275 mW
JG	500 mW	8.4 mW/°C	90°C	500 mW	500 mW	210 mW
L	500 mW	6.6 mW/°C	74°C	500 mW	429 mW	165 mW
P	500 mW	8.0 mW/°C	88°C	500 mW	500 mW	200 mW

electrical characteristics at specified free-air temperature (see Note 5)

PARAMETER		TEST CONDITIONS†		LM118, LM218			LM318			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_O = 0	25°C		2	4		4	10	mV
			Full range			6			15	
I_{IO}	Input offset current	V_O = 0	25°C		6	50		30	200	nA
			Full range			100			300	
I_{IB}	Input bias current	V_O = 0	25°C		120	250		150	500	nA
			Full range			500			750	
V_{ICR}	Common-mode input voltage range	$V_{CC\pm}$ = ±15 V	Full range	±11.5			±11.5			V
V_{OM}	Maximum peak output voltage swing	$V_{CC\pm}$ = ±15 V, R_L = 2 kΩ	Full range	±12	±13		±12	±13		V
A_{VD}	Large-signal differential voltage amplification	$V_{CC\pm}$ = ±15 V, V_O = ±10 V, $R_L \geq$ 2 kΩ	25°C	50	200		25	200		V/mV
			Full range	25			20			
B_1	Unity-gain bandwidth	$V_{CC\pm}$ = ±15V	25°C		15			15		MHz
r_i	Input resistance		25°C	1*	3		0.5	3		MΩ
CMRR	Common-mode rejection ratio	V_{IC} = V_{ICR} min	Full range	80	100		70	100		dB
k_{SVR}	Supply voltage rejection ratio ($\Delta V_{CC}/\Delta V_{IO}$)		Full range	70	80		65	80		dB
I_{CC}	Supply current	No load, V_O = 0	25°C		5	8		5	10	mA

†All characteristics are measured under open-loop conditions with common-mode input voltage unless otherwise specified. Full range for LM118 is −55°C to 125°C, full range for LM218 is −25°C to 85°C, and for LM318 is 0°C to 70°C.

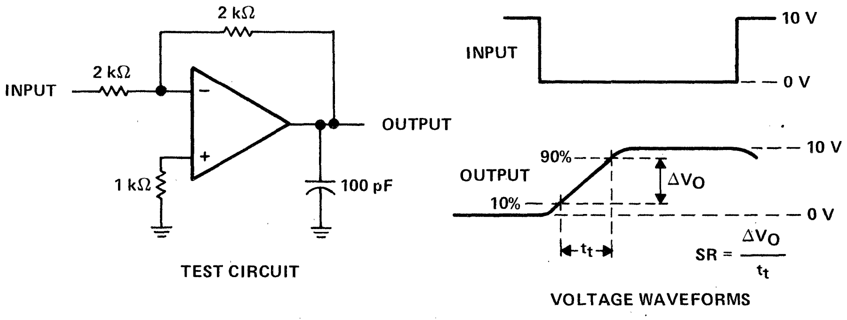
NOTE 5: Unless otherwise noted, V_{CC} = ±5 V to ±20 V. All typical values are at $V_{CC\pm}$ = ±15 V, T_A = 25°C.

operating characteristics, V_{CC+} = 15 V, V_{CC} = 15 V, T_A = 25°C

PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
SR	Slew rate at unit gain	ΔV_I = 10 V,	C_L = 10 pF,	See Figure 1	50*	70		V/μs

*On products compliant to MIL-STD-883, Class B, this parameter is not production tested.

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT

VOLTAGE WAVEFORMS

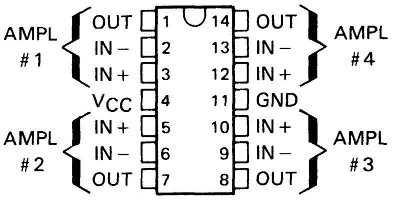
FIGURE 1. SLEW RATE

LM124, LM124A, LM224, LM224A
LM324, LM324A, LM2902, LM2902Q
QUADRUPLE OPERATIONAL AMPLIFIERS

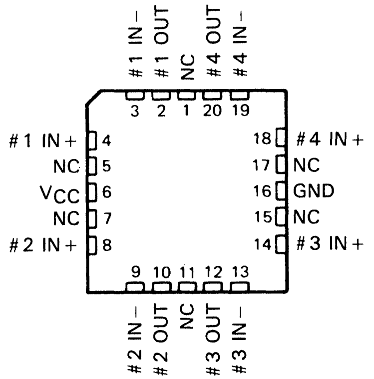
D1990, SEPTEMBER 1975—REVISED JULY 1991

- **Wide Range of Supply Voltages:**
  Single Supply . . . 3 V to 30 V (LM2902 and LM2902Q 3 V to 26 V), or Dual Supplies
- **Low Supply Current Drain Independent of Supply Voltage . . . 0.8 mA Typ**
- **Common-Mode Input Voltage Range Includes Ground Allowing Direct Sensing Near Ground**
- **Low Input Bias and Offset Parameters:**
  - **Input Offset Voltage . . . 3 mV Typ**
    - **A Versions . . . 2 mV Typ**
  - **Input Offset Current . . . 2 nA Typ**
  - **Input Bias Current . . . 20 nA Typ**
    - **A Versions . . . 15 nA Typ**
- **Differential Input Voltage Range Equal to Maximum-Rated Supply Voltage . . . 32 V (26 V for LM2902 and LM2902Q)**
- **Open-Loop Differential Voltage Amplification . . . 100 V/mV Typ**
- **Internal Frequency Compensation**

LM124, LM124A . . . J OR W PACKAGE
ALL OTHERS . . . D, DB, J, N, OR PW PACKAGE
(TOP VIEW)

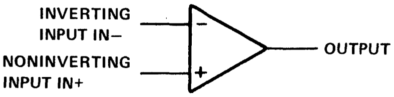


LM124, LM124A
FK PACKAGE
(TOP VIEW)



NC—No internal connection

symbol (each amplifier)



description

These devices consist of four independent, high-gain frequency-compensated operational amplifiers that were designed specifically to operate from a single supply over a wide range of voltages. Operation from split supplies is also possible so long as the difference between the two supplies is 3 V to 30 V (for the LM2902 and LM2902Q, 3 V to 26 V), and V_{CC} is at least 1.5 V more positive than the input common-mode voltage. The low supply current drain is independent of the magnitude of the supply voltage.

Applications include transducer amplifiers, d-c amplification blocks, and all the conventional operational amplifier circuits that now can be more easily implemented in single-supply-voltage systems. For example, the LM124 can be operated directly off of the standard 5-V supply that is used in digital systems and will easily provide the required interface electronics without requiring additional ±15-V supplies.

The LM124 and LM124A are characterized for operation over the full military temperature range of −55°C to 125°C. The LM224 and LM224A are characterized for operation from −25°C to 85°C. The LM324 and LM324A are characterized for operation from 0°C to 70°C. The LM2902 and LM2902Q are characterized for operation from −40°C to 105°C.

The LM2902Q is manufactured to demanding automotive requirements.

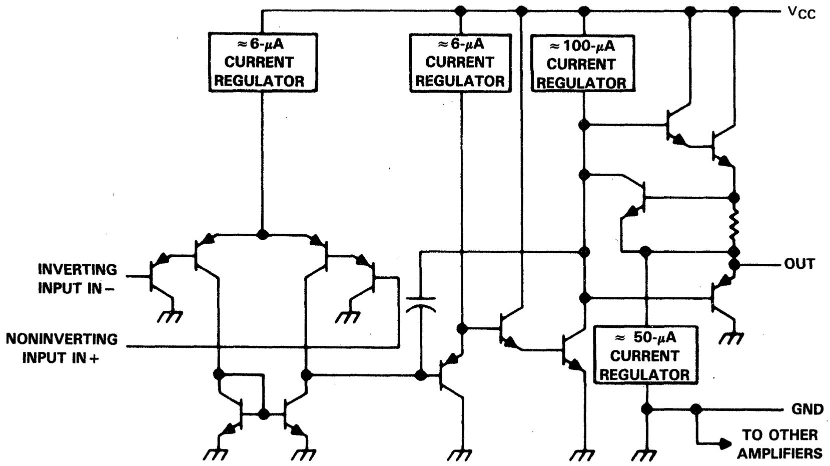
AVAILABLE OPTIONS

T_A	V_{IO} MAX AT 25°C	SMALL OUTLINE (D)†	VERY SMALL OUTLINE (DB)‡	CHIP CARRIER (FK)	CERAMIC DIP (J)	PLASTIC DIP (N)	TSSOP (PW)‡	FLAT PACK (W)	CHIP FORM (Y)
0°C	7 mV	LM324D	LM324DBLE	—	—	LM324N	LM324PWLE		LM324Y
to									
70°C	3 mV	—	—	—	—	LM324AN			
25°C	5 mV	LM224D	—	—	—	LM224N			
to									
85°C	3 mV	—	—	—	—	LM224AN			
−40°C		LM2902D	LM2902DBLE	—	—	LM2902N	LM2902PWLE		
to	7 mV								
105°C		LM2902QD				LM2902QN			
−55°C	5 mV	—	—	LM124FK	LM124J	—		LM124W	
to									
125°C	2 mV	—	—	LM124AFK	LM124AJ	—			

† The D package is available taped and reeled. Add the suffix R to the device type (e.g., LM324DR).

‡ The DB and PW packages are only available left-end taped and reeled.

schematic (each amplifier)

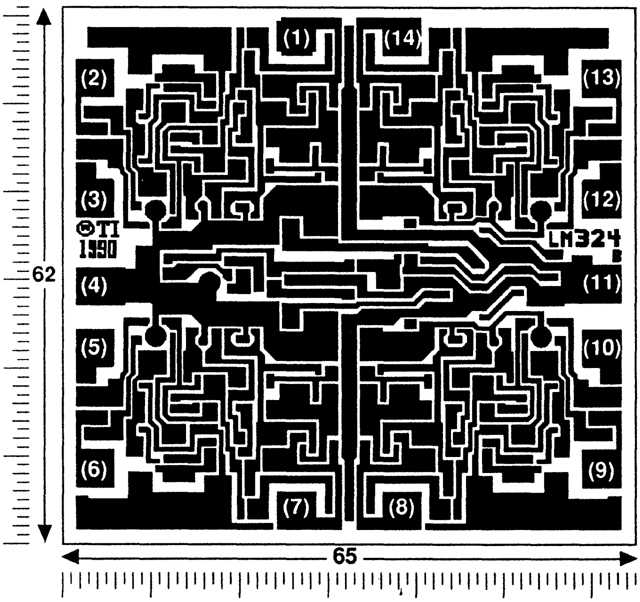


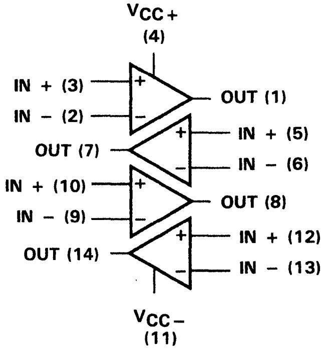
Component count (total device)
- Epi-FET — 1
- Diodes — 4
- Resistors — 11
- Transistors — 95
- Capacitors — 4

chip information

These chips, properly assembled, display characteristics similar to the LM324, (see the LM324Y electrical table). Thermal compression or ultrasonic bonding may be used on the doped aluminum bonding pads. Chips may be mounted with conductive epoxy or a gold-silicon preform.

BONDING PAD ASSIGNMENTS





CHIP THICKNESS:
15 TYPICAL

BONDING PADS:
4 X 4 MINIMUM

T_J max = 150°C

TOLERANCES
ARE ±10%

ALL DIMENSIONS
ARE IN MILS

PIN (11) INTERNALLY CONNECTED
TO BACKSIDE OF CHIP

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

		LM124, LM124A, LM224, LM224A, LM324, LM324A	LM2902, LM2902Q	UNIT
Supply voltage, V_{CC} (see Note 1)		32	26	V
Differential voltage (see Note 2)		±32	±26	V
Input voltage range (either input)		−0.3 to 32	−0.3 to 26	V
Duration of output short-circuit (one amplifier) to ground at (or below) T_A = 25°C, (V_{CC} ≤ 15 V) (see Note 3)		unlimited	unlimited	
Continuous total dissipation		See Dissipation Rating Table		
Operating free-air temperature range	LM124, LM124A	−55 to 125		°C
	LM224, LM224A	−25 to 85		
	LM324, LM324A	0 to 70		
	LM2902, LM2902Q		−40 to 105	
Storage temperature range		−65 to 150	−65 to 150	°C
Case temperature for 60 seconds	FK package	260		°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds	J or W package	300	300	°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	D, DB, N, or PW package	260	260	°C

NOTES: 1. All voltage values, except differential voltages and V_{CC} specified for the measurement of I_{OS}, are with respect to the network ground terminal.

2. Differential voltages are at the noninverting input terminal with respect to the inverting input terminal.

3. Short circuits from outputs to V_{CC} can cause excessive heating and eventual destruction.

DISSIPATION RATING TABLE

PACKAGE	T_A ≤ 25°C POWER RATING	DERATING FACTOR	DERATE ABOVE T_A	T_A = 70°C POWER RATING	T_A = 85°C POWER RATING	T_A = 125°C POWER RATING
D	900 mW	7.6 mW/°C	32°C	608 mW	494 mW	N/A
DB	775 mW	6.2 mW/°C	25°C	496 mW	403 mW	N/A
FK	900 mW	11.0 mW/°C	68°C	880 mW	715 mW	275 mW
J (LM124_)	900 mW	11.0 mW/°C	68°C	880 mW	715 mW	275 mW
J (all others)	900 mW	8.2 mW/°C	40°C	656 mW	533 mW	N/A
N	900 mW	9.2 mW/°C	52°C	736 mW	598 mW	N/A
PW	700 mW	5.6 mW/°C	25°C	448 mW	364 mW	N/A
W	900 mW	8.0 mW/°C	37°C	640 mW	520 mW	200 mW

electrical characteristics at specified free-air temperature, V_{CC} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		LM124_, LM224			LM324			LM2902, LM2902Q			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IO}	Input offset voltage	V_{CC} = 5 V to MAX, $V_{IC} = V_{ICR}$ min, V_O = 1.4 V	25°C		3	5		3	7		3	7	mV
			Full range			7			9			10	
I_{IO}	Input offset current	V_O = 1.4 V	25°C		2	30		2	50		2	50	nA
			Full range			100			150			200	
I_{IB}	Input bias current	V_O = 1.4 V	25°C		−20	−150		−20	−250		−20	−250	nA
			Full range			−300			−500			−500	
V_{ICR}	Common-mode input voltage range	V_{CC} = 5 V to MAX	25°C	0 to $V_{CC}-1.5$			0 to $V_{CC}-1.5$			0 to $V_{CC}-1.5$			V
			Full range	0 to $V_{CC}-2$			0 to $V_{CC}-2$			0 to $V_{CC}-2$			
V_{OH}	High-level output voltage	R_L = 2 kΩ	25°C	$V_{CC}-1.5$			$V_{CC}-1.5$						V
		R_L = 10 kΩ	25°C							$V_{CC}-1.5$			
		V_{CC} = MAX, R_L = 2 kΩ	Full range	26			26			22			
		V_{CC} = MAX, R_L = 10 kΩ	Full range	27	28		27	28		23	24		
V_{OL}	Low-level output voltage	$R_l \le 10$ kΩ	Full range		5	20		5	20		5	100	mV
A_{VD}	Large-signal differential voltage amplification	V_{CC} = 15 V, V_O = 1 V to 11 V, $R_L \ge 2$ kΩ	25°C	50	100		25	100			100		V/mV
			Full range	25			15			15			
CMRR	Common-mode rejection ratio	$V_{IC} = V_{ICR}$ min	25°C	70	80		65	80		50	80		dB
k_{SVR}	Supply voltage rejection ratio ($\Delta V_{CC}/\Delta V_{IO}$)		25°C	65	100		65	100		50	100		dB
V_{o1}/V_{o2}	Crosstalk attenuation	f = 1 kHz to 20 kHz	25°C		120			120			120		dB
I_{IO}	Output current	V_{CC} = 15 V, V_{ID} = 1 V, V_O = 0	25°C	−20	−30	−60	−20	−30	−60	−20	−30	−60	mA
			Full range	−10			−10			−10			
		V_{CC} = 15 V, V_{ID} = −1 V, V_O = 15 V	25°C	10	20		10	20		10	20		
			Full range	5			5			5			
		V_{ID} = −1 V, V_O = 200 mV	25°C	12	30		12	30			30		μA
I_{OS}	Short-circuit output current	V_{CC} at 5 V, GND at −5 V, V_O = 0	25°C		±40	±60		±40	±60		±40	±60	mA
I_{CC}	Supply current (four amplifiers)	V_O = 2.5 V, No load	Full range		0.7	1.2		0.7	1.2		0.7	1.2	mA
		V_{CC} = MAX, $V_O = 0.5\ V_{CC}$, No load	Full range		1.1	3		1.1	3		1.1	3	

†All characteristics are measured under open-loop conditions with zero common-mode input voltage unless otherwise specified. "MAX" V_{CC} for testing purposes is 26 V for LM2902 and LM2902Q, 30 V for the others. Full range is −55°C to 125°C for LM124 and LM124A, −25°C to 85°C for LM224, 0°C to 70°C for LM324, and −40°C to 105°C for LM2902 and LM2902Q.

‡All typical values are at T_A = 25°C.

electrical characteristics at specified free-air temperature, V_{CC} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		LM124A			LM224A			LM324A			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IO}	Input offset voltage	V_{CC} = 5 V to 30 V, V_{IC} = V_{ICR} min, V_O = 1.4 V	25°C			2		2	3		2	3	mV
			Full range			4			4			5	
I_{IO}	Input offset current	V_O = 1.4 V	25°C			10			2	15	2	30	nA
			Full range			30			30			75	
I_{IB}	Input bias current	V_O = 1.4 V	25°C			−50		−15	−80		−15	−100	nA
			Full range			−100			−100			−200	
V_{ICR}	Common-mode input voltage range	V_{CC} = 30 V	25°C	0 to $V_{CC}-1.5$			0 to $V_{CC}-1.5$			0 to $V_{CC}-1.5$			V
			Full range	0 to $V_{CC}-2$			0 to $V_{CC}-2$			0 to $V_{CC}-2$			
V_{OH}	High-level output voltage	R_L = 2 kΩ	25°C	$V_{CC}-1$			$V_{CC}-1$			$V_{CC}-1$			V
		V_{CC} = 30 V, R_L = 2 kΩ	Full range	26			26			26			
		V_{CC} = 30 V, R_L = 10 kΩ	Full range	27			27	28		27	28		
V_{OL}	Low-level output voltage	$R_l \le$ 10 kΩ	Full range			20		5	20		5	20	mV
A_{VD}	Large-signal differential voltage amplification	V_{CC} = 15 V, V_O = 1 V to 11 V, $R_L \ge$ 2 kΩ	25°C	50			50	100		25	100		V/mV
			Full range	25			25			15			
CMRR	Common-mode rejection ratio	V_{IC} = V_{ICR} min	25°C	70			70	80		65	80		dB
k_{SVR}	Supply voltage rejection ratio ($\Delta V_{CC}/\Delta V_{IO}$)		25°C	65			65	100		65	100		dB
V_{o1}/V_{o2}	Crosstalk attenuation	f = 1 kHz to 20 kHz	25°C		120			120			120		dB
I_{IO}	Output current	V_{CC} = 15 V, V_{ID} = 1 V, V_O = 0	25°C	−20			−20	−30	−60	−20	−30	−60	mA
			Full range	−10			−10			−10			
		V_{CC} = 15 V, V_{ID} = −1 V, V_O = 15 V	25°C	10			10	20		10	20		
			Full range	5			5			5			
		V_{ID} = −1 V, V_O = 200 mV	25°C	12			12	30		12	30		µA
I_{OS}	Short-circuit output current	V_{CC} at 5 V, GND at −5 V, V_O = 0	25°C		±40	±60		±40	±60		±40	±60	mA
I_{CC}	Supply current (four amplifiers)	V_O = 2.5 V, No load	Full range		1.5	2.4		1.5	2.4		1.5	2.4	mA
		V_{CC} = 30 V, V_O = 15, No load	Full range		1.1	3		1.1	3		1.1	3	

† All characteristics are measured under open-loop conditions with zero common-mode input voltage unless otherwise specified. Full range is −55°C to 125°C for LM124A, −25°C to 85°C for LM224A, and 0°C to 70°C for LM324A.

‡ All typical values are at T_A = 25°C.

electrical characteristics, V_{CC} = 5 V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS†	LM324Y			UNIT
			MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_{CC} = 5 V to MAX, V_{IC} = V_{ICR}min, V_O = 1.4 V		3	7	mV
I_{IO}	Input offset current			2	50	nA
I_{IB}	Input bias current			−20	−250	nA
V_{ICR}	Common-mode input voltage range	V_{CC} = 5 V to MAX	0 to V_{CC} −1.5			V
V_{OH+}	High-level output voltage	R_L = 10 kΩ	V_{CC} − 1.5			V
A_{VD}	Large-signal differential voltage amplification	V_{CC} = 15 V, V_O = 1 V to 11 V, R_L ≥ 2 kΩ	15	100		V/mV
CMRR	Common-mode rejection ratio	V_{IC} = V_{ICR} min	65	80		dB
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm}/\Delta V_{IO}$)		65	100		dB
I_O	Output current	V_{CC} = 15 V, V_{ID} = 1 V, V_O = 0	−20	−30	−60	mA
		V_{CC} = 15 V, V_{ID} = −1 V, V_O = 15 V	10	20		
		V_{ID} = 1 V, V_O = 200 mV	12	30		
I_{OS}	Short-circuit output current	V_{CC} at 5 V, GND at −5 V, V_O = 0		±40	±60	mA
I_{CC}	Supply current (four amplifiers)	V_O = 2.5 V_{CC}, No load		0.7	1.2	mA
		V_{CC} = MAX, V_O = 0.5 V_{CC}, No load		1.1	3	

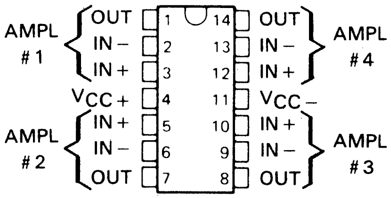
† All characteristics are measured under open-loop conditions with zero common-mode input voltage unless otherwise specified. "MAX" V_{CC} for testing purposes is 30 V.

LM148, LM248, LM348
QUADRUPLE OPERATIONAL AMPLIFIERS

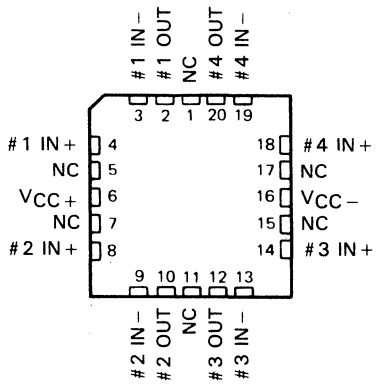
D2551, OCTOBER 1979—REVISED SEPTEMBER 1990

- **uA741 Operating Characteristics**
- **Low Supply Current Drain . . . 0.6 mA Typ (per amplifier)**
- **Low Input Offset Voltage**
- **Low Input Offset Current**
- **Class AB Output Stage**
- **Input/Output Overload Protection**
- **Designed to be Interchangeable with National LM148, LM248, and LM348.**

LM148 . . . J PACKAGE
LM248, LM348 . . . D OR N PACKAGE
(TOP VIEW)



LM148 . . . FK PACKAGE
(TOP VIEW)



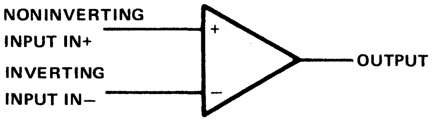
NC—No internal connection

description

The LM148, LM248, and LM348 are quadruple, independent, high-gain, internally compensated operational amplifiers designed to have operating characteristics similar to the uA741. These amplifiers exhibit low supply current drain, and input bias and offset currents that are much less than those of the uA741.

The LM148 is characterized for operation over the full military temperature range of −55°C to 125°C, the LM248 is characterized for operation from −25°C to 85°C, and the LM348 is characterized for operation from 0°C to 70°C.

symbol (each amplifier)



AVAILABLE OPTIONS

T_A	V_{IO} MAX AT 25°C	PACKAGE			
		SMALL OUTLINE (D)	CHIP CARRIER (FK)	CERAMIC DIP (J)	PLASTIC DIP (N)
0°C to 70°C	6 mV	LM348D	—	—	LM348N
−25°C to 85°C	6 mV	LM248D	—	—	LM248N
−55°C to 125°C	5 mV	—	LM148FK	LM148J	—

The D package is available taped and reeled. Add the suffix R to the device type, (e.g., LM348DR).

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

		LM148	LM248	LM348	UNIT
Supply voltage V_{CC+} (see Note 1)		22	18	18	V
Supply voltage V_{CC-} (see Note 1)		−22	−18	−18	V
Differential input voltage (see Note 2)		44	36	36	V
Input voltage (either input, see Notes 1 and 3)		±22	±18	±18	V
Duration of output short-circuit (see Note 4)		unlimited	unlimited	unlimited	
Continuous total power dissipation		See Dissipation Rating Table			
Operating free-air temperature range		−55 to 125	−25 to 85	0 to 70	°C
Storage temperature range		−65 to 150	−65 to 150	−65 to 150	°C
Case temperature for 60 seconds	FK package	260			°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds	J package	300			°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	D or N package		260	260	°C

NOTES: 1. All voltage values, except differential voltages, are with respect to the midpoint between V_{CC+} and V_{CC-}.
2. Differential voltages are at the noninverting input terminal with respect to the inverting terminal.
3. The magnitude of the input voltage must never exceed the magnitude of the supply voltage or the value specified in the table, whichever is less.
4. The output may be shorted to ground or either power supply. Temperature and/or supply voltages must be limited to ensure that the dissipation rating is not exceeded.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR	DERATE ABOVE T_A	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING	$T_A = 125°C$ POWER RATING
D	900 mW	7.6 mW/°C	32°C	608 mW	494 mW	N/A
FK	900 mW	11.0 mW/°C	68°C	880 mW	715 mW	275 mW
J	900 mW	11.0 mW/°C	68°C	880 mW	715 mW	275 mW
N	900 mW	9.2 mW/°C	52°C	736 mW	598 mW	N/A

recommended operating conditions

	MIN	MAX	
Supply voltage, V_{CC+}	4	18	V
Supply voltage, V_{CC-}	−4	−18	V

electrical characteristics, $V_{CC\pm} = \pm 15$ V

PARAMETER		TEST CONDITIONS†		LM148			LM248			LM348			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	$V_O = 0$	25°C		1	5		1	6		1	6	mV
			Full range			6			7.5			7.5	
I_{IO}	Input offset current	$V_O = 0$	25°C		4	25		4	50		4	50	nA
			Full range			75			125			100	
I_{IB}	Input bias current	$V_O = 0$	25°C		30	100		30	200		30	200	nA
			Full range			325			500			400	
V_{ICR}	Common-mode input voltage range		Full range	±12			±12			±12			V
V_{OM}	Maximum peak output voltage swing	$R_L = 10$ kΩ	25°C	±12	±13		±12	±13		±12	±13		V
		$R_L \geq 10$ kΩ	Full range	±12			±12			±12			
		$R_L = 2$ kΩ	25°C	±10	±12		±10	±12		±10	±12		
		$R_L \geq 2$ kΩ	Full range	±10			±10			±10			
A_{VD}	Large-signal differential voltage amplification	$V_O = \pm 10$ V, $R_L \geq 2$ kΩ	25°C	50	160		25	160		25	160		V/mV
			Full range	25			15			15			
r_i	Input resistance‡		25°C	0.8	2.5		0.8	2.5		0.8	2.5		MΩ
B_1	Unity-gain bandwidth	$A_{VD} = 1$	25°C		1			1			1		MHz
ϕ_M	Phase margin	$A_{VD} = 1$	25°C		60°			60°			60°		
CMRR	Common-mode rejection ratio	$V_{IC} = V_{ICR}$ min, $V_O = 0$	25°C	70	90		70	90		70	90		dB
			Full range	70			70			70			
k_{SVR}	Supply voltage rejection ratio ($\Delta V_{CC\pm}/\Delta V_{IO}$)	$V_{CC\pm} = \pm 9$ V to ± 15 V, $V_O = 0$	25°C	77	96		77	96		77	96		dB
			Full range	77			77			77			
I_{OS}	Short-circuit output current		25°C		±25			±25			±25		mA
I_{CC}	Supply current (four amplifiers)	No load, $V_O = 0$	25°C					2.4	4.5		2.4	4.5	mA
		No load, $V_O = V_{OM}$†			2.4	3.6							
V_{o1}/V_{o2}	Crosstalk attenuation	f = 1 Hz to 20 kHz,	25°C		120			120			120		dB

†All characteristics are measured under open-loop conditions with zero common-mode input voltage unless otherwise specified. Full range for T_A is −55°C to 125°C for LM148, −25°C to 85°C for LM248, and 0°C to 70°C for LM348.

‡This parameter is not production tested.

operating characteristics, $V_{CC\pm}$ = ±15 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain	R_L = 2 kΩ, C_L = 100 pF, See Figure 1		0.5		V/μs

PARAMETER MEASUREMENT INFORMATION

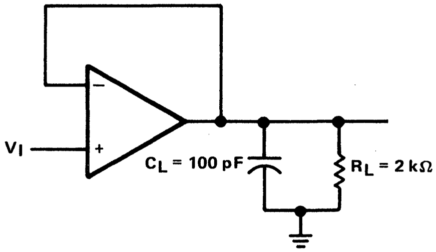
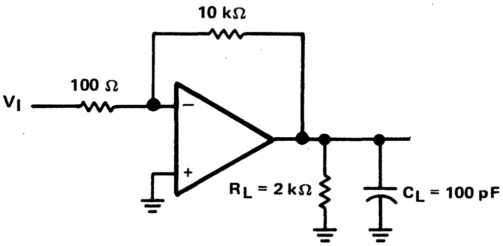


FIGURE 1. UNITY-GAIN AMPLIFIER



A_{VD} = −100

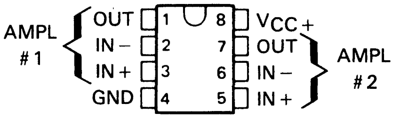
FIGURE 2. INVERTING AMPLIFIER

LM158, LM258, LM358, LM158A
LM258A, LM358A, LM2904, LM2904Q
DUAL OPERATIONAL AMPLIFIERS

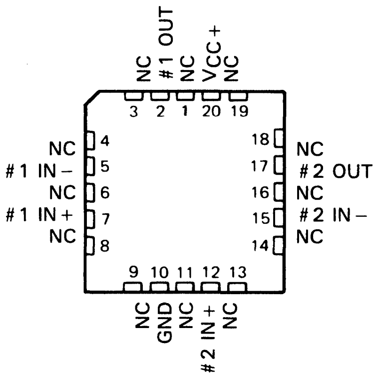
D2231, JUNE 1976—REVISED JULY 1991

- **Wide Range of Supply Voltages:**
  Single Supply . . . 3 V to 30 V
  (LM2904 and LM2904Q
  3 V to 26 V) or Dual Supplies
- **Low Supply Current Drain Independent of Supply Voltage . . . 0.7 mA Typ**
- **Common-Mode Input Voltage Range Includes Ground Allowing Direct Sensing Near Ground**
- **Low Input Bias and Offset Parameters:**
  Input Offset Voltage . . . 3 mV Typ
  A Versions . . . 2 mV Typ
  Input Offset Current . . . 2 nA Typ
  Input Bias Current . . . 20 nA Typ
  A Versions . . . 15 nA Typ
- **Differential Input Voltage Range Equal to Maximum-Rated Supply Voltage . . . ±32 V (±26 V for LM2904 and LM2904Q)**
- **Open-Loop Differential Voltage Amplification . . . 100 V/mV Typ**
- **Internal Frequency Compensation**

D, DB, JG, P, OR PW PACKAGE
(TOP VIEW)



LM158, LM158A
FK PACKAGE
(TOP VIEW)

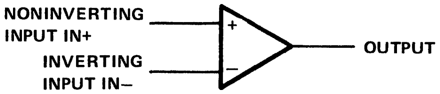


NC—No internal connection

description

These devices consist of two independent, high-gain, frequency-compensated operational amplifiers that were designed specifically to operate from a single supply over a wide range of voltages. Operation from split supplies is also possible so long as the difference between the two supplies is 3 V to 30 V (3 V to 26 V for the LM2904 and LM2904Q), and the V_{CC} pin is at least 1.5 V more positive than the input common-mode voltage. The low supply current drain is independent of the magnitude of the supply voltage.

symbol (each amplifier)



Applications include transducer amplifiers, d-c amplification blocks, and all the conventional operational amplifier circuits that now can be more easily implemented in single-supply-voltage systems. For example, these devices can be operated directly off of the standard 5-V supply that is used in digital systems and will easily provide the required interface electronics without requiring additional ±15-V supplies.

The LM158 and LM158A are characterized for operation over the full military temperature range of −55°C to 125°C. The LM258 and LM258A are characterized for operation from −25°C to 85°C, the LM358 and LM358A from 0°C to 70°C, and the LM2904 and LM2904Q from −40°C to 105°C.

The LM2904Q is manufactured to demanding automotive requirements.

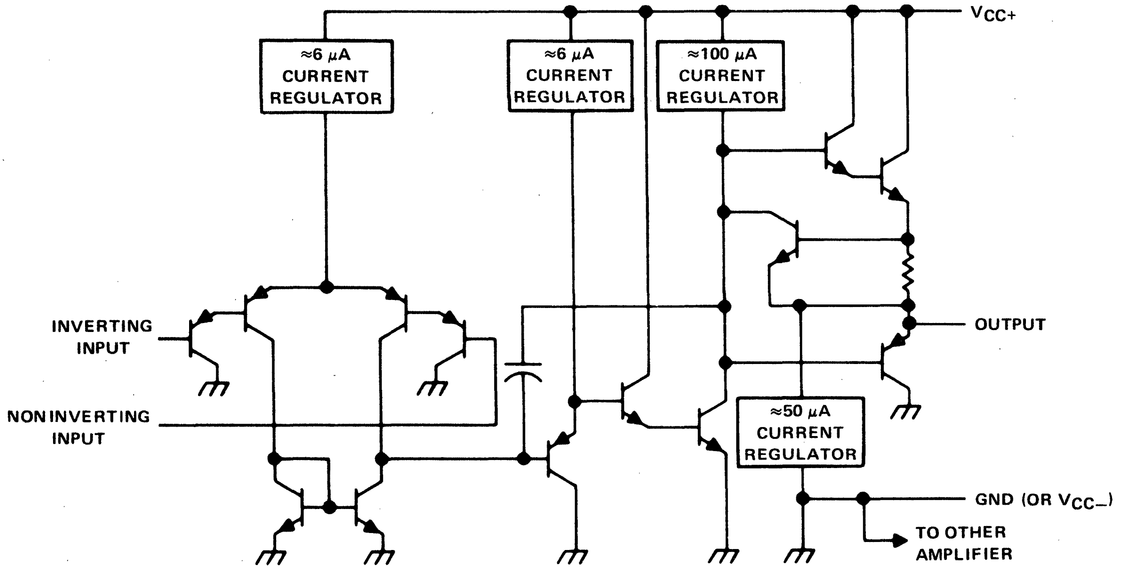
TEXAS INSTRUMENTS

AVAILABLE OPTIONS

T_A	V_{IO} MAX AT 25°C	PACKAGE						
		SMALL OUTLINE (D)	SSOP (DB)	CHIP CARRIER (FK)	CERAMIC DIP (JG)	PLASTIC DIP (P)	TSSOP (PW)	CHIP FORM (Y)
0°C to 70°C	7 mV 3 mV	LM358D	LM358DB			LM358P LM358AP	LM358PW	LM358Y
−25°C to 85°C	5 mV 3 mV	LM258D				LM258P LM258AP		
−40°C to 105°C	7 mV 7 mV	LM2904D LM2904QD	LM2904DB —			LM2904P LM2904QP	LM2904PW —	
−55°C to 125°C	5 mV 2 mV	LM158D		LM158FK LM158AFK	LM158JG LM158AJG	LM158P		

The D package is available taped and reeled. Add the suffix R (e.g., LM358DR).
The DB and PW packages are only available left-end taped and reeled. Add the suffix LE (e.g., LM358DBLE).

schematic (each amplifier)

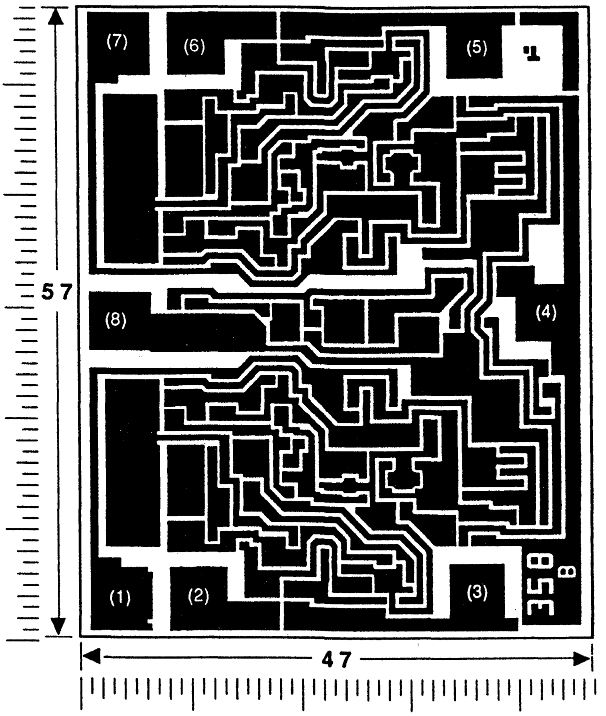


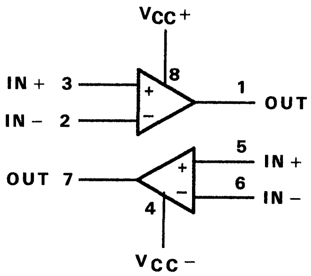
Component count (total device)
- Epi-FET — 1
- Diodes — 2
- Resistors — 7
- Transistors — 51
- Capacitors — 2

chip information

These chips, properly assembled, display characteristics similar to the LM358. Thermal compression or ultrasonic bonding may be used on the doped aluminum bonding pads. Chips may be mounted with conductive epoxy or a gold-silicon preform.

BONDING PAD ASSIGNMENTS





CHIP THICKNESS: 15 TYPICAL

BONDING PADS: 4 X 4 MINIMUM

T_J max = 150°C

TOLERANCES ARE ± 10%

ALL DIMENSIONS ARE IN MILS

NO BACKSIDE METALIZATION

PIN (4) INTERNALLY CONNECTED TO BACKSIDE OF CHIP

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

		LM158, LM158A LM258, LM258A LM358, LM358A	LM2904, LM2904Q	UNIT
Supply voltage, V_{CC} (see Note 1)		32	26	V
Differential voltage (see Note 2)		±32	±26	V
Input voltage range (either input)		0.3 to 32	0.3 to 26	V
Duration of output short-circuit (one amplifier) to ground at (or below) 25°C free-air temperature ($V_{CC} \leq 15$ V) (see Note 3)		unlimited	unlimited	
Continuous total dissipation		See Dissipation Rating Table		
Operating free-air temperature range	LM158, LM158A	−55 to 125		°C
	LM258, LM258A	−25 to 85		
	LM358, LM358A	0 to 70		
	LM2904, LM2904Q		−40 to 105	
Storage temperature range		−65 to 150	−65 to 150	°C
Case temperature for 60 seconds	FK package	260		°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds	JG package	300	300	°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	D, DB, P, or PW package	260	260	°C

NOTES: 1. All voltage values, except differential voltages, and V_{CC} specified for measurement of I_{OS}, are with respect to the network ground terminal.
2. Differential voltages are at the noninverting input terminal with respect to the inverting input terminal.
3. Short circuits from outputs to V_{CC} can cause excessive heating and eventual destruction.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING	$T_A = 125°C$ POWER RATING
D	725 mW	5.8 mW/°C	464 mW	377 mW	145 mW
DB	525 mW	4.2 mW°C	336 mW	273 mW	—
FK	1375 mW	11.0 mW/°C	880 mW	715 mW	275 mW
JG	1050 mW	8.4 mW/°C	672 mW	546 mW	210 mW
P	1000 mW	8.0 mW/°C	640 mW	520 mW	200 mW
PW	525 mW	4.2 mW/°C	336 mW	273 mW	—

electrical characteristics at specified free-air temperature, V_{CC} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		LM158, LM258			LM358			LM2904, LM2904Q			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IO}	Input offset voltage	V_{CC} = 5 V to MAX, V_{IC} = V_{ICR} min, V_O = 1.4 V	25°C		3	5		3	7		3	7	mV
			Full range			7			9			10	
α_{VIO}	Average temperature coefficient of input offset voltage		Full range		7			7			7		μV/°C
I_{IO}	Input offset current	V_O = 1.4 V	25°C		2	30		2	50		2	50	nA
			Full range			100			150			200	
α_{IIO}	Average temperature coefficient of input offset current		Full range		10			10			10		pA/°C
I_{IB}	Input bias current	V_O = 1.4 V	25°C		−20	−150		−20	−250		−20	−250	nA
			Full range			−300			−500			−500	
V_{ICR}	Common-mode input voltage range	V_{CC} = 5 V to MAX	25°C	0 to $V_{CC}-1$			0 to $V_{CC}-1$			0 to $V_{CC}-1$			V
			Full range	0 to $V_{CC}-2$			0 to $V_{CC}-2$			0 to $V_{CC}-2$			
V_{OH}	High-level output voltage	R_L ≥ 2 kΩ	25°C	$V_{CC}-1.5$			$V_{CC}-1.5$						V
		R_L ≥ 10 kΩ	25°C							$V_{CC}-1.5$			
		V_{CC} = MAX, R_L = 2 kΩ	Full range	26			26			22			
		V_{CC} = MAX, R_L ≥ 10 kΩ	Full range	27	28		27	28		23	24		
V_{OL}	Low-level output voltage	R_L ≤ 10 kΩ	Full range		5	20		5	20		5	100	mV

A_{VD}	Large-signal differential voltage amplification	V_{CC} = 15 V, V_O = 1 V to 11 V, R_L = ≥ 2 kΩ	25°C	50	100		25	100			100		V/mV
			Full range	25			15			15			
CMRR	Common-mode rejection ratio	V_{CC} = 5 V to MAX, V_{IC} = V_{ICR} min	25°C	70	80		65	80		50	80		dB
k_{SVR}	Supply voltage rejection ratio ($\Delta V_{CC}/\Delta V_{IO}$)	V_{CC} = 5 V to MAX	25°C	65	100		65	100		50	100		dB
V_{o1}/V_{o2}	Crosstalk attenuation	f = 1 kHz to 20 kHz	25°C		120			120			120		dB
I_O	Output current	V_{CC} = 15 V, V_{ID} = 1 V, V_O = 0	25°C	−20	−30		−20	−30		−20	−30		mA
			Full range	−10			−10			−10			
		V_{CC} = 15 V, V_{ID} = −1 V, V_O = 15 V	25°C	10	20		10	20		10	20		
			Full range	5			5			5			
		V_{ID} = −1 V, V_O = 200 mV	25°C	12	30		12	30			30		μA
I_{OS}	Short-circuit output current	V_{CC} at 5 V, GND at −5 V, V_O = 0	25°C		±40	±60		±40	±60		±40	±60	mA
I_{CC}	Supply current (two amplifiers)	V_O = 2.5 V, No load	Full range		0.7	1.2		0.7	1.2		0.7	1.2	mA
		V_{CC} = MAX, V_O = 0.5 V_{CC}, No load	Full range		1	2		1	2		1	2	

[†] All characteristics are measured under open-loop conditions with zero common-mode input voltage unless otherwise specified. "MAX" V_{CC} for testing purposes is 26 V for LM2904, 30 V for others. Full range is −55°C to 125°C for LM158, −25°C to 85°C for LM258, 0°C to 70°C for LM358, and −40°C to 85°C for LM2904 and LM2904Q.

[‡] All typical values are at T_A = 25°C.

electrical characteristics at specified free-air temperature, V_{CC} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		LM158A			LM258A			LM358A			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_{CC} = 5 V to 30 V, V_{IC} = V_{ICR} min, V_O = 1.4 V	25°C			2		2	3		2	3	mV
			Full range			4			4			5	
α_{VIO}	Average temperature coefficient of input offset voltage		Full range		7	15		7	15		7	20	μV/°C
I_{IO}	Input offset current	V_O = 1.4 V	25°C		2	10		2	15		2	30	nA
			Full range			30			30			75	
α_{IIO}	Average temperature coefficient of input offset current		Full range		10	200		10	200		10	300	pA/°C
I_{IB}	Input bias current	V_O = 1.4 V	25°C		−15	−50		−15	−80		−15	−100	nA
			Full range			−100			−100			−200	
V_{ICR}	Common-mode input voltage range	V_{CC} = 30 V	25°C	0 to $V_{CC}-1.5$			0 to $V_{CC}-1.5$			to $V_{CC}-1.5$			V
			Full range	0 to $V_{CC}-2$			0 to $V_{CC}-2$			to $V_{CC}-2$			
V_{OH}	High-level output voltage	R_L ≥ 2 kΩ	25°C	$V_{CC}-1.5$			$V_{CC}-1.5$		$V_{CC}-1.5$				V
		V_{CC} = 30 V, R_L = 2 kΩ	Full range	26			26			26			
		V_{CC} = 30 V, R_L ≥ 10 kΩ	Full range	27	28		27	28		27	28		
V_{OL}	Low-level output voltage	R_L ≤ 10 kΩ	Full range		5	20		5	20		5	20	mV

A_{VD}	Large-signal differential voltage amplification	V_{CC} = 15 V, V_O = 1 V to 11 V, $R_L \geq 2$ kΩ	25°C	50	100		50	100		25	100		V/mV
			Full range	25			25			15			
CMRR	Common-mode rejection ratio		25°C	70	80		70	80		65	80		dB
k_{SVR}	Supply voltage rejection ratio ($\Delta V_{CC}/\Delta V_{IO}$)		25°C	65	100		65	100		65	100		dB
V_{o1}/V_{o2}	Crosstalk attenuation	f = 1 kHz to 20 kHz	25°C		120			120			120		dB
I_O	Output current	V_{CC} = 15 V, V_{ID} = 1 V, V_O = 0	25°C	−20	−30	−60	−20	−30	−60	−20	−30	−60	mA
			Full range	−10			−10			−10			
		V_{CC} = 15 V, V_{ID} = −1 V, V_O = 15 V	25°C	10	20		10	20		10	20		
			Full range	5			5			5			
		V_{ID} = −1 V, V_O = 200 mV	25°C	12	30		12	30		12	30		µA
I_{OS}	Short-circuit output current	V_{CC} at 5 V, GND at −5 V, V_O = 0	25°C		±40	±60		±40	±60		±40	±60	mA
I_{CC}	Supply current (two amplifiers)	V_O = 2.5 V, No load	Full range		0.7	1.2		0.7	1.2		0.7	1.2	mA
		V_{CC} = 30 V, V_O = 15 V, No load	Full range		1	2		1	2			2	

† All characteristics are measured under open-loop conditions with zero common-mode input voltage unless otherwise specified. Full range is −55°C to 125°C for LM158A, −25°C to 85°C for LM258A, and 0°C to 70°C for LM358A.

‡ All typical values are at T_A = 25°C.

electrical characteristics at V_{CC} = 5 V, T_A = 25°C (unless otherwise noted)

PARAMETER		CONDITIONS†	MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	V_{CC} = 5 V to MAX, V_{IC} = V_{ICR}min, V_O = 1.4 V		3	7	mV
I_{IO}	Input offset current			2	50	nA
I_{IB}	Input bias current			−20	−250	nA
V_{ICR}	Common-mode input voltage range	V_{CC} = 5 V to MAX	0 to V_{CC} − 1.5			V
V_{OH+}	High-level output voltage	R_L = 10 kΩ	V_{CC} − 1.5			V
A_{VD}	Large-signal differential voltage amplification	V_{CC} = 15 V, V_O = 1 V to 11 V, R_L ≥ 2 kΩ	15	100		V/mV
CMRR	Common-mode rejection ratio	V_{IC} = V_{ICR} min	65	80		dB
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm}/\Delta V_{IO}$)		65	100		dB
I_O	Output current	V_{CC} = 15 V, V_{ID} = 1 V, V_O = 0	−20	−30	−60	mA
		V_{CC} = 15 V, V_{ID} = −1 V, V_O = 15 V	10	20		
		V_{ID} = 1 V, V_O = 200 mV	12	30		
I_{OS}	Short-circuit output current	V_{CC} at 5 V, GND at −5 V, V_O = 0		±40	±60	mA
I_{CC}	Supply current (four amplifiers)	V_O = 2.5 V_{CC}, No load		0.7	1.2	mA
		V_{CC} = MAX, V_O = 0.5 V_{CC}, No load		1	2	

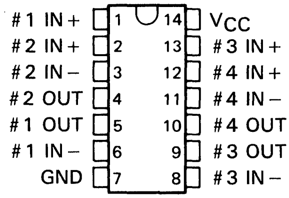
† All characteristics are measured under open-loop conditions with zero common-mode input voltage unless otherwise specified. "MAX" V_{CC} for testing purposes is 30 V.

LM2900, LM3900
QUADRUPLE OPERATIONAL AMPLIFIERS

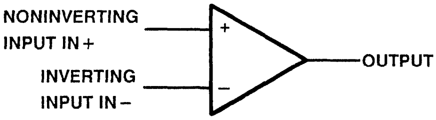
D2531, JULY 1979—REVISED SEPTEMBER 1990

- **Wide Range of Supply Voltages, Single or Dual Supplies**
- **Wide Bandwidth**
- **Large Output Voltage Swing**
- **Output Short-Circuit Protection**
- **Internal Frequency Compensation**
- **Low Input Bias Current**
- **Designed to be Interchangeable with National Semiconductor LM2900 and LM3900, Respectively**

N PACKAGE
(TOP VIEW)



symbol (each amplifier)

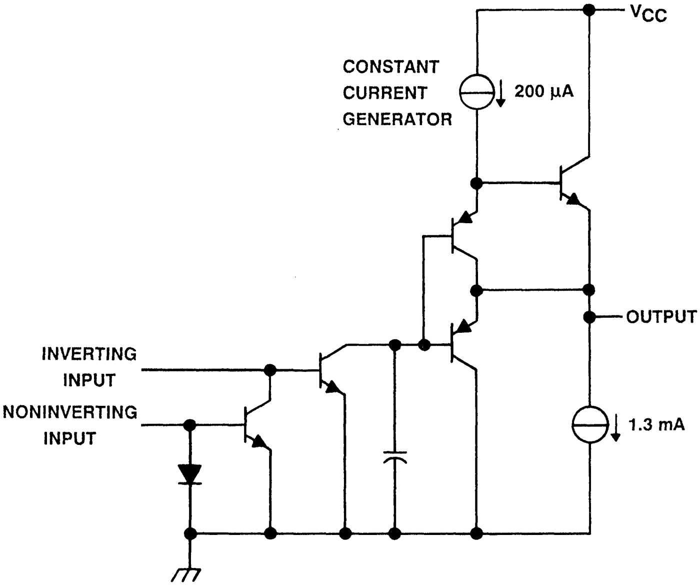


description

These devices consist of four independent, high-gain frequency-compensated Norton operational amplifiers that were designed specifically to operate from a single supply over a wide range of voltages. Operation from split supplies is also possible. The low supply current drain is essentially independent of the magnitude of the supply voltage. These devices provide wide bandwidth and large output voltage swing.

The LM2900 is characterized for operation from −40°C to 85°C, and the LM3900 is characterized for operation from 0°C to 70°C.

schematic (each amplifier)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

	LM2900	LM3900	UNIT
Supply voltage, V_{CC} (see Note 1)	36	36	V
Input current	20	20	mA
Duration of output short circuit (one amplifier) to ground at (or below) 25°C free-air temperature (see Note 2)	unlimited	unlimited	
Continuous total dissipation	See Dissipation Rating Table		
Operating free-air temperature range	−40 to 85	0 to 70	°C
Storage temperature range	−65 to 150	−65 to 150	°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260	260	°C

NOTES: 1. All voltage values, except differential voltages, are with respect to the network ground terminal.
2. Short circuits from outputs to V_{CC} can cause excessive heating and eventual destruction.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING
N	1150 mW	9.2 mW/°C	736 mW	598 mW

recommended operating comditions

	LM2900		LM3900		UNIT
	MIN	MAX	MIN	MAX	
Supply voltage, V_{CC} (single supply)	4.5	32	4.5	32	V
Supply voltage, V_{CC+} (dual supply)	2.2	16	2.2	16	V
Supply voltage, V_{CC-} (dual supply)	−2.2	−16	−2.2	−16	V
Input current (see Note 3)		−1		−1	mA
Operating free-air temperature, T_A	−40	85	0	70	°C

NOTE 3: Clamp transistors are included that prevent the input voltages from swinging below ground more than approximately −0.3 V. The negative input currents that may result from large signal overdrive with capacitive input coupling must be limited externally to values of approximately −1 mA. Negative input currents in excess of −4 mA will cause the output voltage to drop to a low voltage.These values apply for any one of the input terminals. If more than one of the input terminals are simultaneously driven negative, maximum currents are reduced. Common-mode current biasing can be used to prevent negative input voltages.

electrical characteristics, V_{CC} = 15 V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		LM2900			LM3900			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
I_{IB}	Input bias current (inverting input)	I_{I+} = 0	T_A = 25°C		30	200		30	200	nA
			T_A = Full range		300			300		
$\frac{I_{I-}}{I_{I+}}$	Mirror gain	I_{I+} = 20 µA to 200 µA T_A = Full range, See Note 4		0.9		1.1	0.9		1.1	µA/µA
	Change in mirror gain				2	5		2	5	%
	Mirror current	$V_{I+} = V_{I-}$, T_A = Full range, See Note 4			10	500		10	500	µA
A_{VD}	Large-signal differential voltage amplification	V_O = 10 V, R_L = 10 kΩ, f = 100 Hz		1.2	2.8		1.2	2.8		V/mV
r_i	Input resistance (inverting input)				1			1		MΩ
r_o	Output resistance				8			8		kΩ
B_1	Unity-gain bandwidth (inverting input)				2.5			2.5		MHz
k_{SVR}	Supply voltage rejection ratio ($\Delta V_{CC}/\Delta V_{IO}$)				70			70		dB
V_{OH}	High-level output voltage	I_{I+} = 0, I_{I-} = 0	R_L = 2 kΩ	13.5			13.5			V
			V_{CC} = 30 V, No load		29.5			29.5		
V_{OL}	Low-level output voltage	I_{I+} = 0, I_{I-} = 10 µA, R_L = 2 kΩ			0.09	0.2		0.09	0.2	V
I_{OHS}	Short-circuit output current (output internally high)	I_{I+} = 0, I_{I-} = 0, V_O = 0		−6	−18		−6	−10		mA
	Pull-down current			0.5	1.3		0.5	1.3		mA
I_{OL}	Low-level output current‡	I_{I-} = 5 µA, V_{OL} = 1 V			5			5		mA
I_{CC}	Supply current (four amplifiers)	No load			6.2	10		6.2	10	mA

†All characteristics are measured under open-loop conditions with zero common-mode voltage unless otherwise specified. Full range for T_A is −40°C to 85°C for LM2900, and 0°C to 70°C for LM3900.

‡The output current-sink capability can be increased for large-signal conditions by overdriving the inverting input.

NOTE 4: These parameters are measured with the output balanced midway between V_{CC} and ground.

operating characteristics, $V_{CC\pm}$ = ±15 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SR Slew rate at unit gain	Low-to-high output	V_O = 10 V, C_L = 100 pF, R_L = 2 kΩ		0.5		V/µs
	High-to-low output			20		

TYPICAL CHARACTERISTICS†

INPUT BIAS CURRENT (INVERTING INPUT)
vs
FREE-AIR TEMPERATURE

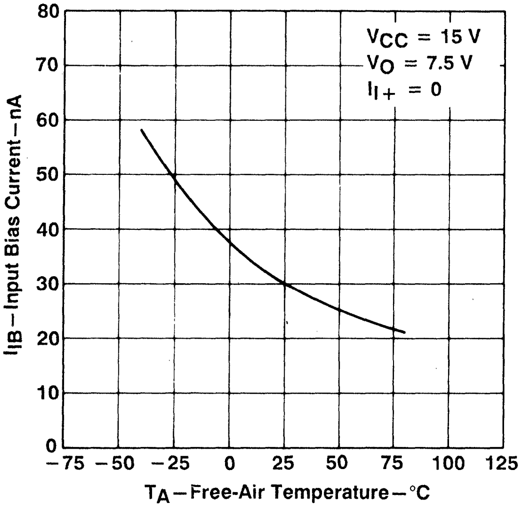


FIGURE 1

MIRROR GAIN
vs
FREE-AIR TEMPERATURE

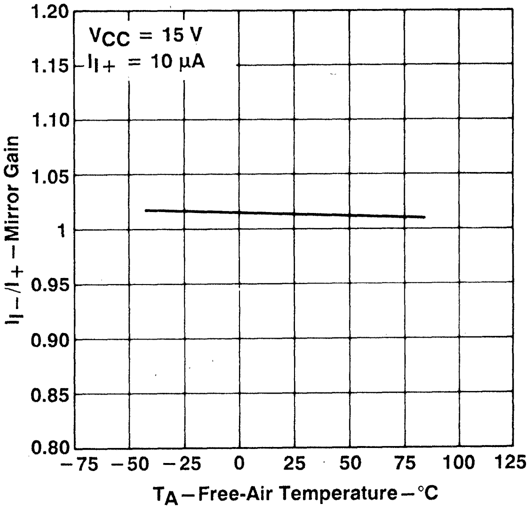


FIGURE 2

LARGE SIGNAL
DIFFERENTIAL VOLTAGE AMPLIFICATION
vs
FREQUENCY

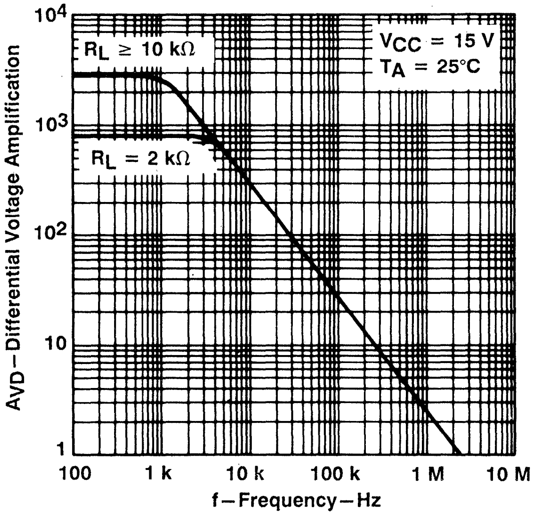


FIGURE 3

LARGE SIGNAL
DIFFERENTIAL VOLTAGE AMPLIFICATION
vs
SUPPLY VOLTAGE

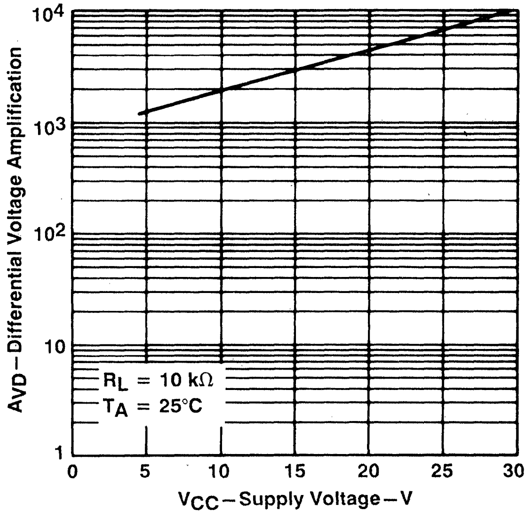


FIGURE 4

---

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

LARGE SIGNAL
DIFFERENTIAL VOLTAGE AMPLIFICATION
vs
FREE-AIR TEMPERATURE

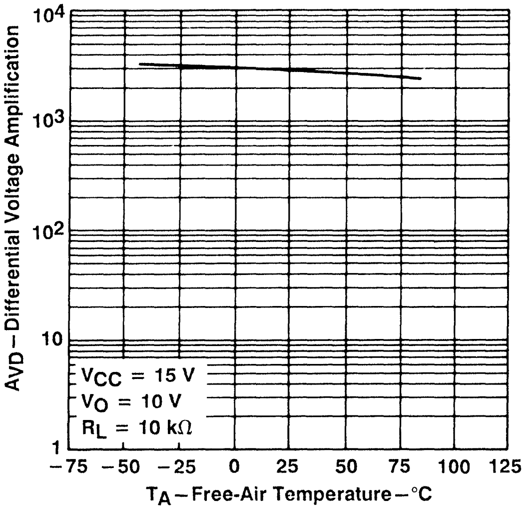


FIGURE 5

SUPPLY VOLTAGE REJECTION RATIO
vs
FREQUENCY

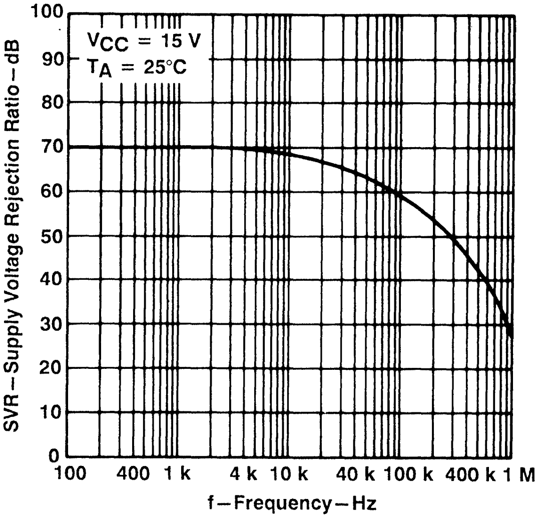


FIGURE 6

PEAK-TO-PEAK OUTPUT VOLTAGE
vs
FREQUENCY

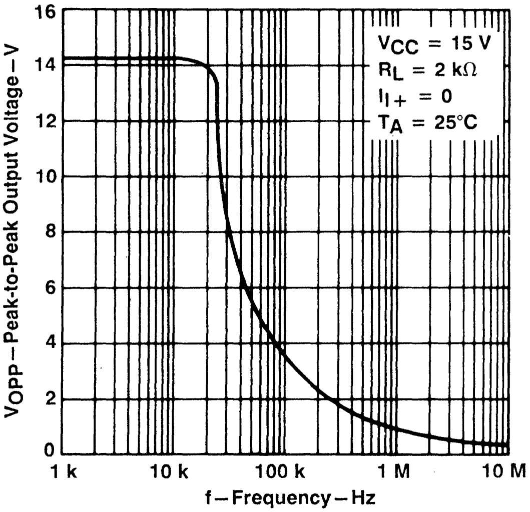


FIGURE 7

LM2900
SHORT-CIRCUIT OUTPUT CURRENT
(OUTPUT INTERNALLY HIGH)
vs
SUPPLY VOLTAGE

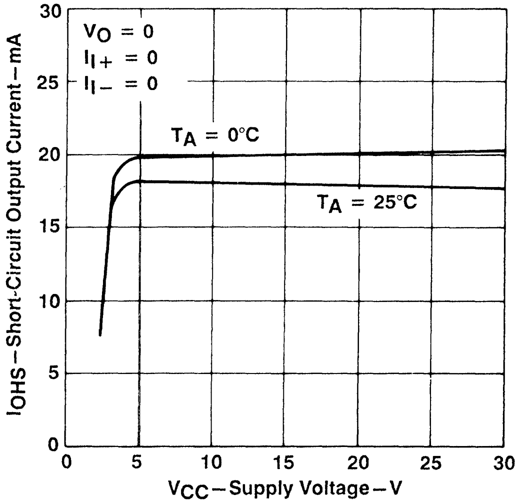


FIGURE 8

---

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

LOW-LEVEL OUTPUT CURRENT
vs
SUPPLY VOLTAGE

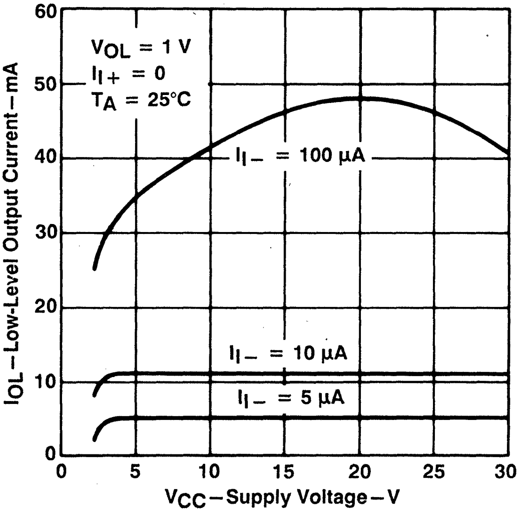


FIGURE 9

PULL-DOWN CURRENT
vs
SUPPLY VOLTAGE

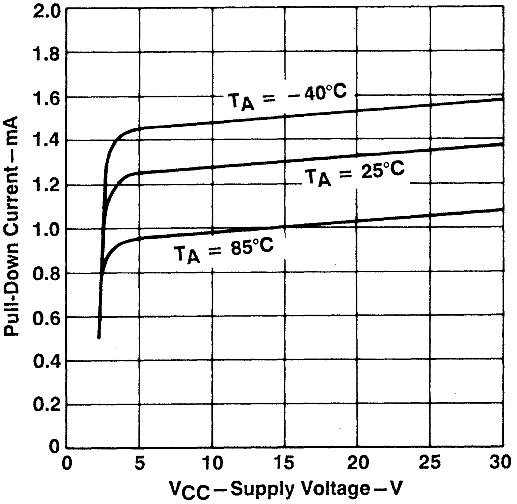


FIGURE 10

PULL-DOWN CURRENT
vs
FREE-AIR TEMPERATURE

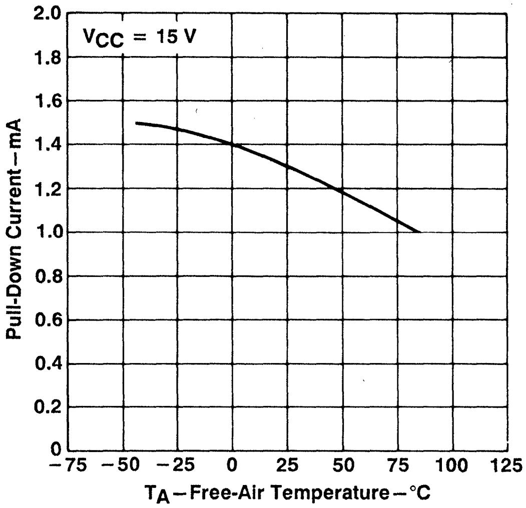


FIGURE 11

TOTAL SUPPLY CURRENT
vs
SUPPLY VOLTAGE

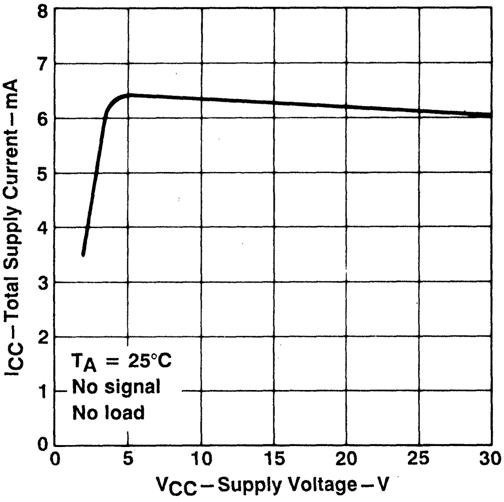


FIGURE 12

---

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL APPLICATION DATA

Norton (or current-differencing) amplifiers can be used in most standard general-purpose op-amp applications. Performance as a dc amplifier in a single-power-supply mode is not as precise as a standard integrated-circuit operational amplifier operating from dual supplies. Operation of the amplifier can best be understood by noting that input currents are differenced at the inverting input terminal and this current then flows through the external feedback resistor to produce the output voltage. Common-mode current biasing is generally useful to allow operating with signal levels near (or even below) ground.

Internal transistors clamp negative input voltages at approximately −0.3 V but the magnitude of current flow has to be limited by the external input network. For operation at high temperature, this limit should be approximately −100 μA.

Noise immunity of a Norton amplifier is less than that of standard bipolar amplifiers. Circuit layout is more critical since coupling from the output to the noninverting input can cause oscillations. Care must also be exercised when driving either input from a low-impedance source. A limiting resistor should be placed in series with the input lead to limit the peak input current. Current up to 20 mA will not damage the device but the current mirror on the noninverting input will saturate and cause a loss of mirror gain at higher current levels, especially at high operating temperatures.

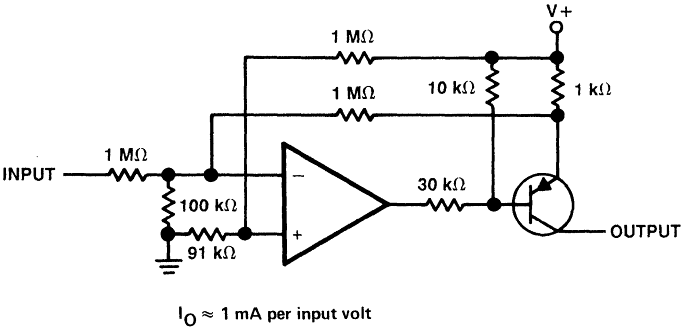


FIGURE 13. VOLTAGE-CONTROLLED CURRENT SOURCE

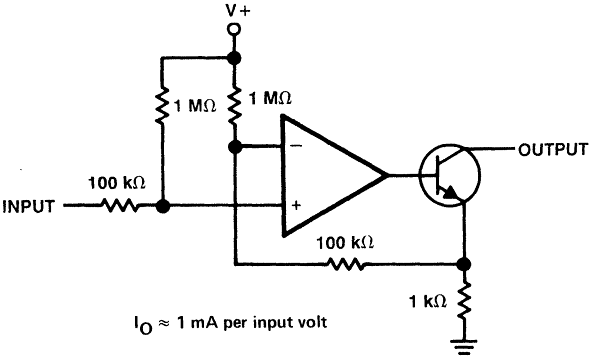


FIGURE 14. VOLTAGE-CONTROLLED CURRENT SINK

LT1007, LT1007A, LT1037, LT1037A
LOW-NOISE, HIGH-SPEED, PRECISION OPERATIONAL AMPLIFIERS

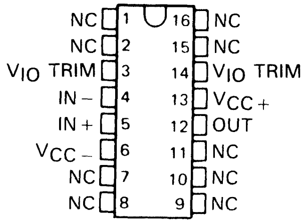
D3195, FEBRUARY 1989—REVISED JUNE 1991

- **Maximum Equivalent Input Noise Voltage:**
  3.8 nV/√Hz at 1 kHz
  4.5 nV/√Hz at 10 Hz
- **Low Peak-to-Peak Equivalent Input Noise Voltage: 60 nV Typ from 0.1 Hz to 10 Hz**
- **Slew Rate (LT1037 and LT1037A): 11 V/μs Min**

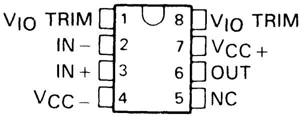
LT1007A and LT1037A Specifications:

- **High Voltage Amplification:**
  7 V/μV Min, R_L = 2 kΩ
  3 V/μV Min, R_L = 600 Ω
- **Low Input Offset Voltage 25 μV Max**
- **Low Input Offset Voltage Temperature Coefficient: 0.6 μV/°C Max**
- **Common-Mode Rejection Ratio: 117 dB Min**

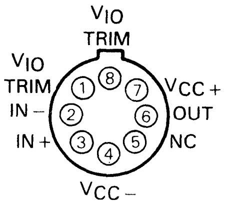
DW SMALL-OUTLINE PACKAGE
(TOP VIEW)



JG AND P
DUAL-IN-LINE PACKAGES
(TOP VIEW)



L PLUG-IN PACKAGE
(TOP VIEW)



Pin 4 (L Package) is in electrical contact with the case
NC—No internal connection

description

These monolithic operational amplifiers feature extremely low noise performance and outstanding precision and speed specifications. The typical differential voltage amplification (at T_A = 25°C) of these devices is an extremely high 20 V/μV driving a 2-kΩ load to ±12 V and 12 V/μV driving a 600-Ω load to ±10 V.

In the design, processing, and testing of the device, particular attention has been paid to the optimization of the entire distribution of several key parameters. Consequently, the specifications of even the lowest-cost grades (the LT1007C and the LT1037C) have been greatly improved compared to equivalent grades of competing amplifiers.

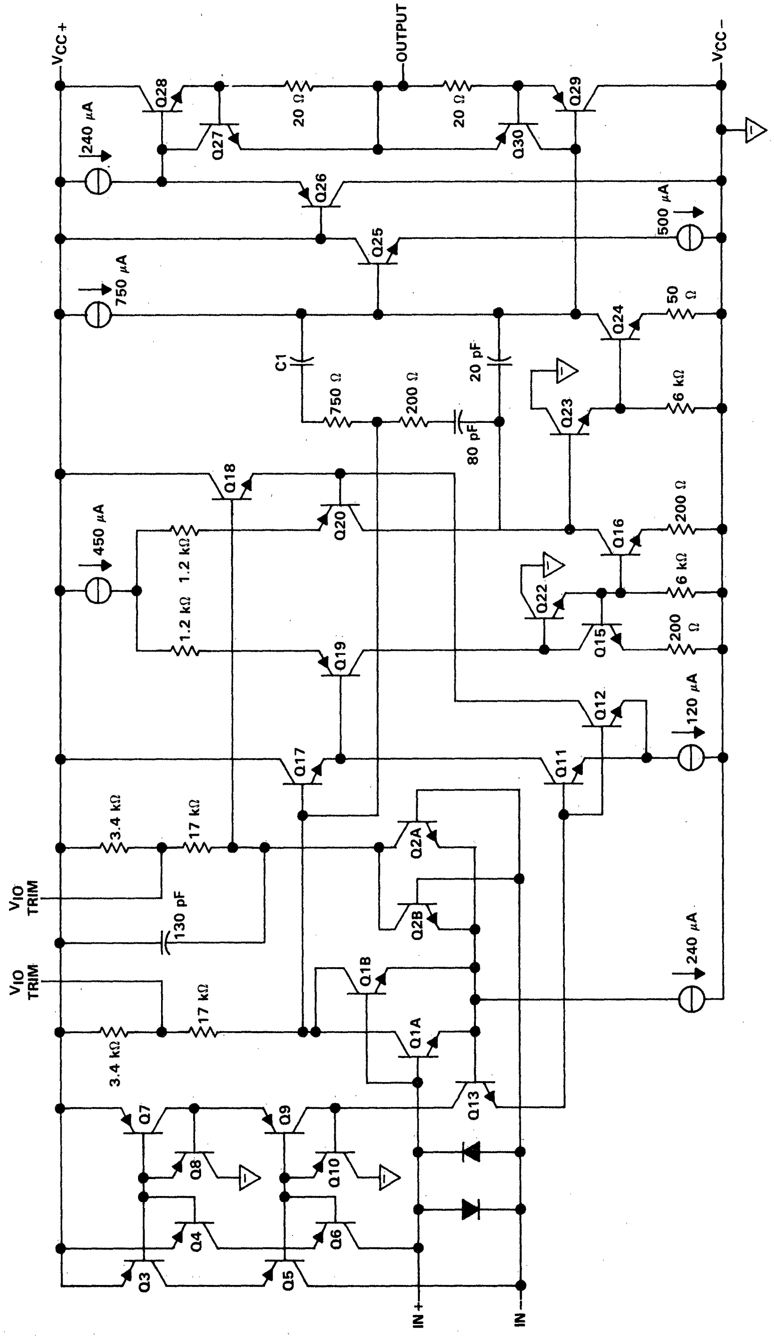
AVAILABLE OPTIONS

T_A	V_{IO} MAX AT 25°C	PACKAGE			
		SMALL-OUTLINE (DW)	CERAMIC DIP (JG)	METAL CAN (L)	PLASTIC DIP (P)
0°C to 70°C	60 μV	LT1007CDW	—	—	LT1007CP
	25 μV	—	—	—	LT1007ACP
	60 μV	LT1037CDW	—	—	LT1037CP
	25 μV	—	—	—	LT1037ACP
−55°C to 125°C	60 μV	—	LT1007MJG	LT1007ML	LT1007MP
	25 μV	—	LT1007AMJG	LT1007AML	LT1007AMP
	60 μV	—	LT1037MJG	LT1037ML	LT1037MP
	25 μV	—	LT1037AMJG	LT1037AML	LT1037AMP

The DW packages are available taped and reeled. Add the suffix "R" to the device type, (e.g., LT1007CDWR).

TEXAS
INSTRUMENTS

schematic



C1 = 110 pF for LT1007
C1 = 12 pF for LT1037
All component values shown are nominal.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC+} (see Note 1)	22 V
Supply voltage, V_{CC-}	−22 V
Input voltage	$V_{CC\pm}$
Duration of output short-circuit	Unlimited
Differential input current (see Note 2)	±25 mA
Power dissipation	See Dissipation Rating Table
Operating free-air temperature range:	
LT1007C, LT1007AC, LT1037C, LT1037AC	0°C to 70°C
LT1007M, LT1007AM, LT1037M, LT1037AM	−55°C to 125°C
Storage temperature range	−65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: DW and P packages	260°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: JG and L packages	300°C

NOTES: 1. All voltage values, unless otherwise noted, are with respect to the midpoint between V_{CC+} and V_{CC-}.
2. The inputs are protected by back-to-back diodes. Current limiting resistors are not used in order to achieve low noise. Excessive input current will flow if a differential input voltage in excess of approximately ±0.7 V is applied between the inputs, unless some limiting resistance is used.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 125°C$ POWER RATING
DW	1025 mW	8.2 mW/°C	656 mW	N/A
JG	1050 mW	8.4 mW/°C	672 mW	210 mW
L	825 mW	6.6 mW/°C	528 mW	165 mW
P	1000 mW	8 mW/°C	640 mW	200 mW

recommended operating conditions

		C-SUFFIX			M-SUFFIX			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC+}		4	15	22	4	15	22	V
Supply voltage, V_{CC-}		−4	−15	−22	−4	−15	−22	V
Input voltage, V_I	$T_A = 25°C$	±11			±11			V
	T_A = full range	±10.5			±10.3			V
Operating free-air temperature, T_A		0		70	−55		125	°C

electrical characteristics, V_{CC+} = 15 V, V_{CC-} = −15 V

PARAMETER		TEST CONDITIONS	T_A	LT1007C, LT1037C			LT1007AC, LT1037AC			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	See Note 3	25°C		20	60		10	25	µV
			0°C to 70°C			110			50	
αV_{IO}	Average temperature coefficient of input offset voltage		0°C to 70°C			1			0.6	µV/°C
I_{IO}	Input offset current		25°C		12	50		7	30	nA
			0°C to 70°C			70			40	
I_{IB}	Input bias current		25°C		±15	±55		±10	±35	nA
			0°C to 70°C			±75			±45	
V_{OM}	Peak output voltage swing	R_L = 2 kΩ	25°C	±12.5	±13.5		±13	±13.8		V
		R_L = 600 Ω	25°C	±10.5	±12.5		±11	±12.5		
		R_L = 2 kΩ	0°C to 70°C	±12			±12.5			
A_{VD}	Large-signal differential voltage amplification	$R_L \geq$ 2 kΩ, V_O = ±12 V	25°C	5	20		7	20		V/µV
		$R_L \geq$ 1 kΩ, V_O = ±10 V	25°C	3.5	16		5	16		
		$R_L \geq$ 600 Ω, V_O = ±10 V	25°C	2	12		3	12		
		$R_L \geq$ 2 kΩ, V_O = ±10 V	0°C to 70°C	2.5			4			
		$R_L \geq$ 1 kΩ, V_O = ±10 V	0°C to 70°C	2			2.5			
$r_{i(CM)}$	Common-mode input resistance		25°C		5			7		GΩ
r_o	Open-loop output resistance		25°C		70			70		Ω
CMRR	Common-mode rejection ratio	V_{IC} = ±11 V	25°C	110	126		117	130		dB
		V_{IC} = ±10.5 V	0°C to 70°C	106			114			
k_{SVR}	Supply voltage rejection ratio	$V_{CC\pm}$ = ±4 V to ±18 V	25°C	106	126		110	130		dB
		$V_{CC\pm}$ = ±4.5 V to ±18 V	0°C to 70°C	102			106			
P_D	Power dissipation	LT1007C, LT1007AC	25°C		80	140		80	120	mW
		LT1037C, LT1037AC	25°C		85	140		80	130	
			0°C to 70°C			160			144	

NOTE 3: V_{IO} measurements are performed by automatic test equipment approximately 0.5 seconds after application of power.

electrical characteristics, V_{CC+} = 15 V, V_{CC-} = −15 V

PARAMETER	TEST CONDITIONS	T_A	LT1007M, LT1037M			LT1007AM, LT1037AM			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO} Input offset voltage	See Note 3	25°C		20	60		10	25	µV
		−55°C to 125°C			160			60	
αV_{IO} Average temperature coefficient of input offset voltage		−55°C to 125°C			1			0.6	µV/°C
I_{IO} Input offset current		25°C		12	50		7	30	nA
		−55°C to 125°C			85			50	
I_{IB} Input bias current		25°C		±15	±55		±10	±35	nA
		−55°C to 125°C			±95			±60	
V_{OM} Peak output voltage swing	R_L = 2 kΩ	25°C	±12.5	±13.5		±13	±13.8		V
	R_L = 600 Ω	25°C	±10.5	±12.5		±11	±12.5		
	R_L = 2 kΩ	−55°C to 125°C	±12			±12.5			
A_{VD} Large-signal differential voltage amplification	R_L ≥ 2 kΩ, V_O = ±12 V	25°C	5	20		7	20		V/µV
	R_L ≥ 1 kΩ, V_O = ±10 V	25°C	3.5	16		5	16		
	R_L ≥ 600 Ω, V_O = ±10 V	25°C	2	12		3	12		
	R_L ≥ 2 kΩ, V_O = ±10 V	−55°C to 125°C	2			3			
	R_L ≥ 1 kΩ, V_O = ±10 V	−55°C to 125°C	1.5			2			
$r_{i(CM)}$ Common-mode input resistance		25°C		5			7		GΩ
r_o Open-loop output resistance		25°C		70			70		Ω
CMRR Common-mode rejection ratio	V_{IC} = ±11 V	25°C	110	126		117	130		dB
	V_{IC} = ±10.3 V	−55°C to 125°C	104			112			
k_{SVR} Supply voltage rejection ratio	$V_{CC\pm}$ = ±4 V to ±18 V	25°C	106	126		110	130		dB
	$V_{CC\pm}$ = ±4.5 V to ±18 V	−55°C to 125°C	100			104			
P_D Power dissipation	LT1007M, LT1007AM	25°C		80	140		80	120	mW
	LT1037M, LT1037AM	25°C		85	140		80	130	
		−55°C to 125°C			170			150	

NOTE 3: V_{IO} measurements are performed by automatic test equipment approximately 0.5 seconds after application of power.

operating characteristics $V_{CC\pm} = \pm 15$ V, $T_A = 25°C$

PARAMETER		TEST CONDITIONS	LT1007, LT1007A			LT1037, LT1037A			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
SR	Slew rate	$R_L \ge 2$ kΩ, $A_{VD} \ge 1$ (LT1007, LT1007A) $R_L \ge 2$ kΩ, $A_{VD} \ge 5$ (LT1037, LT1037A)	1.7	2.5		11	15		V/μs
V_{NPP}	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 10 Hz, See Note 4		0.06	0.13		0.06	0.13	μV
V_n	Equivalent input noise noise voltage	f = 10 Hz		2.8	4.5		2.8	4.5	nV/√Hz
		f = 1 kHz		2.5	3.8		2.5	3.8	
I_n	Equivalent input noise current	f = 10 Hz, See Note 5		1.5	4		1.5	4	pA/√Hz
		f = 1 kHz, See Note 5		0.4	0.6		0.4	0.6	
GBW	Gain bandwidth product	f = 100 kHz	5	8					MHz
		f = 10 kHz, $A_V \ge 15$				45	60		

NOTES: 4. See the test circuit and frequency response curve for 0.1 Hz to 10 Hz noise (Figure 39) in the Applications Information section.
5. See the test circuit for current noise measurement (Figure 40) in the Applications Information section.

TYPICAL CHARACTERISTICS

table of graphs

			FIGURE
V_{IO}	Input offset voltage	vs Temperature	1
ΔV_{IO}	Change in input offset voltage	vs Time after power on	2
		vs Time (long-term stability)	3
I_{IO}	Input offset current	vs Temperature	4
I_{IB}	Input bias current	vs Temperature	5
		over common-mode range	6
	Common-mode limit voltage	vs Free-air temperature	7
V_{OM}	Maximum peak output voltage swing	vs Load resistance	8
		vs Frequency	9
A_{VD}	Differential voltage amplification	vs Frequency	10
		vs Frequency (LT1007)	11
		vs Frequency (LT1037)	12
		vs Temperature	13
		vs Load resistance	14
		vs Supply voltage	15
		at 2 kΩ and 600 Ω	16
V_{ID}	Differential input voltage	vs Output voltage	16
CMRR	Common-mode rejection ratio	vs Frequency	17
k_{SVR}	Supply voltage rejection ratio	vs Frequency	18
SR	Slew rate	vs Free-air temperature (LT1007)	19
		vs Free-air temperature (LT1037)	20
ϕ	Phase shift	vs Frequency (LT1007)	11
		vs Frequency (LT1037)	12
ϕ_m	Phase margin	vs Free-air temperature (LT1007)	19
		vs Free-air temperature (LT1037)	20
V_n	Equivalent input noise voltage	vs Free-air temperature	21
		vs Time (0.01-Hz to 1-Hz noise)	22
		vs Frequency	23
		vs Bandwidth	24
		vs Supply voltage	25
I_n	Equivalent input noise current	vs Frequency	26
	Total noise	vs Source resistance	27
GBW	Gain bandwidth product	vs Free-air temperature (LT1007)	19
		vs Free-air temperature (LT1037)	20
I_{OS}	Short-circuit output current	vs Time (from short to GND)	28
I_{CC}	Supply current	vs Supply voltage	29
z_o	Closed-loop output impedance	vs Frequency	30
	Pulse response (LT1037)	Small-signal (C_{load} = 15 pF)	31
		Large-signal	32
	Pulse response (LT1007)	Small-signal (C_{load} = 15 pF)	33
		Large-signal	34

TYPICAL CHARACTERISTICS†

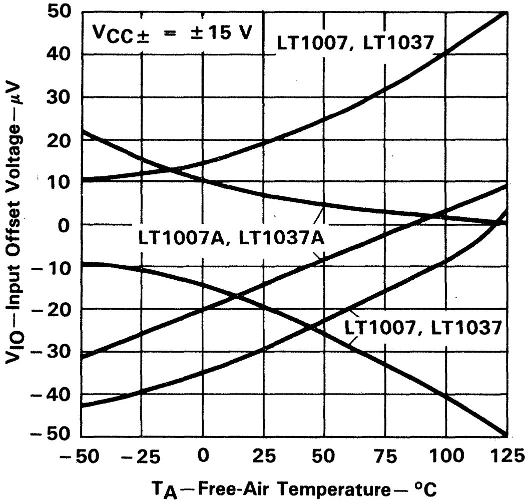

INPUT OFFSET VOLTAGE
OF REPRESENTATIVE UNITS
vs
FREE-AIR TEMPERATURE

Figure 1

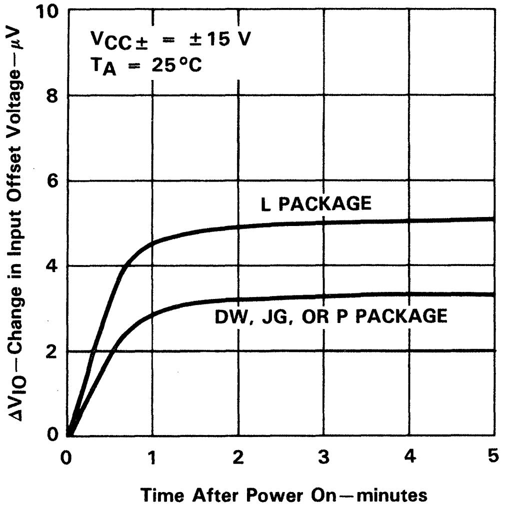

INPUT OFFSET VOLTAGE CHANGE
vs
TIME AFTER POWER ON

Figure 2

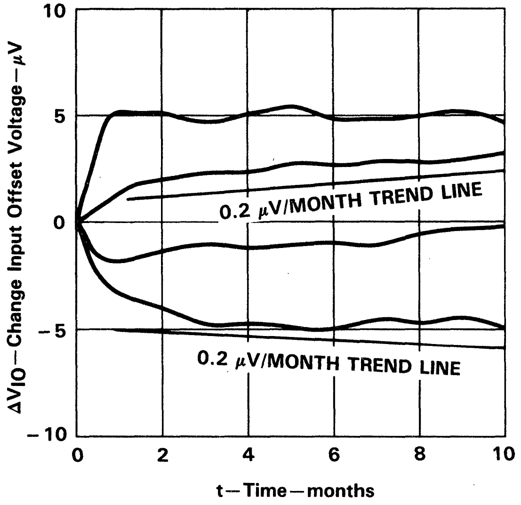

LONG TERM STABILITY OF
INPUT OFFSET VOLTAGE
FOR FOUR REPRESENTATIVE UNITS

Figure 3

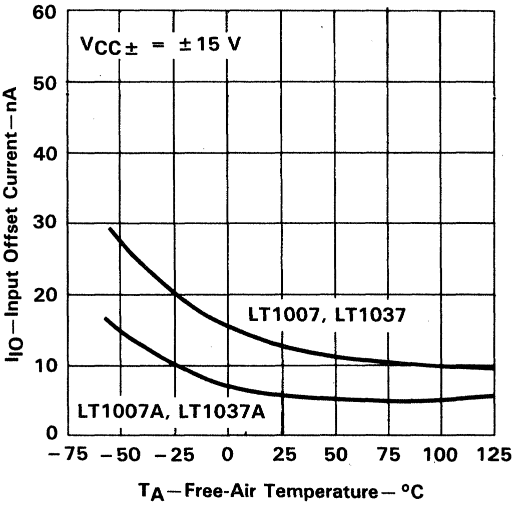

INPUT OFFSET CURRENT
vs
TEMPERATURE

Figure 4

---

†Data at high and low temperatures are applicable within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

INPUT BIAS CURRENT
vs
FREE-AIR TEMPERATURE

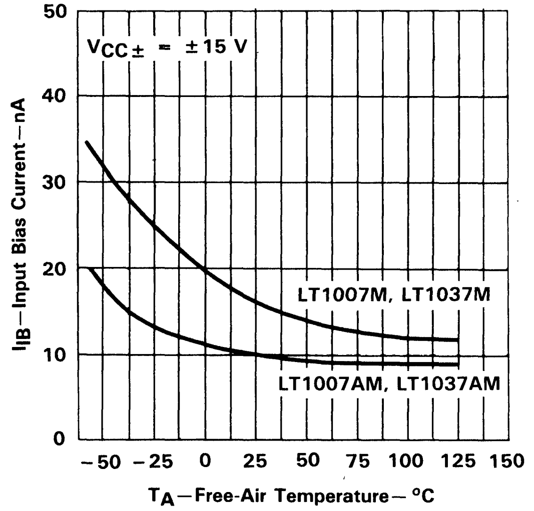


Figure 5

INPUT BIAS CURRENT
vs
COMMON-MODE INPUT VOLTAGE

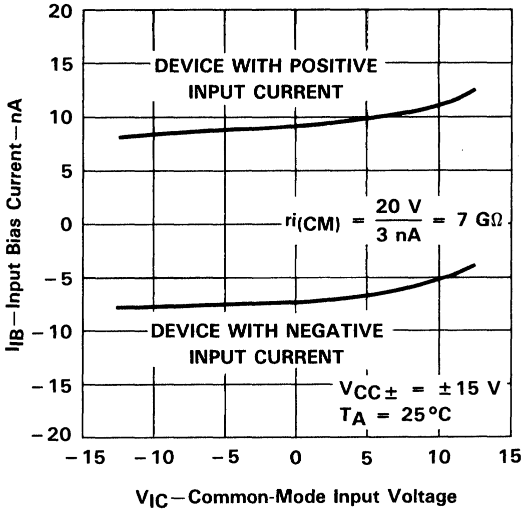


Figure 6

COMMON-MODE INPUT VOLTAGE RANGE LIMITS
vs
FREE-AIR TEMPERATURE

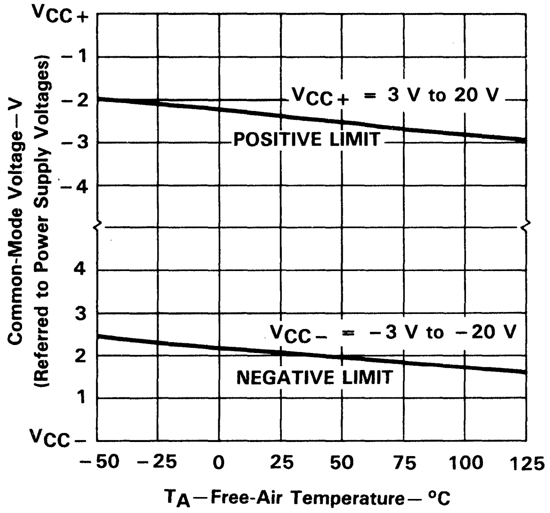


Figure 7

PEAK OUTPUT VOLTAGE SWING
vs
LOAD RESISTANCE

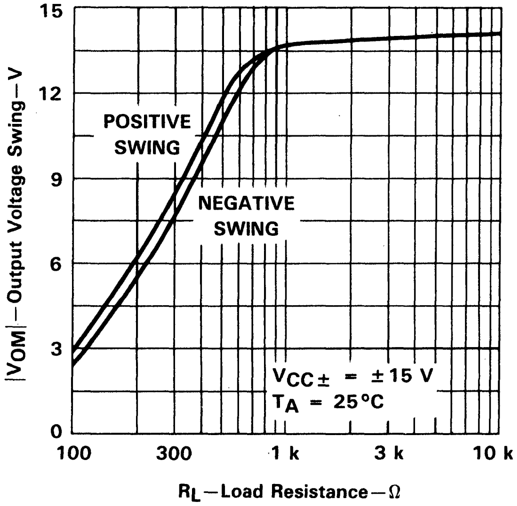


Figure 8

---

†Data at high and low temperatures are applicable within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS

PEAK-TO-PEAK OUTPUT VOLTAGE SWING
vs
FREQUENCY

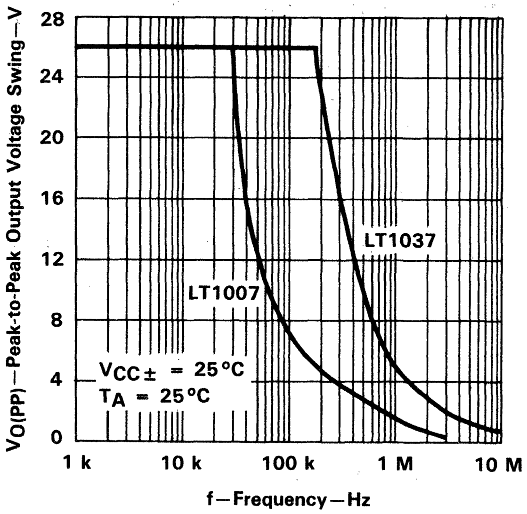


Figure 9

DIFFERENTIAL VOLTAGE AMPLIFICATION
vs
FREQUENCY

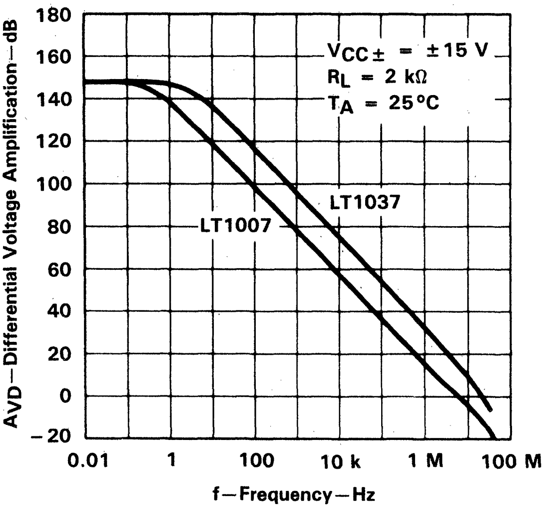


Figure 10

LT1007
DIFFERENTIAL VOLTAGE AMPLIFICATION
AND PHASE SHIFT
vs
FREQUENCY

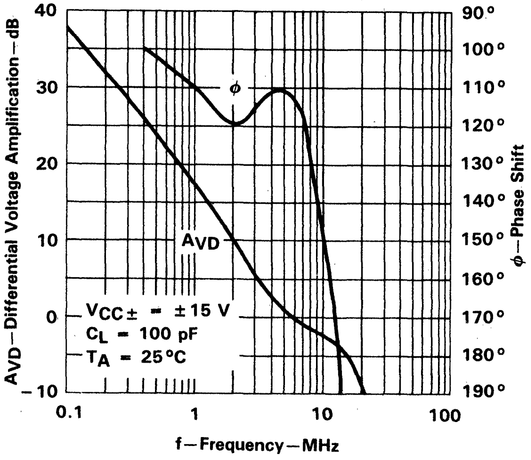


Figure 11

LT1037
DIFFERENTIAL VOLTAGE AMPLIFICATION
AND PHASE SHIFT
vs
FREQUENCY

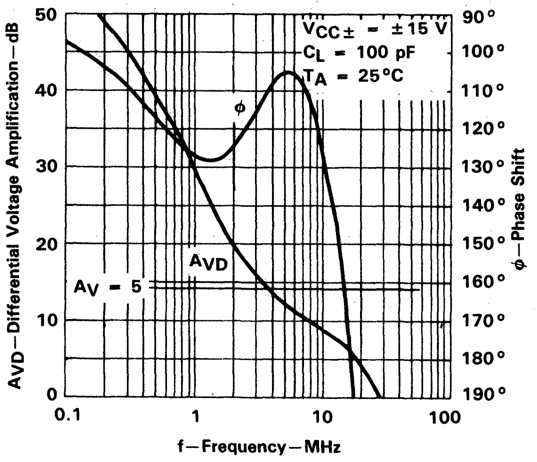


Figure 12

TYPICAL CHARACTERISTICS†

DIFFERENTIAL VOLTAGE AMPLIFICATION
vs
FREE-AIR TEMPERATURE

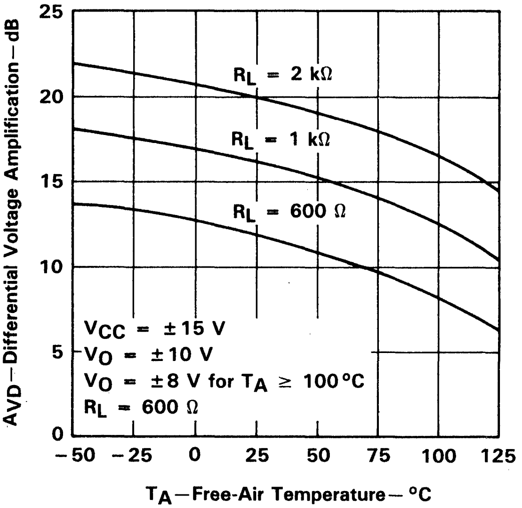


Figure 13

DIFFERENTIAL VOLTAGE AMPLIFICATION
vs
LOAD RESISTANCE

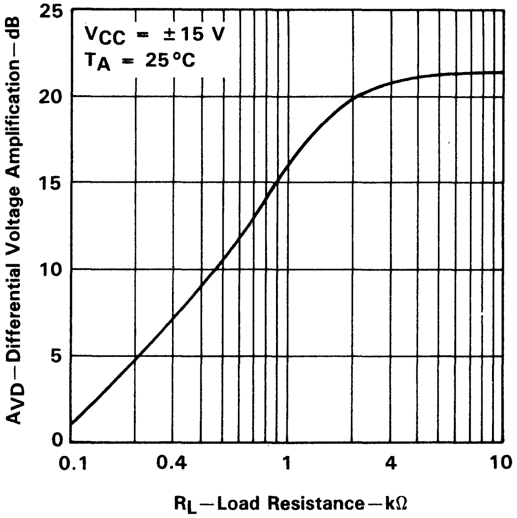


Figure 14

DIFFERENTIAL VOLTAGE AMPLIFICATION
vs
SUPPLY VOLTAGE

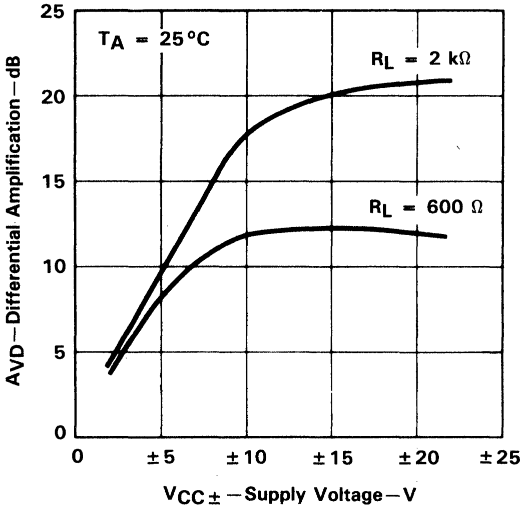


Figure 15

DIFFERENTIAL INPUT VOLTAGE
vs
OUTPUT VOLTAGE

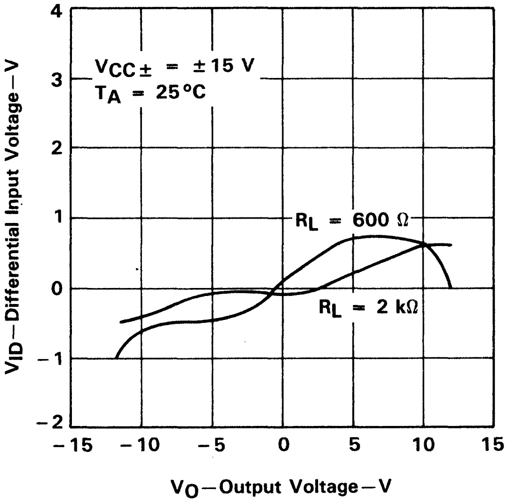


Figure 16

---

†Data at high and low temperatures are applicable within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

COMMON-MODE REJECTION RATIO
vs
FREQUENCY

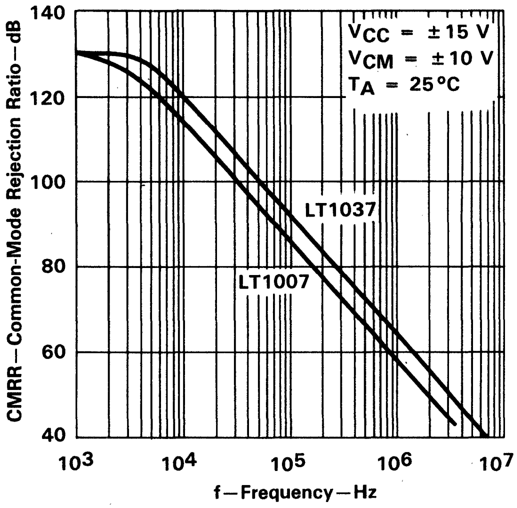


Figure 17

SUPPLY VOLTAGE REJECTION RATIO
vs
FREQUENCY

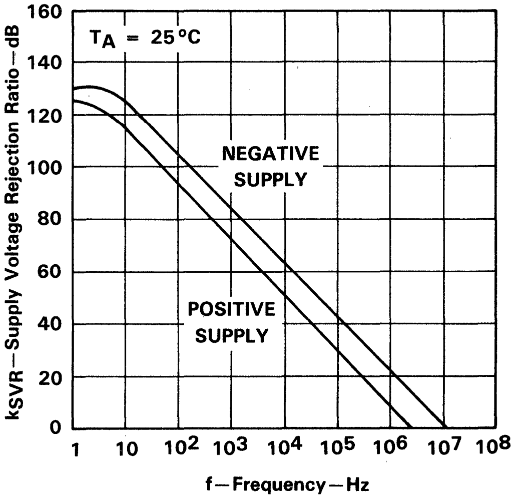


Figure 18

LT1007
SLEW RATE, PHASE MARGIN AND
GAIN BANDWIDTH PRODUCT
vs
FREE-AIR TEMPERATURE

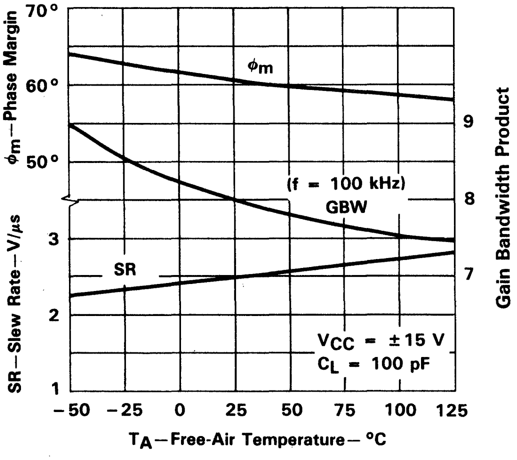


Figure 19

LT1037
SLEW RATE, PHASE MARGIN AND
GAIN BANDWIDTH PRODUCT
vs
FREE-AIR TEMPERATURE

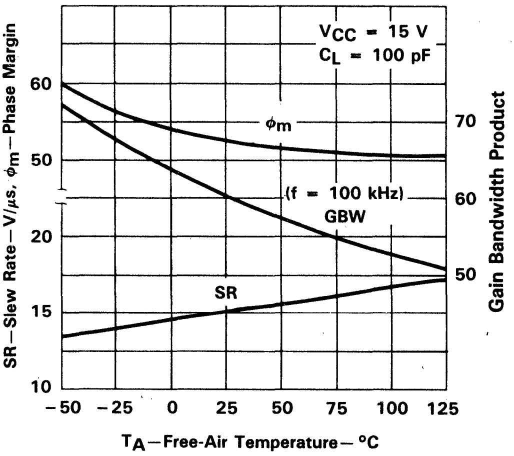


Figure 20

---

†Data at high and low temperatures are applicable within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

EQUIVALENT INPUT NOISE VOLTAGE
vs
FREE-AIR TEMPERATURE

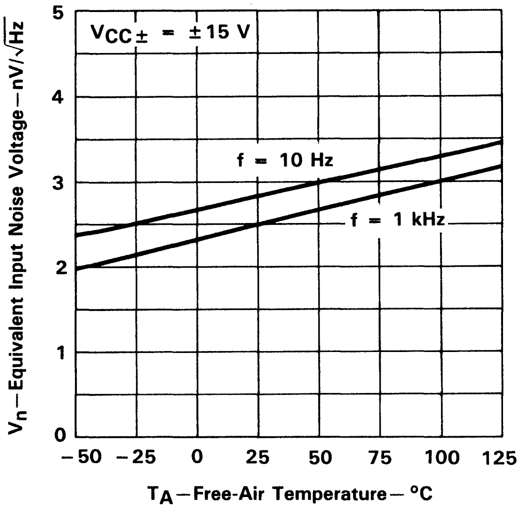


Figure 21

EQUIVALENT INPUT NOISE VOLTAGE
OVER A 100-SECOND TIME PERIOD

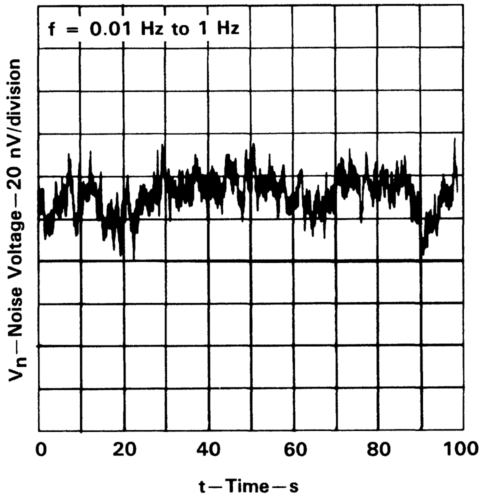


Figure 22

EQUIVALENT INPUT NOISE VOLTAGE
vs
FREQUENCY

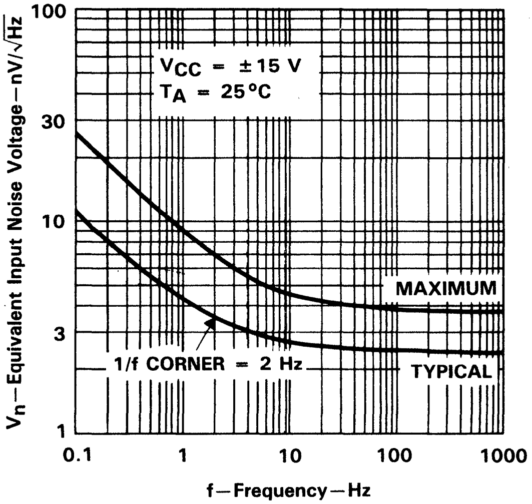


Figure 23

BROADBAND NOISE VOLTAGE
0.1 Hz TO INDICATED FREQUENCY

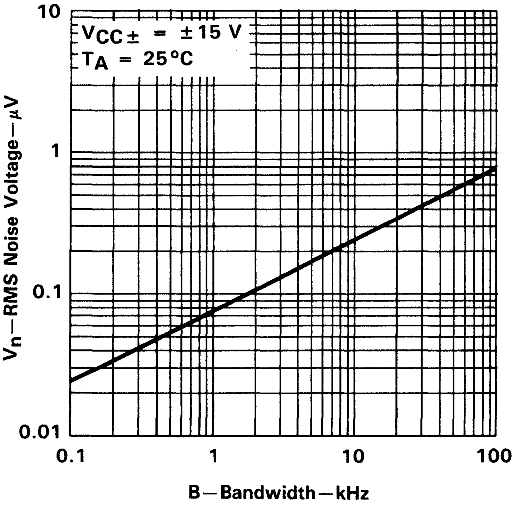


Figure 24

---

†Data at high and low temperatures are applicable within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

EQUIVALENT INPUT NOISE VOLTAGE
vs
SUPPLY VOLTAGE

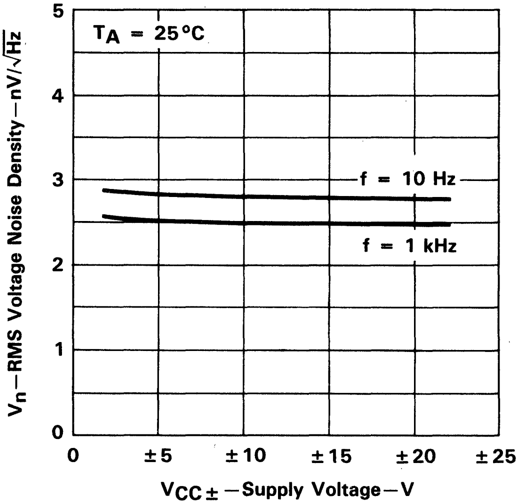


Figure 25

EQUIVALENT INPUT NOISE CURRENT
vs
FREQUENCY

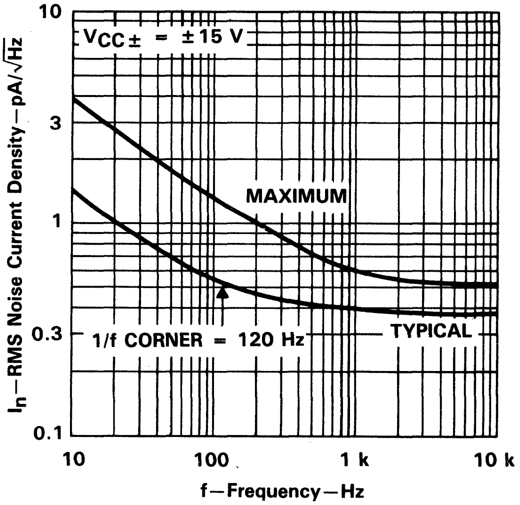


Figure 26

TOTAL NOISE VOLTAGE
vs
SOURCE RESISTANCE

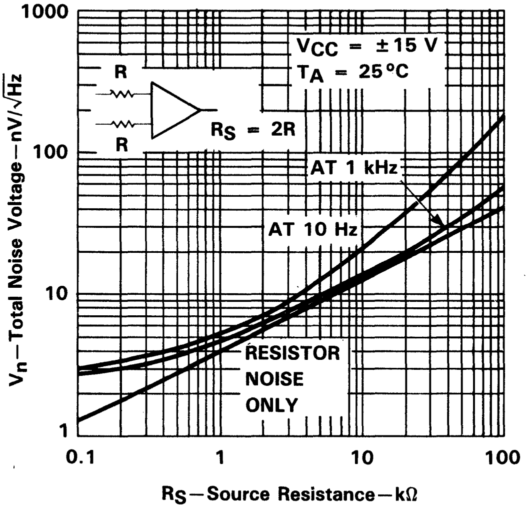


Figure 27

SHORT-CIRCUIT OUTPUT CURRENT
vs
ELAPSED TIME

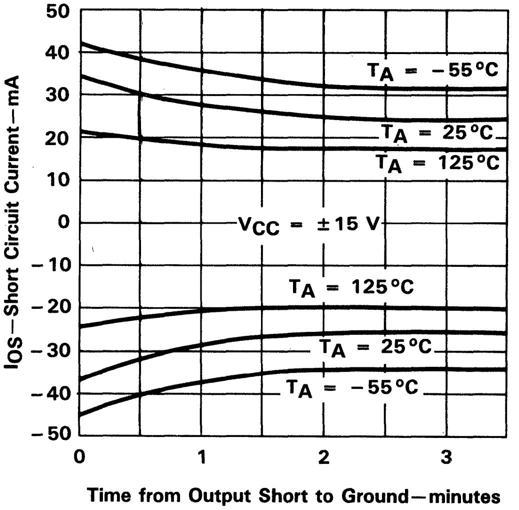


Figure 28

---

† Data at high and low temperatures are applicable within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

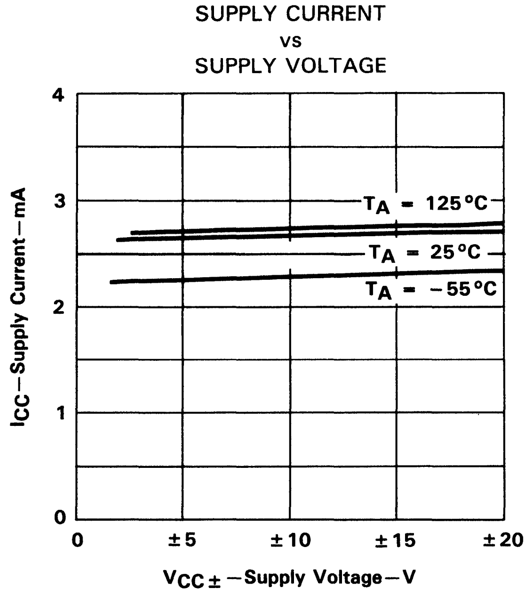


Figure 29

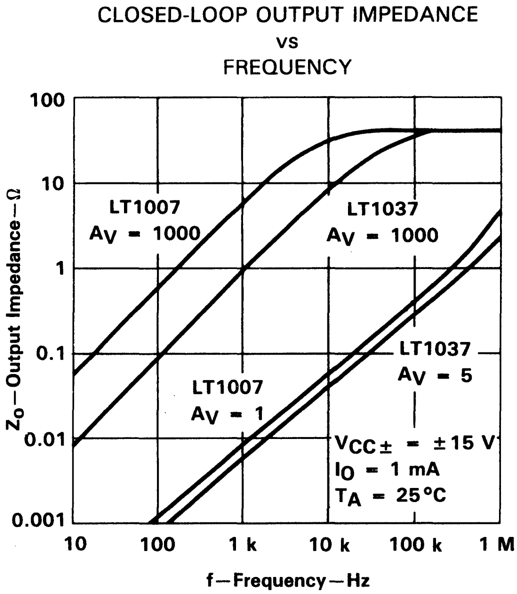


Figure 30

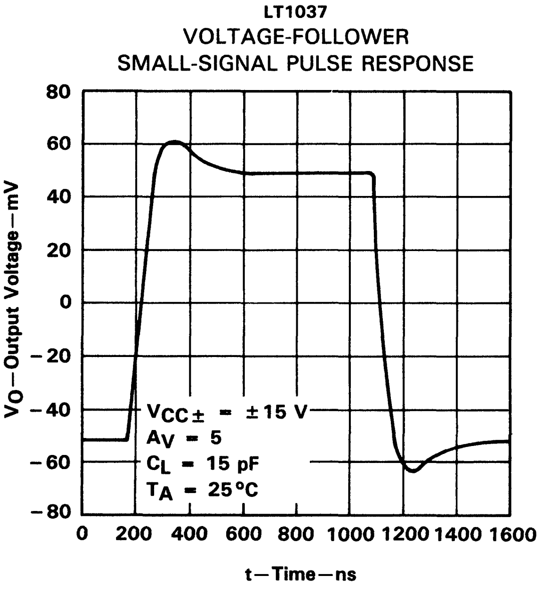


Figure 31

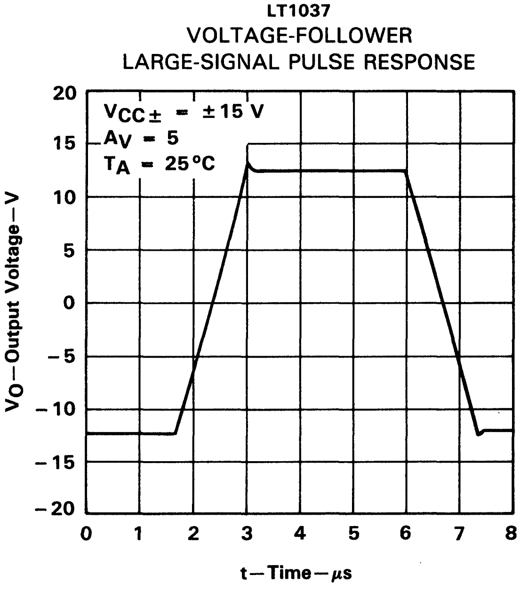
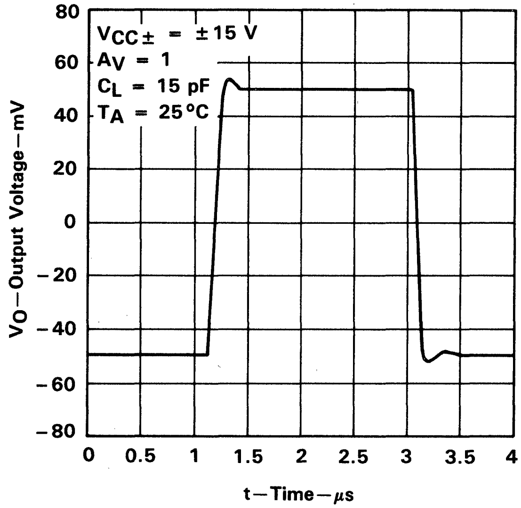


Figure 32

---

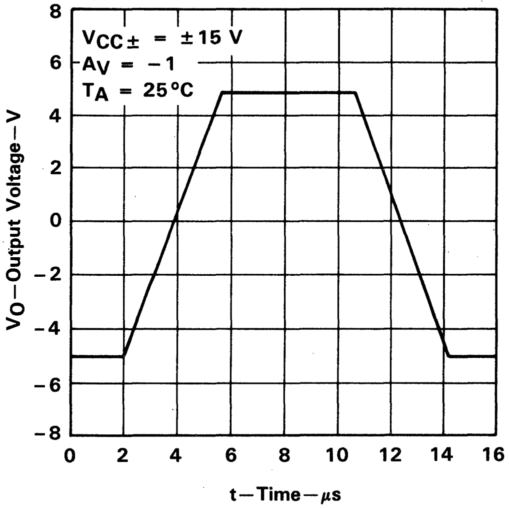
†Data at high and low temperatures are applicable within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS



LT1007
VOLTAGE-FOLLOWER
SMALL-SIGNAL PULSE RESPONSE

Figure 33



LT1007
VOLTAGE-FOLLOWER
LARGE-SIGNAL PULSE RESPONSE

Figure 34

TYPICAL APPLICATION DATA

general

The LT1007- and LT1037-series devices may be inserted directly into OP-07, OP-27, OP-37, and 5534 sockets with or without removal of external-compensation or nulling components. In addition, the LT1007 and LT1037 may be fitted to µA741 sockets by removing or modifying external nulling components.

offset voltage adjustment

The input offset voltage and its change with temperature of the LT1007 and LT1037 are permanently trimmed to a low level at wafer testing . However, if further adjustment of V_{IO} is necessary, the use of a 10-kΩ nulling potentiometer, as shown in Figure 35, will not degrade drift with temperature. Trimming to a value other than zero creates a drift of V_{IO}/300 µV/°C (e.g., if V_{IO} is adjusted to 300 µV, the change in temperature coefficient will be 1 µV/°C).

The adjustment range with a 10-kΩ potentiometer is approximately ±2.5 mV. If a smaller adjustment range is needed, the sensitivity and resolution of the nulling can be improved by using a smaller potentiometer in conjunction with fixed resistors. The example in Figure 36 has an approximate null range of ±200 µV.

offset voltage and drift

Unless proper care is exercised, thermocouple effects at the contacts to the input terminals, caused by temperature gradients across dissimilar metals, can exceed the inherent temperature coefficient of the amplifier. Air currents should be minimized, package leads should be short, input leads should be close together, and input leads should be at the same temperature.

TYPICAL APPLICATION DATA

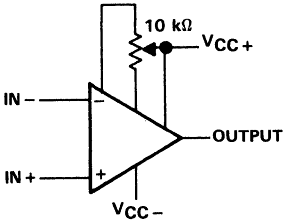


Figure 35. Standard Adjustment

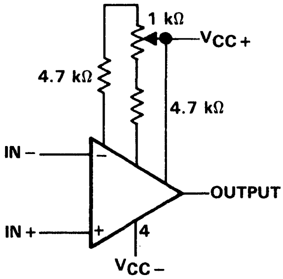


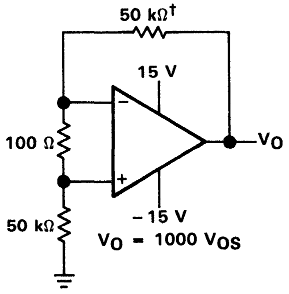
Figure 36. Improved Sensitivity Adjustment

The circuit shown in Figure 37 can be used to measure offset voltage. In addition, with the supply voltages increased to ±20 V, it can be used as the burn-in configuration for the LT1007 and LT1037.

When $R_F \leq 100\ \Omega$ and the input is driven with a fast large-signal pulse (>1 V), the output waveform will be as shown in Figure 38.

During the fast-feedthrough-like portion of the output, the input protection diodes effectively short the output to the input and a current, limited only by the output short-circuit protection, is drawn by the signal generator. When R_F is $\geq 500\ \Omega$, the output is capable of handling the current requirements ($I_L \leq 20$ mA at 10 V), the amplifier stays in its active mode, and a smooth transition occurs.

When R_F is >2 kΩ, a pole will be created with R_F and the amplifier's input capacitance, creating additional phase shift and reducing the phase margin. A small capacitor (20 pF to 50 pF) in parallel with R_F will eliminate this problem.



†Resistors must have low thermoelectric potential

Figure 37. Test Circuit for Offset Voltage and Offset Voltage Drift With Temperature

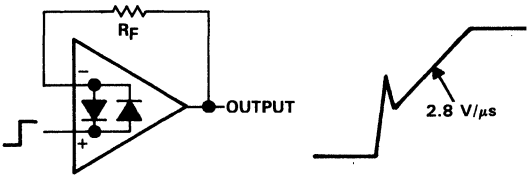


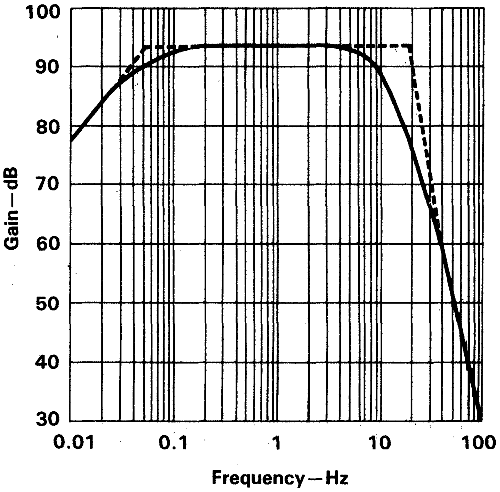
Figure 38. Pulse Operation

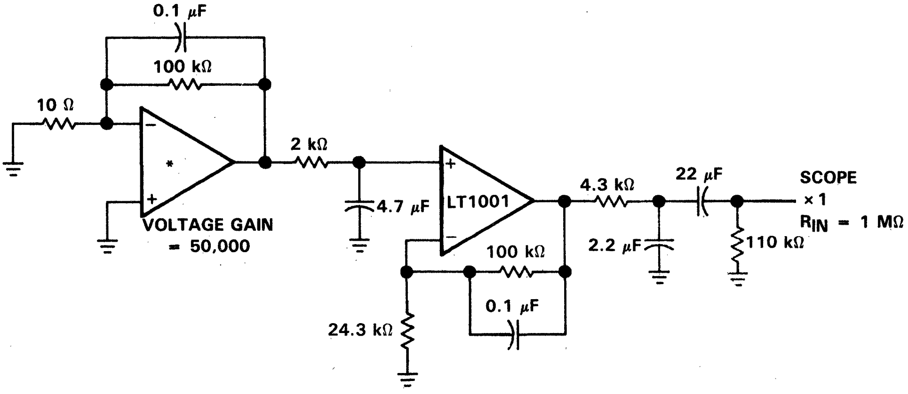
TYPICAL APPLICATION DATA

noise testing

Figure 39 shows a test circuit for 0.1-Hz to 10-Hz peak-to-peak noise measurement of the LT1007 and LT1037. The frequency response of this noise tester indicates that the 0.1 Hz corner is defined by only one zero. Because the time limit acts as an additional zero to eliminate noise contributions from the frequency band below 0.1 Hz, the test time to measure 0.1-Hz to 10-Hz noise should not exceed 10 seconds.

0.1 Hz to 10 Hz p-p NOISE TESTER
FREQUENCY RESPONSE





*Device under test
NOTE: All capacitor values are for non-polarized capacitors only.

Figure 39. 0.1-Hz to 10-Hz Noise Test Circuit

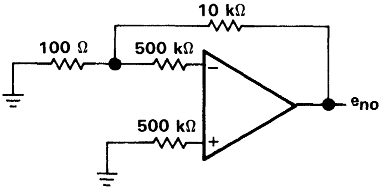
TYPICAL APPLICATION DATA

Special test precautions are required to measure the typical 60-nV peak-to-peak noise performance of the LT1007 and LT1037:

1. The device should be warmed up for at least five minutes. As the operational amplifier warms up, the offset voltage typically changes 3 μV, due to the chip temperature increasing 10 °C to 20 °C from the moment the power supplies are turned on. In the 10-second measurement interval, these temperature-induced effects can easily exceed tens of nanovolts.
2. The device must be well shielded from air currents to eliminate thermoelectric effects. In excess of a few nanovolts, thermoelectric effects would invalidate the measurements.
3. Sudden motion in the vicinity of the device can produce a feedthrough effect that increases observed noise.

When measuring noise on a large number of units, a noise-voltage density test is recommended. A 10-Hz noise-voltage density measurement will correlate well with a 0.1-Hz to 10-Hz peak-to-peak noise reading since both results are determined by the white noise and the location of the 1/f corner frequency.

Figure 40 shows a circuit that measures noise current and presents the formula for calculating noise current.



$$i_n = \frac{[v_n^2 - (130\text{ nV})^2]^{1/2}}{1\text{ M}\Omega \times 100}$$

Figure 40. Noise Test Circuit

The LT1007 and LT1037 achieve low noise, in part, by operating the input stage at 120 μA versus the typical 10 μA for most other operational amplifiers. Voltage noise is directly proportional to the square root of the stage current; therefore, the LT1007 and LT1037 noise current is relatively high. At low frequencies, the low 1/f current-noise corner frequency (≈ 120 Hz) minimizes noise current to some extent.

In most practical applications, however, noise current will not limit system performance; this is illustrated in Figure 27, where:

$$\text{total noise} = [(\text{noise voltage})^2\ (\text{noise current} \times R_S)^2 + (\text{resistor noise})^2]^{1/2}$$

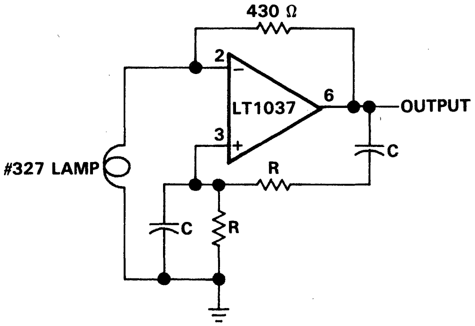
Three regions can be identified as a function of source resistance:

(i)	$R_S \le 400\ \Omega$	Voltage noise dominates in region (i)
(ii)	$R_S = 400\ \Omega$ to $50\ k\Omega$ at 1 kHz $R_S = 400\ \Omega$ to $8\ k\Omega$ at 10 Hz	Resistor noise dominates in region (ii)
(iii)	$R_S > 50\ k\Omega$ at 1 kHz $R_S > 8\ k\Omega$ at 10 Hz	Current noise dominates in region (iii)

The LT1007 and LT1037 should not be used in region (iii) where total system noise is at least six times higher than the noise voltage of the operational amplifier (i.e., the low-voltage noise specification is completely wasted).

TYPICAL APPLICATIONS

The sine wave generator application shown below, utilizes the low-noise and low-distortion characteristics of the LT1037.



$f = \frac{1}{2\pi RC}$
R = 1591.5Ω ±0.1%
C = 0.1 μF ±0.1%

TOTAL HARMONIC DISTORTION ≤ 0.0025%
NOISE ≤ 0.001%
AMPLITUDE = ±8 V
OUTPUT FREQUENCY = 1.000 kHz FOR VALUES GIVEN ± 0.4%

Figure 41. Ultra-Pure 1-kHz Sine-Wave Generator

EQUIVALENT INPUT NOISE VOLTAGE OVER A 10-SECOND PERIOD

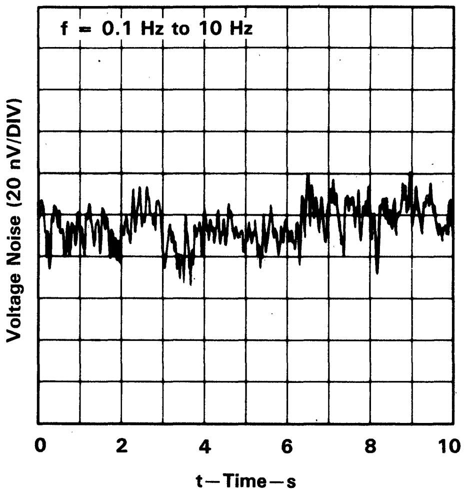
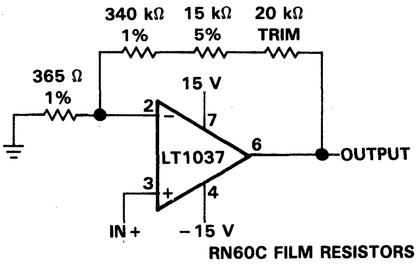


Figure 42



The high gain and wide bandwidth of the LT1037 and (LT1007) is useful in low-frequency high-closed-loop-gain amplifier applications. A typical precision Op Amp may have an open loop gain of one million with 500 kHz bandwidth. As the gain error plot shows, this device is capable of 0.1% amplifying accuracy up to 0.3 Hz only. Even instrumentation range signals can vary at a faster rate. The LT1037's "gain precision—bandwidth product" is 200 times higher, as shown.

Figure 43. Gain 1000 Amplifier With 0.01% Accuracy, DC to 5 Hz

TYPICAL APPLICATIONS

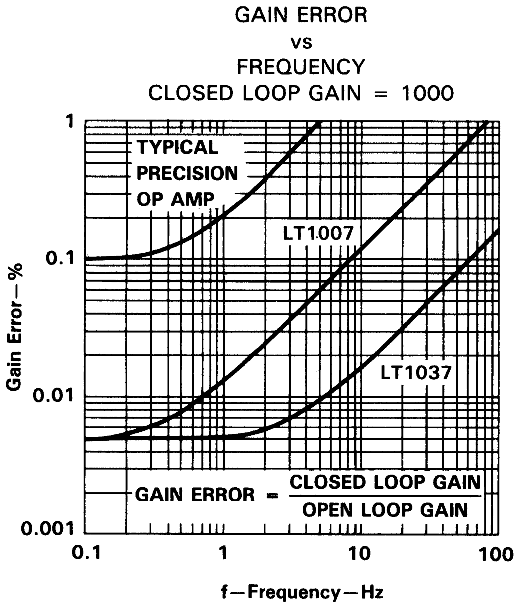
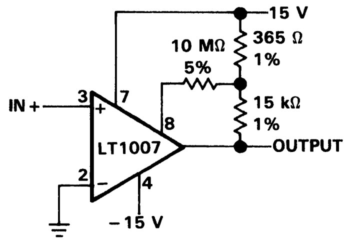


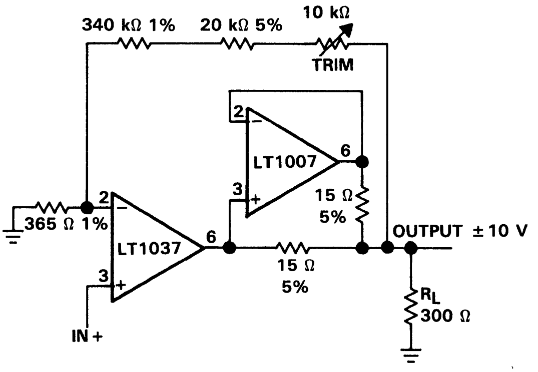
Figure 44



Positive feedback to one of the nulling terminals creates approximately 5 μV of hysteresis. Output can sink 16 mA.

Input offset voltage is typically changed less than 5 μV due to the feedback.

Figure 45. Microvolt Comparator With Hysteresis



The addition of the LT1007 doubles the amplifier's output drive to ±33 mA. Gain accuracy is 0.02%, slightly degraded compared to above because of self heating of the LT1037 under load.

Figure 46. Precision Amplifier Drives 300-Ω Load to ± 10 V

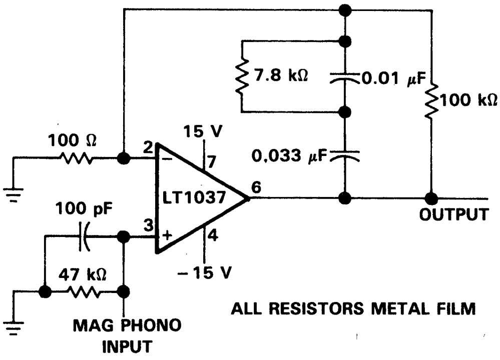
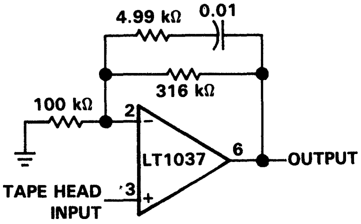


Figure 47. Phono Preamplifier

TYPICAL APPLICATIONS



ALL RESISTORS METAL FILM

Figure 48. Tape Head Amplifier

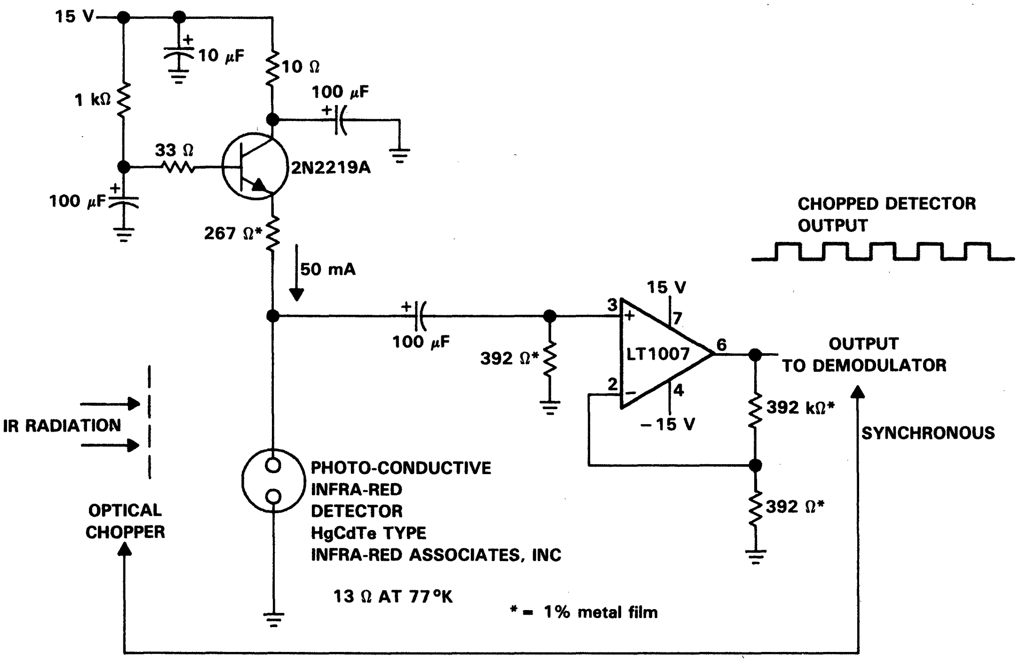
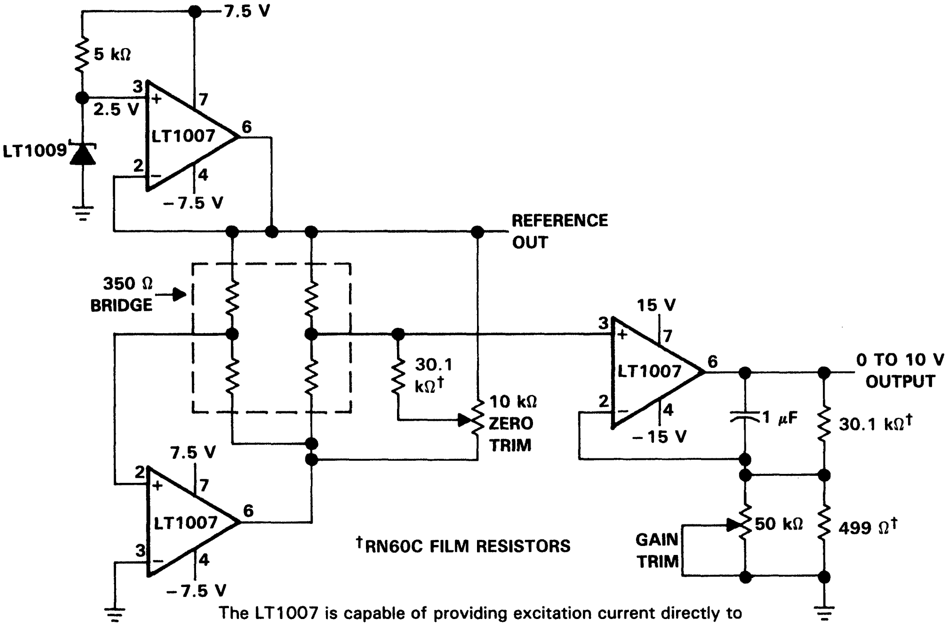


Figure 49. Infra-Red Detector Preamplifier

TYPICAL APPLICATIONS



The LT1007 is capable of providing excitation current directly to bias the 350-Ω bridge at 5 V. With only 5 V across the bridge (as opposed to the usual 10 V) total power dissipation and bridge warm-up drift is reduced. The bridge output signal is halved, but the LT1007 can amplify the reduced signal accurately.

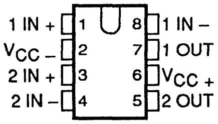
Figure 50. Strain Gauge Signal Conditioner With Bridge Excitation

LT1013, LT1013A, LT1013D, LT1013Y
DUAL PRECISION OPERATIONAL AMPLIFIERS

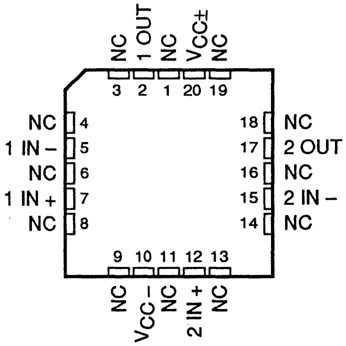
D3237, MAY 1988 – REVISED AUGUST 1991

- **Single-Supply Operation:**
  Input Voltage Range Extends to Ground
  Output Swings to Ground While Sinking Current
- **Input Offset Voltage . . . 150 μV Max at 25°C for LT1013A**
- **Offset Voltage Temperature Coefficient 2.5 μV/°C Max for LT1013A**
- **Input Offset Current . . . 0.8 nA Max at 25°C for LT1013A**
- **High Gain . . . 1.5 V/μV Min (R_L = 2 kΩ), 0.8 V/μV Min (R_L = 600 kΩ) for LT1013A**
- **Low Supply Current . . . 0.5 mA Max at T_A = 25°C for LT1013A**
- **Low Peak-to-Peak Noise Voltage 0.55 μV Typ**
- **Low Current Noise . . . 0.07 pA/√Hz Typ**

D PACKAGE
(TOP VIEW)

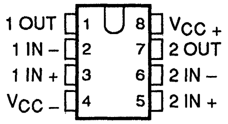


FK PACKAGE
(TOP VIEW)



NC – No internal connection

JG OR P PACKAGE
(TOP VIEW)



description

The LT1013 is a dual precision operational amplifier featuring low offset voltage temperature coefficient, high gain, low supply current, and low noise.

The LT1013 can be operated from a single 5-V power supply; the common-mode input voltage range includes ground, and the output can also swing to within a few millivolts of ground. Crossover distortion is eliminated. The LT1013 can be operated with both dual ±15-V and single 5-V supplies.

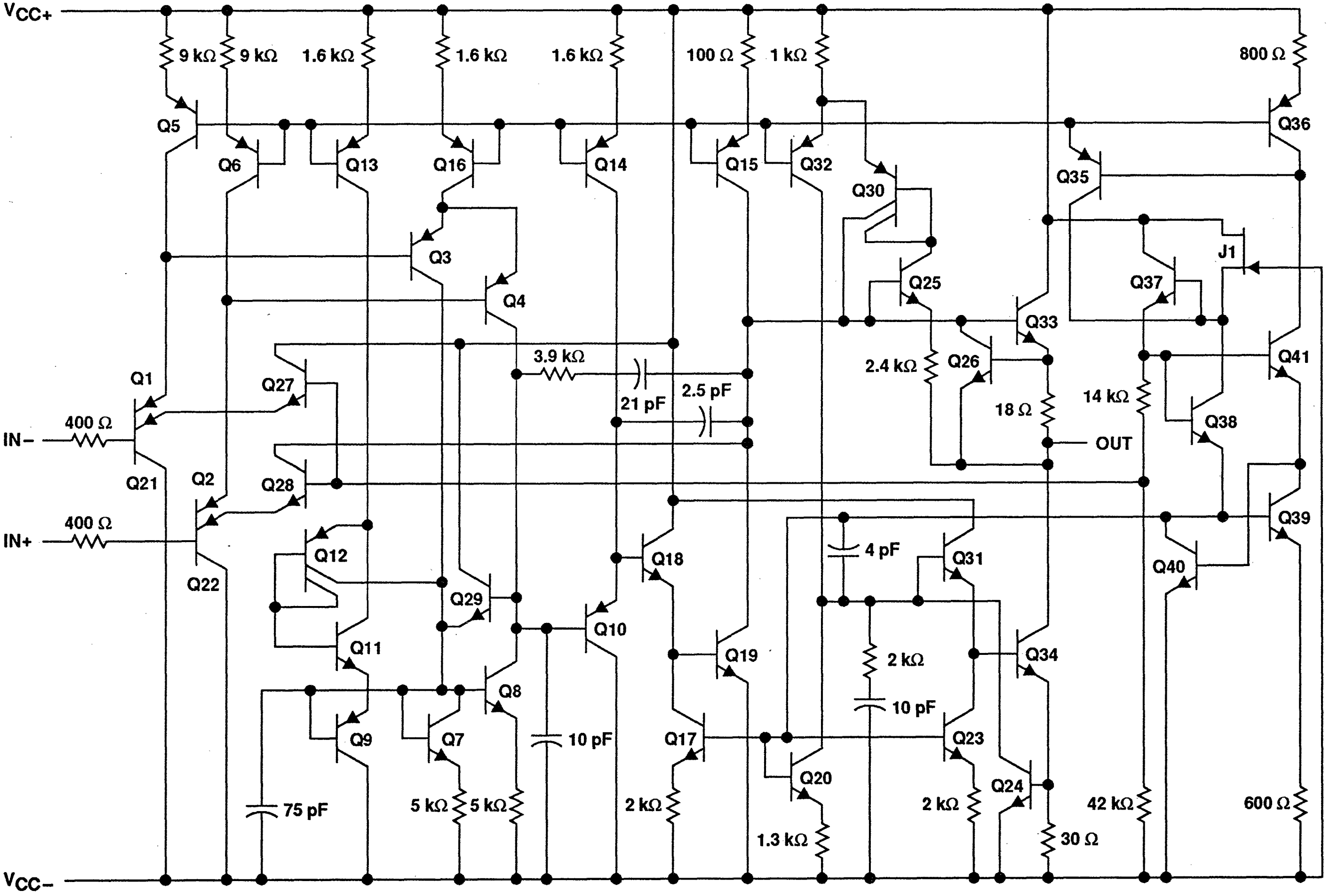
The LT1013C and LT1013AC, and LT1013D are characterized for operation from 0°C to 70°C. The LT1013I and LT1013AI, and LT1013DI are characterized for operation from −40°C to 105°C. The LT1013M and LT1013AM, and LT1013DM are characterized for operation over the full military temperature range of –55°C to 125°C.

AVAILABLE OPTIONS

T_A	V_{IO} max AT 25°C	PACKAGE				CHIP FORM (Y)
		SMALL OUTLINE (D)	CHIPCARRIER (FK)	CERAMIC DIP (JG)	PLASTIC DIP (P)	
0°C to 70°C	150 μV	–	–	–	LT1013ACP	LT1013Y
	300 μV	–	–	–	LT1013CP	
	800 μV	LT1013DD	–	–	LT1013DP	
–40°C to 105°C	150 μV	–	–	–	LT1013AIP	
	300 μV	–	–	–	LT1013IP	
	800 μV	LT1013DID	–	–	LT1013DIP	
–55°C to 125°C	150 μV	–	LT1013AMFK	–	LT1013AMP	
	300 μV	–	LT1013MFK	LT1013MJG	LT1013MP	
	800 μV	LT1013DMD	–	LT1013DMJG	LT1013DMP	

The D package is available taped and reeled. Add the suffix R to the device type (e.g., LT1013DDR).

schematic (each amplifier)

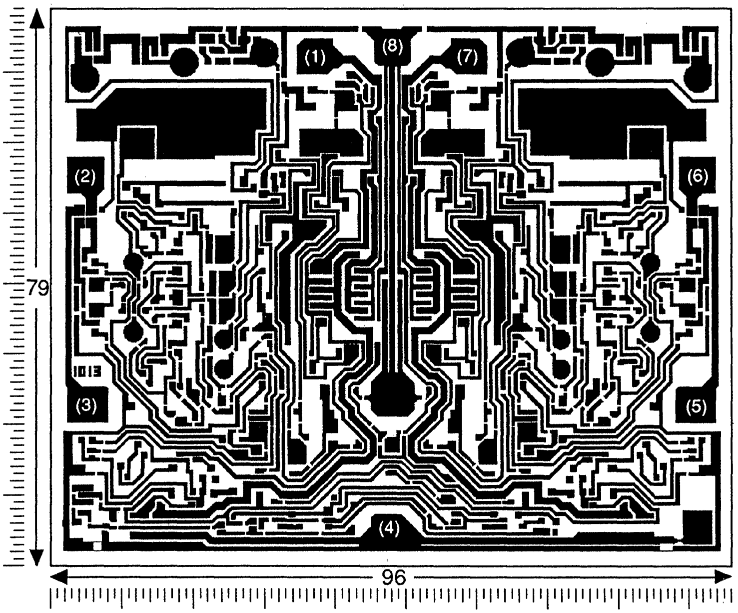


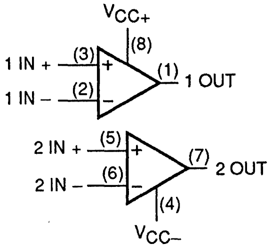
Component values are nominal.

LT1013Y chip information

These chips, properly assembled, display characteristics similar to the LT1013 (see electrical table). Thermal compression or ultrasonic bonding may be used on the doped aluminum bonding pads. Chips may be mounted with conductive epoxy or a gold-silicon preform.

BONDING PAD ASSIGNMENTS





CHIP THICKNESS:
15 TYPICAL

BONDING PADS:
4 X 4 MINIMUM

T_J max = 150°C

TOLERANCES
ARE ± 10%

ALL DIMENSIONS
ARE IN MILS

PIN (4) INTERNALLY
CONNECTED TO
BACKSIDE OF CHIP

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC+} (see Note 1)	22 V
Supply voltage, V_{CC-} (see Note 1)	−22 V
Differential input voltage (see Note 2)	±30 V
Input voltage range, V_I (any input, see Note 1)	V_{CC-} − 5 V to V_{CC+}
Duration of short-circuit current at (or below) 25°C (see Note 3)	unlimited
Operating free-air temperature range, T_A: LT1013C, LT1013AC, LT1013D	−0°C to 70°C
LT1013I, LT1013AI, LT1013DI	−40°C to 105°C
LT1013M, LT1013AM, LT1013DM	−55°C to 125°C
Storage temperature range	−65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D or P package	260°C
Case temperature for 60 seconds: FK package	260°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: JG package	300°C

NOTES: 1. All voltage values, except differential voltages, are with respect to the midpoint between V_{CC+} and V_{CC-}.
2. Differential voltages are at the noninverting input with respect to the inverting input.
3. The output may be shorted to either supply.

electrical characteristics at specified free-air temperature, $V_{CC\pm} = \pm 15$ V, $V_{IC} = 0$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A†	LT1013C			LT1013AC			LT1013DC			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IO}	Input offset voltage	R_S = 50 Ω	25°C		60	300		40	150		200	800	μV
			Full range			400			240			1000	
α_{VIO}	Temperature coefficient of input offset voltage		Full range		0.4	2.5		0.3	2		0.7	5	μV/°C
	Long-term drift of input offset voltage		25°C		0.5			0.4			0.5		μV/mo
I_{IO}	Input offset current		25°C		0.2	1.5		0.15	0.8		0.2	1.5	nA
			Full range			2.8			1.5			2.8	
I_{IB}	Input bias current		25°C		−15	−30		−12	−20		−15	−30	nA
			Full range			−38			−25			−38	
V_{ICR}	Common-mode input voltage range		25°C	−15 to 13.5	−15.3 to 13.8		−15 to 13.5	−15.3 to 13.8		−15 to 13.5	−15.3 to 13.8		V
			Full range	−15 to 13			−15 to 13			−15 to 13			
V_{OM}	Maximum peak output voltage swing	R_L = 2 kΩ	25°C	±12.5	±14		±13	±14		±12.5	±14		V
			Full range	±12			±12.5			±12			
A_{VD}	Large-signal differential voltage amplification	V_O = ±10 V, R_L = 600 Ω	25°C	0.5	0.2		0.8	2.5		0.5	2		V/μV
		V_O = ±10 V, R_L = 2 kΩ	25°C	1.2	7		1.5	8		1.2	7		
			Full range	0.7			1			0.7			
CMRR	Common-mode rejection ratio	V_{IC} = −15 V to 13.5 V	25°C	97	114		100	117		97	114		dB
		V_{IC} = −14.9 V to 13 V	Full range	94			98			94			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC} / \Delta V_{IO}$)	$V_{CC\pm}$ = ±2 V to ±18 V	25°C	100	117		103	120		100	117		dB
			Full range	97			101			97			
	Channel separation	V_O = ±10 V, R_L = 2 kΩ	25°C	120	137		123	140		120	137		dB
r_{id}	Differential input resistance		25°C	70	300		100	400		70	300		MΩ
r_{ic}	Common-mode input resistance		25°C		4			5			4		GΩ
I_{CC}	Supply current per amplifier		25°C		0.35	0.55		0.35	0.5		0.35	0.55	mA
			Full range			0.7			0.55			0.6	

† Full range is 0°C to 70°C.

‡ All typical values are at T_A = 25°C.

electrical characteristics at specified free-air temperature, V_{CC+} = 5 V, V_{CC-} = 0, V_O = 1.4 V, V_{IC} = 0 (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A†	LT1013C			LT1013AC			LT1013DC			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	R_S = 50 Ω	25°C		90	450		60	250		250	950	µV
			Full range			570			350			1200	
I_{IO}	Input offset current		25°C		0.3	2		0.2	1.3		0.3	2	nA
			Full range			6			3.5			6	
I_{IB}	Input bias current		25°C		–18	– 50		– 15	– 35		– 18	– 50	nA
			Full range			– 90			– 55			– 90	
V_{ICR}	Common-mode input voltage range		25°C	0 to 3.5	–0.3 to 3.83.8		0 to 3.5	– 0.3 to 3.8		0 3.5	0.3 to 3.8		V
			Full range	0 to 3			0 to 3			0 to 3			
V_{OM}	Maximum peak output voltage swing	Output low, No load	25°C		15	25		15	25		15	25	mV
		Output low, R_L = 600 Ω to GND	25°C		5	10		5	10		5	10	
			Full range			13			13			13	
		Output low, I_{sink} = 1 mA	25°C		220	350		220	350		220	350	
		Output high, No load	25°C	4	4.4		4	4.4		4	4.4		V
		Output high, R_L = 600 Ω to GND	25°C	3.4	4		3.4	4		3.4	4		
			Full range	3.2			3.3			3.2			
A_{VD}	Large-signal differential voltage amplification	V_O = 5 mV to 4 V, R_L = 500 Ω	25°C		1			1			1		V/µV
I_{CC}	Supply current per amplifier		25°C		0.32	0.5		0.31	0.45		0.32	0.5	mA
			Full range			0.55			0.5			0.55	

†Full range is –0°C to 70°C.

operating characteristics, $V_{CC\pm}$ = ±15 V, V_{IC} = 0, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SR	Slew rate		0.2	0.4		V/µs
V_n	Equivalent input noise voltage	f = 10 Hz		24		nV/√Hz
		f = 1 kHz		22		
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 10 Hz		0.55		µV
I_n	Equivalent input noise current	f = 10 Hz		0.07		pA/√Hz

electrical characteristics at specified free-air temperature, $V_{CC\pm}$ = ±15 V, V_{IC} = 0 (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A†	LT1013I			LT1013AI			LT1013DI			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IO}	Input offset voltage	R_S = 50 Ω	25°C		60	300		40	150		200	800	µV
			Full range			550			300			1000	
α_{VIO}	Temperature coefficient of input offset voltage		Full range		0.4	2.5		0.3	2		0.7	5	µV/°C
	Long-term drift of input offset voltage		25°C		0.5			0.4			0.5		µV/mo
I_{IO}	Input offset current		25°C		0.2	1.5		0.15	0.8		0.2	1.5	nA
			Full range			2.8			1.5			2.8	
I_{IB}	Input bias current		25°C		−15	−30		−12	−20		−15	−30	nA
			Full range			−38			−25			−38	
V_{ICR}	Common-mode input voltage range		25°C	−15 to 13.5	−15.3 to 13.8		−15 to 13.5	−15.3 to 13.8		−15 to 13.5	−15.3 to 13.8		V
			Full range	−15 to 13			−15 to 13			−15 to 13			
V_{OM}	Maximum peak output voltage swing	R_L = 2 kΩ	25°C	±12.5	±14		±13	±14		±12.5	±14		V
			Full range	±12			±12.5			±12			
A_{VD}	Large-signal differential voltage amplification	V_O = ±10 V, R_L = 600 Ω	25°C	0.5	0.2		0.8	2.5		0.5	2		V/µV
		V_O = ±10 V, R_L = 2 kΩ	25°C	1.2	7		1.5	8		1.2	7		
			Full range	0.7			1			0.7			
CMRR	Common-mode rejection ratio	V_{IC} = −15 V to 13.5 V	25°C	97	114		100	117		97	114		dB
		V_{IC} = −14.9 V to 13 V	Full range	94			97			94			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC} / \Delta V_{IO}$)	$V_{CC\pm}$ = ±2 V to ±18 V	25°C	100	117		103	120		100	117		dB
			Full range	97			101			97			
	Channel separation	V_O = ±10 V, R_L = 2 kΩ	25°C	120	137		123	140		120	137		dB
r_{id}	Differential input resistance		25°C	70	300		100	400		70	300		MΩ
r_{ic}	Common-mode input resistance		25°C		4			5			4		GΩ
I_{CC}	Supply current per amplifier		25°C		0.35	0.55		0.35	0.5		0.35	0.55	mA
			Full range			0.7			0.55			0.6	

† Full range is – 40°C to 105°C.
‡ All typical values are at T_A = 25°C.

electrical characteristics at specified free-air temperature, V_{CC+} = 5 V, V_{CC-} = 0, V_O = 1.4 V, V_{IC} = 0 (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A†	LT1013I			LT1013AI			LT1013DI			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	R_S = 50 Ω	25°C		90	450		60	250		250	950	µV
			Full range			570			350			1200	
I_{IO}	Input offset current		25°C		0.3	2		0.2	1.3		0.3	2	nA
			Full range			6			3.5			6	
I_{IB}	Input bias current		25°C		–18	– 50		– 15	– 35		– 18	– 50	nA
			Full range			– 90			– 55			– 90	
V_{ICR}	Common-mode input voltage range		25°C	0 to 3.5	–0.3 to 3.8		0 to 3.5	– 0.3 to 3.8		0 3.5	0.3 to 3.8		V
			Full range	0 to 3			0 to 3			0 to 3			
V_{OM}	Maximum peak output voltage swing	Output low, No load	25°C		15	25		15	25		15	25	mV
		Output low, R_L = 600 Ω to GND	25°C		5	10		5	10		5	10	
			Full range			13			13			13	
		Output low, I_{sink} = 1 mA	25°C		220	350		220	350		220	350	
		Output high, No load	25°C	4	4.4		4	4.4		4	4.4		V
		Output high, R_L = 600 Ω to GND	25°C	3.4	4		3.4	4		3.4	4		
			Full range	3.2			3.3			3.2			
A_{VD}	Large-signal differential voltage amplification	V_O = 5 mV to 4 V, R_L = 500 Ω	25°C		1			1			1		V/µV
I_{CC}	Supply current per amplifier		25°C		0.32	0.5		0.31	0.45		0.32	0.5	mA
			Full range			0.55			0.5			0.55	

†Full range is –40°C to 105°C.

operating characteristics, $V_{CC\pm}$ = ±15 V, V_{IC} = 0, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SR	Slew rate		0.2	0.4		V/µs
V_n	Equivalent input noise voltage	f = 10 Hz		24		nV/√Hz
		f = 1 kHz		22		
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 10 Hz		0.55		µV
I_n	Equivalent input noise current	f = 10 Hz		0.07		pA/√Hz

electrical characteristics at specified free-air temperature, $V_{CC\pm} = \pm 15$ V, $V_{IC} = 0$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A†	LT1013M			LT1013AM			LT1013DM			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IO}	Input offset voltage	R_S = 50 Ω	25°C		60	300		40	150		200	800	µV
			Full range			550			300			1000	
α_{VIO}	Temperature coefficient of input offset voltage		Full range		0.5	2.5*		0.4	2*		0.5	2.5*	µV/°C
	Long-term drift of input offset voltage		25°C		0.5			0.4			0.5		µV/mo
I_{IO}	Input offset current		25°C		0.2	1.5		0.15	0.8		0.2	1.5	nA
			Full range			5			2.5			5	
I_{IB}	Input bias current		25°C		−15	−30		−12	−20		−15	−30	nA
			Full range			−45			−30			−45	
V_{ICR}	Common-mode input voltage range		25°C	−15 to 13.5	−15.3 to 13.8		−15 to 13.5	−15.3 to 13.8		−15 to 13.5	−15.3 to 13.8		V
			Full range	−14.9 to 13			−14.9 to 13			−14.9 to 13			
V_{OM}	Maximum peak output voltage swing	R_L = 2 kΩ	25°C	±12.5	±14		±13	±14		±12.5	±14		V
			Full range	±11.5			±12			±11.5			
A_{VD}	Large-signal differential voltage amplification	V_O = ±10 V, R_L = 600 Ω	25°C	0.5	2		0.8	2.5		0.5	2		V/µV
		V_O = ±10 V, R_L = 2 kΩ	25°C	1.2	7		1.5	8		1.2	7		
			Full range	0.25			0.5			0.25			
CMRR	Common-mode rejection ratio	V_{IC} = −15 V to 13.5 V	25°C	97	117		100	117		97	114		dB
		V_{IC} = −14.9 V to 13 V	Full range	94			97			94			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC} / \Delta V_{IO}$)	$V_{CC\pm}$ = ±2 V to ±18 V	25°C	100	117		103	120		100	117		dB
			Full range	97			100			97			
	Channel separation	V_O = ±10 V, R_L = 2 kΩ	25°C	120	137		123	140		120	137		dB
r_{id}	Differential input resistance		25°C	70	300		100	400		70	300		MΩ
r_{ic}	Common-mode input resistance		25°C		4			5			4		GΩ
I_{CC}	Supply current per amplifier		25°C		0.35	0.55		0.35	0.5		0.35	0.55	mA
			Full range			0.7			0.6			0.7	

*On products compliant to MIL-STD-883, Class B, this parameter is not production tested.

†Full range is −55°C to 125°C.

‡All typical values are at T_A = 25°C.

electrical characteristics at specified free-air temperature, V_{CC+} = 5 V, V_{CC-} = 0, V_O = 1.4 V, V_{IC} = 0 (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A†	LT1013M			LT1013AM			LT1013DM			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	R_S = 50 Ω	25°C		90	450		60	250		250	950	µV
			Full range		400	1500		250	900		800	2000	
		R_S = 50 Ω, V_{IC} = 0.1 V	125°C		200	750		120	450		560	1200	
I_{IO}	Input offset current		25°C		0.3	2		0.2	1.3		0.3	2	
			Full range			10			6			10	nA
I_{IB}	Input bias current		25°C		−18	−50		−15	−35		−18	−50	
			Full range			−120			−80			−120	nA
V_{ICR}	Common-mode input voltage range		25°C	0 to 3.5	−0.3 to 3.8		0 to 3.5	−0.3 to 3.8		0 to 3.5	−0.3 to 3.8		V
			Full range	0 to 3			0 to 3			0 to 3			
V_{OM}	Maximum peak output voltage swing	Output low, No load	25°C		15	25		15	25		15	25	mV
		Output low, R_L = 600 Ω to GND	25°C		5	10		5	10		5	10	
			Full range			18			15			18	
		Output low, I_{sink} = 1 mA	25°C		220	350		220	350		220	350	
		Output high, No load	25°C	4	4.4		4	4.4		4	4.4		V/µV
		Output high, R_L = 600 Ω to GND	25°C	3.4	4		3.4	4		3.4	4		
			Full range	3.1			3.2			3.1			
A_{VD}	Large-signal differential voltage amplification	V_O = 5 mV to 4 V, R_L = 500 Ω	25°C		1			1			1		mA
I_{CC}	Supply current per amplifier		25°C		0.32	0.5		0.31	0.45		0.32	0.5	
			Full range			0.65			0.55			0.65	

†Full range is −55°C to 125°C.

operating characteristics, $V_{CC\pm}$ = ±15 V, V_{IC} = 0, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SR	Slew rate		0.2	0.4		V/µs
V_n	Equivalent input noise voltage	f = 10 Hz		24		nV/√Hz
		f = 1 kHz		22		
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 10 Hz		0.55		µV
I_n	Equivalent input noise current	f = 10 Hz		0.07		pA/√Hz

electrical characteristics at $V_{CC+} = 5$ V, $V_{CC-} = 0$, $V_O = 1.4$ V, $V_{IC} = 0$, $T_A = 25°C$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	$R_S = 50\ \Omega$		250	950	µV
I_{IO}	Input offset current			0.3	2	nA
I_{IB}	Input bias current			−18	−50	nA
V_{ICR}	Common-mode input voltage range		0 to 3.5	0.3 to 3.8		V
V_{OM}	Maximum peak output voltage swing	Output low, No load		15	25	mV
		Output low, $R_L = 600\ \Omega$ to GND		5	10	
		Output low, $I_{sink} = 1$ mA		220	350	
		Output high, No load	4	4.4		V
		Output high, $R_L = 600\ \Omega$ to GND	3.4	4		
A_{VD}	Large-signal differential voltage amplification	$V_O = 5$ mV to 4 V, $R_L = 500\ \Omega$		1		V/µV
I_{CC}	Supply current per amplifier			0.32	0.5	mA

electrical characteristics at $V_{CC\pm} = \pm 15$ V, $V_{IC} = 0$, $T_A = 25°C$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	$R_S = 50\ \Omega$		200	800	µV
	Long-term drift of input offset voltage			0.5		µV/mo
I_{IO}	Input offset current			0.2	1.5	nA
I_{IB}	Input bias current			−15	−30	nA
V_{ICR}	Common-mode input voltage range		−15 to 13.5	−15.3 to 13.8		V
V_{OM}	Maximum peak output voltage swing	$R_L = 2\ k\Omega$	±12.5	±14		V
A_{VD}	Large-signal differential voltage amplification	$V_O = \pm 10$ V, $R_L = 600\ \Omega$	0.5	2		V/µV
		$V_O = \pm 10$ V, $R_L = 2\ \Omega$	1.2	7		dB
CMRR	Common-mode rejection ratio	$V_{IC} = -15$ V to 13.5 V	97	114		
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC}/\Delta V_{IO}$)	$V_{CC\pm} = \pm 2$ V to ±18 V	100	117		dB
	Channel separation	$V_O = \pm 10$ V, $R_L = 2\ \Omega$	120	137		dB
r_{id}	Differential input resistance		70	300		MΩ
r_{ic}	Common-mode input resistance			4		GΩ
I_{CC}	Supply current per amplifier			0.35	0.55	mA

operating characteristics, $V_{CC\pm} = \pm 15$ V, $V_{IC} = 0$, $T_A = 25°C$

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SR	Slew rate		0.2	0.4		V/µs
V_n	Equivalent input noise voltage	f = 10 Hz		24		nV/√Hz
		f = 1 kHz		22		
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 10 Hz		0.55		µV
I_n	Equivalent input noise current	f = 10 Hz		0.07		pA/√Hz

TYPICAL CHARACTERISTICS†

table of graphs

			FIGURE
V_{IO}	Input offset voltage	vs Source resistance vs Temperature	1 2
ΔV_{IO}	Change in input offset voltage	vs Time	3
I_{IO}	Input offset current	vs Temperature	4
I_{IB}	Input bias current	vs Temperature	5
V_{IC}	Common-mode input voltage	vs Input bias current	6
A_{VD}	Differential voltage amplification	vs Load resistance vs Frequency	7, 8 9, 10
	Channel separation	vs Frequency	11
	Output saturation voltage	vs Temperature	12
CMRR	Common-mode rejection ratio	vs Frequency	13
k_{SVR}	Supply voltage rejection ratio	vs Frequency	14
I_{CC}	Supply current	vs Temperature	15
I_{OS}	Short-circuit output current	vs Time	16
V_n	Equivalent input noise voltage	vs Frequency	17
I_n	Equivalent input noise current	vs Frequency	17
$V_{N(PP)}$	Peak-to-peak input noise voltage	vs Time	18
	Pulse response	Small-signal Large-signal	19, 21 20, 22, 23
	Phase shift	vs Frequency	9

TYPICAL CHARACTERISTICS†

INPUT OFFSET VOLTAGE
vs
BALANCED SOURCE RESISTANCE

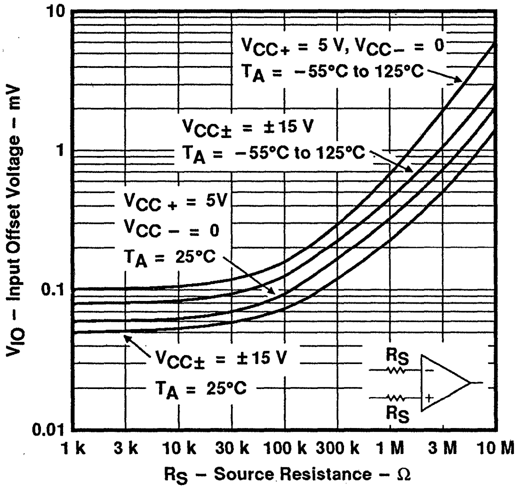


Figure 1

INPUT OFFSET VOLTAGE
OF REPRESENTATIVE UNITS
vs
FREE-AIR TEMPERATURE

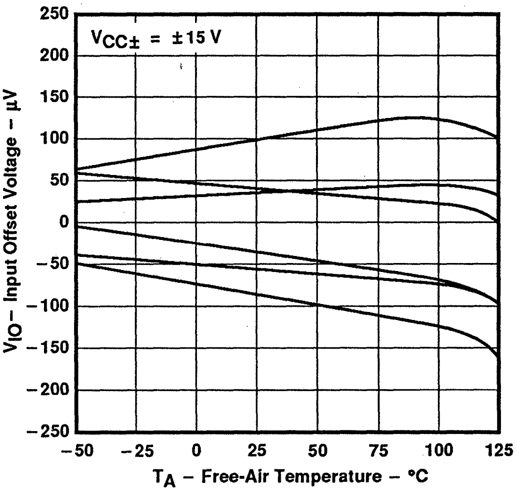


Figure 2

WARM-UP CHANGE
IN INPUT OFFSET VOLTAGE
vs
ELAPSED TIME

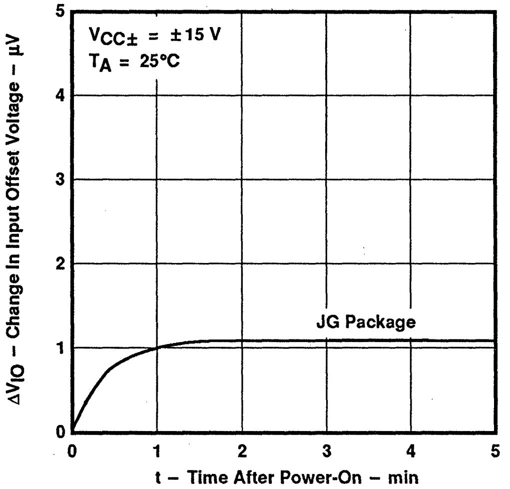


Figure 3

INPUT OFFSET CURRENT
vs
FREE-AIR TEMPERATURE

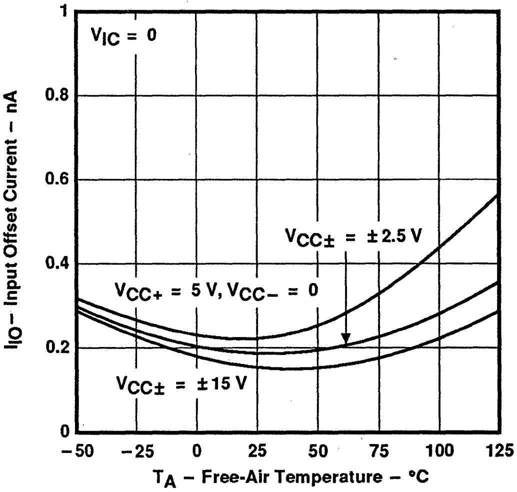


Figure 4

---

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

INPUT BIAS CURRENT
vs
FREE-AIR TEMPERATURE

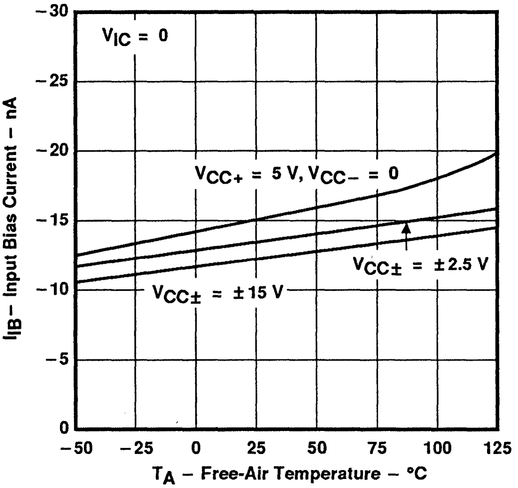


Figure 5

COMMON-MODE INPUT VOLTAGE
vs
INPUT BIAS CURRENT

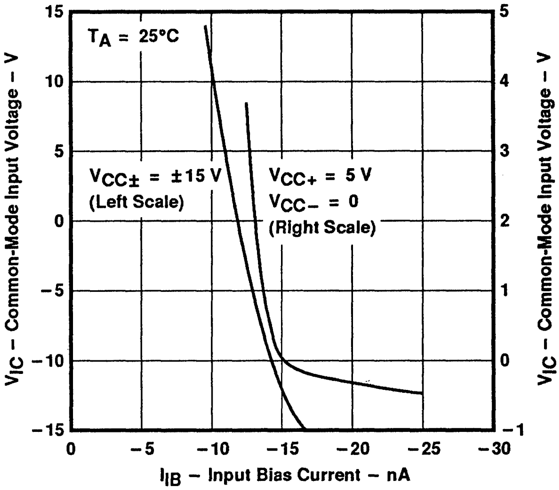


Figure 6

DIFFERENTIAL VOLTAGE AMPLIFICATION
vs
LOAD RESISTANCE

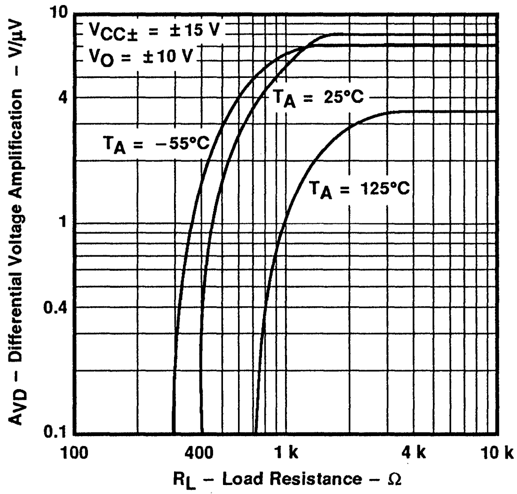


Figure 7

DIFFERENTIAL VOLTAGE AMPLIFICATION
vs
LOAD RESISTANCE

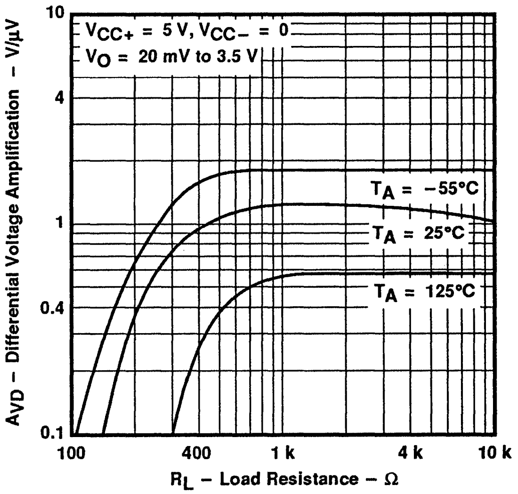


Figure 8

---

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

DIFFERENTIAL VOLTAGE AMPLIFICATION
and PHASE SHIFT
vs
FREQUENCY

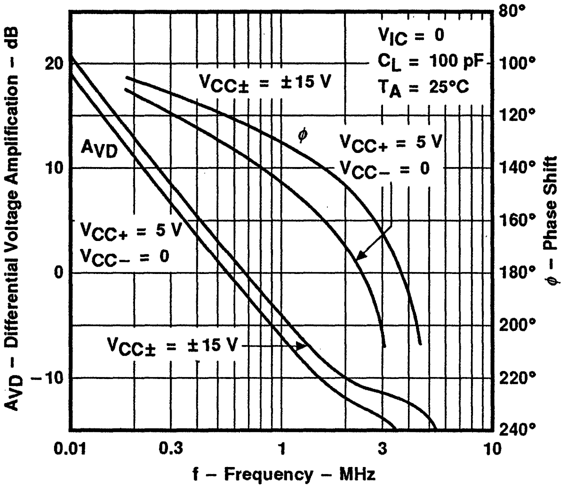


Figure 9

DIFFERENTIAL VOLTAGE AMPLIFICATION
vs
FREQUENCY

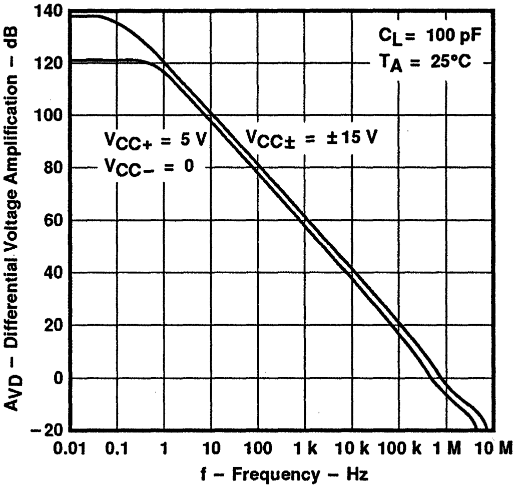


Figure 10

CHANNEL SEPARATION
vs
FREQUENCY

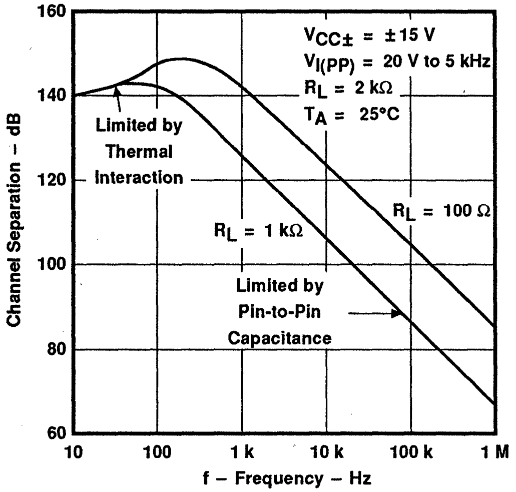


Figure11

OUTPUT SATURATION VOLTAGE
vs
FREE-AIR TEMPERATURE

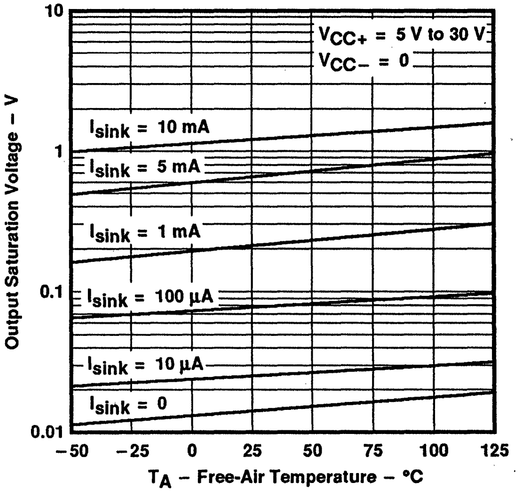


Figure 12

---

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

COMMON-MODE REJECTION RATIO
vs
FREQUENCY

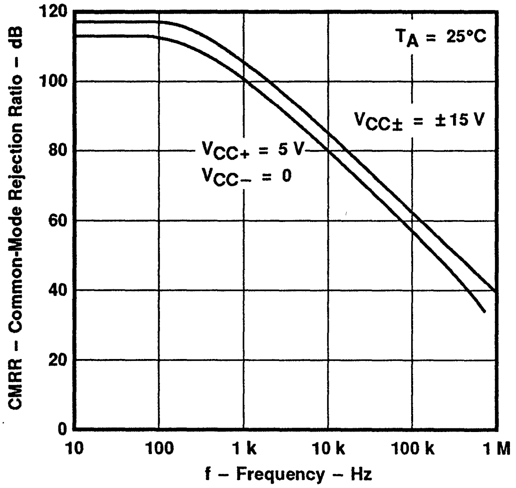


Figure 13

SUPPLY VOLTAGE REJECTION RATIO
vs
FREQUENCY

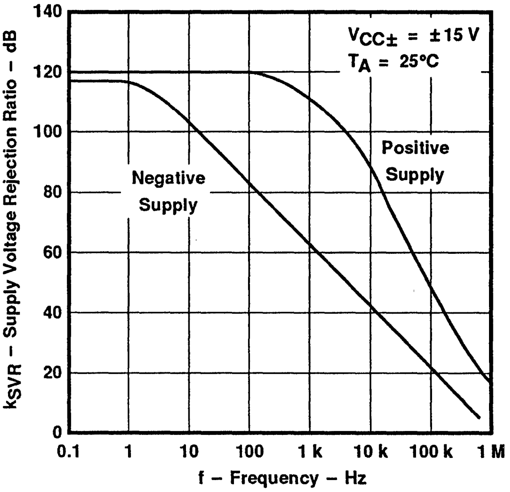


Figure 14

SUPPLY CURRENT
vs
FREE-AIR TEMPERATURE

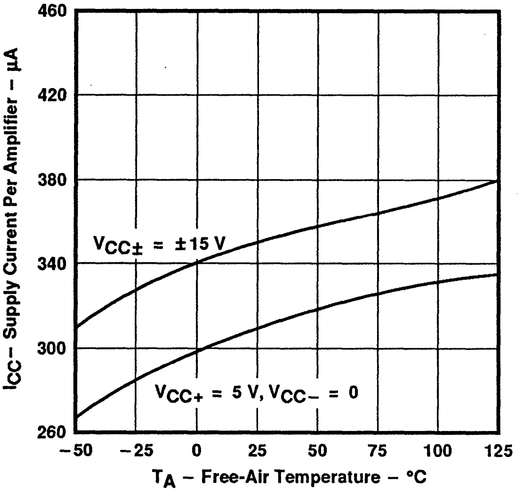


Figure 15

SHORT-CIRCUIT OUTPUT CURRENT
vs
ELAPSED TIME

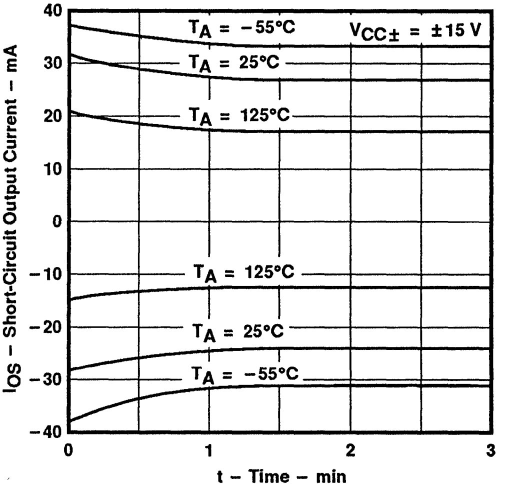


Figure 16

---

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS

EQUIVALENT INPUT NOISE VOLTAGE
and EQUIVALENT INPUT NOISE CURRENT
vs
FREQUENCY

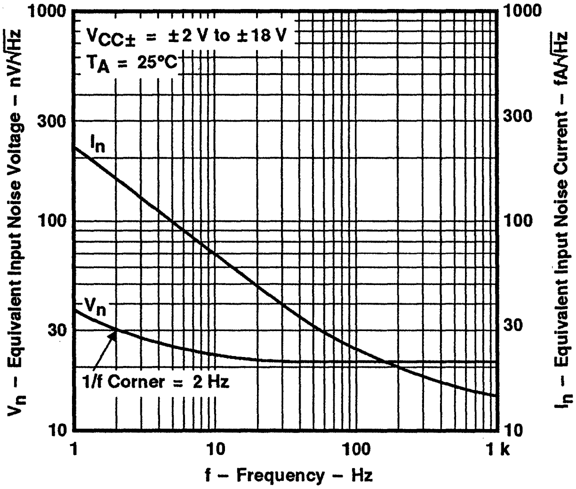


Figure 17

PEAK-TO-PEAK INPUT NOISE VOLTAGE
OVER A
10-SECOND PERIOD

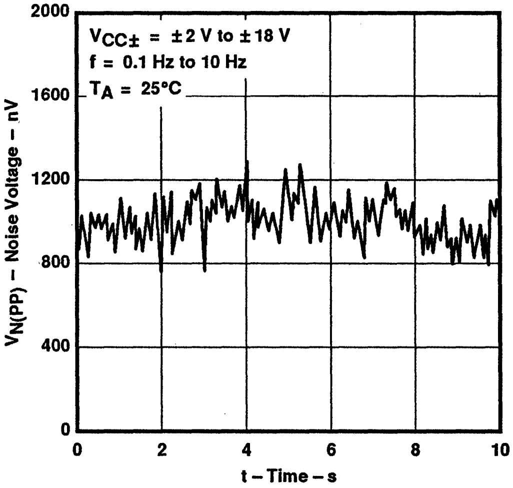


Figure 18

VOLTAGE-FOLLOWER
SMALL-SIGNAL
PULSE RESPONSE

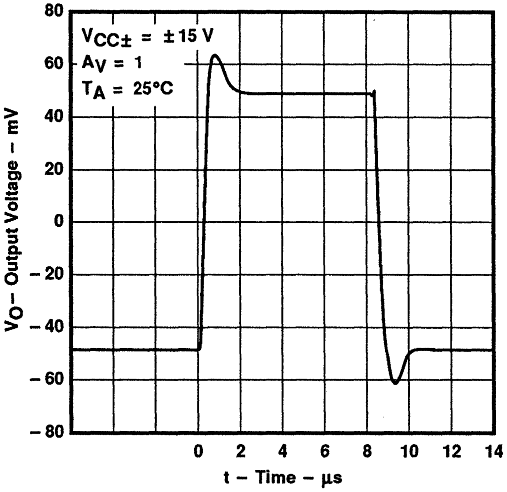


Figure 19

VOLTAGE-FOLLOWER
LARGE-SIGNAL
PULSE RESPONSE

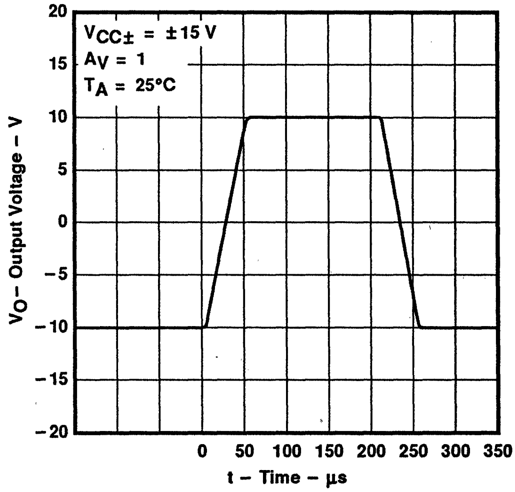


Figure 20

TYPICAL CHARACTERISTICS

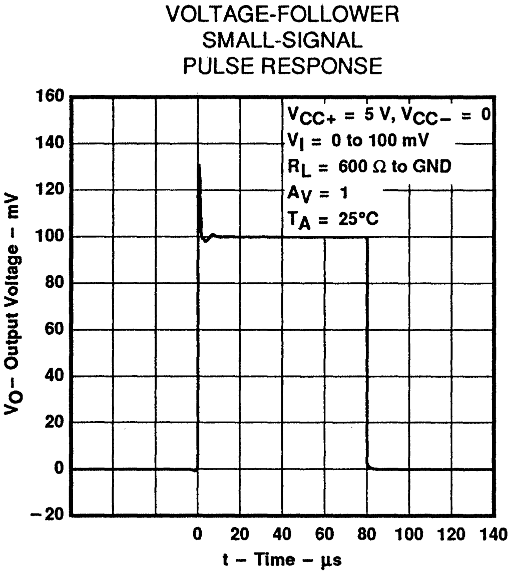


Figure 21

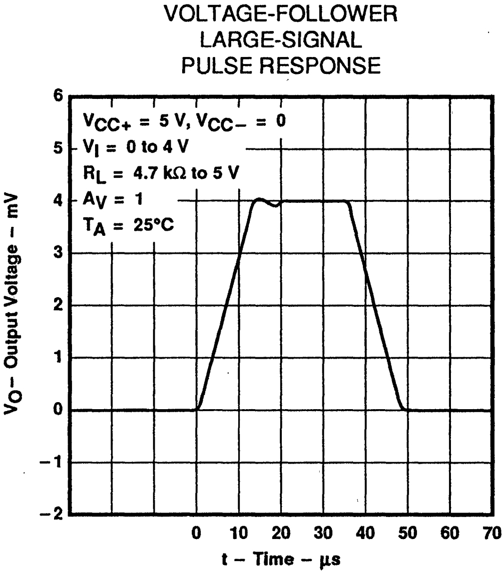


Figure 22

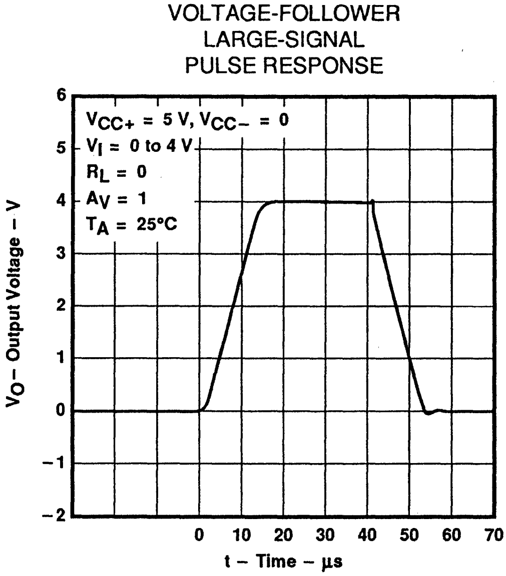


Figure 23

APPLICATION INFORMATION

single-supply operation

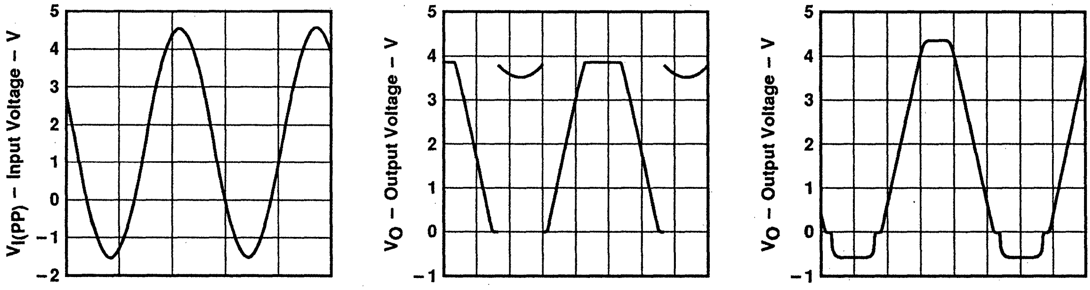
The LT1013 is fully specified for single-supply operation (V_{CC-} = 0). The common-mode input voltage range includes ground, and the output swings within a few millivolts of ground.

Furthermore, the LT1013 has specific circuitry that addresses the difficulties of single-supply operation, both at the input and at the output. At the input, the driving signal can fall below 0 V, either inadvertently or on a transient basis. If the input is more than a few hundred millivolts below ground, the LT1013 is designed to deal with the following two problems that can occur:

1. On many other op amps, when the input is more than a diode drop below ground, unlimited current will flow from the substrate (V_{CC-} terminal) to the input, which can destroy the unit. On the LT1013, the 400-Ω resistors in series with the input (see schematic) protect the device even when the input is 5 V below ground.
2. When the input is more than 400 mV below ground (at T_A = 25°C), the input stage of similar type op amps saturates and phase reversal occurs at the output. This can cause lock-up in servo systems. Because of a unique phase-reversal protection circuitry (Q21, Q22, Q27, and Q28), the LT1013 outputs do not reverse, even when the inputs are at −1.5 V (see Figure 24).

This phase-reversal protection circuitry, however, does not function when the other operational amplifier on the LT1013 is driven hard into negative saturation at the output. Phase-reversal protection does not work on amplifier 1 when 2s output is in negative saturation or on amplifier 2 when 1s output is in negative saturation.

At the output, other single-supply designs either cannot swing to within 600 mV of ground or cannot sink more than a few microamperes while swinging to ground. The all-NPN output stage of the LT1013 maintains its low output resistance and high gain characteristics until the output is saturated. In dual-supply operations, the output stage is free of crossover distortion.



(a) $V_{I(PP)}$ = −1.5 V to 4.5 V

(b) OUTPUT PHASE REVERSAL EXHIBITED BY LM358

(c) NO PHASE REVERSAL EXHIBITED BY LT1013

Figure 24. Voltage-Follower Response With Input Exceeding the Negative Common-Mode Input Voltage Range

APPLICATION INFORMATION

comparator applications

The single-supply operation of the LT1013 lends itself for use as a precision comparator with TTL-compatible output. In systems using both operational amplifiers and comparators, the LT1013 can perform multiple duties. Refer to Figures 25 and 26.

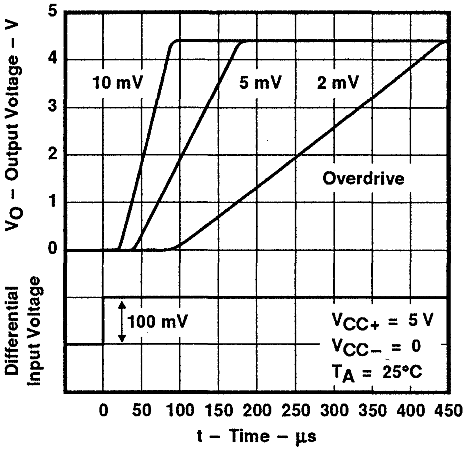


Figure 25. Low-to-High-Level Output Response for Various Input Overdrives

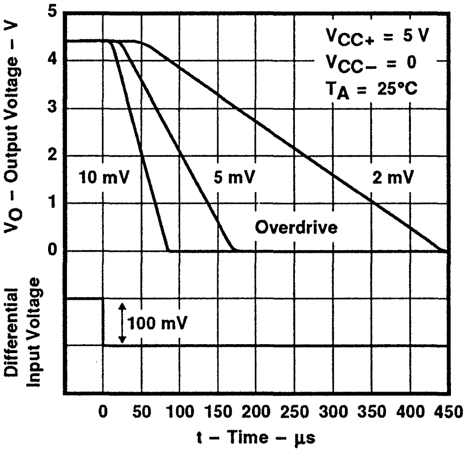


Figure 26. High-to-Low-Level Output Response for Various Input Overdrives

low-supply operation

The minimum supply voltage for proper operation of the LT1013 is 3.4 V (three Ni-Cad batteries). Typical supply current at this voltage is 290 µA; therefore, power dissipation is only 1 mW per amplifier.

offset voltage and noise testing

The test circuit for measuring input offset voltage and its temperature coefficient is shown in Figure 30. This circuit with supply voltages increased to ±20 V is also used as the burn-in configuration.

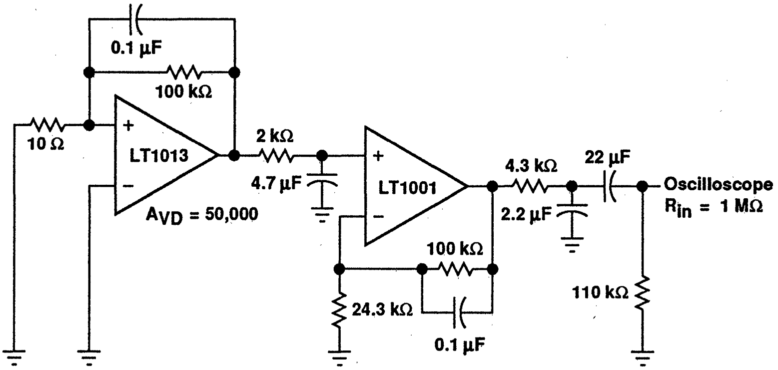
The peak-to-peak equivalent input noise voltage of the LT1013 is measured using the test circuit shown in Figure 27. The frequency response of the noise tester indicates that the 0.1-Hz corner is defined by only one zero. The test time to measure 0.1-Hz to 10-Hz noise should not exceed 10 seconds, as this time limit acts as an additional zero to eliminate noise contributions from the frequency band below 0.1 Hz.

An input noise voltage test is recommended when measuring the noise of a large number of units. A 10-Hz input noise voltage measurement correlates well with a 0.1-Hz peak-to-peak noise reading because both results are determined by the white noise and the location of the 1/f corner frequency.

Current noise is measured by the circuit and formula shown in Figure 28. The noise of the source resistors is subtracted.

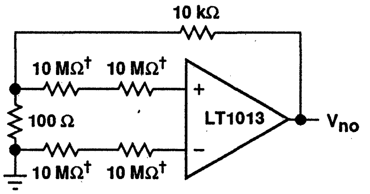
APPLICATION INFORMATION

offset voltage and noise testing (continued)



NOTE: All capacitor values are for nonpolarized capacitors only.

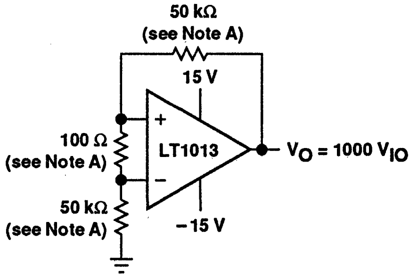
Figure 27. 0.1-Hz to 10-Hz Peak-to-Peak Noise Test Circuit



†Metal film resistor

$$I_n = \frac{[V_{no}^2 - (820\ \text{nV})^2]^{1/2}}{40\ \text{M}\Omega \times 100}$$

Figure 28. Noise Current Test Circuit and Formula

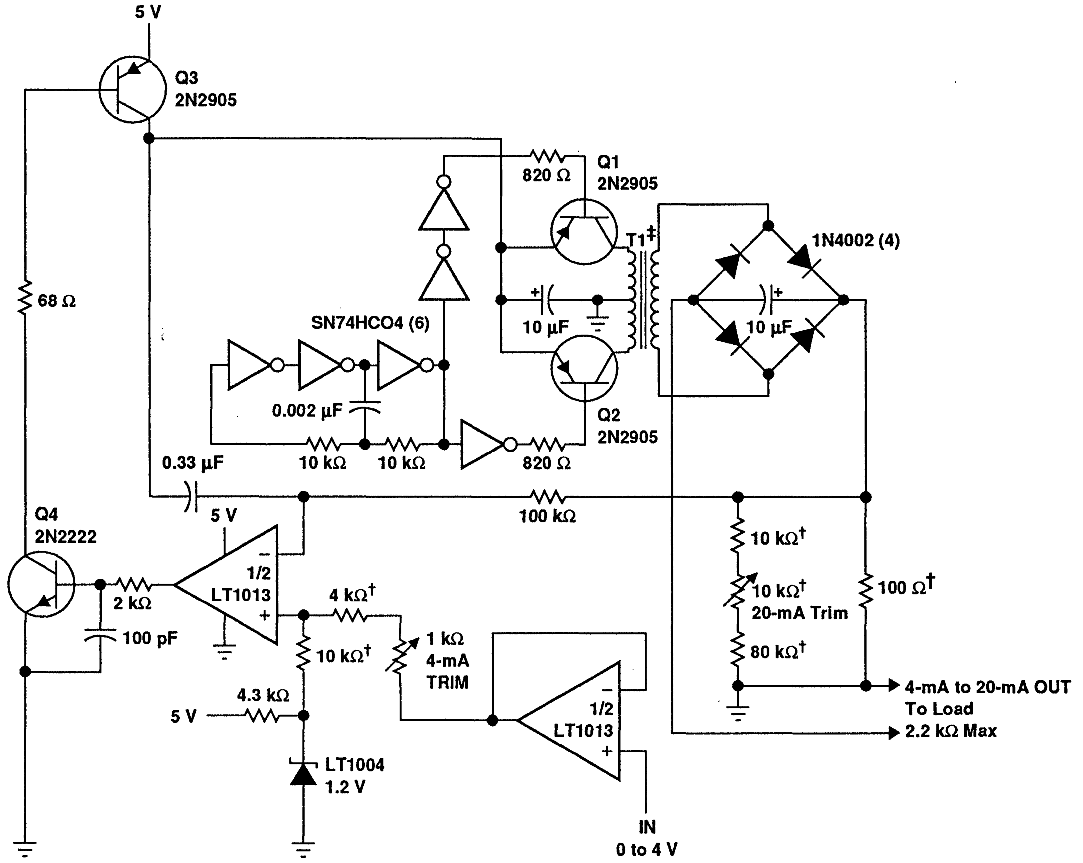


NOTE A: Resistors must have low thermoelectric potential.

Figure 29. Test Circuit for V_{IO} and αV_{IO}

APPLICATION INFORMATION

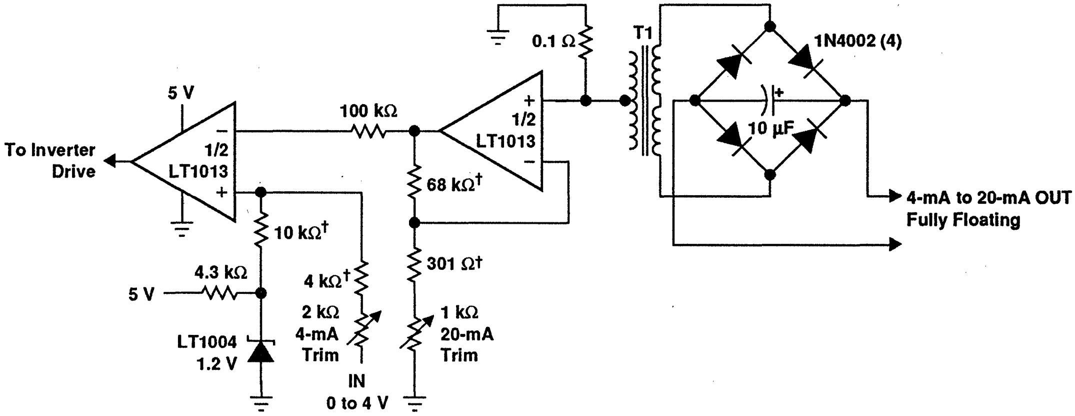
typical applications



†1% film resistor. Match 10-kΩ resistors 0.05%.
‡T1 = PICO-31080

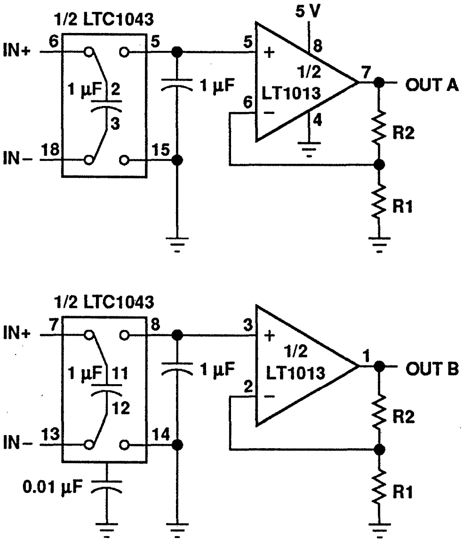
Figure 30. 5-V Powered 4-mA – 20-mA Current Loop Transmitter With 12-Bit Accuracy

APPLICATION INFORMATION



†1% film resistor

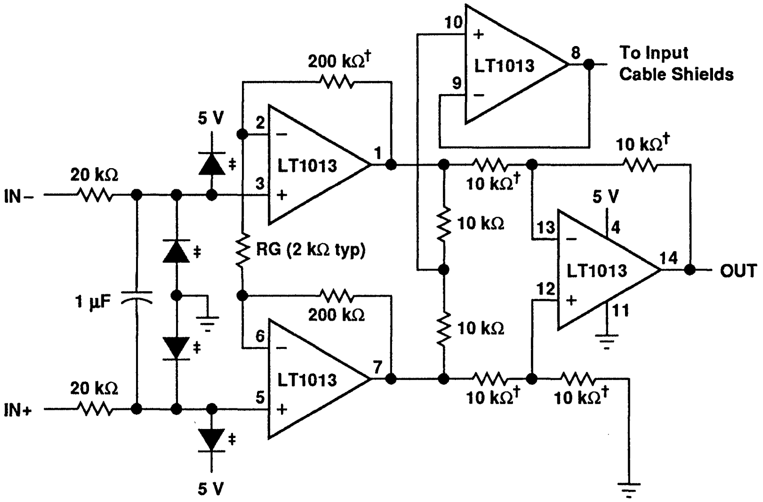
Figure 31. Fully Floating Modification to 4-mA – 20-mA Current Loop Transmitter With 8-Bit Accuracy



NOTE: V_{IO} = 150 µV, A_{VD} = (R1/R2) + 1, CMRR = 120 dB, V_{ICR} = 0 to 5 V

Figure 32. 5-V Single-Supply Dual Instrumentation Amplifier

APPLICATION INFORMATION



†1% film resistor. Match 10-kΩ resistors 0.05%.
‡For high source impedances, use 2N2222 as diodes.
NOTE: A_{VD} = (400,000/RG) + 1

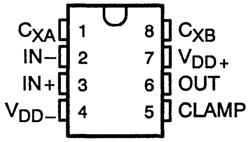
Figure 33. 5-V Powered Precision Instrumentation Amplifier

LTC1052
CHOPPER-STABILIZED OPERATIONAL AMPLIFIER

D3238, MAY 1988–REVISED JULY 1991

- **Input Offset Voltage . . . 5 μV Max at 25°C**
- **Temperature Coefficient of Input Offset Voltage . . . 0.001 μV/°C Typ**
- **Long-Term Drift of Input Offset Voltage 100 nV/mo Typ**
- **Maximum Input Bias Current . . . 30 pA at 25°C**
- **Minimum Differential Voltage Amplification Over Full Temperature Range . . . 120 dB**
- **Minimum Common-Mode Rejection Ratio Over Full Temperature Range . . . 120 dB**
- **Minimum Supply Voltage Rejection Ratio Over Full Temperature Range . . . 120 dB**
- **Single-Supply Operation from 4.75 V to 16 V (Input Voltage Range Extends to Ground)**
- **External Capacitors Can Be Returned to V_{CC-} with No Noise Degradation**

D OR P PACKAGE
(TOP VIEW)



AVAILABLE OPTIONS

T_A	V_{IO} MAX at 25°C	PACKAGE	
		SMALL OUTLINE (D)	PLASTIC DIP (P)
−40°C to 85°C	5 μV	LTC1052CD	LTC1052CP
−55°C to 125°C	5 μV	LTC1052MD	LTC1052MP

The D package is available taped and reeled. Add the suffix R, (e.g., LTC1052CDR).

description

The LTC1052 is a low-noise chopper-stabilized operational amplifier manufactured using CMOS silicon-gate technology. The device is well-suited for applications such as thermocouple amplifiers, strain-gauge amplifiers, low-level signal processing, and medical instrumentation.

Chopper stabilization constantly corrects input offset voltage errors, including both errors in the initial input offset voltage and errors in input offset voltage due to time, temperature, and common-mode input voltage. The chopper circuitry is internal and completely transparent to the user. Only two external capacitors are required to alternately sample and hold the offset correction voltage and the amplified input signal.

Low-frequency (1/f) noise is also improved by the chopping technique. Instead of noise increasing continuously at a rate of 3 dB/octave, the internal chopping causes noise to decrease at low frequencies. Picoampere input currents further enhance the performance of this device.

The C-suffix devices are characterized for operation from −40°C to 85°C. The M-suffix devices are characterized for operation over the full military temperature range of −55°C to 125°C.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{DD+} (see Notes 1 and 2)	8 V
Supply voltage, V_{DD-} (see Notes 1 and 2)	−8 V
Input voltage range, V_I (any input, see Note 1)	±16 V
Duration of short-circuit current at (or below) 25°C (see Note 2)	unlimited
Operating free-air temperature, T_A: C-suffix	−40°C to 85°C
M-suffix	−55°C to 125°C
Storage temperature range	−65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C

NOTES: 1. All voltage values, except differential voltages, are with respect to the midpoint between V_{DD+} and V_{DD-}.
2. Connecting any terminal to voltages greater than V_{DD+} or less than V_{DD-} may cause destructive latch-up. No sources operating from external supplies should be applied prior to device power up.
3. The output may be shorted to either supply.

electrical characteristics at specified free-air temperature, $V_{DD\pm}$ = ±5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A†	LTC1052C			LTC1052M			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IO}	Input offset voltage	V_{IC} = 0, R_S = 50 Ω	25°C		0.5	5		0.5	5	µV
α_{VIO}	Temperature coefficient of input offset voltage		Full range		0.01	0.05		0.01	0.05	µV/°C
	Long-term drift of input offset voltage		25°C		100			100		nV/mo
I_{IO}	Input offset current		25°C		5	30		5	30	pA
			Full range			350			2000	
I_{IB}	Input bias current		25°C		1	30		1	30	pA
			Full range			175			1000	
V_{ICR}	Common-mode input voltage range	R_S = 50 Ω	Full range	−5 to 2.7			−5 to 2.7			V
V_{OM}	Maximum peak output voltage swing	R_L = 100 kΩ, See Note 4	25°C		4.95			4.95		V
		R_L = 10 kΩ, See Note 4	Full range	4.7			4.7			
A_{VD}	Large-signal differential voltage amplification	V_O = ±4 V, R_L = 10 kΩ	25°C	120	150		120	150		dB
			Full range	120			120			
f_{ch}	Internal chopping frequency		25°C		330			330		Hz
	On-state clamp current	R_L = 100 kΩ	25°C		100			100		µA
			Full range	25			25			
	Off-state clamp current	V_O = −4 V to 4 V	25°C		10	100		10	100	pA
			Full range			1			2	nA
CMRR	Common-mode rejection ratio	V_O = 0, V_{IC} = V_{ICR} min, R_S = 50 Ω	25°C	120	140		120	140		dB
			Full range	120			120			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm}/\Delta V_{IO}$)	$V_{CC\pm}$ = 2.375 V to ±8 V, V_O = 0, R_S = 50 Ω	25°C	120	150		120	150		dB
			Full range	120			120			
I_{DD}	Supply current	V_O = 0, No load	25°C		1.7	2		1.7	2	mA
			Full range			3			3	

† Full range is −40°C to 85°C for the LTC1052C and −55°C to 125°C for the LTC1052M.
‡ All typical values are at T_A = 25°C.
NOTE 4: Output clamp is not connected.

operating characteristics, $V_{DD\pm} = \pm 5$ V, $T_A = 25°C$

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SR	Slew rate	$R_L = 10\ k\Omega$, $C_L = 50$ pF		4		V/µs
V_{NPP}	Peak-to-peak equivalent input noise voltage	$R_S = 100\ k\Omega$ to 10 Hz		1.5		µV
		$R_S = 100\ k\Omega$ to 1 Hz		0.5		
I_n	Input noise current (see Note 5)	f = 10 Hz		0.6		fA/√Hz
GBP	Gain bandwidth product			1.2		MHz

NOTE 5: Equivalent input noise current is calculated as follows: $I_n = (2q \times I_{IB})^{1/2}$, where $q = 1.6 \times 10^{-19}$.

MC1458, MC1558
DUAL GENERAL-PURPOSE OPERATIONAL AMPLIFIERS

D972, FEBRUARY 1971—REVISED OCTOBER 1990

- **Short-Circuit Protection**
- **Wide Common-Mode and Differential Voltage Ranges**
- **No Frequency Compensation Required**
- **Low Power Consumption**
- **No Latch-Up**
- **Designed to be Interchangeable With Motorola MC1558/MC1458 and Signetics S5558/N5558**

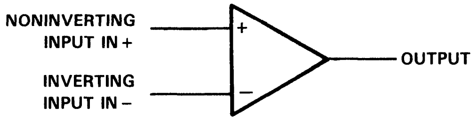
description

The MC1458 and MC1558 are dual general-purpose operational amplifiers with each half electrically similar to the uA741 except that offset null capability is not provided.

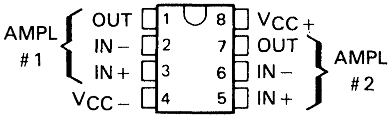
The high-common-mode input voltage range and the absence of latch-up make these amplifiers ideal for voltage-follower applications. The devices are short-circuit protected and the internal frequency compensation ensures stability without external components.

The MC1458 is characterized for operation from 0 °C to 70 °C. The MC1558 is characterized for operation over the full military temperature range of −55 °C to 125 °C.

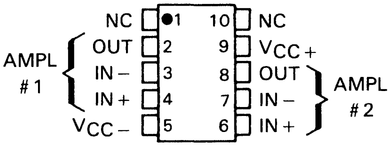
symbol (each amplifier)



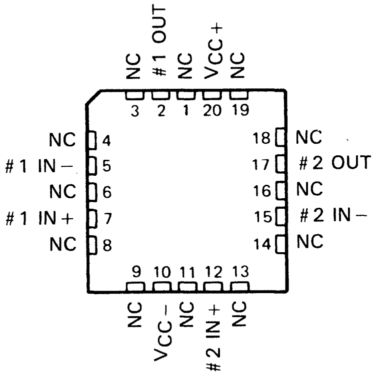
MC1458 . . . D OR P PACKAGE
MC1558 . . . JG PACKAGE
(TOP VIEW)



MC1558 . . . U FLAT PACKAGE
(TOP VIEW)



MC1558 . . . FK PACKAGE
(TOP VIEW)



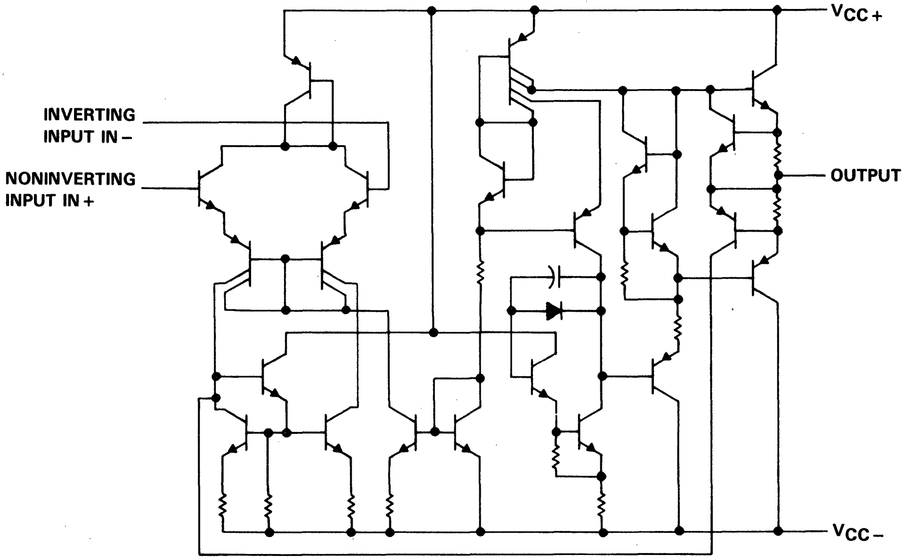
NC—No internal connection

AVAILABLE OPTIONS

SYMBOLIZATION		OPERATING TEMPERATURE RANGE	V_{IO} MAX at 25 °C
DEVICE	PACKAGE SUFFIX		
MC1458	D,P	0 °C to 70 °C	6 mV
MC1558	FK,JG,U	−55 °C to 125 °C	5 mV

The D packages are available taped and reeled. Add the suffix R to the device type, (i.e., MC1458DR)

schematic (each amplifier)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

		MC1458	MC1558	UNIT
Supply voltage V_{CC+} (see Note 1)		18	22	V
Supply voltage V_{CC-} (see Note 1)		−18	−22	V
Differential input voltage (see Note 2)		±30	±30	V
Input voltage at either input (see Notes 1 and 3)		±15	±15	V
Duration of output short-circuit (see Note 4)		unlimited	unlimited	
Continuous total dissipation		See Dissipation Rating Table		
Operating free-air temperature range		0 to 70	−55 to 125	°C
Storage temperature range		65 to 150	−65 to 150	°C
Case temperature for 60 seconds: FK package			260	°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds	JG or U package		300	°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	D or P package	260		°C

NOTES: 1. All voltage values, unless otherwise noted, are with respect to the midpoint between V_{CC+} and V_{CC-}.
2. Differential voltages are at the noninverting input terminal with respect to the inverting input terminal.
3. The magnitude of the input voltage must never exceed the magnitude of the supply voltage or 15 volts, whichever is less.
4. The output can be shorted to ground or either power supply. For the MC1558 only, the unlimited duration of the short-circuit applies at (or below) 125°C case temperature or 70°C free-air temperature.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR	DERATE ABOVE T_A	$T_A = 70°C$ POWER RATING	$T_A = 125°C$ POWER RATING
D	680 mW	5.8 mW/°C	33°C	464 mW	–
FK	680 mW	11.0 mW/°C	88°C	880 mW	275 mW
JG	680 mW	8.4 mW/°C	69°C	672 mW	210 mW
P	680 mW	8.0 mW/°C	65°C	640 mW	–
U	675 mW	5.4 mW/°C	25°C	432 mW	135 mW

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, $V_{CC\pm}$	±5		±15	V

electrical characteristics at specified free-air temperature, $V_{CC+} = 15$ V, $V_{CC-} = -15$ V

PARAMETER		TEST CONDITIONS†		MC1458			MC1558			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	$V_O = 0$	25°C		1	6		1	5	mV
			Full range			7.5			6	
I_{IO}	Input offset current	$V_O = 0$	25°C		20	200		20	200	nA
			Full range			300			500	
I_{IB}	Input bias current	$V_O = 0$	25°C		80	500		80	500	nA
			Full range			800			1500	
V_{ICR}	Common-mode input voltage range		25°C	±12	±13		±12	±13		V
			Full range	±12			±12			
V_{OM}	Maximum peak output voltage swing	$R_L = 10$ kΩ	25°C	±12	±14		±12	±14		V
		$R_L \geq 10$ kΩ	Full range	±12			±12			
		$R_L = 2$ kΩ	25°C	±10	±13		±10	±13		
		$R_L \geq 2$ kΩ	Full range	±10			±10			
A_{VD}	Large-signal differential voltage amplification	$R_L \geq 2$ kΩ, $V_O = \pm 10$ V	25°C	20	200		50	200		V/mV
			Full range	15			25			
B_{OM}	Maximum-output-swing bandwidth (closed-loop)	$R_L = 2$ kΩ, $V_O \geq \pm 10$ V, $A_{VD} = 1$, THD ≤ 5%	25°C		14			14		kHz
B_1	Unity-gain bandwidth		25°C		1			1		MHz
ϕ_m	Phase margin	$A_{VD} = 1$	25°C		65°C			65°C		
A_m	Gain margin		25°C		11			11		dB
r_i	Input resistance		25°C	0.3*	2		0.3*	2		MΩ
r_o	Output resistance	$V_O = 0$, See Note 5	25°C		75			75		Ω
C_i	Input capacitance		25°C		1.4			1.4		pF
z_{ic}	Common-mode input impedance	f = 20 Hz	25°C		200			200		MΩ
CMRR	Common-mode rejection ratio	$V_{IC} = V_{ICR}$ min, $V_O = 0$	25°C	70	90		70	90		dB
			Full range	70			70			
k_{SVS}	Supply voltage sensitivity ($\Delta V_{IO}/\Delta V_{CC}$)	$V_{CC} = \pm 9$ V to ±15 V, $V_O = 0$	25°C		30	150		30	150	μV/V
			Full range			150			150	
V_n	Equivalent input noise voltage (closed-loop)	$A_{VD} = 100$, $R_S = 0$, f = 1 kHz, BW = 1 Hz	25°C		45			45		nV/√Hz

*This parameter is not production tested.

†All characteristics are specified under open-loop operating conditions with zero common-mode input voltage unless otherwise specified. Full range for MC1458 is 0°C to 70°C and for MC1558 is −55°C to 125°C.

NOTE 5: This typical value applies only at frequencies above a few hundred hertz because of the effect of drift and thermal feedback.

electrical characteristics at specified free-air temperature, V_{CC+} = 15 V, V_{CC-} = −15 V (continued)

PARAMETER		TEST CONDITIONS†		MC1458			MC1558			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
I_{OS}	Short-circuit output current		25°C		±25	±40		±25	±40	mA
I_{CC}	Supply current (both amplifiers)	No load, $V_O = 0$	25°C		3.4	5.6		3.4	5	mA
			Full range			6.6			6.6	
P_D	Total power dissipation (both amplifiers)	No load, $V_O = 0$	25°C		100	170		100	150	mW
			Full range			200			200	
V_{o1}/V_{o2}	Crosstalk attenuation		25°C		120			120		dB

†All characteristics are specified under open-loop operating conditions with zero common-mode input voltage unless otherwise spedified. Full range for MC1458 is 0°C to 70°C and for MC1558 is −55°C to 125°C.

operating characteristics, V_{CC+} = 15 V, V_{CC-} = −15 V, T_A = 25°C

PARAMETER		TEST CONDITIONS		MC1458			MC1558			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
t_r	Rise time	V_I = 20 mV, C_L = 100 pF,	R_L = 2 kΩ, See Figure 1		0.3			0.3		µs
	Overshoot factor				5%			5%		
SR	Slew rate at unity gain	V_I = 10 V, C_L = 100 pF,	R_L = 2 kΩ, See Figure 1		0.5			0.5		V/µs

PARAMETER MEASUREMENT INFORMATION

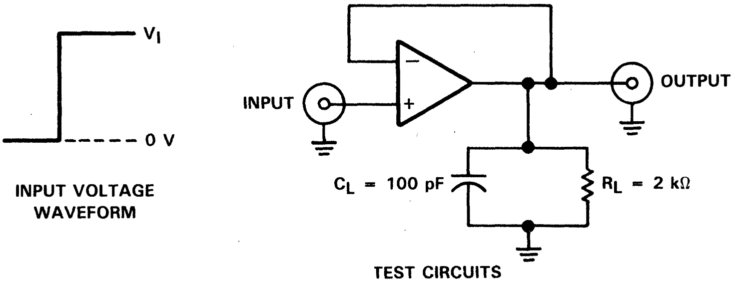


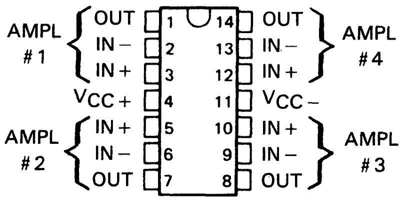
FIGURE 1. RISE TIME, OVERSHOOT, AND SLEW RATE

MC3303, MC3403
QUADRUPLE LOW-POWER OPERATIONAL AMPLIFIERS

D2517, FEBRUARY 1979—REVISED SEPTEBMER 1990

- **Wide Range of Supply Voltages**
  Single Supply . . . 3 V to 36 V
  or Dual Supplies
- **Class AB Output Stage**
- **True Differential Input Stage**
- **Low Input Bias Current**
- **Internal Frequency Compensation**
- **Short-Circuit Protection**
- **Designed to be Interchangeable with Motorola MC3303, MC3403**

D OR N PACKAGE
(TOP VIEW)

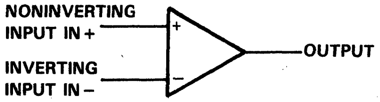


description

The MC3303 and the MC3403 are quadruple operational amplifiers similar in performance to the uA741 but with several distinct advantages. They are designed to operate from a single supply over a range of voltages from 3 V to 36 V. Operation from split supplies is also possible provided the difference between the two supplies is 3 V to 36 V. The common-mode input range includes the negative supply. Output range is from the negative supply to V_{CC} − 1.5 V. Quiescent supply currents are less than one-half those of the uA741.

The MC3303 is characterized for operation from −40°C to 85°C and the MC3403 is characterized for operation from 0°C to 70°C.

symbol (each amplifier)

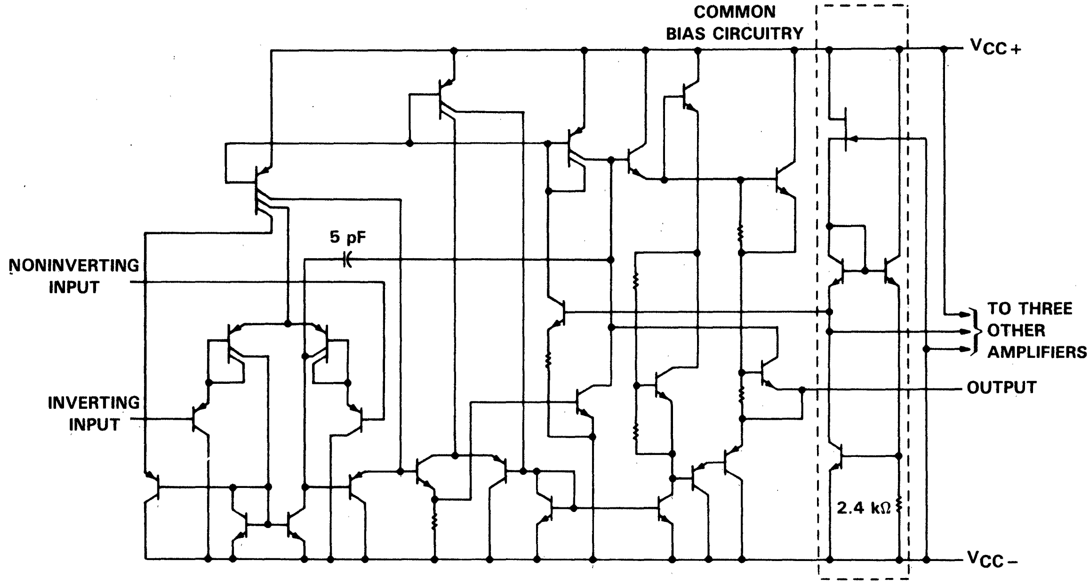


AVAILABLE OPTIONS

T_A	V_{IO} MAX AT 25°C	PACKAGE SMALL-OUTLINE (D)	PACKAGE PLASTIC DIP (N)
0°C to 70°C	10 mV	MC3403D	MC3403N
−40°C to 85°C	8 mV	MC3303D	MC3303N

D packages are available taped and reeled. Add "R" suffix to the device type, (e.g., MC3403DR).

schematic (each amplifier)



Component values shown are nominal.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

	MC3303	MC3403	UNIT
Supply voltage V_{CC+} (see Note 1)	18	18	V
Supply voltage V_{CC-} (see Note 1)	−18	−18	V
Supply voltage V_{CC+} with respect to V_{CC-}	36	36	V
Differential input voltage (see Note 2)	±36	±36	V
Input voltage (see Notes 1 and 3)	±18	±18	V
Continuous total power dissipation	See Dissipation Rating Table		
Operating free-air temperature range	−40 to 85	0 to 70	°C
Storage temperature range	−65 to 150	−65 to 150	°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260	260	°C

NOTES: 1. These voltage values are with respect to the midpoint between V_{CC+} and V_{CC-}.
2. Differential voltages are at the noninverting input terminal with respect to the inverting terminal.
3. Neither input must ever be more positive then V_{CC+} or more negative than V_{CC-}.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING
D	950 mW	7.6 mW/°C	608 mW	494 mW
N	1150 mW	9.2 mW/°C	736 mW	598 mW

recommended operating conditions

	MIN	NOM	MAX	UNIT
Single supply voltage, V_{CC}	5		30	V
Supply voltage, V_{CC+}	2.5		15	V
Dual supply voltage, V_{CC-}	−2.5		−15	V

electrical characteristics at specified free-air temperature; V_{CC+} = 14 V, V_{CC-} = 0 V for MC3303; $V_{CC\pm}$ = ±15 V for MC3403

PARAMETER		TEST CONDITIONS†		MC3303			MC3403			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	See Note 4	25°C		2	8		2	10	mV
			Full range			10			12	
α_{VIO}	Temperature coefficient of input offset voltage	See Note 4	Full range		10			10		μV/°C
I_{IO}	Input offset current	See Note 4	25°C		30	75		30	50	nA
			Full range			250			200	
α_{IIO}	Temperature coefficient of input offset current	See Note 4	Full range		50			50		pA/°C
I_{IB}	Input bias current	See Note 4	25°C		−0.2	−0.5		−0.2	−0.5	μA
			Full range			−1			−0.8	
V_{ICR}	Common-mode input voltage range‡		25°C	V_{CC-} to 12	V_{CC-} to 12.5		V_{CC-} to 13	V_{CC-} to 13.5		V
V_{OM}	Peak output voltage swing	R_L = 10 kΩ	25°C	12	12.5		±12	±13.5		V
		R_L = 2 kΩ	25°C	10	12		±10	±13		
		R_L = 2 kΩ	Full range	10			±10			
A_{VD}	Large-signal differential voltage amplification	V_O = ±10 V, R_L = 2 kΩ	25°C	20	200		20	200		V/mV
			Full range	15			15			
B_{OM}	Maximum-output-swing bandwidth	V_{OPP} = 20 V, A_{VD} = 1, THD ≤ 5%, R_L = 2 kΩ	25°C		9			9		kHz
B_1	Unity-gain bandwidth	V_O = 50 mV, R_L = 10 kΩ	25°C		1			1		MHz
ϕ_m	Phase margin	C_L = 200 pF, R_L = 2 kΩ	25°C		60°			60°		
r_i	Input resistance	f = 20 Hz	25°C	0.3	1		0.3	1		MΩ
r_o	Output resistance	f = 20 Hz	25°C		75			75		Ω
CMRR	Common-mode rejection ratio	V_{IC} = V_{ICR} min	25°C	70	90		70	90		dB
k_{SVS}	Supply voltage sensitivity ($\Delta V_{IO}/\Delta V_{CC}$)	V_{CC} = ±2.5 to ±15 V	25°C		30	150		30	150	μV/V
I_{OS}	Short-circuit output current§		25°C	±10	±30	±45	±10	±30	±45	mA
I_{CC}	Total supply current	No load, See Note 4	25°C		2.8	7		2.8	7	mA

[†] All characteristics are measured under open-loop conditions with zero common-mode voltage unless otherwise specified. Full range for T_A is −40°C to 85°C for MC3303, and 0°C to 70°C for MC3403.

[‡] The V_{ICR} limits are directly linked volt-for-volt to supply voltage; the positive limit is 2 V less than V_{CC+}.

[§] Temperature and/or supply voltages must be limited to ensure that the dissipation rating is not exceeded.

NOTE 4: V_{IO}, I_{IO}, I_{IB}, and I_{CC} are defined at V_O = 0 for MC3403, and V_O = 7 V for MC3303.

electrical characteristics, V_{CC+} = 5 V, V_{CC-} = 0 V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS†	MC3303			MC3403			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_O = 2.5 V			10		2	10	mV
I_{IO}	Input offset current	V_O = 2.5 V			75		30	50	nA
I_{IB}	Input bias current	V_O = 2.5 V			−0.5		−0.2	−0.5	pA
V_{OM}	Peak output voltage swing‡	R_L = 10 kΩ	3.3	3.5		3.3	3.5		V
		R_L = 10 kΩ, V_{CC+} = 5 V to 30 V	$V_{CC+} - 1.7$			$V_{CC+} - 1.7$			
A_{VD}	Large-signal differential voltage amplification	V_O = 1.7 V to 3.3 V, R_L = 2 kΩ	20	200		20	200		V/mV
k_{SVS}	Supply voltage sensitivity ($\Delta V_{IO}/\Delta V_{CC\pm}$)	V_{CC} = ±15 V to ±2.5 V			150			150	µV/V
I_{CC}	Supply current	No load, V_O = 2.5 V		2.5	7		2.5	7	mA
V_{o1}/V_{o2}	Crosstalk attenuation	f = 1 kHz to 20 kHz		120			120		dB

†All characteristics are measured under open-loop conditions with zero common-mode input voltage unless otherwise specified.
‡Output will swing essentially to ground.

operating characteristics, V_{CC+} = 14 V, V_{CC-} = 0 V for MC3303; $V_{CC\pm}$ = ±15 V for MC3403; T_A = 25°C, A_{VD} = 1 (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain	V_I = ±10 V, C_L = 100 pF, R_L = 2 kΩ, See Figure 1		0.6		V/µs
t_r	Rise time	ΔV_O = 50 mV, C_L = 100 pF, R_L = 10 kΩ, See Figure 1		0.35		µs
t_f	Fall time			0.35		µs
	Overshoot factor			20%		
	Crossover distortion	V_{IPP} = 30 mV, V_{OPP} = 2 V, f = 10 kHz		1%		

PARAMETER MEASUREMENT INFORMATION

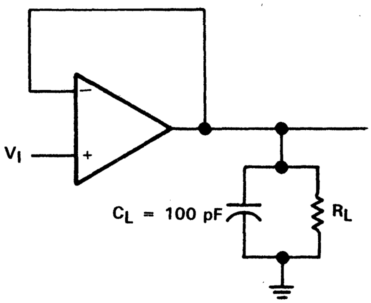


FIGURE 1. UNITY-GAIN AMPLIFIER

TYPICAL CHARACTERISTICS†

INPUT BIAS CURRENT
vs
FREE-AIR TEMPERATURE

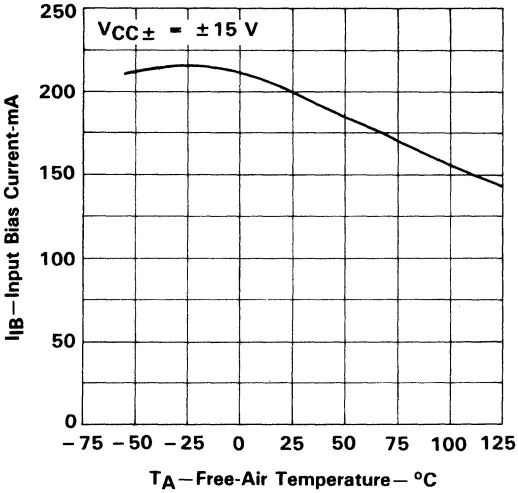


FIGURE 2

INPUT BIAS CURRENT
vs
SUPPLY VOLTAGE

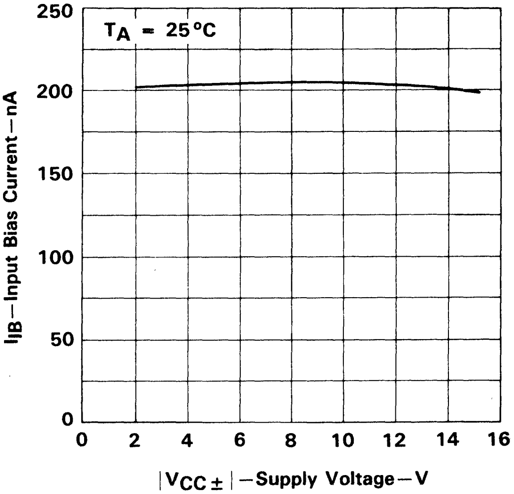


FIGURE 3

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE
vs
SUPPLY VOLTAGE

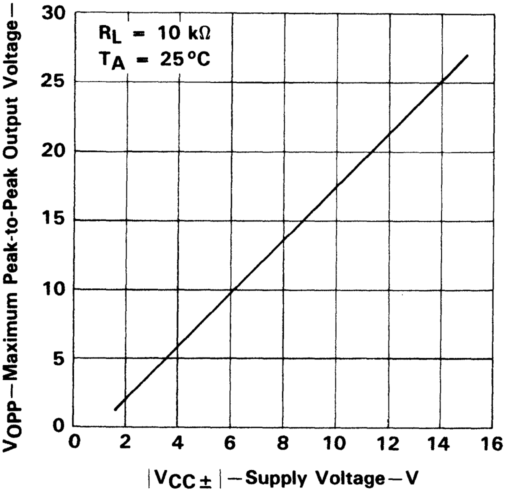


FIGURE 4

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE
vs
FREQUENCY

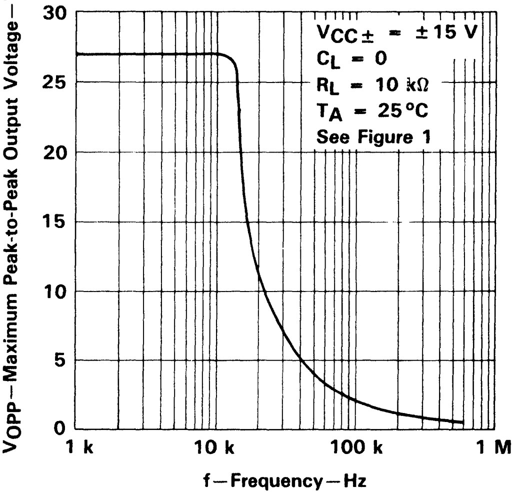


FIGURE 5

---

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS[†]

LARGE-SIGNAL
DIFFERENTIAL VOLTAGE AMPLIFICATION
vs
FREQUENCY

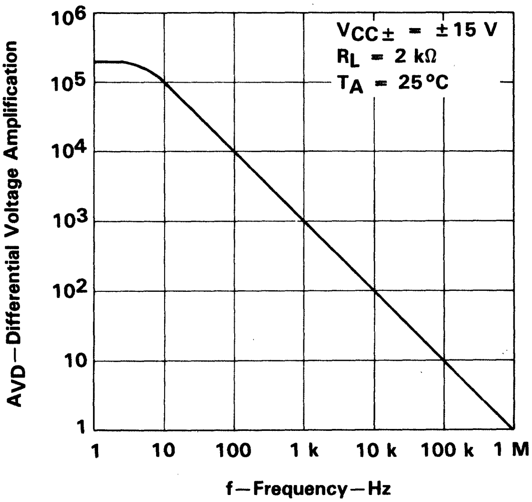


FIGURE 6

VOLTAGE-FOLLOWER
LARGE-SIGNAL PULSE RESPONSE

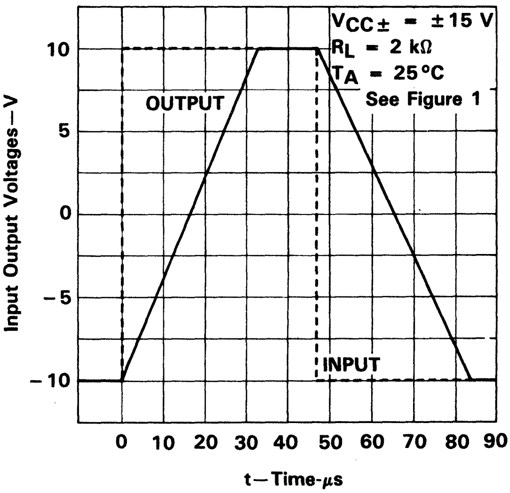


FIGURE 7

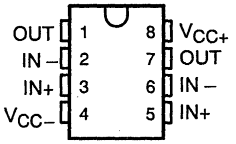
[†] Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

NE5532, NE5532A, NE5532I, NE5532AI
DUAL LOW-NOISE OPERATIONAL AMPLIFIERS

D2563, NOVEMBER 1979–REVISED SEPTEMBER 1990

- **Equivalent Input Noise Voltage . . . 5 nv/$\sqrt{\text{Hz}}$ Typ at 1 kHz**
- **Unity-Gain Bandwidth . . . 10 MHz Typ**
- **Common-Mode Rejection Ratio . . . 100 dB Typ**
- **High DC Voltage Gain . . . 100 V/mV Typ**
- **Peak-to-Peak Output Voltage Swing . . . 32 V Typ With $V_{CC\pm} = \pm 18$ V and $R_L = 600\ \Omega$**
- **High Slew Rate . . . 9 V/μs Typ**
- **Wide Supply Voltage Range . . . ±3 V to ±20 V**
- **Designed to Be Interchangeable With Signetics NE5532 and NE5532A**

P PACKAGE
(TOP VIEW)

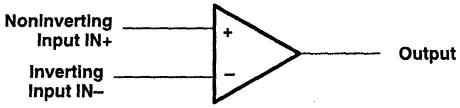


description

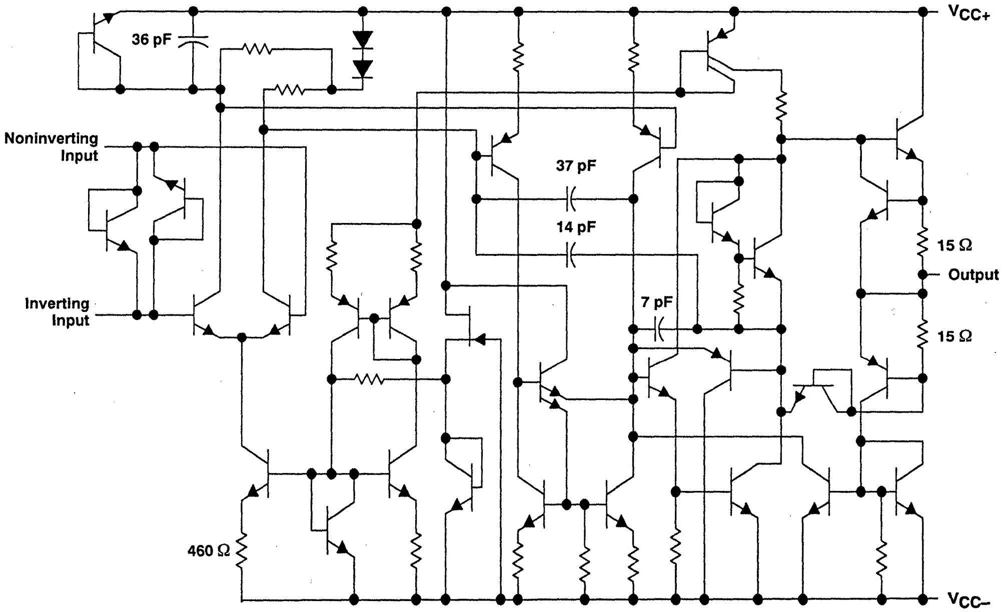
The NE5532 and NE5532A are monolithic high-performance operational amplifiers combining excellent dc and ac characteristics. They feature very low noise, high output drive capability, high unity-gain and maximum-output-swing bandwidths, low distortion, high slew rate, input-protection diodes, and output short-circuit protection. These operational amplifiers are internally compensated for unity gain operation. The NE5532A has specified maximum limits for equivalent input noise voltage.

The NE5532 and NE5532A are characterized for operation from 0°C to 70°C. The NE5532I and NE5532AI are characterized for operation from −40°C to 85°C.

symbol (each amplifier)



schematic (each amplifier)



Component values shown are nominal.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC+} (see Note 1)	22 V
Supply voltage, V_{CC-} (see Note 1)	−22 V
Input voltage, either input (see Notes 1 and 2)	$V_{CC\pm}$
Input current (see Note 3)	± 10 mA
Duration of output short circuit (see Note 4)	unlimited
Continuous total power dissipation	See Dissipation Rating Table
Operating free-air temperature range: NE5532, NE5532A	0°C to 70°C
NE5532I, NE5532AI	−40°C to 85°C
Storage temperature range	−65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C

NOTES: 1. All voltage values, except differential voltages, are with respect to the midpoint between V_{CC+} and V_{CC-}.
2. The magnitude of the input voltage must never exceed the magnitude of the supply voltage.
3. Excessive input current will flow if a differential input voltage in excess of approximately 0.6 V is applied between the inputs unless some limiting resistance is used.
4. The output may be shorted to ground or either power supply. Temperature and/or supply voltages must be limited to ensure the maximum dissipation rating is not exceeded.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	OPERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING
P	1000 mW	8 mW/°C	640 mW	520 mW

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC+}	5		15	V
Supply voltage, V_{CC-}	−5		−15	V

electrical characteristics, $V_{CC\pm} = +15$ V, $T_A = 25°C$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	$V_O = 0$	$T_A = 25°C$		0.5	4	mV
			T_A = Full range			5	
I_{IO}	Input offset current	$T_A = 25°C$			10	150	nA
		T_A = Full range				200	
I_{IB}	Input bias current	$T_A = 25°C$			200	800	nA
		T_A = Full range				1000	
V_{ICR}	Common-mode input voltage range			±12	±13		V
V_{OPP}	Maximum peak-to-peak output voltage swing	$R_L \geq 600\ \Omega$	$V_{CC\pm} = \pm15$ V	24	26		V
			$V_{CC\pm} = \pm18$ V	30	32		
A_{VD}	Large-signal differential voltage amplification	$R_L \geq 600\ \Omega$, $V_O = \pm10$ V	$T_A = 25°C$	15	50		V/mV
			T_A = Full range	10			
		$R_L \geq 2\ k\Omega$, $V_O = \pm10$ V	$T_A = 25°C$	25	100		
			T_A = Full range	15			
A_{vd}	Small-signal differential voltage amplification	f = 10 kHz			2.2		V/mV
B_{OM}	Maximum-output-swing bandwidth	$R_L = 600\ \Omega$, $V_O = \pm10$ V			140		kHz
		$R_L = 600\ \Omega$, $V_{CC\pm} = \pm18$ V, $V_O = \pm14$ V			100		
B_1	Unity-gain bandwidth	$R_L = 600\ \Omega$, $C_L = 100$ pF			10		MHz
r_i	Input resistance			30	300		kΩ
z_o	Output impedance	$A_{VD} = 30$ dB, $R_L = 600\ \Omega$, f = 10 kHz			0.3		Ω
CMRR	Common-mode rejection ratio	$V_{IC} = V_{ICR}$ min		70	100		dB
k_{SVR}	Supply voltage rejection ratio ($\Delta V_{CC\pm}/\Delta V_{IO}$)	$V_{CC\pm} = \pm9$ V to ±15 V, $V_O = 0$		80	100		dB
I_{OS}	Output short-circuit current				38		mA
I_{CC}	Total supply curent	No load, $V_O = 0$			8	16	mA
V_{01}/V_{02}	Crosstalk attenuation	$V_{01} = 10$ V peak, f = 1 kHz			110		dB

† All characteristics are measured under open-loop conditions with zero common-mode input voltage unless otherwise specified. Full range for T_A is 0°C to 70°C for NE5532/NE5532A and −40°C to 85°C for NE5532I/NE5532AI.

operating characteristics, $V_{CC\pm} = \pm15$ V, $T_A = 25°C$

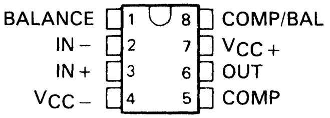
PARAMETER		TEST CONDITIONS	NE5532/NE5532I			NE5532A/NE5532AI			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
SR	Slew rate at unity gain			9			9		V/μs
	Overshoot factor	$V_I = 100$ mV, $A_{VD} = 1$, $R_L = 600\ \Omega$, $C_L = 100$ pF		10%			10%		
V_n	Equivalent input noise voltage	f = 30 Hz		8			8	10	nV/√Hz
		f = 1 kHz		5			5	6	
I_n	Equivalent input noise current	f = 30 Hz		2.7			2.7		pA/√Hz
		f = 1 kHz		0.7			0.7		

NE5534, NE5534A, SE5534, SE5534A
LOW-NOISE OPERATIONAL AMPLIFIERS

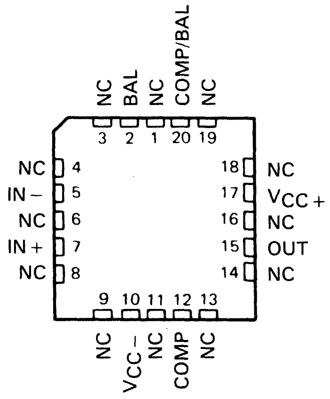
D2532, JULY 1979—REVISED SEPTEMBER 1990

- **Equivalent Input Noise Voltage 3.5 nV/√Hz Typ**
- **Unity-Gain Bandwidth . . . . . . 10 MHz Typ**
- **Common-Mode Rejection Ratio 100 dB Typ**
- **High DC Voltage Gain . . . . 100 V/mV Typ**
- **Peak-to-Peak Output Voltage Swing 32 V Typ with $V_{CC\pm} = \pm 18$ V and $R_L = 600\ \Omega$**
- **High Slew Rate . . . . 13 V/μs Typ**
- **Wide Supply Voltage Range ±3 V to ±20 V**
- **Low Harmonic Distortion**
- **Designed to be Interchangeable with Signetics NE5534, NE5534A, SE5534, and SE5534A**

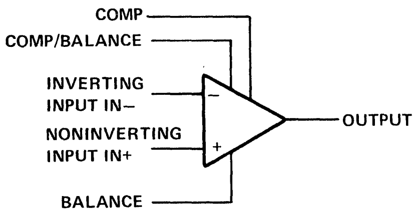
NE5534, NE5534A . . . D OR P PACKAGE
SE5534, SE5534A . . . JG PACKAGE
(TOP VIEW)



SE5534, SE5534A
FK CHIP CARRIER PACKAGE
(TOP VIEW)



symbol



AVAILABLE OPTIONS

T_A	V_{IO} MAX AT 25°C	PACKAGE			
		SMALL OUTLINE (D)	CERAMIC (FK)	CERAMIC DIP (JG)	PLASTIC DIP (P)
0°C to 70°C	4 mV	NE5534D	—	—	NE5534P
		NE5534AD	—	—	NE5534AP
−55°C to 125°C	2 mV	—	SE5534FK	SE5534JG	—
		—	SE5534AFK	SE5534AJG	—

The D package is available taped and reeled. Add the suffix R to the device type, (e.g., NE5534DR).

SE5534A FROM TI NOT RECOMMENDED FOR NEW DESIGNS

description

The NE5534, NE5534A, SE5534, and SE5534A are monolithic high-performance operational amplifiers combining excellent dc and ac characteristics. Some of the features include very low noise, high output drive capability, high unity-gain and maximum-output-swing bandwidths, low distortion, and high slew rate.

These operational amplifiers are internally compensated for a gain equal to or greater than three. Optimization of the frequency response for various applications can be obtained by use of an external compensation capacitor between pins 5 and 8. The devices feature input-protection diodes, output short-circuit protection, and offset-voltage nulling capability.

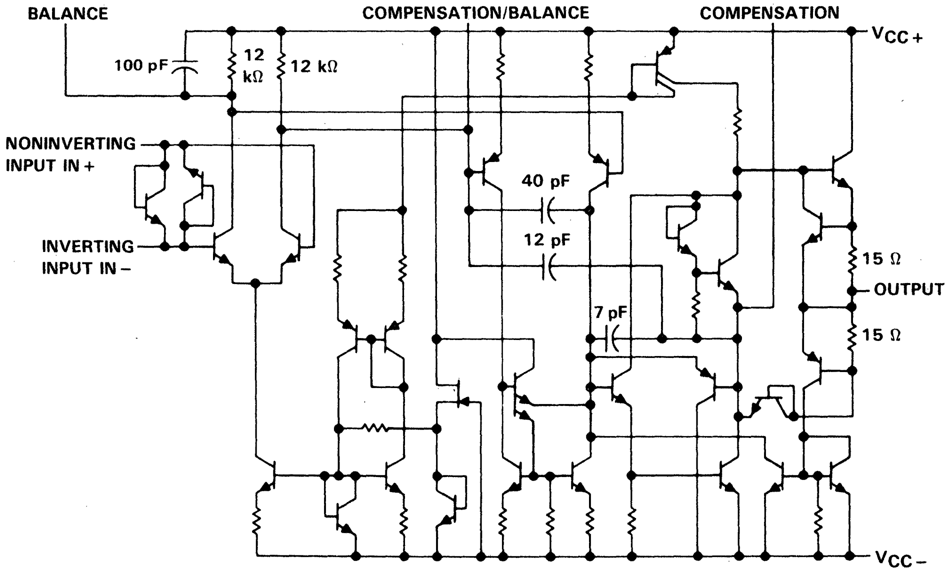
TEXAS INSTRUMENTS
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

description (continued)

For the NE5534A, a maximum limit is specified for equivalent input noise voltage.

The NE5534 and NE5534A are characterized for operation from 0 °C to 70 °C. The SE5534 and SE5534A are characterized for operation over the full military temperature range of −55 °C to 125 °C.

schematic



All component values shown are nominal.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC+} (see Note 1)	22 V
Supply voltage, V_{CC-} (see Note 1)	−22 V
Input voltage either input (see Notes 1 and 2)	V_{CC+}
Input current (see Note 3)	±10 mA
Duration of output short-circuit (see Note 4)	unlimited
Continuous total power dissipation	See Dissipation Rating Table
Operating free-air temperature range: NE5534, NE5534A	0 °C to 70 °C
SE5534, SE5534A	−55 °C to 125 °C
Storage temperature range	−65 °C to 150 °C
Case temperature for 60 seconds: FK package	260 °C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: JG package	300 °C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D or P package	260 °C

NOTES:
1. All voltage values, except differential voltages, are with respect to the midpoint between V_{CC+} and V_{CC-}.
2. The magnitude of the input voltage must never exceed the magnitude of the supply voltage.
3. Excessive current will flow if a differential input voltage in excess of approximately 0.6 V is applied between the inputs unless some limiting resistance is used.
4. The output may be shorted to ground or either power supply. Temperature and/or supply voltages must be limited to ensure the maximum dissipation rating is not exceeded.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 125°C$ POWER RATING
D	725 mW	5.8 mW/°C	464 mW	N/A
FK (see Note 5)	1375 mW	11.0 mW/°C	880 mW	275 mW
JG	1050 mW	8.4 mW/°C	672 mW	210 mW
P	1000 mW	8.0 mW/°C	640 mW	N/A

NOTE 5: For the FK package, power rating and derating factor will vary with actual mounting technique used. The values stated here are believed to be conservative.

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC+}	5		15	V
Supply voltage, V_{CC-}	−5		−15	V

electrical characteristics, $V_{CC\pm} = \pm 15$ V, $T_A = 25°C$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		NE5534, NE5534A			SE5534, SE5534A			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	$V_O = 0$, $R_S = 50\ \Omega$	$T_A = 25°C$		0.5	4		0.5	2	mV
			T_A = full range			5			3	
I_{IO}	Input offset current	$V_O = 0$	$T_A = 25°C$		20	300		10	200	nA
			T_A = full range			400			500	
I_{IE}	Input bias current	$V_O = 0$	$T_A = 25°C$		500	1500		400	800	nA
			T_A = full range			2000			1500	
V_{ICR}	Common-mode input voltage range			±12	±13		±12	±13		V
V_{OPP}	Maximum peak-to-peak output voltage swing	$R_L \ge 600\ \Omega$	$V_{CC\pm} = \pm 15$ V	24	26		24	26		V
			$V_{CC\pm} = \pm 18$ V	30	32		30	32		
A_{VD}	Large-signal differential voltage amplification	$V_O = \pm 10$ V, $R_L \ge 600\ \Omega$	$T_A = 25°C$	25	100		50	100		V/mV
			T_A = full range	15			25			
A_{vd}	Small-signal differential voltage amplification	f = 10 kHz	$C_C = 0$		6			6		V/mV
			$C_C = 22$ pF		2.2			2.2		
B_{OM}	Maximum-output-swing bandwidth	$V_O = \pm 10$ V,	$C_C = 0$		200			200		kHz
		$V_O = \pm 10$ V,	$C_C = 22$ pF		95			95		
		$V_{CC\pm} = \pm 18$ V, $R_L = 600\ \Omega$,	$V_O = \pm 14$ V, $C_C = 22$ pF		70			70		
B_1	Unity-gain bandwidth	$C_C = 22$ pF,	$C_L = 100$ pF		10			10		MHz
r_i	Input resistance			30	100		50	100		kΩ
z_C	Output impedance	$A_{VD} = 30$ dB, $C_C = 22$ pF,	$R_L = 600\ \Omega$, f = 10 kHz		0.3			0.3		Ω
CMRR	Common-mode rejection ratio	$V_O = 0$, $R_S = 50\ \Omega$	$V_{IC} = V_{ICR}$ min,	70	100		80	100		dB
k_{SVR}	Supply voltage rejection ratio $(\Delta V_{CC}/\Delta V_{IO})$	$V_{CC+} = \pm 9$ V to ± 15 V, $V_O = 0$,	$R_S = 50\ \Omega$	80	100		86	100		dB
I_{OS}	Output short-circuit current				38			38		mA
I_{CC}	Supply current	No load, $V_O = 0$	$T_A = 25°C$		4	8		4	6.5	mA
			T_A = full range						9	

† All characteristics are measured under open-loop conditions with zero common-mode input voltage unless otherwise specified. Full range is T_A = 0°C to 70°C for NE5534 and NE5534A and −55°C to 125°C for SE5534 and SE5534A.

operating characteristics, $V_{CC\pm} = \pm 15$ V, $T_A = 25$°C

PARAMETER		TEST CONDITIONS	SE5534, NE5534			SE5534A, NE5534A			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
SR	Slew rate at unity gain	$C_C = 0$		13			13		V/µs
		$C_C = 22$ pF		6			6		
t_r	Rise time	$V_I = 50$ mV, $A_{VD} = 1$, $R_L = 600\ \Omega$, $C_C = 22$ pF, $C_L = 100$ pF		20			20		ns
	Overshoot factor			20%			20%		
t_r	Rise time	$V_I = 50$ mV, $A_{VD} = 1$, $R_L = 600\ \Omega$, $C_C = 47$ pF, $C_L = 500$ pF		50			50		ns
	Overshoot factor			35%			35%		
V_n	Equivalent input noise voltage	f = 30 Hz		7			5.5	7	nV/√Hz
		f = 1 kHz		4			3.5	4.5	
I_n	Equivalent input noise current	f = 30 Hz		2.5			1.5		pA/√Hz
		f = 1 kHz		0.6			0.4		
F	Average noise figure	$R_S = 5$ kΩ, f = 10 Hz to 20 kHz					0.9		dB

TYPICAL CHARACTERISTICS†

NORMALIZED INPUT BIAS CURRENT
and INPUT OFFSET CURRENT
vs
FREE-AIR TEMPERATURE

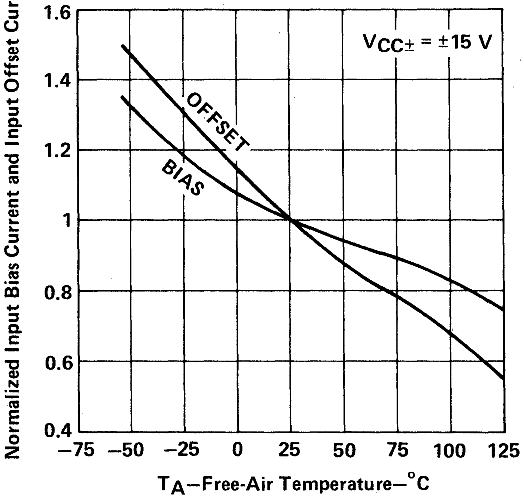


FIGURE 1

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE
vs
FREQUENCY

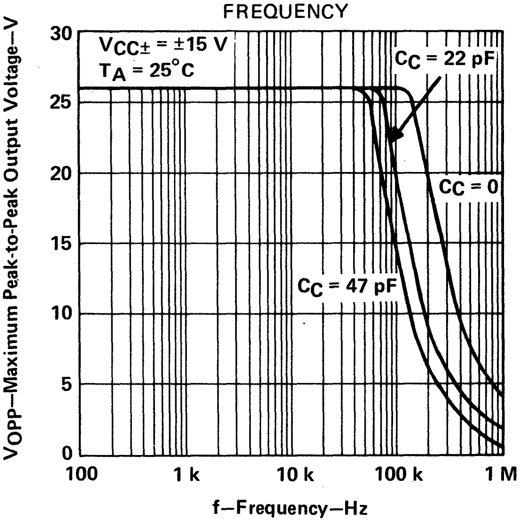


FIGURE 2

---

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS[†]

LARGE-SIGNAL
DIFFERENTIAL VOLTAGE AMPLIFICATION
vs
FREQUENCY

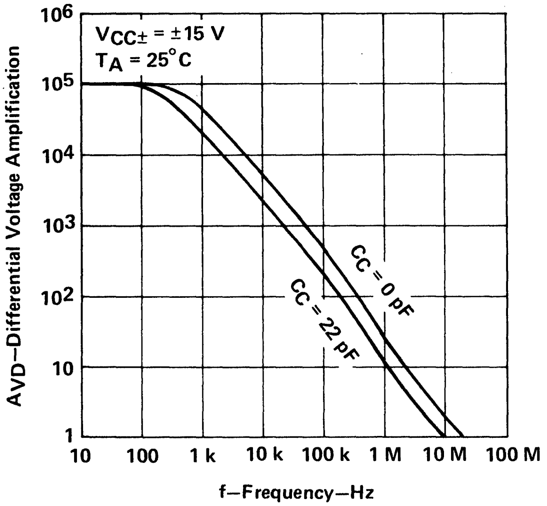


FIGURE 3

NORMALIZED SLEW RATE and
UNITY-GAIN BANDWIDTH
vs
SUPPLY VOLTAGE

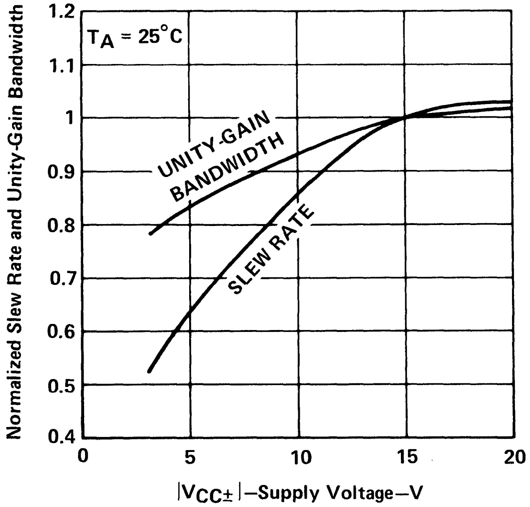


FIGURE 4

NORMALIZED SLEW RATE and
UNITY-GAIN BANDWIDTH
vs
FREE-AIR TEMPERATURE

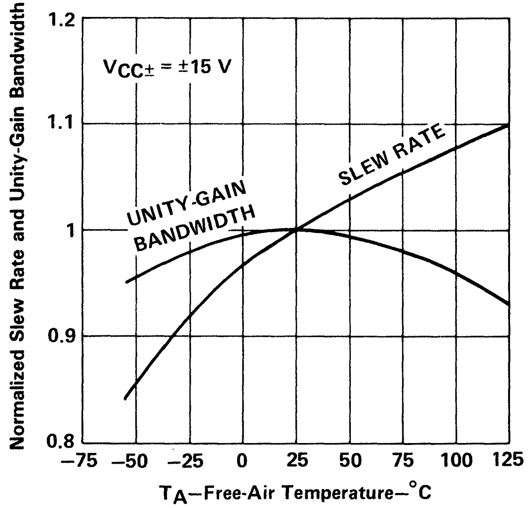


FIGURE 5

TOTAL HARMONIC DISTORTION
vs
FREQUENCY

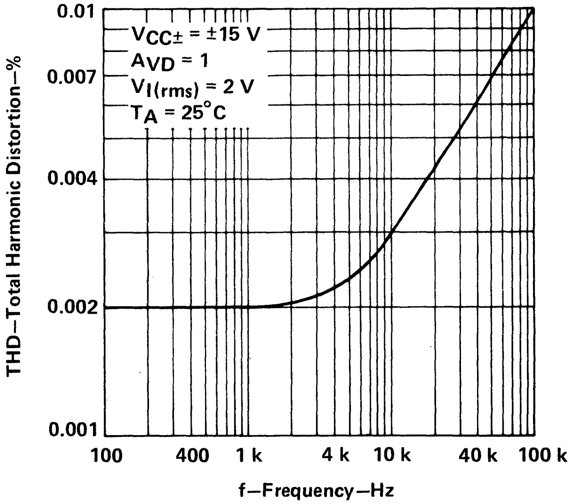


FIGURE 6

[†] Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS

EQUIVALENT INPUT NOISE VOLTAGE
vs
FREQUENCY

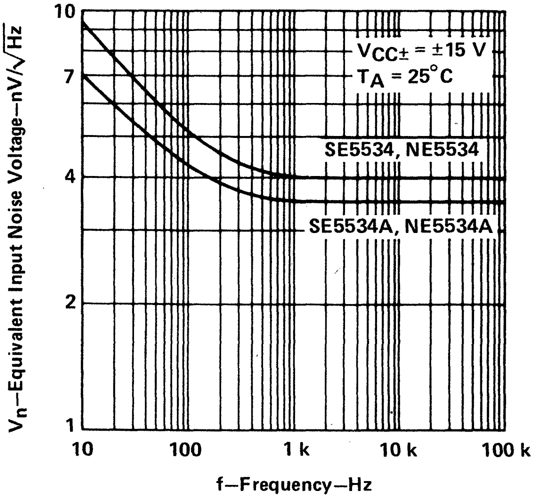


FIGURE 7

EQUIVALENT INPUT NOISE CURRENT
vs
FREQUENCY

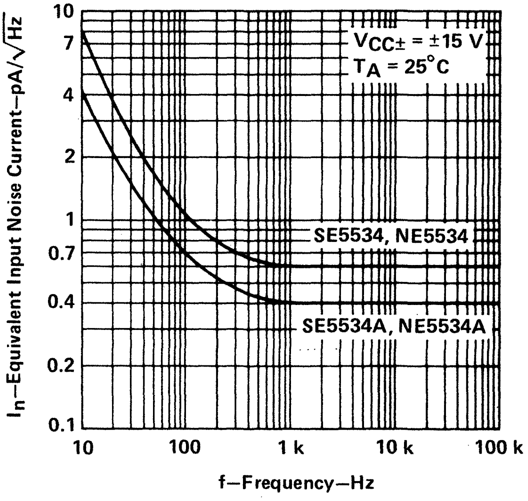


FIGURE 8

TOTAL EQUIVALENT INPUT NOISE VOLTAGE
vs
SOURCE RESISTANCE

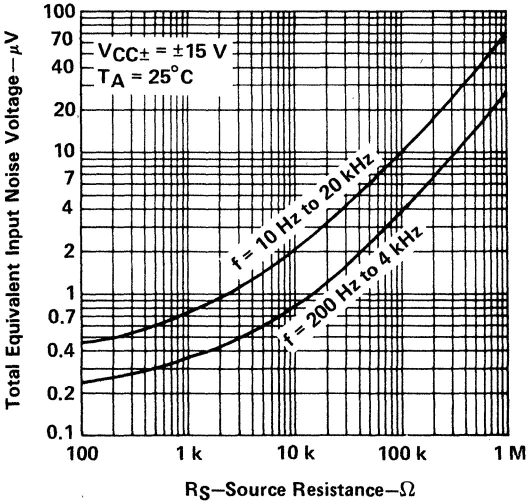


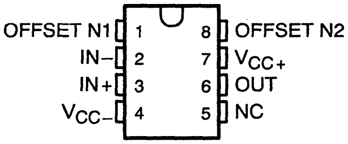
FIGURE 9

OP07C, OP07D, OP07Y
LOW-OFFSET VOLTAGE OPERATIONAL AMPLIFIERS

D2757, OCTOBER 1983–REVISED SEPTEMBER 1991

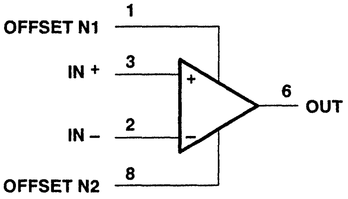
- **Low Noise**
- **No External Components Required**
- **Replaces Chopper Amplifiers at a Lower Cost**
- **Single-Chip Monolithic Fabrication**
- **Wide Input Voltage Range**
  0 to ±14 V Typ
- **Wide Supply Voltage Range**
  ±3 V to ±18 V
- **Essentially Equivalent to Fairchild μA714 Operational Amplifiers**
- **Direct Replacement for PMI OP07C and OP07D**

D OR P PACKAGE
(TOP VIEW)



NC–No internal connection

symbol



description

These devices represent a breakthrough in operational amplifier performance. Low offset and long-term stability are achieved by means of a low-noise, chopperless, bipolar-input-transistor amplifier circuit. For most applications, external components are required for offset nulling and frequency compensation. The true differential input, with a wide input voltage range and outstanding common-mode rejection, provides maximum flexibility and performance in high-noise environments and in noninverting applications. Low bias currents and extremely high input impedances are maintained over the entire temperature range. The OP07 is unsurpassed for low-noise, high-accuracy amplification of very low-level signals.

These devices are characterized for operation from 0°C to 70°C.

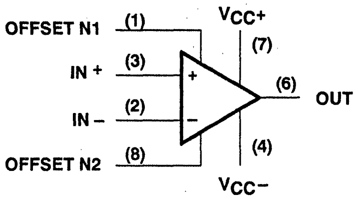
AVAILABLE OPTIONS

T_A	V_{IO}max at 25°C	PACKAGE		CHIP FORM (Y)
		SMALL OUTLINE (D)	PLASTIC DIP (P)	
0°C to 70°C	150 μV	OP07CD OP07DD	OP07CP OP07DP	OP07Y

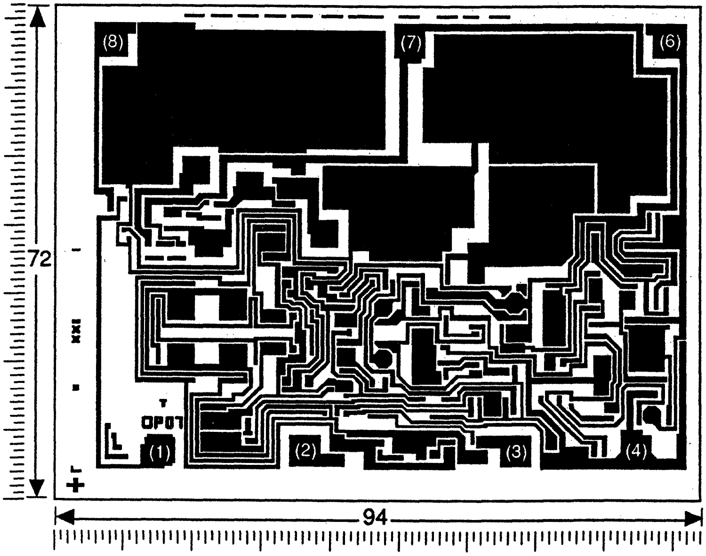
The D package is available taped and reeled. Add the suffix R to the device type (e.g., OP07CDR). The chip form (Y) is tested at T_A = 25°C.

chip information

These chips, properly assembled, display characteristics similar to the OP07. Thermal compression or ultrasonic bonding may be used on the doped aluminum bonding pads. Chips may be mounted with conductive epoxy or a gold-silicon preform.



BONDING PAD ASSIGNMENTS



CHIP THICKNESS: 15 TYPICAL

BONDING PADS: 4 × 4 MINIMUM

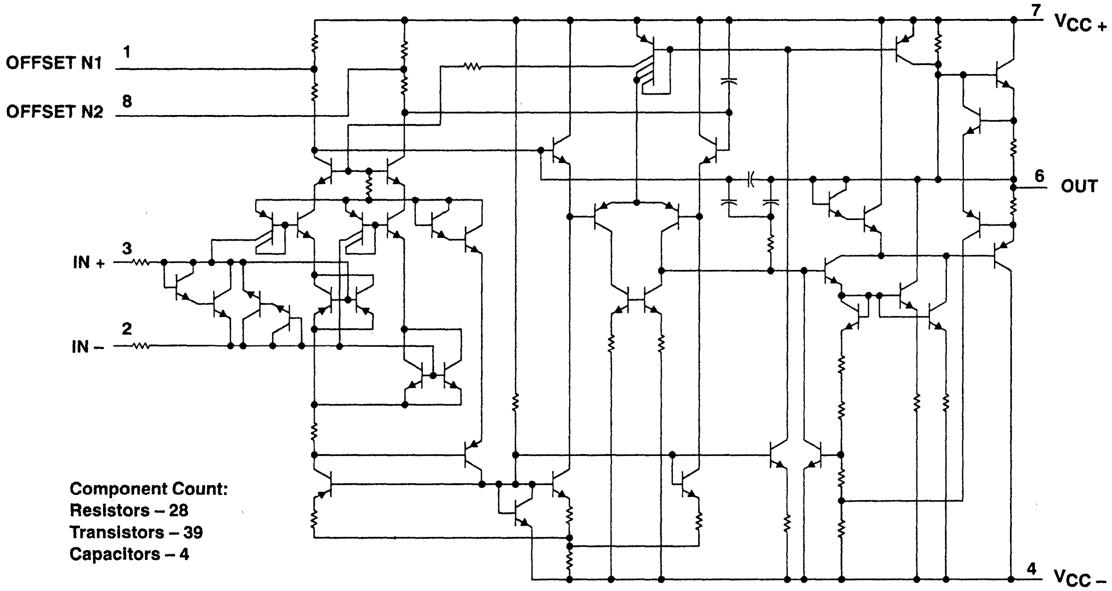
$T_J$max = 150°C

TOLERANCES ARE ± 10%

ALL DIMENSIONS ARE IN MILS

PIN (4) INTERNALLY CONNECTED TO BACKSIDE OF CHIP

schematic



Component Count:
Resistors – 28
Transistors – 39
Capacitors – 4

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC+} (see Note 1)	22 V
Supply voltage, V_{CC-}	−22 V
Differential input voltage (see Note 2)	±30 V
Input voltage, V_I (either input, see Note 3)	±22 V
Duration of output short circuit (see Note 4)	unlimited
Continuous total dissipation at (or below) 25°C free-air temperature (see Note 5)	500 mW
Operating free-air temperature range, T_A	0°C to 70°C
Storage temperature range	−65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C

NOTES: 1. All voltage values, unless otherwise noted, are with respect to the midpoint between V_{CC+} and V_{CC-}.
2. Differential voltages are at the noninverting input terminal with respect to the inverting input terminal.
3. The magnitude of the input voltage must never exceed the magnitude of the supply voltage or 15 V, whichever is less.
4. The output may be shorted to ground or either power supply.
5. For operation above 64°C free-air temperature, derate the D package to 464 mW at 70°C at the rate of 5.8 mW/°C.

recommended operating conditions

		MIN	MAX	UNIT
Supply voltage, $V_{CC\pm}$		±3	±18	V
Common-mode input voltage, V_{IC}	$V_{CC\pm}$ = ±15 V	−13	13	V
Operating free-air temperature, T_A		0	70	°C

electrical characteristics at specified free-air temperature, $V_{CC\pm} = \pm15$ V (unless otherwise noted)

PARAMETER		TEST CONDITIONS†	T_A	OP07C			OP07D			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	$V_O = 0$, $R_S = 50\ \Omega$	25°C		60	150		60	150	µV
			0°C to 70°C		85	250		85	250	
α_{VIO}	Temperature coefficient of input offset voltage	$V_O = 0$, $R_S = 50\ \Omega$	0°C to 70°C		0.5	1.8		0.7	2.5	µV/°C
	Long-term drift of input offset voltage	See Note 6			0.4			0.5		µV/mo
	Offset adjustment range	$R_S = 20\ k\Omega$, See Figure 1	25°C		±4			±4		mV
I_{IO}	Input offset current		25°C		0.8	6		0.8	6	nA
			0°C to 70°C		1.6	8		1.6	8	
α_{IIO}	Temperature coefficient of input offset current		0°C to 70°C		12	50		12	50	pA/°C
I_{IB}	Input bias current		25°C		±1.8	±7		±2	±12	nA
			0°C to 70°C		±2.2	±9		±3	±14	
α_{IIB}	Temperature coefficient of input bias current		0°C to 70°C		18	50		18	50	pA/°C
V_{ICR}	Common-mode input voltage range		25°C	±13	±14		±13	±14		V
			0°C to 70°C	±13	±13.5		±13	±13.5		
V_{OM}	Peak output voltage	$R_L \geq 10\ k\Omega$	25°C	±12	±13		±12	±13		V
		$R_L \geq 2\ k\Omega$		±11.5	±12.8		±11.5	±12.8		
		$R_L \geq 1\ k\Omega$			±12			±12		
		$R_L \geq 2\ k\Omega$	0°C to 70°C	±11	±12.6		±11	±12.6		
A_{VD}	Large-signal differential voltage amplification	$V_{CC\pm} = \pm3$ V, $V_O = \pm0.5$ V, $R_L \geq 500\ k\Omega$	25°C	100	400			400		V/mV
		$V_O = \pm10$ V, $R_L = 2\ k\Omega$	25°C	120	400		120	400		
			0°C to 70°C	100	400		100	400		
B_1	Unity-gain bandwidth		25°C	0.4	0.6		0.4	0.6		MHz
r_i	Input resistance		25°C	8	33		7	31		MΩ
CMRR	Common-mode rejection ratio	$V_{IC} = \pm13$ V, $R_S = 50\ \Omega$	25°C	100	120		94	110		dB
			0°C to 70°C	97	120		94	106		
k_{SVS}	Supply voltage sensitivity ($\Delta V_{IO}/\Delta V_{CC}$)	$V_{CC\pm} = \pm3$ V to ±18 V, $R_S = 50\ \Omega$	25°C		7	32		7	32	µV/V
			0°C to 70°C		10	51		10	51	
P_D	Power dissipation	$V_O = 0$, No load	25°C		80	150		80	150	mW
		$V_{CC\pm} = \pm3$ V, $V_O = 0$, No load			4	8		4	8	

† All characteristics are measured under open-loop conditions with zero common-mode input voltage unless otherwise noted.

NOTE 6: Since long-term drift cannot be measured on the individual devices prior to shipment, this specification is not intended to be a warranty. It is an engineering estimate of the averaged trend line of drift versus time over extended periods after the first thirty days of operation.

operating characteristics, $V_{CC\pm} = \pm 15$ V, $T_A = 25°C$

PARAMETER		TEST CONDITIONS†	OP07C			OP07D			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
V_n	Equivalent input noise voltage	f = 10 Hz		10.5			10.5		nV/√Hz
		f = 100 Hz		10.2			10.3		
		f = 1 kHz		9.8			9.8		
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 10 Hz		0.38			0.38		μV
I_n	Equivalent input noise current	f = 10 Hz		0.35			0.35		pA/√Hz
		f = 100 Hz		0.15			0.15		
		f = 1 kHz		0.13			0.13		
$I_{N(PP)}$	Peak-to-peak equivalent input noise current	f = 0.1 Hz to 10 Hz		15			15		pA
SR	Slew rate	$R_L \geq 2$ kΩ		0.3			0.3		V/μs

† All characteristics are measured under open-loop conditions with zero common-mode input voltage unless otherwise noted.

electrical characteristics, $V_{CC\pm}$ = ±15 V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS†	MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	R_S = 50 Ω		60	150	µV
	Long-term drift of input offset voltage	See Note 6		0.5		µV/mo
	Offset adjustment range	R_S = 20 kΩ, See Figure 1		±4		mV
I_{IO}	Input offset current			0.8	6	nA
I_{IB}	Input bias current			±2	±12	nA
V_{ICR}	Common-mode input voltage range		±13	±14		V
V_{OM}	Peak output voltage	R_L ≤ 10 kΩ	±12	±13		V
		R_L ≤ 2 kΩ	±11.5	±12.8		
		R_L ≤ 1 kΩ		±12		
A_{VD}	Large-signal differential voltage amplification	$V_{CC\pm}$ = ±3 V, V_O = ±0.5 V, R_L ≤ 500 kΩ		400		V/mV
		V_O = ±10 V, R_L = 2 kΩ	120	400		
B_1	Unity-gain bandwidth		0.4	0.6		MHz
r_i	Input resistance		7	31		MΩ
CMRR	Common-mode input resistance	V_{IC} = ±13 V, R_S = 50 Ω	94	110		dB
k_{SVS}	Supply-voltage rejection ratio ($\Delta V_{CC}/\Delta V_{IO}$)	$V_{CC\pm}$ = ±3 V to ±18 V, R_S = 50 Ω		7	32	µV/V
P_D	Power dissipation	V_O = 0, No load		80	150	MΩ
		$V_{CC\pm}$ = ±3 V, V_O = 0, No load		4	8	

NOTE 6: Since long-term drift cannot be measured on the individual devices prior to shipment, this specification is not intended to be a warranty. It is an engineering estimate of the averaged trend line of drift versus time over extended periods after the first thirty days of operation.

operating characteristics, $V_{CC\pm}$ = ±15 V, T_A = 25°C

PARAMETER		TEST CONDITIONS†	MIN	TYP	MAX	UNIT
V_n	Equivalent input noise voltage	f = 10 Hz		10.5		nV/√Hz
		f = 1 kHz		10.3		
		f = 0.1 Hz to 10 Hz		9.8		
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 10 Hz		0.38		µV
I_n	Equivalent input noise current	f = 10 Hz		0.35		pA/√Hz
		f = 100 Hz		0.15		
		f = 1 kHz		0.13		
$I_{N(PP)}$	Peak-to-peak equivalent input noise current	f = 0.1 Hz to 10 Hz		15		pA
SR	Slew rate	R_L = 2 kΩ		0.3		V/µs

† All characteristics are measured under open-loop conditions with zero common-mode input voltage unless otherwise noted.

APPLICATION INFORMATION

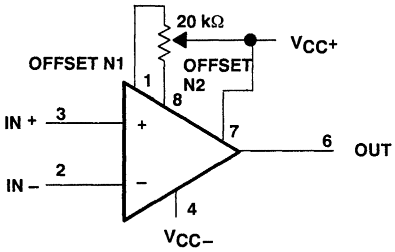


Figure 1. Input Offset Voltage Null Circuit

OP27A, OP27C, OP27E, OP27G
OP37A, OP37C, OP37E, OP37G
LOW-NOISE, HIGH-SPEED, PRECISION OPERATIONAL AMPLIFIERS

D3176, FEBRUARY 1989—REVISED AUGUST 1991

- **Direct Replacements for PMI and LTC OP27 and OP37 Series**

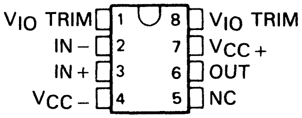
Features of OP27A, OP27C, OP37A, and OP37C:

- **Maximum Equivalent Input Noise Voltage:**
  3.8 $\mathrm{nV}/\sqrt{\mathrm{Hz}}$ at 1 kHz
  5.5 $\mathrm{nV}/\sqrt{\mathrm{Hz}}$ at 10 Hz
- **Very Low Peak-to-Peak Noise Voltage at 0.1 Hz to 10 Hz . . . 80 nV Typ**
- **Low Input Offset Voltage . . . 25 μV Max**
- **High Voltage Amplification . . . 1 V/μV Min**

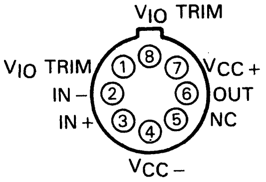
Feature of OP37 Series:

- **Minimum Slew Rate . . . 11 V/μs**

JG OR P PACKAGE
(TOP VIEW)



L PACKAGE
(TOP VIEW)



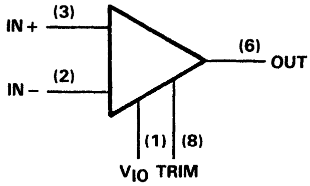
NC—No internal connection

description

The OP27 and OP37 operational amplifiers combine outstanding noise performance with excellent precision and high-speed specifications. The wideband noise is only 3 $\mathrm{nV}/\sqrt{\mathrm{Hz}}$, and with the 1/f noise corner at 2.7 Hz, low noise is maintained for all low-frequency applications.

The outstanding characteristics of the OP27 and OP37 make these devices excellent choices for low-noise amplifier applications requiring precision performance and reliability. Additionally, the OP37 is free of latch-up in high-gain, large-capacitive-feedback configurations.

symbol



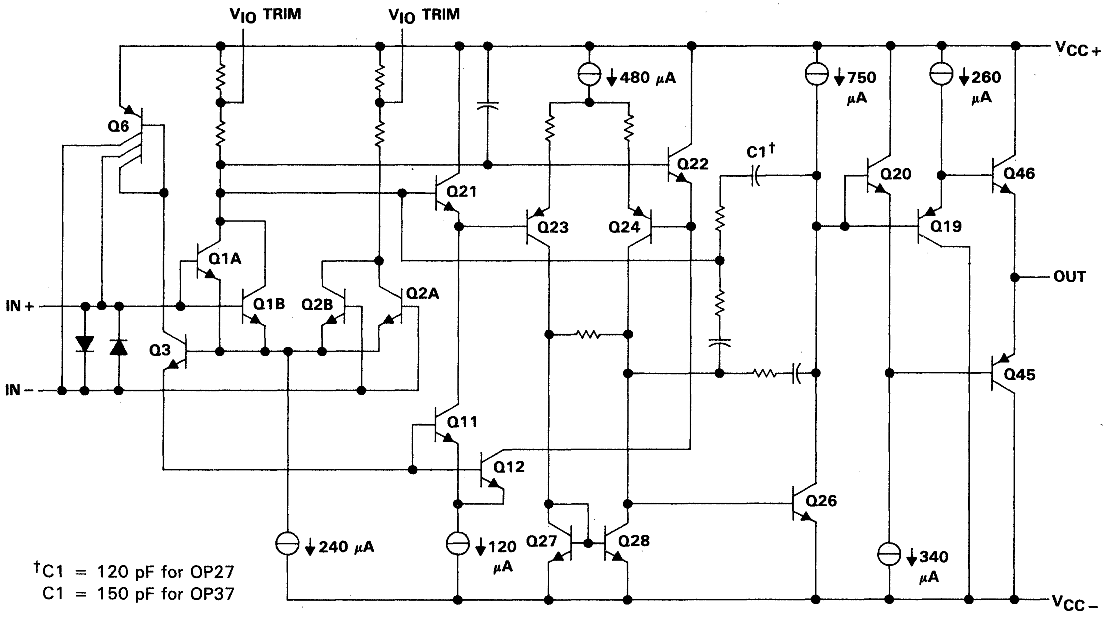
The OP27 series is compensated for unity gain. The OP37 series is decompensated for increased bandwidth and slew rate and is stable down to a gain of 5.

The OP27A, OP27C, OP37A, and OP37C are characterized for operation over the full military temperature range of −55°C to 125°C. The OP27E, OP27G, OP37E, and OP37G are characterized for operation from −25°C to 85°C.

AVAILABLE OPTIONS

T_A	V_{IO} MAX AT 25°C	STABLE GAIN	PACKAGE		
			CERAMIC DIP (JG)	METAL CAN (L)	PLASTIC DIP (P)
−25°C to 85°C	25 μV	1	—	—	OP27EP
		5	—	—	OP37EP
	100 μV	1	—	—	OP27GP
		5	—	—	OP37GP
−55°C to 125°C	25 μV	1	OP27AJG	OP27AL	—
		5	OP37AJG	OP37AL	—
	100 μV	1	OP27CJG	—	—
		5	OP37CJG	—	—

schematic



†C1 = 120 pF for OP27
C1 = 150 pF for OP37

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC+} (see Note 1)	22 V
Supply voltage, V_{CC-} (see Note 1)	−22 V
Input voltage	$V_{CC\pm}$
Duration of output short circuit	unlimited
Differential input current (see Note 2)	±25 mA
Continuous power dissipation	See Dissipation Rating Table
Operating free-air temperature range: OP27A, OP27C, OP37A, OP37C	−55°C to 125°C
OP27E, OP27G, OP37E, OP37G	−25°C to 85°C
Storage temperature range	−65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: JG or L package	300°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: P package	260°C

NOTES: 1. All voltage values are with respect to the midpoint between V_{CC+} and V_{CC-} unless otherwise noted.
2. The inputs are protected by back-to-back diodes. Current-limiting resistors are not used in order to achieve low noise. Excessive input current will flow if a differential input voltage in excess of approximately ±0.7 V is applied between the inputs unless some limiting resistance is used.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 85°C$ POWER RATING	$T_A = 125°C$ POWER RATING
JG	1050 mW	8.4 mW/°C	546 mW	210 mW
L	825 mW	6.6 mW/°C	429 mW	165 mW
P	1000 mW	8.0 mW/°C	520 mW	N/A

recommended operating conditions

		OP27A, OP37A			OP27C, OP37C			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC+}		4	15	22	4	15	22	V
Supply voltage, V_{CC-}		−4	−15	−22	−4	−15	−22	V
Common-mode input voltage, V_{ICR}	$V_{CC\pm}$ = ±15 V, T_A = 25°C			±11			±11	V
	$V_{CC\pm}$ = ±15 V, T_A = −55°C to 125°C			±10.3			±10.2	
Operating free-air temperature, T_A		−55		125	−55		125	°C

electrical characteristics, $V_{CC\pm}$ = ±15 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A	OP27A, OP37A			OP27C, OP37C			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_O = 0, V_{IC} = 0 R_S = 50 Ω, See Note 3	25°C		10	25		30	100	μV
			−55°C to 125°C			60			300	
αV_{IO}	Average temperature coefficient of input offset voltage		−55°C to 125°C		0.2	0.6		0.4	1.8	μV/°C
	Long-term drift of input offset voltage	See Note 4			0.2	1		0.4	2	μV/mo
I_{IO}	Input offset current	V_O = 0, V_{IC} = 0	25°C		7	35		12	75	nA
			−55°C to 125°C			50			135	
I_{IB}	Input bias current	V_O = 0, V_{IC} = 0	25°C		±10	±40		±15	±80	nA
			−55°C to 125°C			±60			±150	
V_{ICR}	Common-mode input voltage range		25°C	±11			±11			V
			−55°C to 125°C	±10.3			±10.2			
V_{OM}	Peak output voltage swing	R_L ≥ 2 kΩ	25°C	±12	±13.8		±11.5	±13.5		V
		R_L ≥ 0.6 kΩ		±10	±11.5		±10	±11.5		
		R_L ≥ 2 kΩ	−55°C to 125°C	±11.5			±10.5			
A_{VD}	Large-signal differential voltage amplification	R_L ≥ 2 kΩ, V_O = ±10 V	25°C	1000	1800		700	1500		V/mV
		R_L ≥ 1 kΩ, V_O = ±10 V		800	1500			1500		
		R_L ≥ 0.6 kΩ, V_O = ±1 V, V_{CC} = ± 4 V		250	700		200	500		
		R_L ≥ 2 kΩ, V_O = ±10 V	−55°C to 125°C	600			300			
$r_{i(CM)}$	Common-mode input resistance				3			2		GΩ
r_o	Output resistance	V_O = 0, I_O = 0	25°C		70			70		Ω
CMRR	Common-mode rejection ratio	V_{IC} = ±11 V	25°C	114	126		100	120		dB
		V_{IC} = ±10 V	−55°C to 125°C	108			94			
k_{SVR}	Supply voltage rejection ratio	$V_{CC\pm}$ = ±4 V to ±18 V	25°C	100	120		94	118		dB
		$V_{CC\pm}$ = ±4.5 V to ±18 V	−55°C to 125°C	96			86			

NOTES: 3. Input offset voltage measurements are performed by automatic test equipment approximately 0.5 seconds after applying power.

4. Long-term drift of input offset voltage refers to the average trend line of offset voltage versus time over extended periods after the first 30 days of operation. Excluding the initial hour of operation, changes in V_{IO} during the first 30 days are typically 2.5 μV. See Figure 3.

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC+}		4	15	22	V
Supply voltage, V_{CC-}		−4	−15	−22	V
Common-mode input voltage, V_{ICR}	$V_{CC\pm} = \pm 15$ V, $T_A = 25°C$			±11	V
	$V_{CC\pm} = \pm 15$ V, $T_A = -55°C$ to 125°C			±10.5	
Operating free-air temperature, T_A		−25		85	°C

electrical characteristics, $V_{CC\pm} = \pm 15$ V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A	OP27E, OP37E			OP27G, OP37G			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	$V_O = 0$, $V_{IC} = 0$ $R_S = 50\ \Omega$, See Note 3	25°C		10	25		30	100	μV
			−25°C to 85°C			50			220	
αV_{IO}	Average temperature coefficient of input offset voltage		−25°C to 85°C		0.2	0.6		0.4	1.8	μV/°C
	Long-term drift of input offset voltage	See Note 4			0.2	1		0.4	2	μV/mo
I_{IO}	Input offset current	$V_O = 0$, $V_{IC} = 0$	25°C		7	35		12	75	nA
			−25°C to 85°C			50			135	
I_{IB}	Input bias current	$V_O = 0$, $V_{IC} = 0$	25°C		±10	±40		±15	±80	nA
			−25°C to 85°C			±60			±150	
V_{ICR}	Common-mode input voltage range		25°C	±11			±11			V
			−25°C to 85°C	±10.5			±10.5			
V_{OM}	Peak output voltage swing	$R_L \geq 2\ k\Omega$	25°C	±12	±13.8		±11.5	±13.5		V
		$R_L \geq 0.6\ k\Omega$		±10	±11.5		±10	±11.5		
		$R_L \geq 2\ k\Omega$	−25°C to 85°C	±11.7			±11			
A_{VD}	Large-signal differential voltage amplification	$R_L \geq 2\ k\Omega$, $V_O = \pm 10$ V	25°C	1000	1800		700	1500		V/mV
		$R_L \geq 1\ k\Omega$, $V_O = \pm 10$ V		800	1500			1500		
		$R_L \geq 0.6\ k\Omega$, $V_O = \pm 1$ V, $V_{CC} = \pm 4$ V		250	700		200	500		
		$R_L \geq 2\ k\Omega$, $V_O = \pm 10$ V	−25°C to 85°C	750			450			
$r_{i(CM)}$	Common-mode input resistance				3			2		GΩ
r_o	Output resistance	$V_O = 0$, $I_O = 0$	25°C		70			70		Ω
CMRR	Common-mode rejection ratio	$V_{IC} = \pm 11$ V	25°C	114	126		100	120		dB
		$V_{IC} = \pm 10$ V	−25°C to 85°C	110			96			
k_{SVR}	Supply voltage rejection ratio	$V_{CC\pm} = \pm 4$ V to ±18 V	25°C	100	120		94	118		dB
		$V_{CC\pm} = \pm 4.5$ V to ±18 V	−25°C to 85°C	97			90			

NOTES: 3. Input offset voltage measurements are performed by automatic test equipment approximately 0.5 seconds after applying power.

4. Long-term drift of input offset voltage refers to the average trend line of offset voltage versus time over extended periods after the first 30 days of operation. Excluding the initial hour of operation, changes in V_{IO} during the first 30 days are typically 2.5 μV. See Figure 3.

OP27 operating characteristics over operating free-air temperature range, $V_{CC\pm} = \pm 15$ V

PARAMETER		TEST CONDITIONS	OP27A, OP27E			OP27C, OP27G			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
SR	Slew rate at unity gain	$A_{VD} \geq 1$, $R_L \geq 2$ kΩ	1.7	2.8		1.7	2.8		V/μs
V_{NPP}	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 10 Hz, RS = 100 Ω, See Figure 34		0.08	0.18		0.09	0.25	μV
V_n	Equivalent input noise voltage	f = 10 Hz, R_S = 100 Ω,		3.5	5.5		3.8	8	nV/√Hz
		f = 30 Hz, R_S = 100 Ω		3.1	4.5		3.3	5.6	
		f = 1 kHz, R_S = 100 Ω		3.0	3.8		3.2	4.5	
I_n	Equivalent input noise current	f = 10 Hz, See Figure 35		1.5	4		1.5		pA/√Hz
		f = 30 Hz, See Figure 35		1.0	2.3		1.0		
		f = 1 kHz, See Figure 35		0.4	0.6		0.4	0.6	
GBW	Gain bandwidth product	f = 100 kHz	5	8		5	8		MHz

OP37 operating characteristics over operating free-air temperature range, $V_{CC\pm} = \pm 15$ V

PARAMETER		TEST CONDITIONS	OP37A, OP37E			OP37C, OP37G			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
SR	Slew rate at unity gain	$A_{VD} \geq 5$, $R_L \geq 2$ kΩ	11	17		11	17		V/μs
V_{NPP}	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 10 Hz, R_S = 100 Ω, See Figure 34		0.08	0.18		0.09	0.25	μV
V_n	Equivalent input noise voltage	f = 10 Hz, R_S = 100 Ω		3.5	5.5		3.8	8	nV/√Hz
		f = 30 Hz, R_S = 100 Ω		3.1	4.5		3.3	5.6	
		f = 1 kHz, R_S = 100 Ω		3.0	3.8		3.2	4.5	
I_n	Equivalent input noise current	f = 10 Hz, See Figure 35		1.5	4		1.5		pA/√Hz
		f = 30 Hz, See Figure 35		1.0	2.3		1.0		
		f = 1 kHz, See Figure 35		0.4	0.6		0.4	0.6	
GBW	Gain bandwidth product	f = 10 kHz	45	63		45	63		MHz
		$A_V \geq 5$, f = 1 MHz		40			40		

TYPICAL CHARACTERISTICS

table of graphs

			FIGURE
V_{IO}	Input offset voltage	vs Temperature	1
ΔV_{IO}	Change in input offset voltage	vs Time after power-on	2
		vs Time (long-term drift)	3
I_{IO}	Input offset current	vs Temperature	4
I_{IB}	Input bias current	vs Temperature	5
V_{ICR}	Common-mode input voltage range	vs Supply voltage	6
V_{OM}	Maximum peak output voltage	vs Load resistance	7
V_{OPP}	Maximum peak-to-peak output voltage	vs Frequency	8, 9
A_{VD}	Differential voltage amplification	vs Supply voltage	10
		vs Load resistance	11
		vs Frequency	12, 13, 14
CMRR	Common-mode rejection ratio	vs Frequency	15
k_{SVR}	Supply voltage rejection ratio	vs Frequency	16
SR	Slew rate	vs Temperature	17
		vs Supply voltage	18
		vs Load resistance	19
ϕ_m	Phase margin	vs Temperature	20, 21
ϕ	Phase shift	vs Frequency	12, 13
V_n	Equivalent input noise voltage	vs Bandwidth	22
		vs Source resistance	23
		vs Supply voltage	24
		vs Temperature	25
		vs Frequency	26
I_n	Equivalent input noise current	vs Frequency	27
GBW	Gain bandwidth product	vs Temperature	20, 21
I_{OS}	Short-circuit output current	vs Time	28
I_{CC}	Supply current	vs Supply voltage	29
	Pulse response	Small-signal	30, 32
		Large-signal	31, 33

TYPICAL CHARACTERISTICS†

INPUT OFFSET VOLTAGE
OF REPRESENTATIVE UNITS
vs
FREE-AIR TEMPERATURE

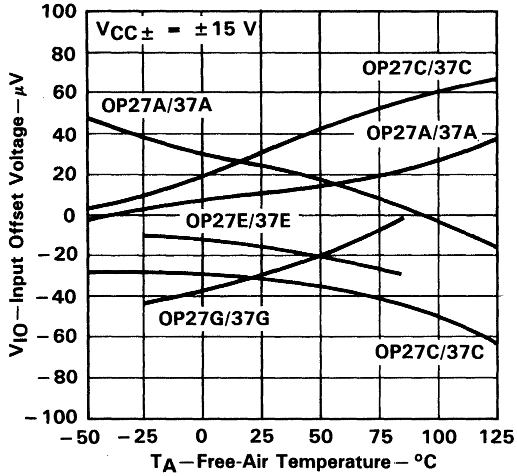


Figure 1

WARM-UP CHANGE IN
INPUT OFFSET VOLTAGE
vs
ELAPSED TIME

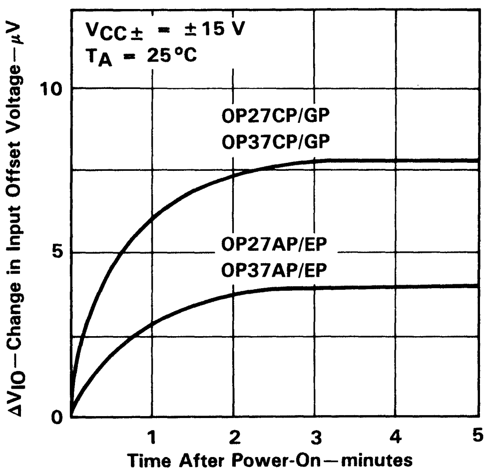


Figure 2

LONG-TERM DRIFT OF
INPUT OFFSET VOLTAGE
OF REPRESENTATIVE UNITS

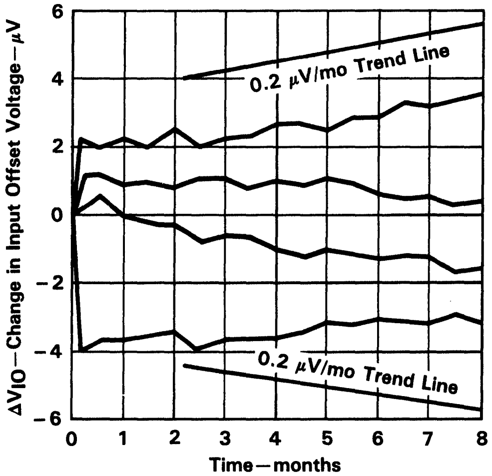


Figure 3

---

†Data for temperatures below −25°C and above 85°C are applicable to the OP27A, OP27C, OP37A, and OP37C only.

TYPICAL CHARACTERISTICS[†]

INPUT OFFSET CURRENT
vs
FREE-AIR TEMPERATURE

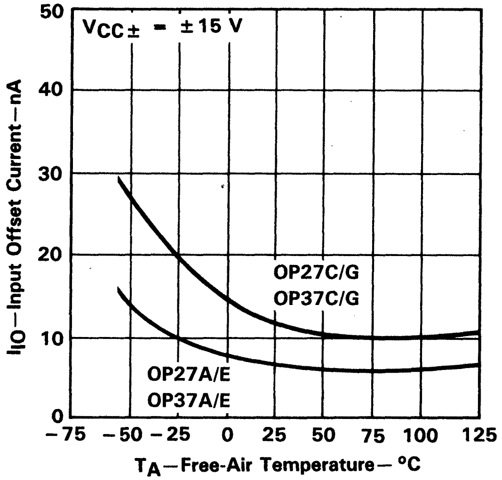


Figure 4

INPUT BIAS CURRENT
vs
FREE-AIR TEMPERATURE

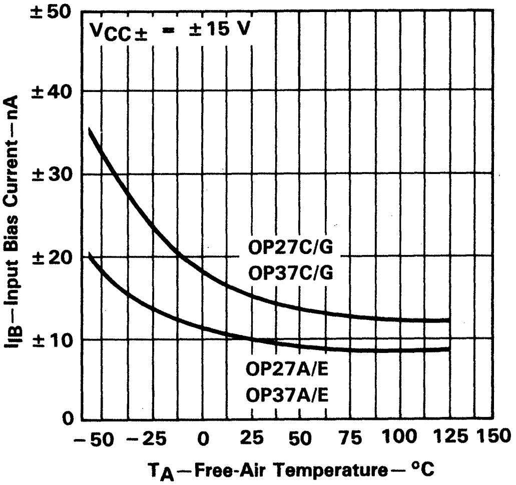


Figure 5

COMMON-MODE INPUT VOLTAGE RANGE LIMITS
vs
SUPPLY VOLTAGE

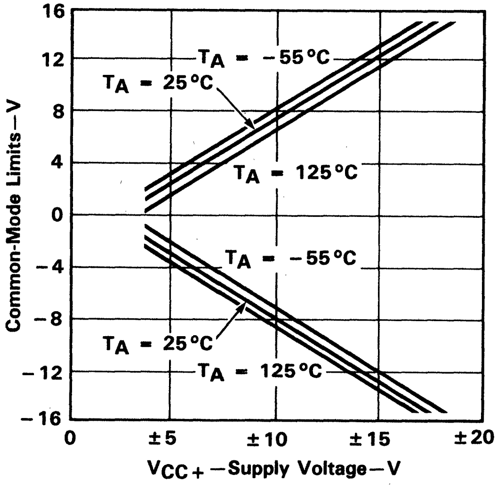


Figure 6

MAXIMUM PEAK OUTPUT VOLTAGE
vs
LOAD RESISTANCE

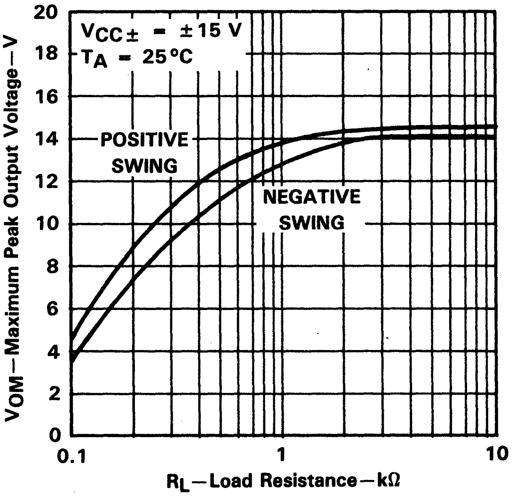


Figure 7

[†] Data for temperatures below −25°C and above 85°C are applicable to the OP27A, OP27C, OP37A, and OP37C only.

TYPICAL CHARACTERISTICS

OP27
MAXIMUM PEAK-TO-PEAK
OUTPUT VOLTAGE
vs
FREQUENCY

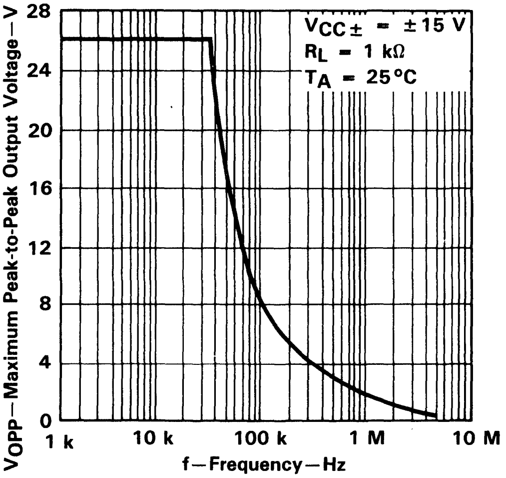


Figure 8

OP37
MAXIMUM PEAK-TO-PEAK
OUTPUT VOLTAGE
vs
FREQUENCY

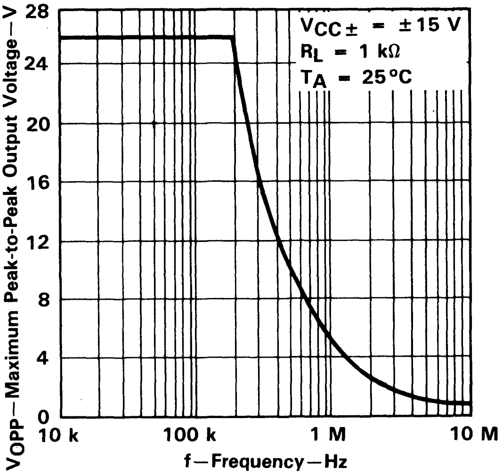


Figure 9

OP27A, OP27E, OP37A, OP37E
LARGE-SIGNAL
DIFFERENTIAL VOLTAGE AMPLIFICATION
vs
TOTAL SUPPLY VOLTAGE

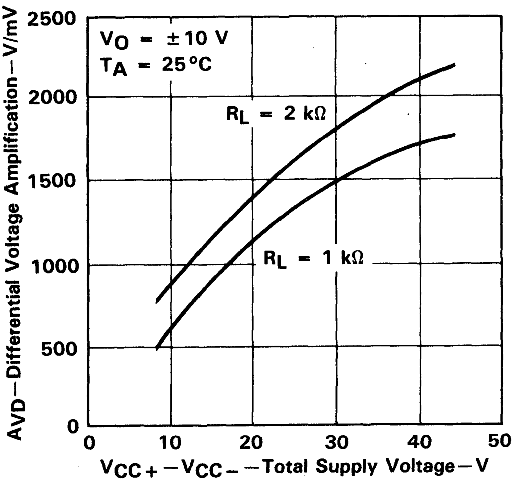


Figure 10

OP27A, OP27E, OP-37A, OP-37E
LARGE-SIGNAL
DIFFERENTIAL VOLTAGE AMPLIFICATION
vs
LOAD RESISTANCE

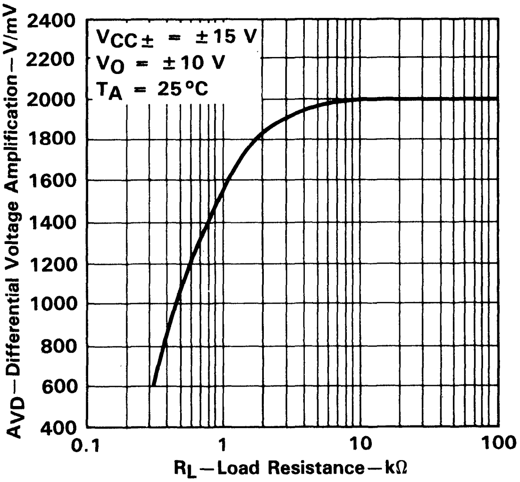


Figure 11

RC4136, RM4136, RV4136
QUAD HIGH-PERFORMANCE OPERATIONAL AMPLIFIERS

D2142, MARCH 1978–REVISED SEPTEMBER 1990

- **Continuous-Short-Circuit Protection**
- **Wide Common-Mode and Differential Voltage Ranges**
- **No Frequency Compensation Required**
- **Low Power Consumption**
- **No Latch-Up**
- **Unity Gain Bandwidth 3 MHz Typical**
- **Gain and Phase Match Between Amplifiers**
- **Designed to Be Interchangeable With Raytheon RC4136, RM4136, and RV4136**
- **Low Noise . . . 8 nV$\sqrt{\text{Hz}}$ Typ at 1 kHz**

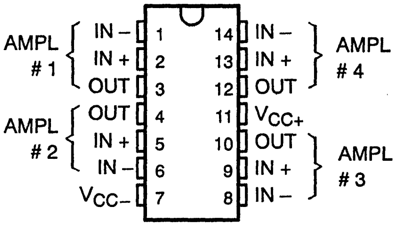
description

The RC4136, RM4136, and RV4136 are quad high-performance operational amplifiers with each amplifier electrically similar to the uA741 except that offset null capability is not provided.

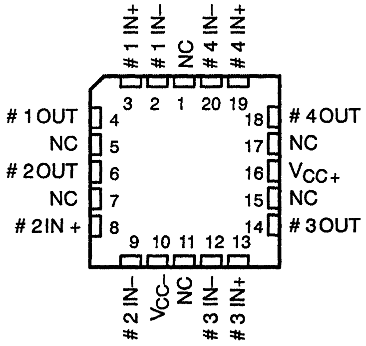
The high common-mode input voltage range and the absence of latch-up make these amplifiers ideal for voltage-follower applications. The devices are short-circuit protected and the internal frequency compensation ensures stability without external components.

The RC4136 is characterized for operation from 0°C to 70°C, the RM4136 is characterized for operation over the full military temperature range of – 55°C to 125°C, and the RV4136 is characterized for operation from – 40°C to 85°C.

RM 4136 . . . J OR W PACKAGE
ALL OTHERS . . . D OR N PACKAGE
(TOP VIEW)

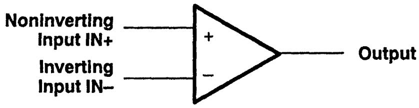


RM4136
FK CHIP CARRIER PACKAGE
(TOP VIEW)



NC–No internal connection

symbol (each amplifier)



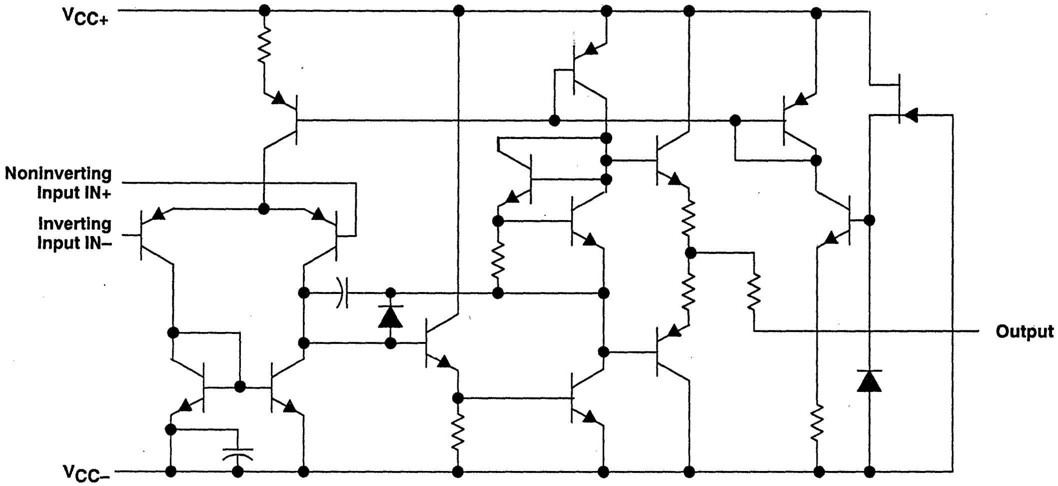
AVAILABLE OPTIONS

T_A	V_{IO} MAX at 25°C	PACKAGE				
		SMALL-OUTLINE (D)	CHIP CARRIER (FK)	CERAMIC DIP (J)	PLASTIC DIP (N)	FLAT (W)
0°C to 70°C	6 mV	RC4136D	—	—	RC4136N	—
– 40°C to 85°C	6 mV	RV4136D	—	—	RV4136N	—
– 55°C to 125°C	4 mV	—	RM4136FK	RM4136J	—	RM4136W

The D packages are available taped and reeled. Add the suffix R to the device type, (e.g., RC4136DR).

On products compliant to MIL-STD-883, Class B, all parameters are tested unless otherwise noted. On all other products, production processing does not necessarily include testing of all parameters.

schematic (each amplifier)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

		RC4136	RM4136	RV4136	UNIT
Supply voltage V_{CC+} (see Note 1)		18	22	18	V
Supply voltage V_{CC-} (see Note 1)		− 18	− 22	− 18	V
Differential input voltage (see Note 2)		± 30	± 30	± 30	V
Input voltage (any input, see Notes 1 and 3)		± 15	± 15	± 15	V
Duration of output short-circuit to ground, one amplifier at a time (see Note 4)		unlimited	unlimited	unlimited	
Continuous total dissipation		See Dissipation Rating Table			
Operating free-air temperature range		0 to 70	− 55 to 125	− 40 to 85	°C
Storage temperature range		− 65 to 150	− 65 to 150	− 65 to 150	°C
Case temperature for 60 seconds	FK package	—	260	—	°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds	J or W package	—	300	—	°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	D or N package	260	—	260	°C

NOTES: 1. All voltage values, unless otherwise noted, are with respect to the midpoint between V_{CC+} and V_{CC-}.
2. Differential voltages are at the noninverting input terminal with respect to the inverting input terminal.
3. The magnitude of the input voltage must never exceed the magnitude of the supply voltage or 15 V, whichever is less.
4. Temperature and/or supply voltages must be limited to ensure that the dissipation rating is not exceeded.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR	DERATE ABOVE T_A	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING	$T_A = 125°C$ POWER RATING
D	800 mW	7.6 mW/°C	45°C	608 mW	494 mW	—
FK	800 mW	11.0 mW/°C	77°C	800 mW	715 mW	275 mW
J	800 mW	11.0 mW/°C	77°C	800 mW	715 mW	275 mW
N	800 mW	9.2 mW/°C	63°C	736 mW	598 mW	—
W	800 mW	8.0 mW/°C	50°C	640 mW	520 mW	200 mW

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC+}	5		15	V
Supply voltage, V_{CC-}	−5		−15	V

electrical characteristics at specified free-air temperature, V_{CC+} = 15 V, V_{CC-} = −15 V

PARAMETER		TEST CONDITIONS†		RC4136			RM4136			RV4136			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_O = 0	25°C		0.5	6		0.5	4		0.5	6	mV
			Full range			7.5			6			7.5	
I_{IO}	Input offset current	V_O = 0	25°C		5	200		5	1.50		5	200	nA
			Full range			300			500			500	
I_{IB}	Input bias current	V_O = 0	25°C		140	500		140	400		140	500	nA
			Full range			800			1500			1500	
V_i	Input voltage range		25°C	±12	±14		±12	±14		±12	±14		V
V_{OM}	Maximum peak output voltage swing	R_L = 10 kΩ	25°C	±12	±14		±12	±14		±12	±14		V
		R_L = 2 kΩ	25°C	±10	±13		±10	±13		±10	±13		
		R_L ≥ 2 kΩ	Full range	±10			±10			±10			
A_{VD}	Large-signal differential voltage amplification	V_O = ± 10V, R_L ≥ 2 kΩ	25°C	20	300		50	350		20	300		V/mV
			Full range	15			25			15			
B_1	Unity-gain bandwith		25°C		3			3.5			3		MHz
r_i	Input resistance		25°C	0.3*	5		0.3*	5		0.3*	5		MΩ
CMRR	Common-mode rejection ratio	V_O = 0, R_S = 50 Ω	25°C	70	90		70	90		70	90		dB
k_{SVS}	Supply voltage sensitivity ($\Delta V_{IO}/\Delta V_{CC}$)	V_{CC} = ± 9 V to ± 15V, V_O = 0	25°C		30	150		30	150		30	150	µV/V
V_n	Equivalent input noise voltage (closed-loop)	A_{VD} = 100, BW = 1 Hz, f = 1 kHz, R_S = 100 Ω	25°C		8			8			8		nV/√Hz
I_{CC}	Supply current (All four amplifiers)	V_O = 0, No load	25°C		5	11.3		5	11.3		5	11.3	mA
			MIN T_A		6	13.7		6	13.3		6	13.7	
			MAX T_A		4.5	10		4.5	10		4.5	10	
P_D	Total power dissipation (All four amplifiers)	V_O = 0, No load	25°C		150	340		150	340		150	340	mW
			MIN T_A		180	400		180	400		180	400	
			MAX T_A		135	300		135	300		135	300	
V_{01}/V_{02}	Crosstalk attenuation	A_{VD} = 100, f = 10 kHz, R_S = 1 kΩ	25°C		105			105			105		dB

* This parameter is not production tested.

† All characteristics are measured under open-loop conditions with zero common-mode input voltage unless otherwise specified. Full range is 0°C to 70°C for RC4136, − 55°C to 125°C for RM4136, and − 40°C to 85°C for RV4136.

operating characteristics, $V_{CC+} = 15$ V, $V_{CC-} = -15$ V, $T_A = 25°C$

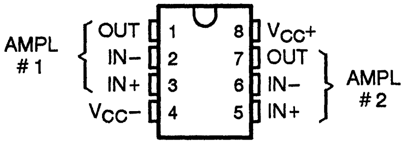
PARAMETER		TEST CONDITIONS		RC4136, RV4136			RM4136			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
t_r	Rise time	$V_I = 20$ mV,	$R_L = 2$ kΩ,		0.13			0.13		µs
	Overshoot factor	$C_L = 100$ pF			5%			5%		
SR	Slew rate at unity gain	$V_I = 10$ V, $C_L = 100$ pF	$R_L = 2$ kΩ,		1.7			1.7		V/µs

RC4558, RM4558, RV4558
DUAL HIGH-PERFORMANCE OPERATIONAL AMPLIFIERS

D2141, MARCH 1976–REVISED AUGUST 1991

- **Continuous-Short-Circuit Protection**
- **Wide Common-Mode and Differential Voltage Ranges**
- **No Frequency Compensation Required**
- **Low Power Consumption**
- **No Latch-Up**
- **Unity Gain Bandwidth 3 MHz Typical**
- **Gain and Phase Match Between Amplifiers**
- **Low Noise . . . 8 nV/√Hz Typ at 1 kHz**
- **Designed to Be Interchangeable With Raytheon RC4558, RM4558, and RV4558**

D, DB, JG, P, OR PW PACKAGE
(TOP VIEW)



description

The RC4558, RM4558, and RV4558 are dual high-performance operational amplifiers with each half electrically similar to the uA741 except that offset null capability is not provided.

The high common-mode input voltage range and the absence of latch-up make these amplifiers ideal for voltage-follower applications. The devices are short-circuit protected and the internal frequency compensation ensures stability without external components.

The RC4558 is characterized for operation from 0°C to 70°C, the RM4558 is characterized for operation over the full military temperature range of −55°C to 125°C, and the RV4558 is characterized for operation from −40°C to 85°C.

AVAILABLE OPTIONS

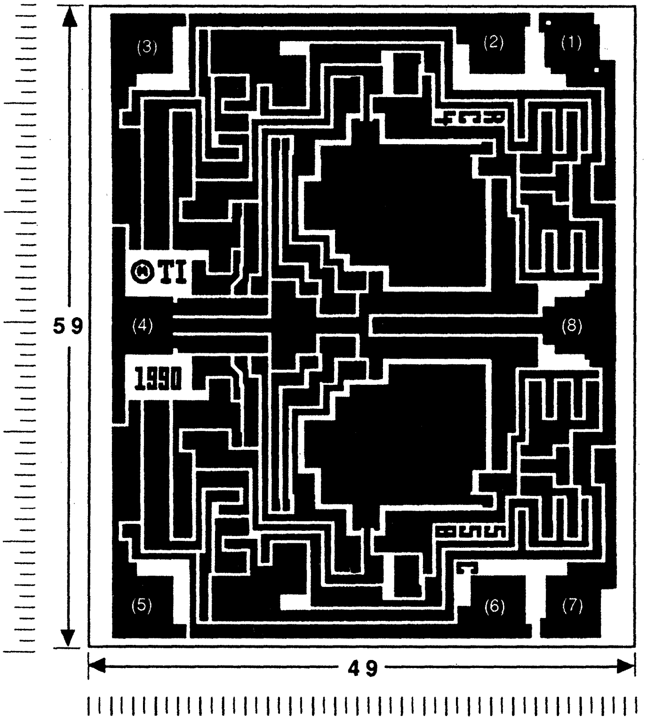
T_A	V_{IO} MAX at 25°C	PACKAGE					
		SMALL-OUTLINE (D)	SSOP (DBLE)	CERAMIC DIP (JG)	PLASTIC DIP (P)	SSOP (PWLE)	CHIP FORM (Y)
0°C to 70°C	6 mV	RC4558D	RC4558DBLE	—	RC4558P	RC4558PWLE	RC4558Y
−40°C to 85°C	6 mV	RV4558D	—	—	RV4558P	—	—
−55°C to 125°C	6 mV	—	—	RM4558JG	—	—	—

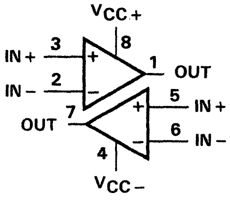
The D package is available taped and reeled. Add the suffix "R" to the device type, (e.g., RC4558DR).
The DB and PW packages are available only left-end taped and reeled.
RC4558Y is tested at 25°C. See page 2–167 for electrical characteristics.

chip information

These chips, properly assembled, display characteristics similar to the RC4558, (see the RC4558Y electrical table). Thermal compression or ultrasonic bonding may be used on the doped aluminum bonding pads. Chips may be mounted with conductive epoxy or a gold-silicon preform.

BONDING PAD ASSIGNMENTS





CHIP THICKNESS: 15 TYPICAL

BONDING PADS: 4 × 4 MINIMUM

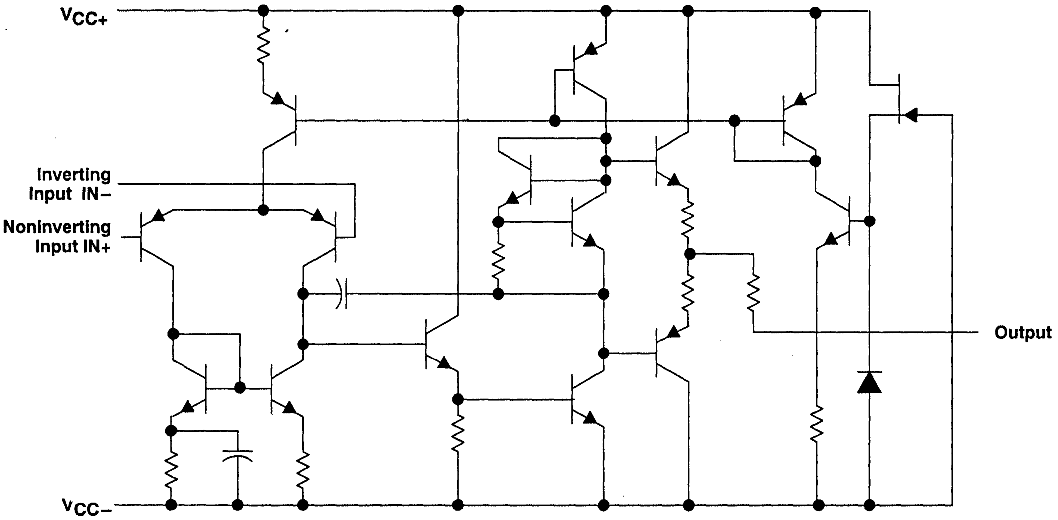
T_J max = 150°C

TOLERANCES ARE ±10%

PIN 4 INTERNALLY CONNECTED TO BACKSIDE OF CHIP

ALL DIMENSIONS ARE IN MILS

schematic (each amplifier)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

	RC4558	RM4558	RV4558	UNIT
Supply voltage V_{CC+} (see Note 1)	18	22	18	V
Supply voltage V_{CC-} (see Note 1)	−18	−22	−18	V
Differential input voltage (see Note 2)	±30	±30	±30	V
Input voltage (any input, see Notes 1 and 3)	±15	±15	±15	V
Duration of output short circuit to ground, one amplifier at a time (see Note 4)	unlimited	unlimited	unlimited	
Continuous total dissipation	See Dissipation Rating Table			
Operating free-air temperature range	0 to 70	−55 to 125	−40 to 85	°C
Storage temperature range	−65 to 150	−65 to 150	−65 to 150	°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: JG package		300		°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D, DB, P, or PW package	260		260	°C

NOTES: 1. All voltage values, unless otherwise noted, are with respect to the midpoint between V_{CC+} and V_{CC-}.
2. Differential voltages are at the noninverting input terminal with respect to the inverting input terminal.
3. The magnitude of the input voltage must never exceed the magnitude of the supply voltage or 15 V, whichever is less.
4. Temperature and/or supply voltages must be limited to ensure that the dissipation rating is not exceeded.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	DERATE ABOVE T_A	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING	$T_A = 125°C$ POWER RATING
D	680 mW	5.8 mW/°C	33°C	464 mW	377 mW	N/A
DB or PW	525 mW	4.2 mW/°C	25°C	336 mW	N/A	N/A
JG	680 mW	8.4 mW/°C	69°C	672 mW	546 mW	210 mW
P	680 mW	8.0 mW/°C	65°C	640 mW	520 mW	N/A

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC+}	5		15	V
Supply voltage, V_{CC-}	−5		−15	V

electrical characteristics at specified free-air temperature, $V_{CC+} = 15$ V, $V_{CC-} = -15$ V

PARAMETER		TEST CONDITIONS†		RC4558			RM4558			RV4558			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	$V_O = 0$	25°C		0.5	6		0.5	5		0.5	6	mV
			Full range			7.5			6			7.5	
I_{IO}	Input offset current	$V_O = 0$	25°C		5	200		5	200		5	200	nA
			Full range			300			500			500	
I_{IB}	Input bias current	$V_O = 0$	25°C		150	500		140	500		140	500	nA
			Full range			800			1500			1500	
V_{ICR}	Common-mode input voltage range		25°C	±12	±14		±12	±14		±12	±14		V
V_{OM}	Maximum output voltage swing	$R_L = 10\ k\Omega$	25°C	±12	±14		±12	±14		±12	±14		V
		$R_L = 2\ k\Omega$	25°C	±10	±13		±10	±13		±10	±13		
		$R_L \geq 2\ k\Omega$	Full range	±10			±10			±10			
A_{VD}	Large-signal differential voltage amplification	$R_L \geq 2\ k\Omega$, $V_O = \pm 10$ V	25°C	20	300		50	350		20	300		V/mV
			Full range	15			25			15			
B_1	Unity-gain bandwith		25°C		3		2	3.5			3		MHz
r_i	Input resistance		25°C	0.3	5		0.3	5		0.3	5		MΩ
CMRR	Common-mode rejection ratio		25°C	70	90		70	90		70	90		dB
k_{SVS}	Supply voltage sensitivity ($\Delta V_{IO}/\Delta V_{CC}$)	$V_{CC} = \pm 15$ V to ±9 V	25°C		30	150		30	150		30	150	μV/V
V_n	Equivalent input noise voltage (closed-loop)	$A_{VD} = 100$, $R_S = 100\ \Omega$, $f = 1$ kHz, BW = 1 Hz	25°C		8			8			8		nV/√Hz
I_{CC}	Supply current (both amplifiers)	No load, $V_O = 0$,	25°C		2.5	5.6		2.5	5.6		2.5	5.6	mA
			MIN T_A		3	6.6		3	6.6		3	6.6	
			MAX T_A		2.3	5		2	5		2.3	5	
P_D	Total power dissipation (both amplifiers)	No load, $V_O = 0$,	25°C		75	170		75	170		75	170	mW
			MIN T_A		90	200		90	200		90	200	
			MAX T_A		70	150		60	150		70	150	
V_{01}/V_{02}	Crosstalk attenuation, Open loop	$R_S = 1\ k\Omega$, $f = 10$ kHz	25°C		85			85			85		dB
	$A_{VD} = 100$		25°C		105			105			105		

† All characteristics are measured under open-loop conditions with zero common-mode input voltage unless otherwise specified. Full range is 0°C to 70°C for RC4558, −55°C to 125°C for RM4558, and −40°C to 85°C for RV4558.

operating characteristics, $V_{CC+} = 15$ V, $V_{CC-} = -15$ V, $T_A = 25°C$

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	
t_r	Rise time	$V_I = 20$ mV, $R_L = 2\ k\Omega$, $C_L = 100$ pF		0.13		ns
	Overshoot			5%		
SR	Slew rate at unity gain	$V_I = 10$ V, $R_L = 2\ k\Omega$, $C_L = 100$ pF	1.1	1.7		V/μs

electrical characteristics, V_{CC+} = 15 V, V_{CC-} = −15 V, T_A = 25°C (unless otherwise noted)

PARAMETER			TEST CONDITIONS†	MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage		$V_O = 0$		0.5	6	mV
I_{IO}	Input offset current		$V_O = 0$		5	200	nA
I_{IB}	Input bias current		$V_O = 0$		150	500	nA
V_{ICR}	Common-mode input voltage range			±12	±14		V
V_{OM}	Maximum output voltage swing		$R_L = 10\ k\Omega$	±12	±14		V
			$R_L = 2\ k\Omega$	±12	±13		
A_{VD}	Large-signal differential voltage amplification		$R_L = 2\ k\Omega$, $V_O = \pm 10$ V	20	300		V/mV
B_1	Unity-gain bandwidth				3		MHz
r_i	Input resistance			0.3	5		MΩ
CMRR	Common-mode rejection ratio			70	90		dB
k_{SVS}	Supply voltage sensitivity ($\Delta V_{IO}/\Delta V_{CC}$)		$V_{CC} = \pm 15$ V to ±9 V		30	150	μV/V
V_n	Equivalent input noise voltage (closed-loop)		$A_{VD} = 100$, $R_S = 100\ \Omega$, f = 1 kHz, BW = 1 Hz		8		$nV/\sqrt{Hz}$
I_{CC}	Supply current (both amplifiers)		No load, $V_O = 0$		2.5	5.6	mA
P_D	Total power dissipation (both amplifiers)		No load, $V_O = 0$		75	170	mW
V_{01}/V_{02}	Crosstalk attentuation	Open loop	$R_S = 1\ k\Omega$, f = 10 kHz		85		dB
		$A_{VD} = 100$			105		

† All characteristics are measured under open-loop conditions with zero common-mode input voltage unless otherwise specified.

operating characteristics, V_{CC+} = 15 V, V_{CC-} = −15 V, T_A = 25°C

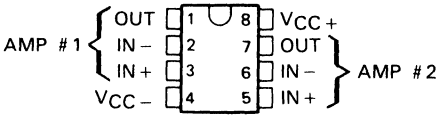
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_r	Rise time	$V_I = 20$ mV, $R_L = 2\ k\Omega$, $C_L = 100$ pF		0.13		ns
	Overshoot			5%		
SR	Slew rate at unity gain	$V_I = 10$ V, $R_L = 2\ k\Omega$, $C_L = 100$ pF	1.1	1.7		V/μs

RC4559
DUAL HIGH-PERFORMANCE OPERATIONAL AMPLIFIER

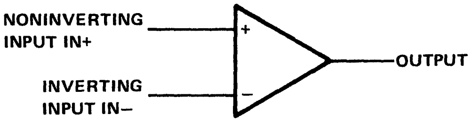
D2785, OCTOBER 1983—REVISED JUNE 1988

- **Matched Gain and Offset Between Amplifiers**
- **Unity-Gain Bandwidth . . . 3 MHz Min**
- **Slew Rate . . . 1.5 V/ns Min**
- **Low Equivalent Input Noise Voltage . . . 2 μV/√Hz Max (20 Hz to 20 kHz)**
- **No Frequency Compensation Required**
- **No Latch Up**
- **Wide Common-Mode Voltage Range**
- **Low Power Consumption**
- **Designed to be Interchangeable with Raytheon RC4559**

D OR P PACKAGE
(TOP VIEW)



symbol (each amplifier)



AVAILABLE OPTIONS

SYMBOLIZATION		OPERATING TEMPERATURE RANGE	V_{IO} MAX at 25°C
DEVICE	PACKAGE SUFFIX		
RC4559	D,P	−0°C to 70°C	6 mV

The D packages are available taped and reeled. Add the suffix R to the device type when ordering. (i.e.,RC4559DR)

description

The RC4559 is a dual high-performance operational amplifier. The high common-mode input voltage and the absence of latch-up make this amplifier ideal for low-noise signal applications such as audio preamplifiers and signal conditioners. This amplifier features a guaranteed dynamic performance and output drive capability that far exceeds that of the general-purpose type amplifiers.

The RC4559 is characterized for operation from 0°C to 70°C.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage V_{CC+} (see Note 1)	18 V
Supply voltage V_{CC-} (see Note 1)	−18 V
Differential input voltage (see Note 2)	±30 V
Input voltage (any input, see Notes 1 and 3)	±15 V
Duration of output short-circuit to ground, one amplifier at a time (see Note 4)	unlimited
Continuous total dissipation	500 mW
Operating free-air temperature range	0°C to 70°C
Storage temperature range	−65°C to 125°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C

NOTES: 1. All voltage values, unless otherwise noted, are with respect to the zero reference level (ground) of the supply voltages where the zero reference level is the midpoint between V_{CC+} and V_{CC-}.
2. Differential voltages are at the noninverting input terminal with respect to the inverting input terminal.
3. The magnitude of the input voltage must never exceed the magnitude of the supply voltage or 15 volts, whichever is less.
4. Temperature and/or supply voltages must be limited to ensure that the dissipation rating is not exceeded.

electrical characteristics at specified free-air temperature, $V_{CC+} = 15$ V, $V_{CC-} = -15$ V

PARAMETER		TEST CONDITIONS†		MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	$V_O = 0$	25°C		2	6	mV
			0°C to 70°C			7.5	
I_{IO}	Input offset current	$V_O = 0$	25°C		5	100	nA
			0°C to 70°C			200	
I_{IB}	Input bias current	$V_O = 0$	25°C		40	250	nA
			0°C to 70°C			500	
V_I	Input voltage range		25°C	±12	±13		V
V_{OM}	Maximum peak output voltage swing	$R_L \geq 3$ kΩ	25°C	±12	±13		V
		$R_L = 600$ Ω	25°C	±9.5	±10		
		$R_L \geq 2$ kΩ	0°C to 70°C	±10			
A_{VD}	Large-signal differential voltage amplification	$V_O = \pm 10$ V, $R_L = 2$ kΩ	25°C	20	300		V/mV
			0°C to 70°C	15			
B_{OM}	Maximum output-swing bandwidth	$V_{OPP} = 20$ V, $R_L = 2$ kΩ	25°C	24	32		kHz
B_1	Unity-gain bandwidth		25°C	3	4		MHz
r_i	Input resistance		25°C	0.3	1		MΩ
CMRR	Common-mode rejection ratio	$V_O = 0$	25°C	80	100		dB
k_{SVS}	Supply voltage sensitivity ($\Delta V_{IO}/\Delta V_{CC}$)	$V_O = 0$	25°C		10	75	µV/V
V_n	Equivalent input noise voltage (closed-loop)	$A_{VD} = 100$, $R_S = 1$ kΩ, f = 20 Hz to 20 kHz	25°C		1.4	2	µV
I_n	Equivalent input noise current	f = 20 Hz to 20 kHz	25°C		25		pA
I_{CC}	Supply current (both amplifiers)	No load, No signal	25°C		3.3	5.6	mA
			0°C		4	6.6	
			70°C		3	5	
V_{o1}/V_{o2}	Crosstalk attenuation	$A_{VD} = 100$, $R_S = 1$ kΩ, f = 10 kHz	25°C		90		dB
			25°C		90		

†All characteristics are specified under open-loop operation, unless otherwise noted.

matching characteristics at $V_{CC+} = 15$ V, $V_{CC-} = -15$ V, $T_A = 25$°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	$V_O = 0$		±0.2		mV
I_{IO}	Input offset current	$V_O = 0$		±7.5		nA
I_{IB}	Input bias current	$V_O = 0$		±15		nA
A_{VD}	Large-signal differential voltage amplification	$V_O = \pm 10$ V, $R_L = 2$ kΩ		±1		dB

operating characteristics, $V_{CC+} = 15$ V, $V_{CC-} = -15$ V, $T_A = 25$°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_r	Rise time	$V_I = 20$ mV, $R_L = 2$ kΩ,		80		µs
	Overshoot	$C_L = 100$ pF		18%		
SR	Slew rate at unity gain	$V_I = 10$ V, $R_L = 2$ kΩ, $C_L = 100$ pF	1.5	2		V/µs

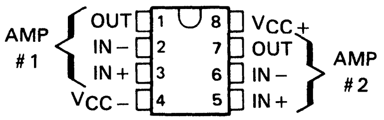
TL022C, TL022M
DUAL LOW-POWER OPERATIONAL AMPLIFIERS

D1661, SEPTEMBER 1973–REVISED SEPTEMBER 1990

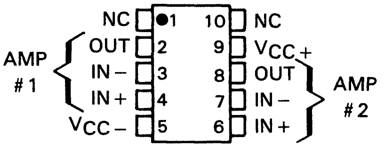
- Very Low Power Consumption
- Power Dissipation with ±2-V Supplies . . . 170 μW Typ
- Low Input Bias and Offset Currents
- Output Short-Circuit Protection
- Low Input Offset Voltage
- Internal Frequency Compensation
- Latch-Up-Free Operation
- Popular Dual Op Amp Pinout

TL022M IS NOT RECOMMENDED FOR NEW DESIGNS

TL022M . . . JG PACKAGE
TL022C . . . D OR P PACKAGE
(TOP VIEW)



TL022M . . . U FLAT PACKAGE
(TOP VIEW)



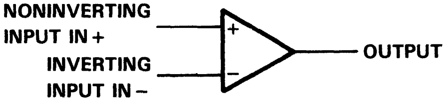
NC—No internal connection

description

The TL022 is a dual low-power operational amplifier designed to replace higher power devices in many applications without sacrificing system performance. High input impedance, low supply currents, and low equivalent input noise voltage over a wide range of operating supply voltages result in an extremely versatile operational amplifier for use in a variety of analog applications including battery-operated circuits. Internal frequency compensation, absence of latch-up, high slew rate, and output short-circuit protection assure ease of use.

The TL022C is characterized for operation from 0°C to 70°C. The TL022M is characterized for operation over the full military temperature range of −55°C to 125°C.

symbol (each amplifier)



AVAILABLE OPTIONS

T_A	V_{IO} MAX AT 25°C	PACKAGE			
		SMALL OUTLINE (D)	CERAMIC DIP (JG)	PLASTIC DIP (P)	CERAMIC FLAT PACK (U)
0°C to 70°C	5 mV	TL022CD	—	TL022CP	—
−55°C to 125°C	5 mV	—	TL022MJG	—	TL022MU

The D package is available taped and reeled. Add the suffix R to the device type, (i.e. TL022CDR).

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

		TL022C	TL022M	UNIT
Supply voltage V_{CC+} (see Note 1)		18	22	V
Supply voltage V_{CC-} (see Note 1)		−18	−22	V
Differential input voltage (see Note 2)		±30	±30	V
Input voltage (any input, see Notes 1 and 3)		±15	±15	V
Duration of output short-circuit (see Note 4)		unlimited	unlimited	
Continuous total dissipation		See Dissipation Rating Table		
Operating free-air temperature range		0 to 70	−55 to 125	°C
Storage temperature range		−65 to 150	−65 to 150	°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds	JG or U package		300	°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	D or P package	260		°C

NOTES: 1. All voltage values, unless otherwise noted, are with respect to the midpoint between V_{CC+} and V_{CC-}.
2. Differential voltages are at the noninverting input terminal with respect to the inverting input terminal.
3. The magnitude of the input voltage must never exceed the magnitude of the supply voltage or 15 V, whichever is less.
4. The output may be shorted to ground or either power supply. For the TL022M only, the unlimited duration of the short-circuit applies at (or below) 125°C case temperature or 75°C free-air temperature.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR	DERATE ABOVE T_A	$T_A = 70°C$ POWER RATING	$T_A = 125°C$ POWER RATING
D	680 mW	5.8 mW/°C	33°C	464 mW	–
JG	680 mW	8.4 mW/°C	69°C	672 mW	210 mW
P	680 mW	8.0 mW/°C	65°C	640 mW	–
U	675 mW	5.4 mW/°C	25°C	432 mW	135 mW

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC+}	5		15	V
Supply voltage, V_{CC-}	−5		−15	V

electrical characteristics at specified free-air temperature, V_{CC+} = 15 V, V_{CC-} = −15 V

PARAMETER		TEST CONDITIONS†		TL022C			TL022M			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_O = 0, R_S = 50 Ω	25°C		1	5		1	5	mV
			Full range			7.5			6	
I_{IO}	Input offset current	V_O = 0	25°C		15	80		5	40	nA
			Full range			200			100	
I_{IB}	Input bias current	V_O = 0	25°C		100	250		50	100	nA
			Full range			400			250	
V_{ICR}	Common-mode input voltage range		25°C	±12	±13		±12	±13		V
			Full range	±12			±12			
V_{OPP}	Maximum peak-to-peak output voltage swing	R_L = 10 kΩ	25°C	20	26		20	26		V
		R_L ≥ 10 kΩ	Full range	20			20			
A_{VD}	Large-signal differential voltage amplication	R_L ≥ 10 kΩ, V_O = ±10 V	25°C	60	80		72	86		dB
			Full range	60			66			
B_1	Unity-gain bandwidth		25°C		0.5			0.5		MHz
CMRR	Common-mode rejection ratio	V_{IC} = V_{ICR} min, R_S = 50 Ω	25°C	60	72		60	72		dB
			Full range	60			60			
k_{SVS}	Supply voltage sensitivity ($\Delta V_{IO}/\Delta V_{CC}$)	V_{CC} = ±9 V to ±15 V, R_S = 50 Ω	25°C		30	200		30	150	µV/V
			Full range			200			150	
V_n	Equivalent input noise voltage	A_{VD} = 20 dB, B = 1 Hz, f = 1 kHz	25°C		50			50		nV/√Hz
I_{OS}	Short-circuit output current		25°C		±6			±6		mA
I_{CC}	Supply current (both amplifiers)	No load, V_O = 0	25°C		130	250		130	250	µA
			Full range			250			250	
P_D	Total dissipation (both amplifiers)	No load, V_O = 0	25°C		3.9	7.5		3.9	6	mW
			Full range			7.5			6	

† All characteristics are measured under open-loop conditions with zero common-mode input voltage unless otherwise specified. Full range for TL022C is 0°C to 70°C and for TL022M is −55°C to 125°C.

operating characteristics, V_{CC+} = 15 V, V_{CC-} = −15 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_r	Rise time	V_I = 20 mV, R_L = 10 kΩ, C_L = 100 pF, See Figure 1		0.3		µs
	Overshoot factor			5%		
SR	Slew rate at unity gain	V_I = 10 V, R_L = 10 kΩ, C_L = 100 pF, See Figure 1		0.5		V/µs

PARAMETER MEASUREMENT INFORMATION

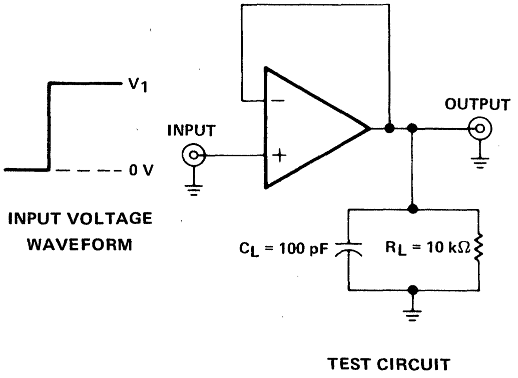


FIGURE 1. RISE TIME, OVERSHOOT FACTOR, AND SLEW RATE

TYPICAL CHARACTERISTICS

TOTAL POWER DISSIPATED
vs
SUPPLY VOLTAGE

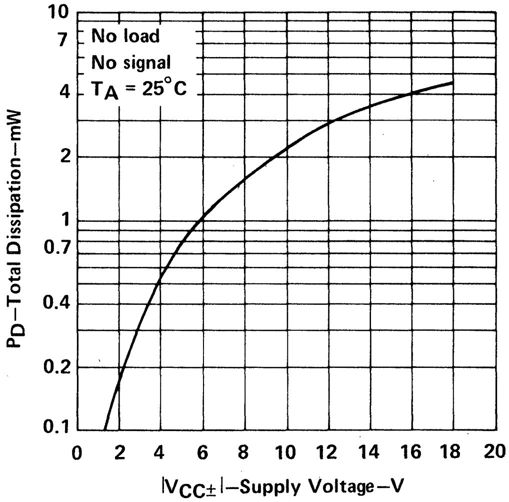
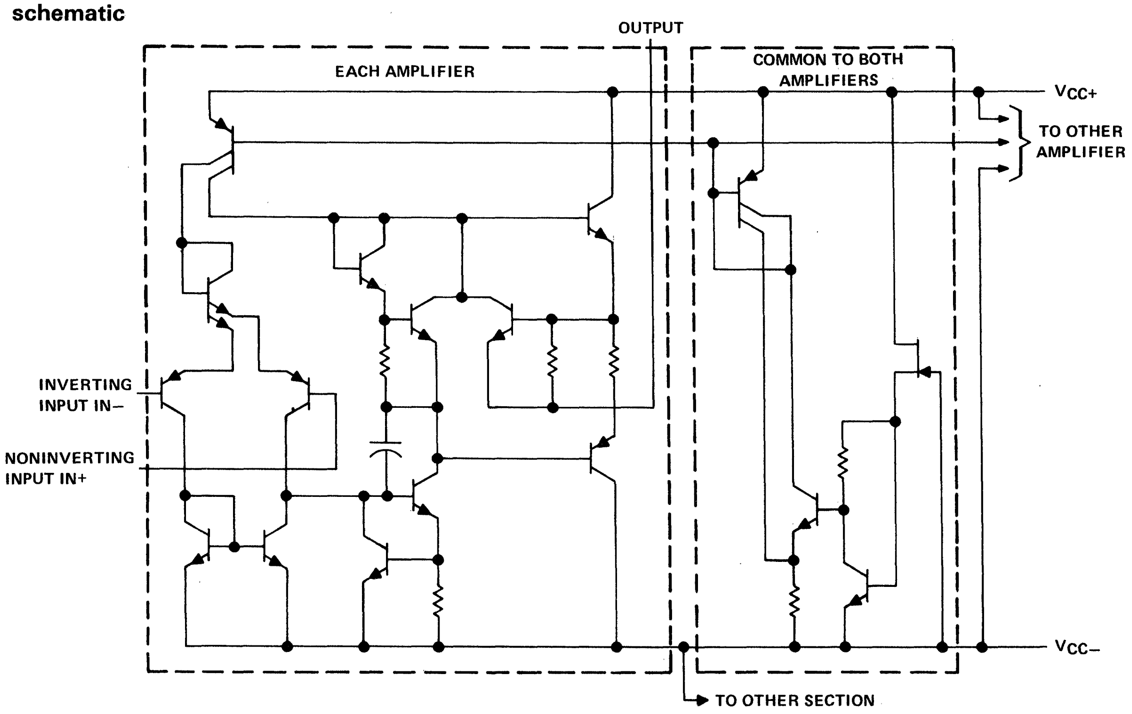


FIGURE 2

schematic

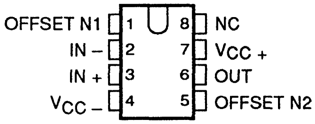


TL031, TL031A
ENHANCED JFET LOW-POWER LOW-OFFSET OPERATIONAL AMPLIFIERS

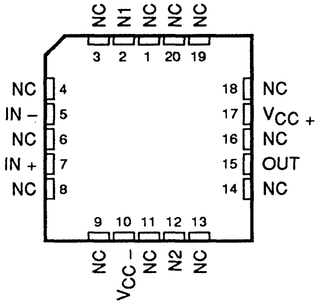
D3151, JULY 1988 – REVISED FEBRUARY 1991

- **Maximum Offset Voltage . . . 800 µV**
- **High Slew Rate . . . 2.9 V/µs Typ**
- **Low Input Bias Current . . . 2 pA Typ**
- **Very Low Power Consumption . . . 6.5 mW Typ**
- **Output Short-Circuit Protection**

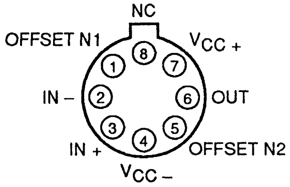
D, JG, or P PACKAGE
(TOP VIEW)



FK PACKAGE
(TOP VIEW)



L PACKAGE
(TOP VIEW)



Pin 4 (L Package) is in electrical contact with the case

NC – No internal connection

description

The TL031 and TL031A operational amplifiers incorporate well-matched, high-voltage JFET and bipolar transistors in a monolithic integrated circuit. These devices offer the significant advantages of Texas Instruments new enhanced JFET process. This process affords not only low initial offset voltage due to the on-chip zener trim capability but also stable offset voltage over time and temperature. In comparison, traditional JFET processes are plagued by significant offset voltage drift.

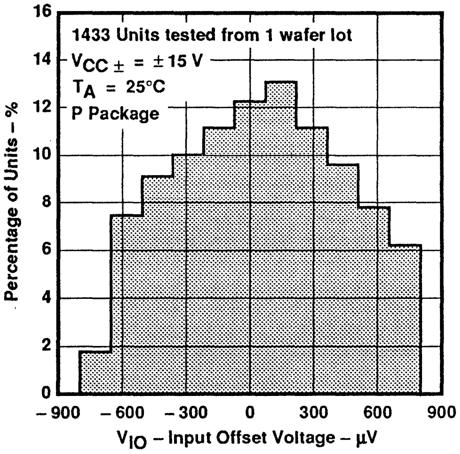
This new enhanced process still maintains the traditional JFET advantages of fast slew rates and low input bias and offset currents. These advantages, coupled with low power consumption, make the TL031 well-suited for new state-of-the-art designs as well as existing design upgrades. The TL031 has been designed to be functionally compatible and pin compatible with the TL061.

AVAILABLE OPTIONS

T_A	V_{IO} max AT 25°C	PACKAGE				
		SMALL-OUTLINE (D)	CHIP CARRIER (FK)	CERAMIC DIP (JG)	METAL CAN (L)	PLASTIC DIP (P)
0°C to 70°C	0.8 mV	TL031ACD	—	—	—	TL031ACP
	1.5 mV	TL031CD	—	—	—	TL031CP
– 40°C to 85°C	0.8 mV	TL031AID	—	—	—	TL031AIP
	1.5 mV	TL031ID	—	—	—	TL031IP
– 55°C to 125°C	0.8 mV	TL031AMD	TL031AMFK	TL031AMJG	TL031AML	TL031AMP
	1.5 mV	TL031MD	TL031MFK	TL031MJG	TL031ML	TL031MP

D packages are available taped and reeled. Add "R" suffix to device type (e.g., TL031CDR).

DISTRIBUTION OF TL031A
INPUT OFFSET VOLTAGE



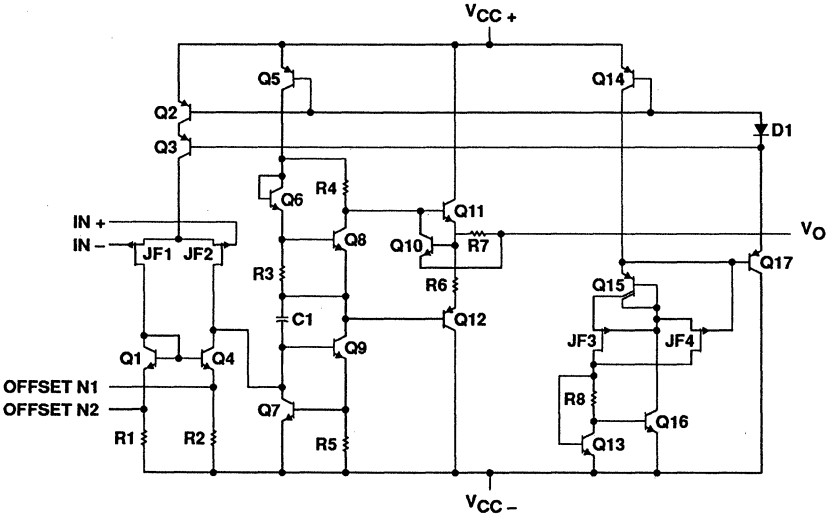
description (continued)

Two offset voltage grades are available: TL031 (1.5 mV max) and TL031A (800 µV max).

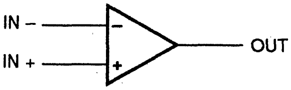
A variety of available packaging options includes small-outline and chip carrier versions for high density system applications.

The C-suffix devices are characterized for operation from 0°C to 70°C. The I-suffix devices are characterized for operation from – 40°C to 85°C. The M-suffix devices are characterized for operation over the full military temperature range of – 55°C to 125°C.

equivalent schematic



symbol (each amplifier)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC+} (see Note 1)	18 V
Supply voltage, V_{CC-} (see Note 1)	– 18 V
Differential input voltage (see Note 2)	± 30 V
Input voltage range, V_I (any input, see Notes 1 and 3)	± 15 V
Input current, I_I (each input)	± 1 mA
Output current, I_O	± 40 mA
Total current into V_{CC+} terminal	160 mA
Total current out of V_{CC-} terminal	160 mA
Duration of short-circuit current at (or below) 25°C (see Note 4)	unlimited
Continuous total dissipation	See Dissipation Rating Table
Operating free-air temperature range, T_A: C-suffix	0°C to 70°C
I-suffix	– 40°C to 85°C
M-suffix	– 55°C to 125°C
Storage temperature range	– 65°C to 150°C
Case temperature for 60 seconds: FK package	260°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D or P package	260°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: JG or L package	300°C

NOTES: 1. All voltage values, except differential voltages, are with respect to the midpoint between V_{CC+} and V_{CC-}.
2. Differential voltages are at the noninverting input with respect to the inverting input.
3. The magnitude of the input voltage must never exceed the magnitude of the supply voltage or 15 V, whichever is less.
4. The output may be shorted to either supply. Temperature and/or supply voltages must be limited to ensure that the maximum dissipation rating is not exceeded.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING	$T_A = 125°C$ POWER RATING
D	725 mW	5.8 mW/°C	464 mW	377 mW	145 mW
FK	1375 mW	11.0 mW/°C	880 mW	715 mW	275 mW
JG	1050 mW	8.4 mW/°C	672 mW	546 mW	210 mW
L	825 mW	6.6 mW/°C	528 mW	429 mW	165 mW
P	1000 mW	8.0 mW/°C	640 mW	520 mW	200 mW

recommended operating conditions

		C-SUFFIX			I-SUFFIX			M-SUFFIX			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		± 5		± 15	± 5		± 15	± 5		± 15	V
Common-mode input voltage, V_{IC}	$V_{CC\pm} = \pm 5$ V	– 1.5		4	– 1.5		4	– 1.5		4	V
	$V_{CC\pm} = \pm 15$ V	– 11.5		14	– 11.5		14	– 11.5		14	
Operating free-air temperature, T_A		0		70	– 40		85	– 55		125	°C

electrical characteristics

PARAMETER		TEST CONDITIONS		T_A†	$V_{CC\pm}$ = ±5 V			$V_{CC\pm}$ = ±15 V			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_O = 0, V_{IC} = 0, R_S = 50 Ω	TL031C	25°C		0.54	3.5		0.5	1.5	mV
				Full range			4.5			2.5	
			TL031AC	25°C		0.41	2.8		0.34	0.8	
				Full range			3.8			1.8	
α_{VIO}	Temperature coefficient of input offset voltage (see Note 7)		TL031C	25°C to 70°C		7.1			5.9		µV/°C
			TL031AC	25°C to 70°C		7.1			5.9	25	
	Input offset voltage long-term drift (see Note 5)			25°C		0.04			0.04		µV/mo
I_{IO}	Input offset current	V_O = 0, V_{IC} = 0, See Figure 5		25°C		1	100		1	100	pA
				70°C		9	200		12	200	
I_{IB}	Input bias current	V_O = 0, V_{IC} = 0, See Figure 5		25°C		2	200		2	200	pA
				70°C		50	400		80	400	
V_{ICR}	Common-mode input voltage range			25°C	−1.5 to 4	−3.4 to 5.4		−11.5 to 14	−13.4 to 15.4		V
				Full range	−1.5 to 4			−11.5 to 14			
V_{OM+}	Maximum positive peak output voltage swing	R_L = 10 kΩ		25°C	3	4.3		13	14		V
				0°C	3	4.2		13	14		
				70°C	3	4.3		13	14		
V_{OM-}	Maximum negative peak output voltage swing	R_L = 10 kΩ		25°C	−3	−4.2		−12.5	−13.9		V
				0°C	−3	−4.1		−12.5	−13.9		
				70°C	−3	−4.2		−12.5	−14		
A_{VD}	Large-signal differential voltage amplification	R_L = 10 kΩ, See Note 6		25°C	4	12		5	14.3		V/mV
				0°C	3	11.1		4	13.5		
				70°C	4	13.3		5	15.2		
r_i	Input resistance			25°C		10^{12}			10^{12}		Ω
C_i	Input capacitance			25°C		5			4		pF
CMRR	Common-mode rejection ratio	V_{IC} = V_{ICR} min, V_O = 0, R_S = 50 Ω		25°C	70	87		75	94		dB
				0°C	70	87		75	94		
				70°C	70	87		75	94		
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm} / \Delta V_{IO}$)	$V_{CC\pm}$ = ±5 V to ±15 V, V_O = 0, R_S = 50 Ω		25°C	75	96		75	96		dB
				0°C	75	96		75	96		
				70°C	75	96		75	96		
P_D	Total power dissipation	No load, V_O = 0		25°C		1.9	2.5		6.5	8.4	mW
				0°C		1.8	2.5		6.3	8.4	
				70°C		1.9	2.5		6.3	8.4	
I_{CC}	Supply current	No load, V_O = 0		25°C		192	250		217	280	µA
				0°C		184	250		211	280	
				70°C		189	250		210	280	

† Full range is 0°C to 70°C.

NOTES: 5. Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at T_A = 150°C extrapolated to T_A = 25°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

6. At $V_{CC\pm}$ = ±5 V, V_O = ±2.3 V; at $V_{CC\pm}$ = ±15 V, V_O = ±10 V.

7. This parameter is tested on a sample basis for the TL031A. For other test requirements, please contact the factory. This statement has no bearing on testing or nontesting of other parameters.

operating characteristics

PARAMETER			TEST CONDITIONS		T_A	$V_{CC\pm} = \pm5$ V			$V_{CC\pm} = \pm15$ V			UNIT
						MIN	TYP	MAX	MIN	TYP	MAX	
SR +	Positive slew rate at unity gain		R_L = 10 kΩ, C_L = 100 pF, See Figure 1, See Note 8		25°C		2.0		2	2.9		V/μs
					0°C		1.8		1.5	2.6		
					70°C		2.2		2	3.2		
SR −	Negative slew rate at unity gain				25°C		3.9		3.5	5.1		V/μs
					0°C		3.7		3.2	5.0		
					70°C		4.0		3.2	5.0		
t_r	Rise time		V_{IPP} = ± 10 mV, R_L = 10 kΩ, C_L = 100 pF, See Figures 1 and 2		25°C		138			132		ns
					0°C		134			127		
					70°C		150			142		
t_f	Fall time				25°C		138			132		ns
					0°C		134			127		
					70°C		150			142		
	Overshoot factor				25°C		11%			5%		
					0°C		10%			4%		
					70°C		12%			6%		
V_n	Equivalent input noise voltage (see Note 9)	TL031C	R_S = 100 Ω, See Figure 3	f = 10 Hz	25°C		61			61		nV/√Hz
				f = 1 kHz			41			41		
		TL031AC		f = 10 Hz	25°C		61			61		
				f = 1 kHz			41			41	60	
I_n	Equivalent input noise current		f = 1 kHz		25°C		0.003			0.003		pA/√Hz
B1	Unity-gain bandwidth		V_i = 10 mV, R_L = 10 kΩ, C_L = 25 pF, See Figure 4		25°C		1			1.1		MHz
					0°C		1			1.1		
					70°C		1			1		
ϕ_m	Phase margin at unity gain		V_i = 10 mV, R_L = 10 kΩ, C_L = 25 pF, See Figure 4		25°C		61°			65°		
					0°C		61°			65°		
					70°C		60°			64°		

NOTES: 8. For $V_{CC\pm} = \pm5$ V, $V_{IPP} = \pm1$ V; for $V_{CC\pm} = \pm15$ V, $V_{IPP} = \pm5$ V.

9. This parameter is tested on a sample basis. For other test requirements, please contact the factory. This statement has no bearing on testing or nontesting of other parameters.

electrical characteristics

PARAMETER		TEST CONDITIONS		T_A†	$V_{CC\pm}$ = ±5 V			$V_{CC\pm}$ = ±15 V			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_O = 0, V_{IC} = 0, R_S = 50 Ω	TL031I	25°C		0.54	3.5		0.5	1.5	mV
				Full range			5.3			3.3	
			TL031AI	25°C		0.41	2.8		0.34	0.8	
				Full range			4.6			2.6	
α_{VIO}	Temperature coefficient of input offset voltage (see Note 7)		TL031I	25°C to 85°C		6.5			6.2		µV/°C
			TL031AI	25°C to 85°C		6.5			6.2	25	
	Input offset voltage long-term drift (see Note 5)			25°C		0.04			0.04		µV/mo
I_{IO}	Input offset current	V_O = 0, V_{IC} = 0, See Figure 5		25°C		1	100		1	100	pA
				85°C		0.02	0.45		0.02	0.45	nA
I_{IB}	Input bias current	V_O = 0, V_{IC} = 0, See Figure 5		25°C		2	200		2	200	pA
				85°C		0.2	0.9		0.2	0.9	nA
V_{ICR}	Common-mode input voltage range			25°C	− 1.5 to 4	− 3.4 to 5.4		− 11.5 to 14	− 13.4 to 15.4		V
				Full range	− 1.5 to 4			− 11.5 to 14			
V_{OM+}	Maximum positive peak output voltage swing	R_L = 10 kΩ		25°C	3	4.3		13	14		V
				− 40°C	3	4.1		13	14		
				85°C	3	4.4		13	14		
V_{OM-}	Maximum negative peak output voltage swing	R_L = 10 kΩ		25°C	− 3	− 4.2		− 12.5	− 13.9		V
				− 40°C	− 3	− 4.1		− 12.5	− 13.8		
				85°C	− 3	− 4.2		− 12.5	− 14		
A_{VD}	Large-signal differential voltage amplification	R_L = 10 kΩ, See Note 6		25°C	4	12		5	14.3		V/mV
				− 40°C	3	8.4		4	11.6		
				85°C	4	13.5		5	15.3		
r_i	Input resistance			25°C		10^{12}			10^{12}		Ω
C_i	Input capacitance			25°C		5			4		pF
CMRR	Common-mode rejection ratio	V_{IC} = V_{ICR} min, V_O = 0, R_S = 50 Ω		25°C	70	87		75	94		dB
				− 40°C	70	87		75	94		
				85°C	70	87		75	94		
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm} / \Delta V_{IO}$)	$V_{CC\pm}$ = ±5 V to ±15 V, V_O = 0, R_S = 50 Ω		25°C	75	96		75	96		dB
				− 40°C	75	96		75	96		
				85°C	75	96		75	96		
P_D	Total power dissipation	No load, V_O = 0		25°C		1.9	2.5		6.5	8.4	mW
				− 40°C		1.4	2.5		5.4	8.4	
				85°C		1.9	2.5		6.2	8.4	
I_{CC}	Supply current	No load, V_O = 0		25°C		192	250		217	280	µA
				− 40°C		144	250		181	280	
				85°C		189	250		207	280	

† Full range is − 40°C to 85°C.

NOTES: 5. Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at T_A = 150°C extrapolated to T_A = 25°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

6. At $V_{CC\pm}$ = ±5 V, V_O = ±2.3 V; at $V_{CC\pm}$ = ±15 V, V_O = ±10 V.
7. This parameter is tested on a sample basis for the TL031A. For other test requirements, please contact the factory. This statement has no bearing on testing or nontesting of other parameters.

operating characteristics

PARAMETER			TEST CONDITIONS		T_A	$V_{CC\pm} = \pm 5$ V			$V_{CC\pm} = \pm 15$ V			UNIT
						MIN	TYP	MAX	MIN	TYP	MAX	
SR +	Positive slew rate at unity gain		R_L = 10 kΩ, C_L = 100 pF, See Figure 1, See Note 8		25°C		2.0		2	2.9		V/µs
					−40°C		1.6		1.5	2.1		
					85°C		2.3		2	3.3		
SR −	Negative slew rate at unity gain				25°C		3.9		3.5	5.1		V/µs
					−40°C		3.3		3.2	4.8		
					85°C		4.1		3.2	4.9		
t_r	Rise time		V_{IPP} = ±10 mV, R_L = 10 kΩ, C_L = 100 pF, See Figures 1 and 2		25°C		138			132		ns
					−40°C		132			123		
					85°C		154			146		
t_f	Fall time				25°C		138			132		ns
					−40°C		132			123		
					85°C		154			146		
	Overshoot factor				25°C		11%			5%		
					−40°C		12%			5%		
					85°C		13%			7%		
V_n	Equivalent input noise voltage (see Note 9)	TL031I	R_S = 100 Ω, See Figure 3	f = 10 Hz	25°C		61			61		nV/√Hz
				f = 1 kHz			41			41		
		TL031AI		f = 10 Hz	25°C		61			61		
				f = 1 kHz			41			41	60	
I_n	Equivalent input noise current		f = 1 kHz		25°C		0.003			0.003		pA/√Hz
B1	Unity-gain bandwidth		V_i = 10 mV, R_L = 10 kΩ, C_L = 25 pF, See Figure 4		25°C		1			1.1		MHz
					−40°C		1			1.1		
					85°C		0.9			1		
ϕ_m	Phase margin at unity gain		V_i = 10 mV, R_L = 10 kΩ, C_L = 25 pF, See Figure 4		25°C		61°			65°		
					−40°C		60°			65°		
					85°C		60°			64°		

NOTES: 8. For $V_{CC\pm} = \pm 5$ V, $V_{IPP} = \pm 1$ V; for $V_{CC\pm} = \pm 15$ V, $V_{IPP} = \pm 5$ V.

9. This parameter is tested on a sample basis. For other test requirements, please contact the factory. This statement has no bearing on testing or nontesting of other parameters.

electrical characteristics

PARAMETER		TEST CONDITIONS		T_A[†]	$V_{CC\pm} = \pm 5$ V			$V_{CC\pm} = \pm 15$ V			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	$V_O = 0$, $V_{IC} = 0$, $R_S = 50\ \Omega$	TL031M	25°C		0.54	3.5		0.5	1.5	mV
				Full range			6.5			4.5	
			TL031AM	25°C		0.41	2.8		0.34	0.8	
				Full range			5.8			3.8	
α_{VIO}	Temperature coefficient of input offset voltage		TL031M	25°C to 125°C		5.1			4.3		µV/°C
			TL031AM	25°C to 125°C		5.1			4.3		
	Input offset voltage long-term drift (see Note 5)			25°C		0.04			0.04		µV/mo
I_{IO}	Input offset current	$V_O = 0$, $V_{IC} = 0$, See Figure 5		25°C		1	100		1	100	pA
				125°C		0.2	10		0.2	10	nA
I_{IB}	Input bias current	$V_O = 0$, $V_{IC} = 0$, See Figure 5		25°C		2	200		2	200	pA
				125°C		7	20		8	20	nA
V_{ICR}	Common-mode input voltage range			25°C	−1.5 to 4	−3.4 to 5.4		−11.5 to 14	−13.4 to 15.4		V
				Full range	−1.5 to 4			−11.5 to 14			
V_{OM+}	Maximum positive peak output voltage swing	$R_L = 10\ k\Omega$		25°C	3	4.3		13	14		V
				−55°C	3	4.1		13	14		
				125°C	3	4.4		13	14		
V_{OM-}	Maximum negative peak output voltage swing	$R_L = 10\ k\Omega$		25°C	−3	−4.2		−12.5	−13.9		V
				−55°C	−3	−4		−12.5	−13.8		
				125°C	−3	−4.3		−12.5	−14		
A_{VD}	Large-signal differential voltage amplification	$R_L = 10\ k\Omega$, See Note 6		25°C	4	12		5	14.3		V/mV
				−55°C	3	7.1		4	10.4		
				125°C	3	12.9		4	15		
r_i	Input resistance			25°C		10^{12}			10^{12}		Ω
C_i	Input capacitance			25°C		5			4		pF
CMRR	Common-mode rejection ratio	$V_{IC} = V_{ICR}$ min, $V_O = 0$, $R_S = 50\ \Omega$		25°C	70	87		75	94		dB
				−55°C	70	87		70	94		
				125°C	70	87		70	94		
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm} / \Delta V_{IO}$)	$V_{CC\pm} = \pm 5$ V to ± 15 V, $V_O = 0$, $R_S = 50\ \Omega$		25°C	75	96		75	96		dB
				−55°C	75	95		75	95		
				125°C	75	96		75	96		
P_D	Total power dissipation	No load, $V_O = 0$		25°C		1.9	2.5		6.5	8.4	mW
				−55°C		1.1	2.5		4.7	8.4	
				125°C		1.8	2.5		5.8	8.4	
I_{CC}	Supply current	No load, $V_O = 0$		25°C		192	250		217	280	µA
				−55°C		114	250		156	280	
				125°C		178	250		197	280	

[†] Full range is − 55°C to 125°C.

NOTES: 5. Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at $T_A = 150°C$ extrapolated to $T_A = 25°C$ using the Arrhenius equation and assuming an activation energy of 0.96 eV.

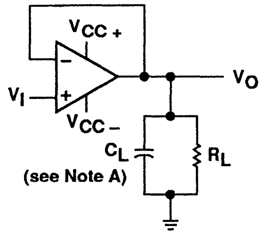
6. At $V_{CC\pm} = \pm 5$ V, $V_O = \pm 2.3$ V; at $V_{CC\pm} = \pm 15$ V, $V_O = \pm 10$ V.

operating characteristics

PARAMETER			TEST CONDITIONS		T_A	$V_{CC\pm} = \pm5$ V MIN	TYP	MAX	$V_{CC\pm} = \pm15$ V MIN	TYP	MAX	UNIT
SR +	Positive slew rate at unity gain		R_L = 10 kΩ, C_L = 100 pF, See Figure 1, See Note 8		25°C		2.0		2	2.9		V/µs
					– 55°C		1.4		1.2	1.9		
					125°C		2.4		1.2	3.5		
SR –	Negative slew rate at unity gain				25°C		3.9		3	5.1		V/µs
					– 55°C		3.2		2.5	4.6		
					125°C		4.1		2.5	4.7		
t_r	Rise time		V_{IPP} = ± 10 mV, R_L = 10 kΩ, C_L = 100 pF, See Figures 1 and 2		25°C		138			132		ns
					– 55°C		142			123		
					125°C		166			158		
t_f	Fall time				25°C		138			132		ns
					– 55°C		142			123		
					125°C		166			158		
	Overshoot factor				25°C		11%			5%		
					– 55°C		16%			6%		
					125°C		14%			8%		
V_n	Equivalent input noise voltage	TL031M	R_S = 100 Ω, See Figure 3	f = 10 Hz	25°C		61			61		nV/√Hz
				f = 1 kHz			41			41		
		TL031AM		f = 10 Hz	25°C		61			61		
				f = 1 kHz			41			41		
I_n	Equivalent input noise current		f = 1 kHz		25°C		0.003			0.003		pA/√Hz
B1	Unity-gain bandwidth		V_I = 10 mV, R_L = 10 kΩ, C_L = 25 pF, See Figure 4		25°C		1			1.1		MHz
					– 55°C		1			1.1		
					125°C		0.9			0.9		
ϕ_m	Phase margin at unity gain		V_I = 10 mV, R_L = 10 kΩ, C_L = 25 pF, See Figure 4		25°C		61°			65°		
					– 55°C		57°			64°		
					125°C		59°			62°		

NOTE 8: For $V_{CC\pm} = \pm5$ V, $V_{IPP} = \pm1$ V; for $V_{CC\pm} = \pm15$ V, $V_{IPP} = \pm5$ V.

PARAMETER MEASUREMENT INFORMATION



NOTE A: C_L includes fixture capacitance.

Figure 1. Slew Rate, Rise/Fall Time, and Overshoot Test Circuit

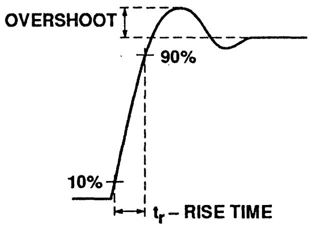


Figure 2. Rise Time and Overshoot Waveform

PARAMETER MEASUREMENT INFORMATION

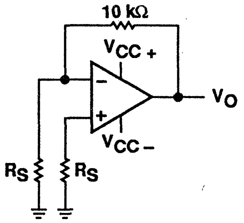
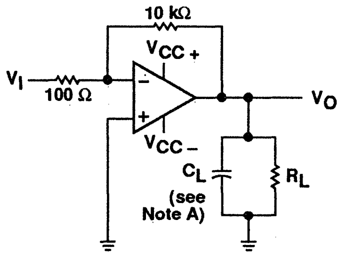


Figure 3. Noise Voltage Test Circuit



NOTE A: C_L includes fixture capacitance.

Figure 4. Unity-Gain Bandwidth and Phase Margin Test Circuit

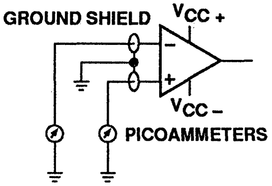


Figure 5. Input Bias and Offset Current Test Circuit

typical values

Typical values as presented in this data sheet represent the median (50% point) of device parametric performance.

input bias and offset current

At the picoamp bias current level typical of the TL031 and TL031A, accurate measurement of the bias current becomes difficult. Not only does this measurement require a picoammeter, but test socket leakages can easily exceed the actual device bias currents. To accurately measure these small currents, Texas Instruments uses a two-step process. The socket leakage is measured using picoammeters with bias voltages applied but with no device in the socket. The device is then inserted into the socket and a second test that measures both the socket leakage and the device input bias current is performed. The two measurements are then subtracted algebraically to determine the bias current of the device.

noise

Because of the increasing emphasis on low noise levels in many of today's applications, the input noise voltage density is sample-tested at f = 1 kHz. Texas Instruments also has additional noise testing capability to meet specific application requirements. Please contact the factory for details.

TYPICAL CHARACTERISTICS

table of graphs

			FIGURE
V_{IO}	Input offset voltage	Distribution	6
α_{VIO}	Temperature coefficient of input offset voltage	Distribution	7
I_{IO}	Input offset current	vs Temperature	8
I_{IB}	Input bias current	vs V_{IC} vs Temperature	9 8
V_I	Input voltage range	vs V_{CC} vs Temperature	10 11
V_{ID}	Differential input voltage	vs Output voltage	12, 13
V_{OM}	Maximum peak output voltage swing	vs V_{CC} vs Output current vs Frequency vs Temperature	14 16, 17 15 18, 19
A_{VD}	Differential voltage amplification	vs R_L vs Frequency vs Temperature	20 21 22
z_o	Output impedance	vs Frequency	23
CMRR	Common-mode rejection ratio	vs Frequency vs Temperature	24, 25 26
k_{SVR}	Supply-voltage rejection ratio	vs Temperature	27
I_{OS}	Short-circuit output current	vs V_{CC} vs Time vs Temperature	28 29 30
I_{CC}	Supply current	vs V_{CC} vs Temperature	32 33
SR	Slew rate	vs R_L vs Temperature	34, 35 36, 37
	Overshoot factor	vs C_L	38
V_n	Equivalent input noise voltage	vs Frequency	31
THD	Total harmonic distortion	vs Frequency	39
B_1	Unity-gain bandwidth	vs V_{CC} vs Temperature	40 41
ϕ_m	Phase margin	vs V_{CC} vs C_L vs Temperature	42 43 44
	Phase shift	vs Frequency	21
	Pulse response	Small-signal Large-signal	45 46, 47

TYPICAL CHARACTERISTICS†

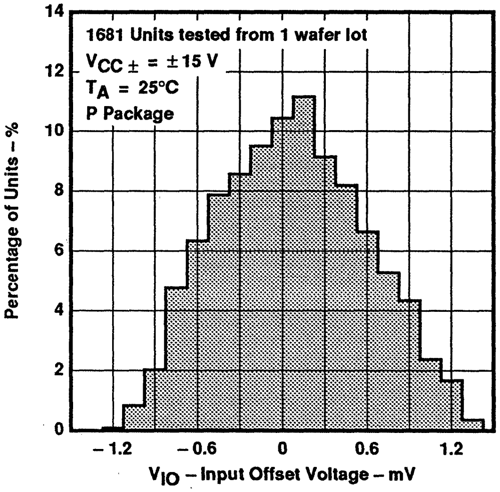

DISTRIBUTION OF TL031
INPUT OFFSET VOLTAGE

Figure 6

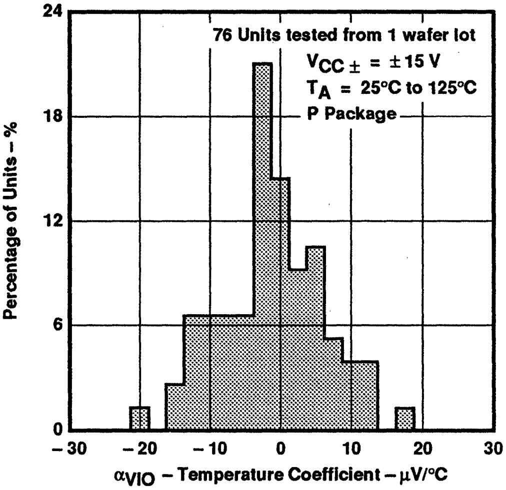

DISTRIBUTION OF TL031
INPUT OFFSET VOLTAGE
TEMPERATURE COEFFICIENT

Figure 7

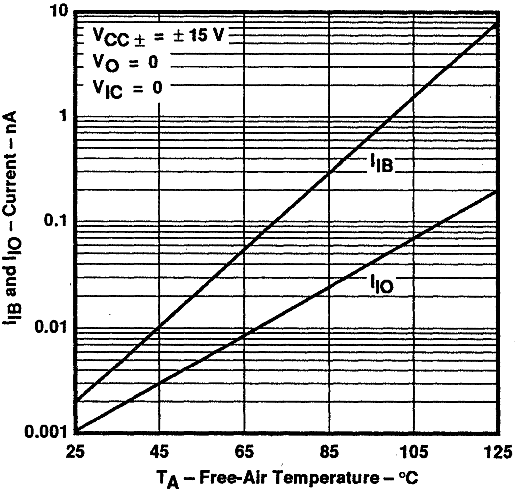

INPUT BIAS CURRENT AND
INPUT OFFSET CURRENT
vs
FREE-AIR TEMPERATURE

Figure 8

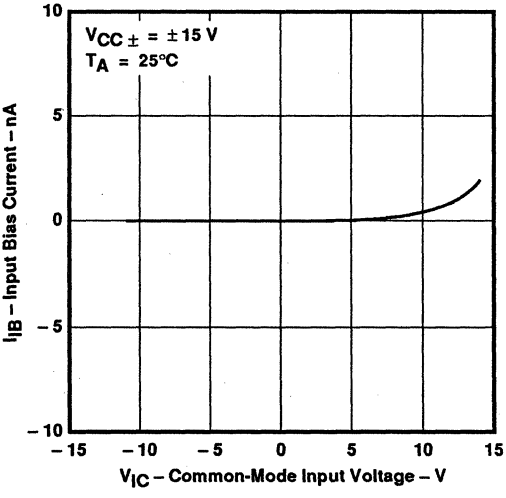

INPUT BIAS CURRENT
vs
COMMON-MODE INPUT VOLTAGE

Figure 9

---

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

COMMON-MODE
INPUT VOLTAGE RANGE LIMITS
vs
SUPPLY VOLTAGE

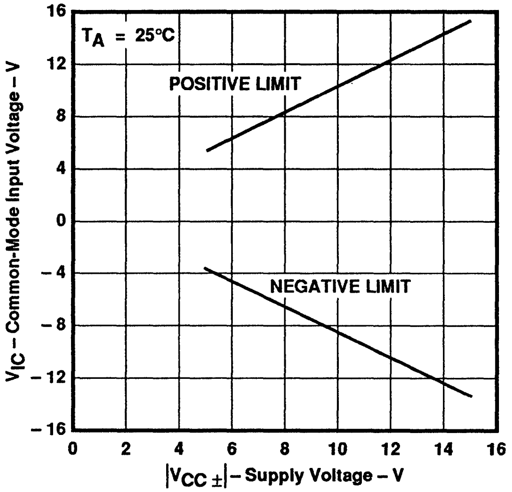


Figure 10

COMMON-MODE
INPUT VOLTAGE RANGE LIMITS
vs
FREE-AIR TEMPERATURE

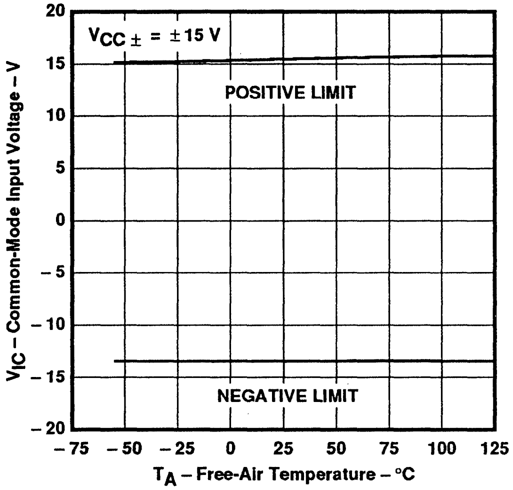


Figure 11

DIFFERENTIAL INPUT VOLTAGE
vs
OUTPUT VOLTAGE

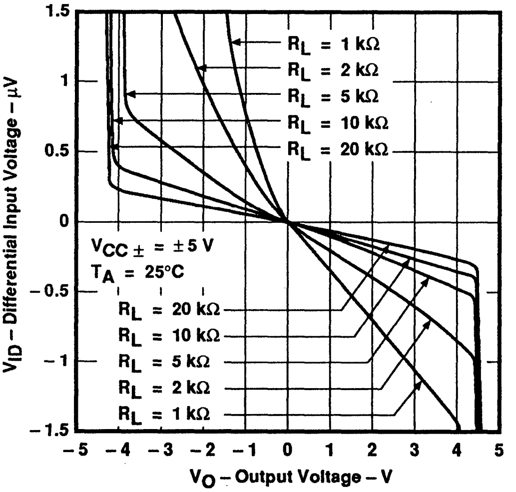


Figure 12

DIFFERENTIAL INPUT VOLTAGE
vs
OUTPUT VOLTAGE

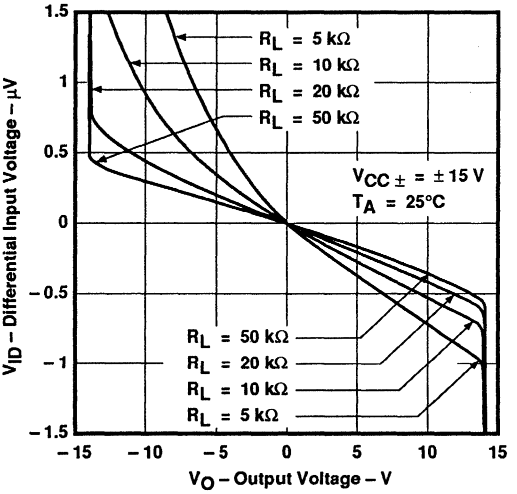


Figure 13

---

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

MAXIMUM PEAK OUTPUT VOLTAGE
vs
SUPPLY VOLTAGE

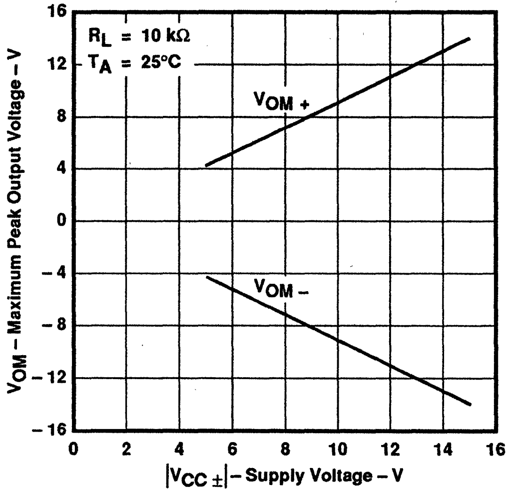


Figure 14

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE
vs
FREQUENCY

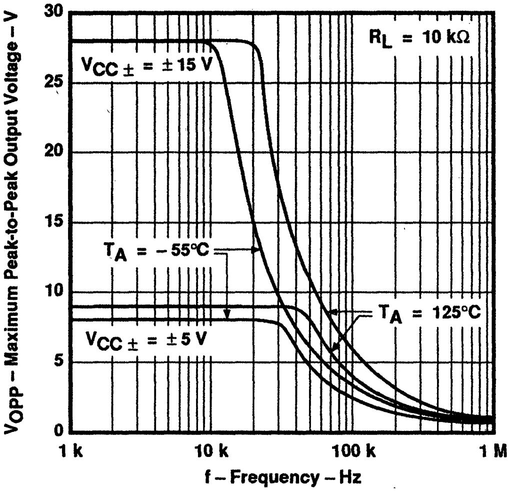


Figure 15

MAXIMUM PEAK OUTPUT VOLTAGE
vs
OUTPUT CURRENT

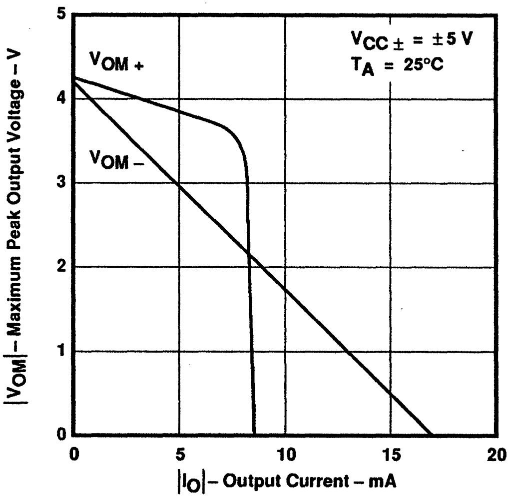


Figure 16

MAXIMUM PEAK OUTPUT VOLTAGE
vs
OUTPUT CURRENT

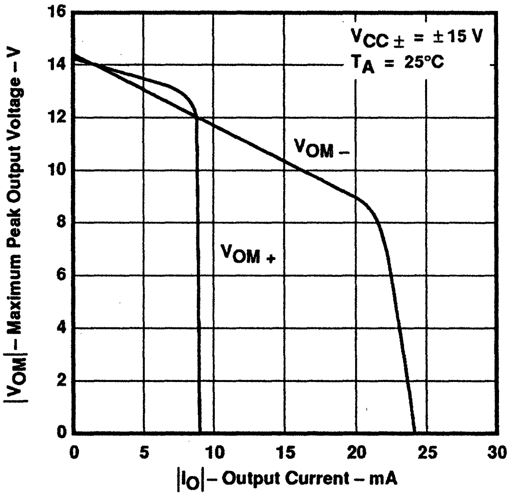


Figure 17

---

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

MAXIMUM PEAK OUTPUT VOLTAGE vs FREE-AIR TEMPERATURE

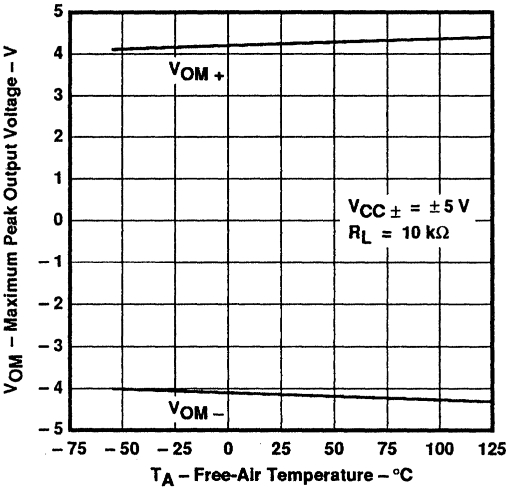


Figure 18

MAXIMUM PEAK OUTPUT VOLTAGE vs FREE-AIR TEMPERATURE

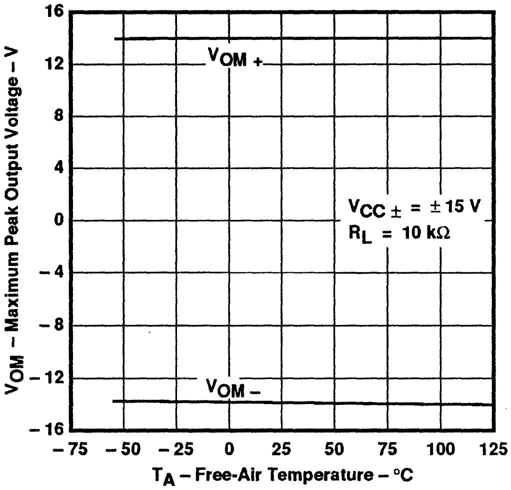


Figure 19

LARGE-SIGNAL VOLTAGE AMPLIFICATION vs LOAD RESISTANCE

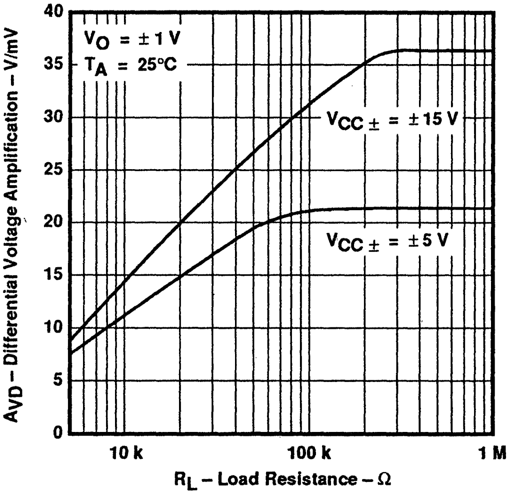


Figure 20

LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION AND PHASE SHIFT vs FREQUENCY

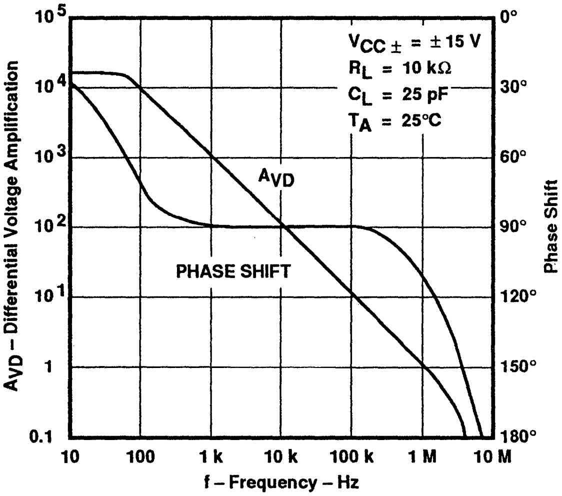


Figure 21

---

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

LARGE-SIGNAL VOLTAGE AMPLIFICATION
vs
FREE-AIR TEMPERATURE

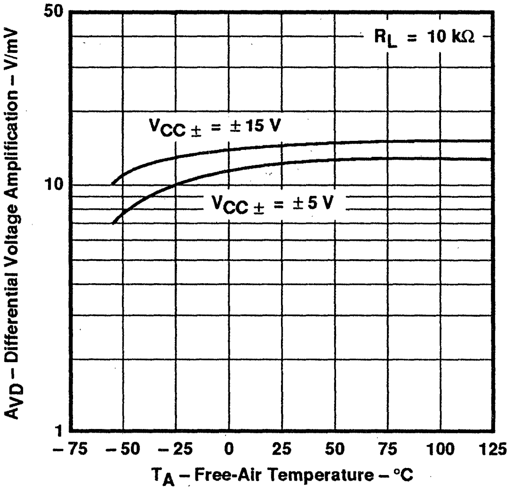


Figure 22

OUTPUT IMPEDANCE
vs
FREQUENCY

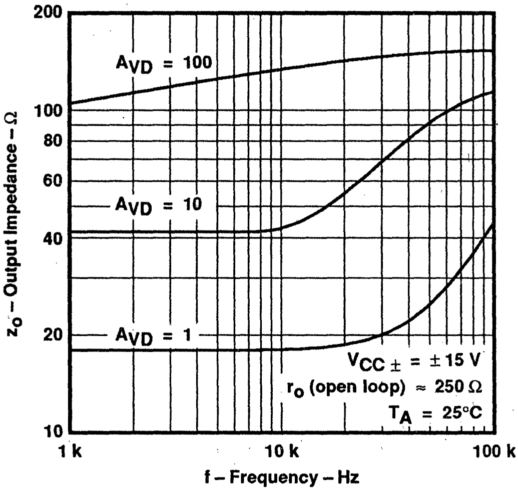


Figure 23

COMMON-MODE REJECTION RATIO
vs
FREQUENCY

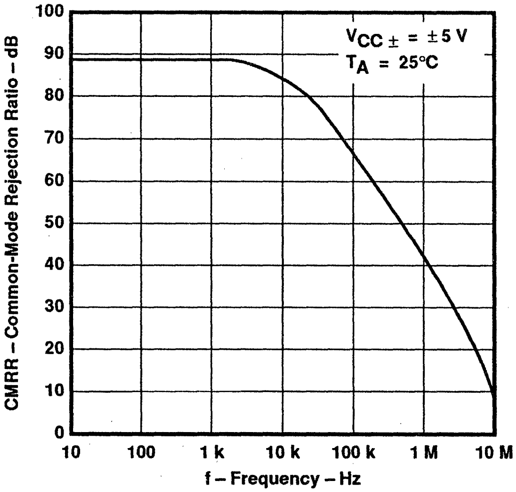


Figure 24

COMMON-MODE REJECTION RATIO
vs
FREQUENCY

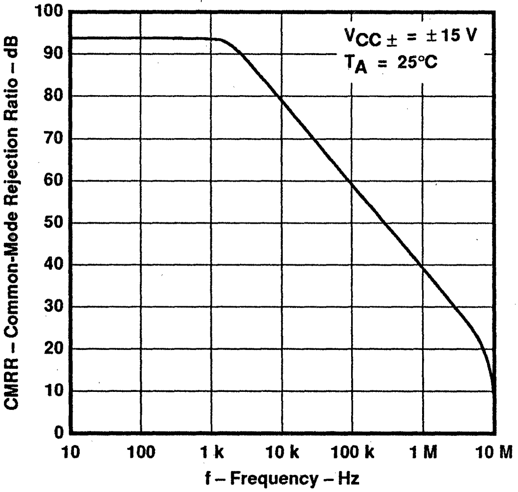


Figure 25

---

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS[†]

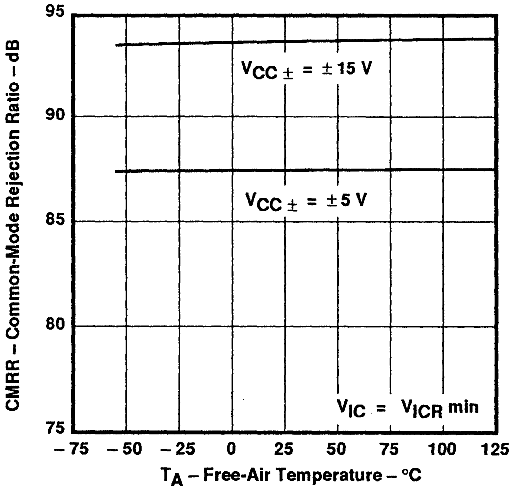

COMMON-MODE REJECTION RATIO
vs
FREE-AIR TEMPERATURE

Figure 26

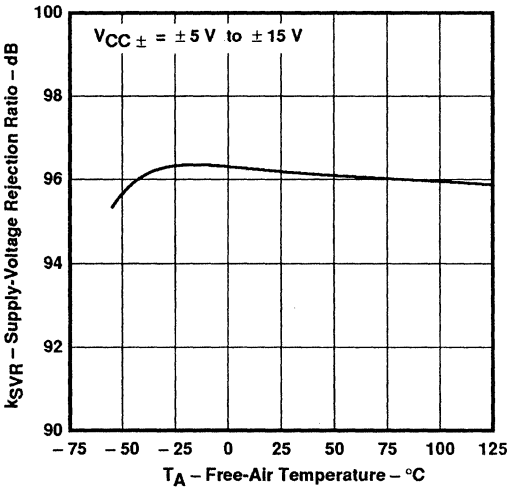

SUPPLY-VOLTAGE REJECTION RATIO
vs
FREE-AIR TEMPERATURE

Figure 27

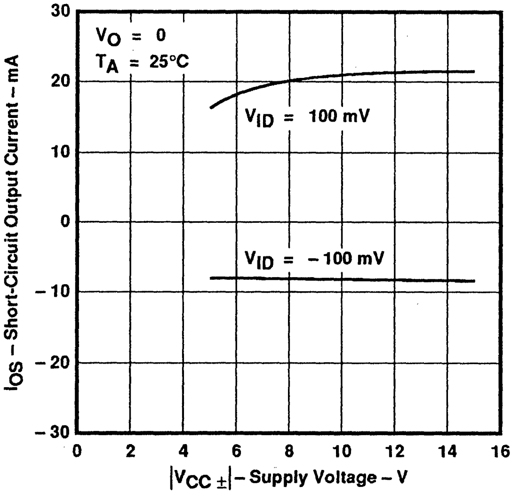

SHORT-CIRCUIT OUTPUT CURRENT
vs
SUPPLY VOLTAGE

Figure 28

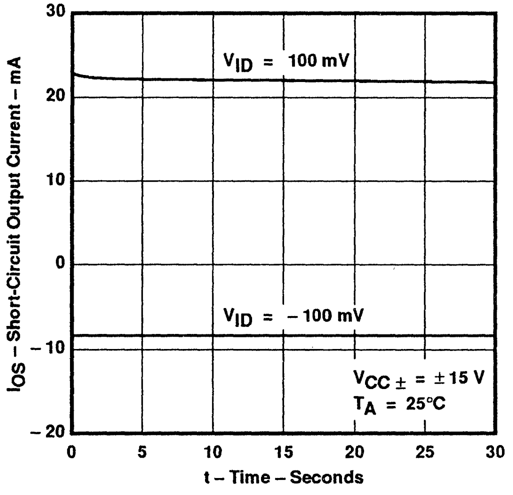

SHORT-CIRCUIT OUTPUT CURRENT
vs
TIME

Figure 29

[†] Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS[†]

SHORT-CIRCUIT OUTPUT CURRENT
vs
FREE-AIR TEMPERATURE

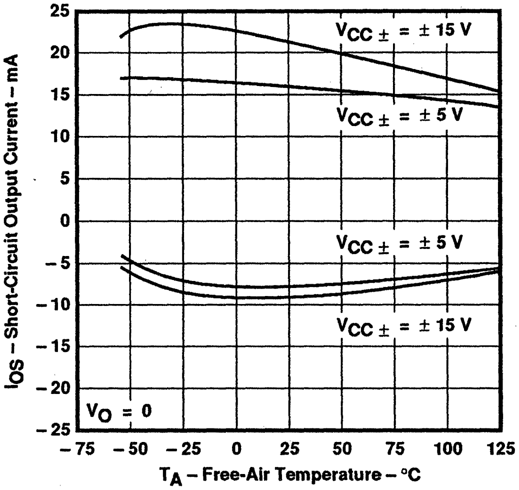


Figure 30

EQUIVALENT INPUT NOISE VOLTAGE
vs
FREQUENCY

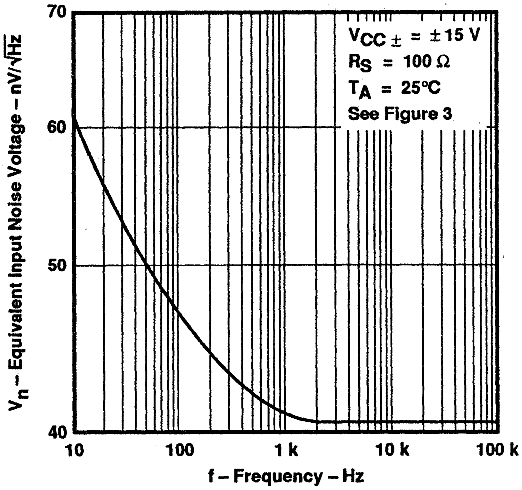


Figure 31

SUPPLY CURRENT
vs
SUPPLY VOLTAGE

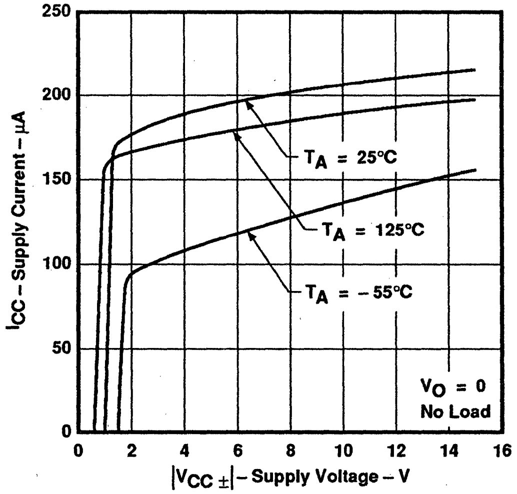


Figure 32

SUPPLY CURRENT
vs
FREE-AIR TEMPERATURE

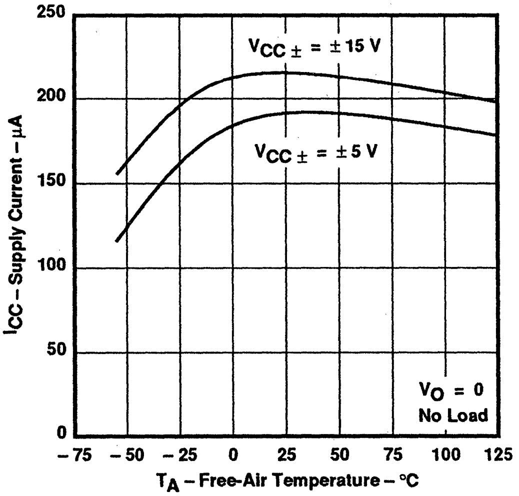


Figure 33

[†] Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

SLEW RATE
vs
LOAD RESISTANCE

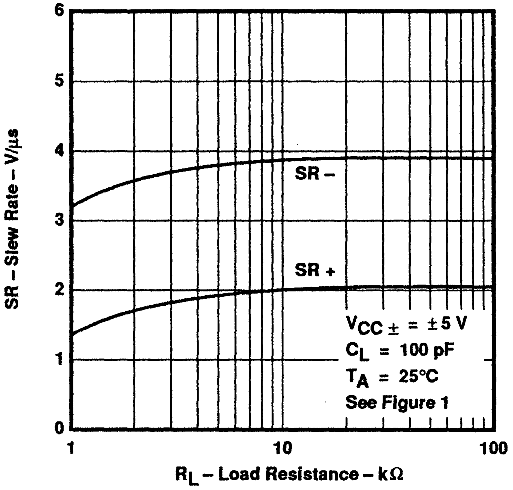


Figure 34

SLEW RATE
vs
LOAD RESISTANCE

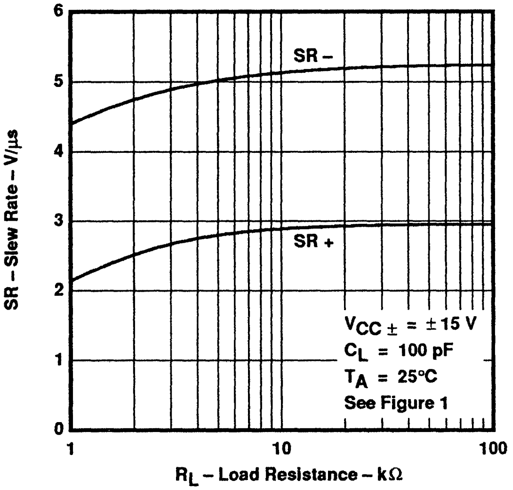


Figure 35

SLEW RATE
vs
FREE-AIR TEMPERATURE

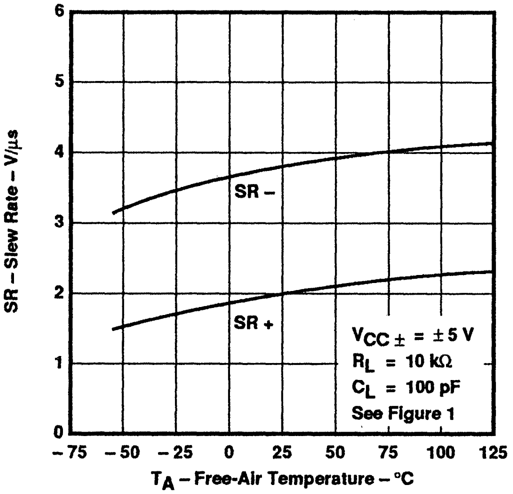


Figure 36

SLEW RATE
vs
FREE-AIR TEMPERATURE

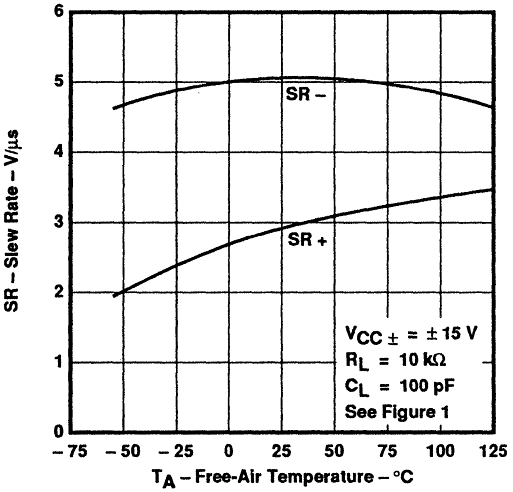


Figure 37

---

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS[†]

OVERSHOOT FACTOR
vs
LOAD CAPACITANCE

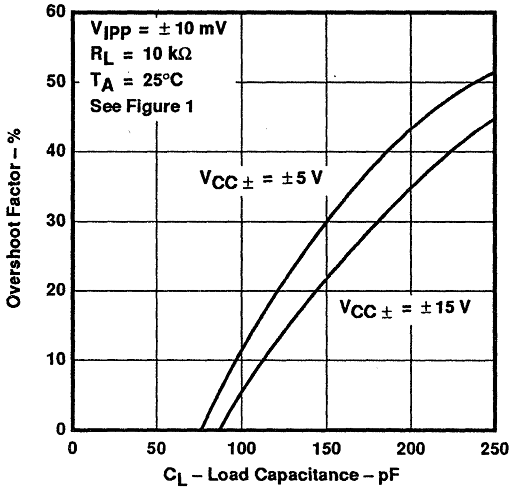


Figure 38

TOTAL HARMONIC DISTORTION
vs
FREQUENCY

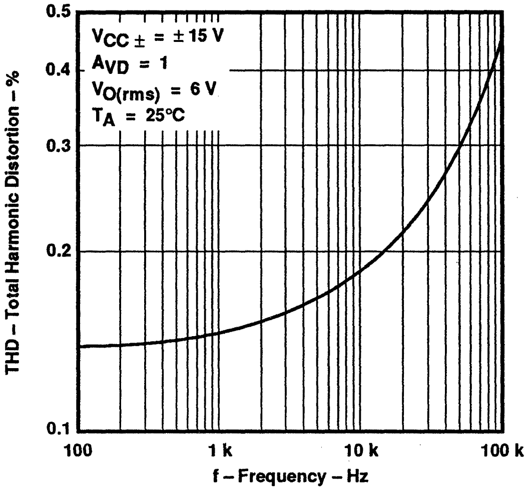


Figure 39

UNITY-GAIN BANDWIDTH
vs
SUPPLY VOLTAGE

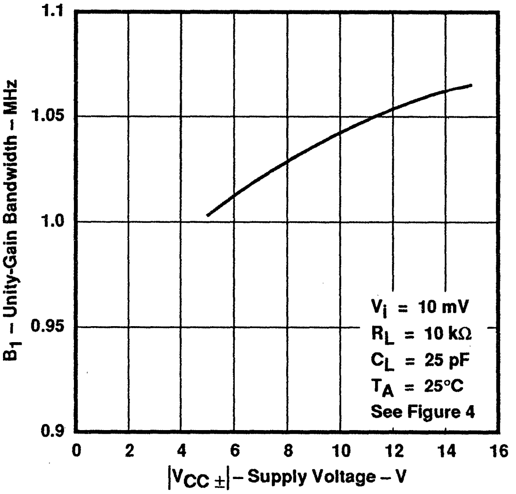


Figure 40

UNITY-GAIN BANDWIDTH
vs
FREE-AIR TEMPERATURE

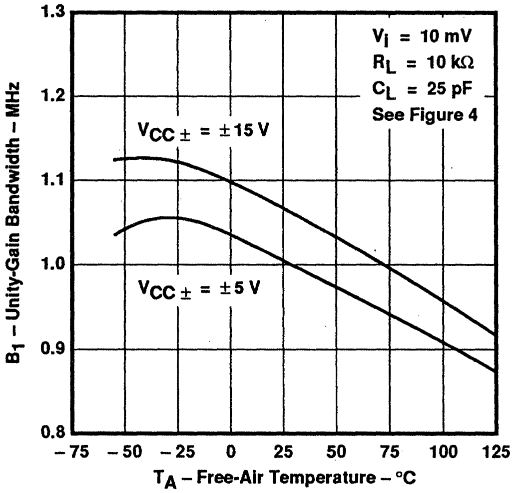


Figure 41

[†] Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

PHASE MARGIN
vs
SUPPLY VOLTAGE

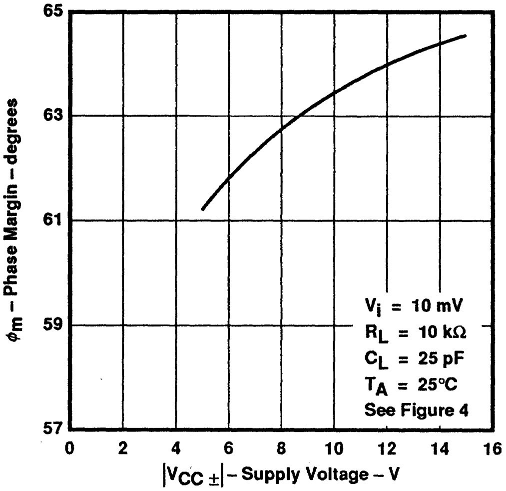


Figure 42

PHASE MARGIN
vs
LOAD CAPACITANCE

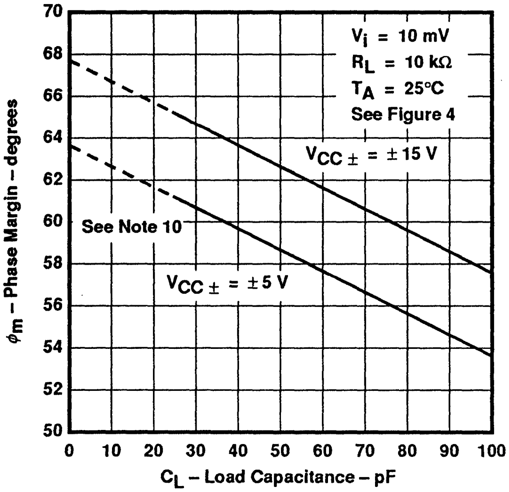


Figure 43

PHASE MARGIN
vs
FREE-AIR TEMPERATURE

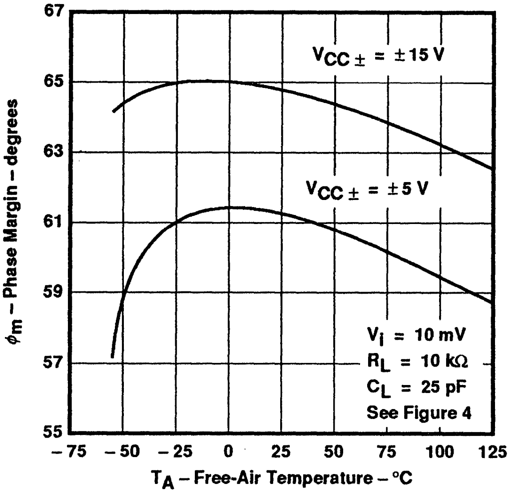


Figure 44

VOLTAGE-FOLLOWER
SMALL-SIGNAL
PULSE RESPONSE

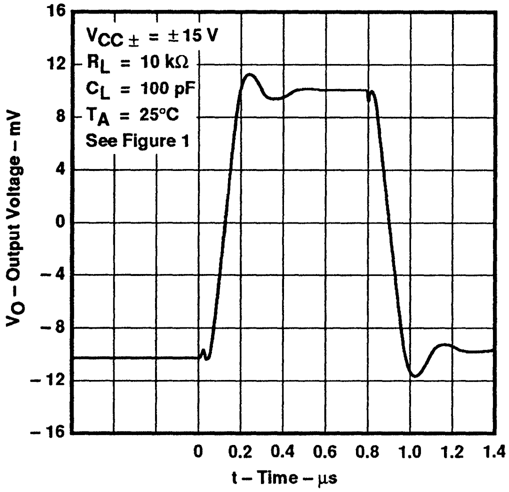


Figure 45

NOTE 10: Values of phase margin below a load capacitance of 25 pF were estimated.

---

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS

VOLTAGE-FOLLOWER
LARGE-SIGNAL
PULSE RESPONSE

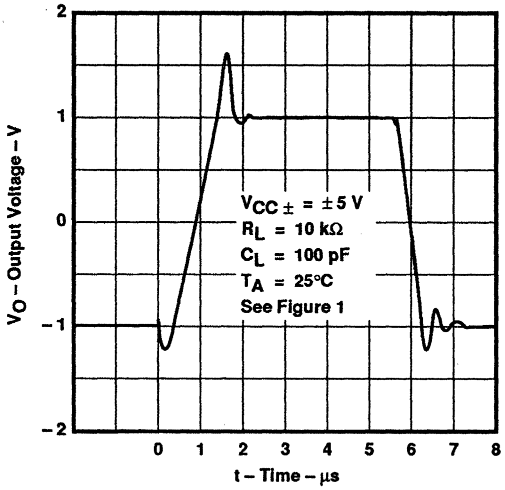


Figure 46

VOLTAGE-FOLLOWER
LARGE-SIGNAL
PULSE RESPONSE

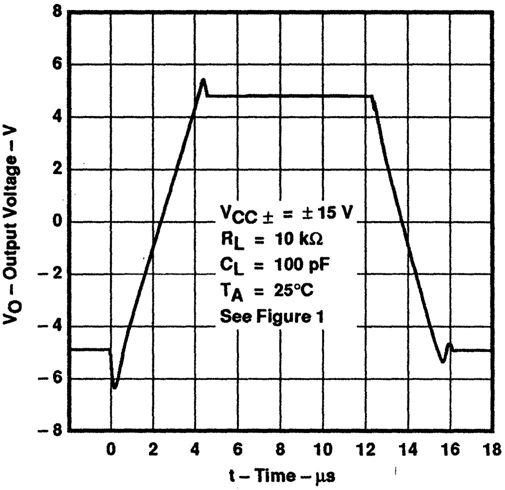


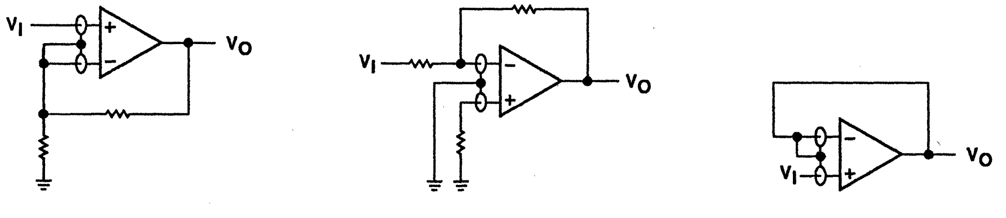
Figure 47

APPLICATION INFORMATION

input characteristics

The TL031 and TL031A are specified with a minimum and a maximum input voltage that, if exceeded at either input, could cause the device to malfunction.

Because of the extremely high input impedance and resulting low bias current requirements, the TL031 and TL031A are well-suited for low-level signal processing; however, leakage currents on printed circuit boards and sockets can easily exceed bias current requirements and cause degradation in system performance. It is a good practice to include guard rings around inputs (see Figure 48). These guards should be driven from a low-impedance source at the same voltage level as the common-mode input.



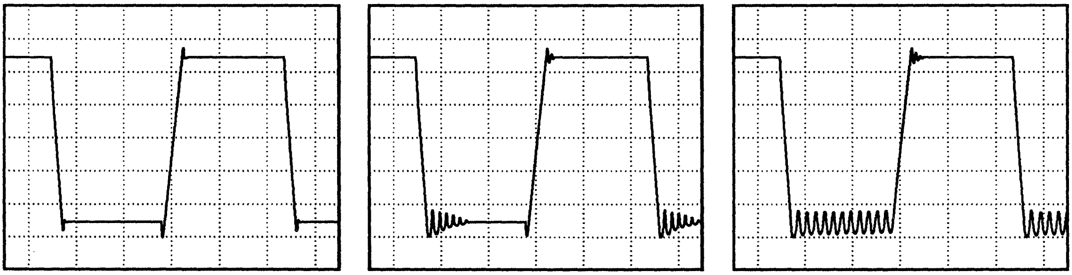
(a) NONINVERTING AMPLIFIER (b) INVERTING AMPLIFIER (c) UNITY-GAIN AMPLIFIER

Figure 48. Use of Guard Rings

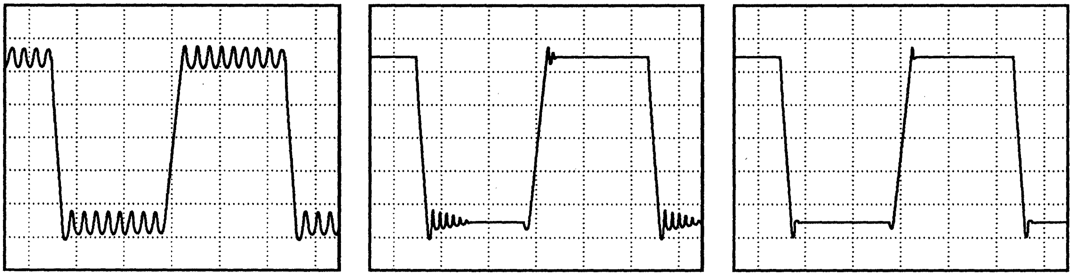
APPLICATION INFORMATION

output characteristics

All operating characteristics (except bandwidth and phase margin) are specified with 100-pF load capacitance. The TL031 and TL031A will drive higher capacitive loads; however, as the load capacitance increases, the resulting response pole occurs at lower frequencies, thereby causing ringing, peaking, or even oscillation. The value of the load capacitance at which oscillation occurs varies with production lots. If an application appears to be sensitive to oscillation due to load capacitance, adding a small resistance in series with the load should alleviate the problem. Capacitive loads of 1000 pF and larger may be driven if enough resistance is added in series with the output (see Figure 49).

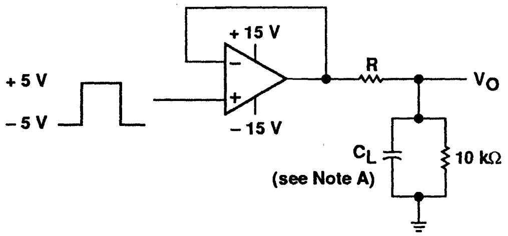


(a) C_L = 100 pF, R = 0 (b) C_L = 300 pF, R = 0 (c) C_L = 350 pF, R = 0



(d) C_L = 1000 pF, R = 0 (e) C_L = 1000 pF, R = 50 Ω (f) C_L = 1000 pF, R = 2 kΩ

Figure 49. Effect of Capacitive Loads



NOTE A: C_L includes fixture capacitance.

Figure 50. Test Circuit for Output Characteristics

APPLICATION INFORMATION

high-Q notch filter

In general, Texas Instruments enhanced JFET operational amplifiers serve as excellent filters. The circuit in Figure 51 provides a narrow notch at a specific frequency. Notch filters are designed to eliminate frequencies that are interfering with the operation of an application. For this filter, the center frequency can be calculated as:

$$f_O = \frac{1}{2\pi R1C1}$$

With the resistors and capacitors shown in Figure 51, the center frequency is 1 kHz. Note that $C1 = C3 = C2 \div 2$ and also that $R1 = R3 = 2 \times R2$. The center frequency can be modified by varying these values. When adjusting the center frequency, be sure that the operational amplifier still has sufficient gain at the frequency of interest.

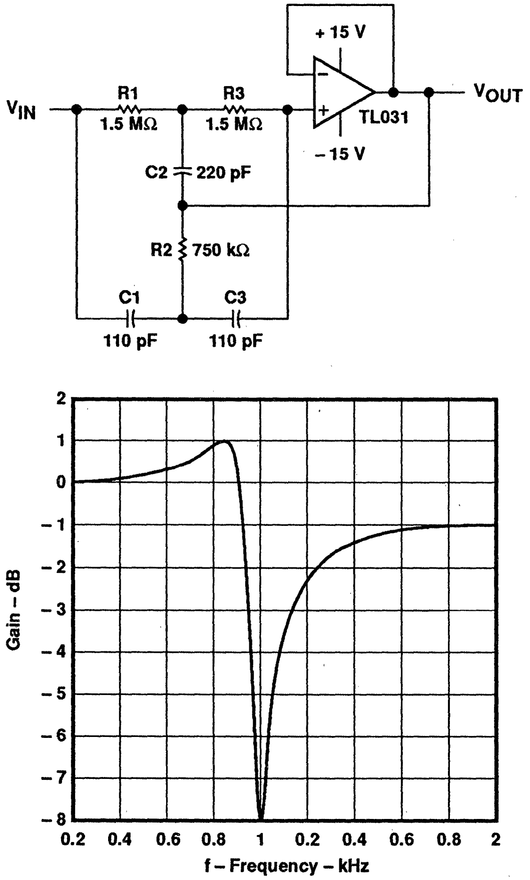


Figure 51. High-Q Notch Filter

APPLICATION INFORMATION

transimpedance amplifier

The low-power precision TL031 allows accurate measurement of low currents. The high input impedance and low offset voltage of the TL031A greatly simplify the design of a transimpedance amplifier. At room temperature, this design achieves ten-bit accuracy with an error of less than ½ LSB.

Assuming that R2 is much less than R1 and ignoring error terms, the output voltage can be expressed as:

$$V_O = -I_{IN} \times R_F \left(\frac{R1 + R2}{R2} \right)$$

Using the resistor values shown in the schematic, for a 1-nA input current, the output voltage equals – 0.1 V. If the V_O limit for the TL031A is measured to be ± 12 V, the maximum input current for these resistor values is ± 120 nA. Similarly, one LSB on a ten-bit scale corresponds to 12 mV of output voltage or 120 pA of input current.

The following equation shows the effect of input offset voltage and input bias current on the output voltage:

$$V_O = -\left[V_{IO} + R_F(I_{IN} + I_{IB})\right]\left(\frac{R1 + R2}{R2} \right)$$

If the application requires input protection for the transimpedance amplifier, do not use standard PN diodes. Instead, use low-leakage Siliconix SN4117 JFETs (or equivalent) connected as diodes across the TL031A inputs as shown in Figuire 52.

As with all precision applications, special care must be taken to eliminate external sources of leakage and interference. Other precautions include using high-quality insulation, cleaning insulating surfaces to remove fluxes and other residue, and enclosing the application within a protective box.

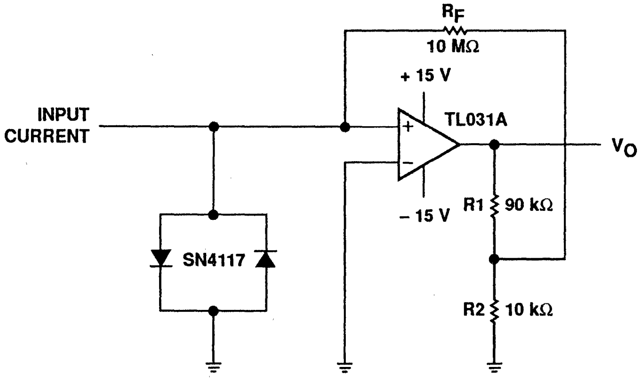


Figure 52. Transimpedance Amplifier

APPLICATION INFORMATION

4- to 20-mA current loops

Often information from an analog sensor must be sent over a distance to the receiving circuitry. For many applications, the most feasible method involves converting voltage information to a current before transmission. The following circuits give two variations of low-power current loops. The circuit in Figure 53 requires three wires from the transmitting to receiving circuitry while the second variation in Figure 54 requires only two wires but includes an extra integrated circuit. Both circuits benefit from the high input impedance of the TL031A since many inexpensive sensors do not have low output impedance.

Assuming that the voltage at the noninverting input of the TL031A is zero, the following equation determines the output current:

$$I_O = V_{IN}\left(\frac{R3}{R1 \times R_S}\right) + 5\,V\left(\frac{R3}{R2 \times R_S}\right) = 0.16 \times V_{IN} + 4\text{ mA}$$

The circuits presently provide 4-to 20-mA output for an input voltage of 0 to 100 mV. By modifying R1, R2, and R3, the input voltage range or the output current range can be adjusted.

Including the offset voltage of the operational amplifier in the above equation clearly illustrates why the low offset TL031A was chosen:

$$I_O = V_{IN}\left(\frac{R3}{R1 \times R_S}\right) + 5\,V\left(\frac{R3}{R2 \times R_S}\right) - V_{IO}\left(\frac{R3}{R1 \times R_S} + \frac{R3}{R2 \times R_S} + \frac{R1}{R_S}\right) = 0.16 \times V_{IN} + 4\text{ mA} - 0.17 \times V_{IO}$$

For example, an offset voltage of 1 mV decreases the output current by 0.17 mA..

Thanks to the low power consumption of the TL031A, both circuits have at least 2 mA available to drive the actual sensor from the 5-V reference node.

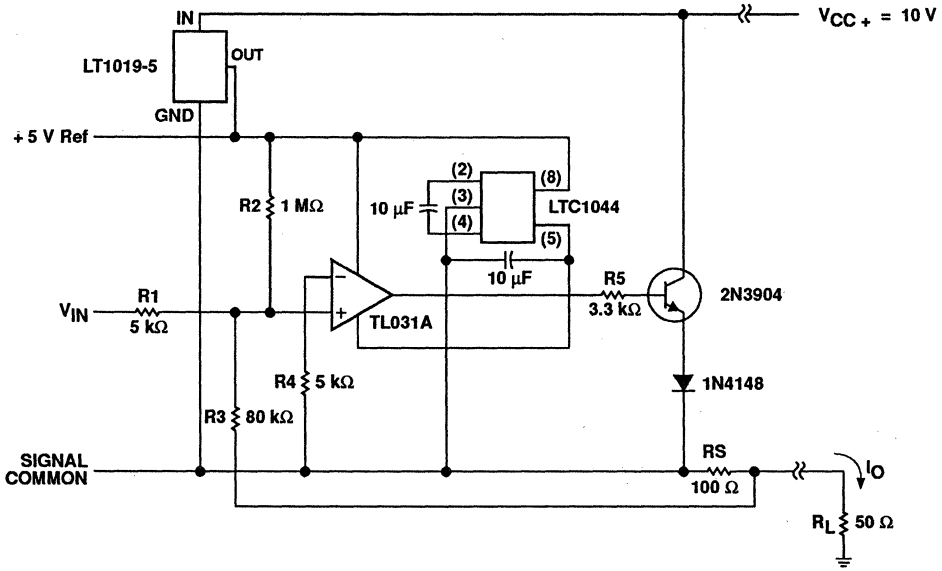


Figure 53. 2-Wire 4- to 20-mA Current Loop

APPLICATION INFORMATION

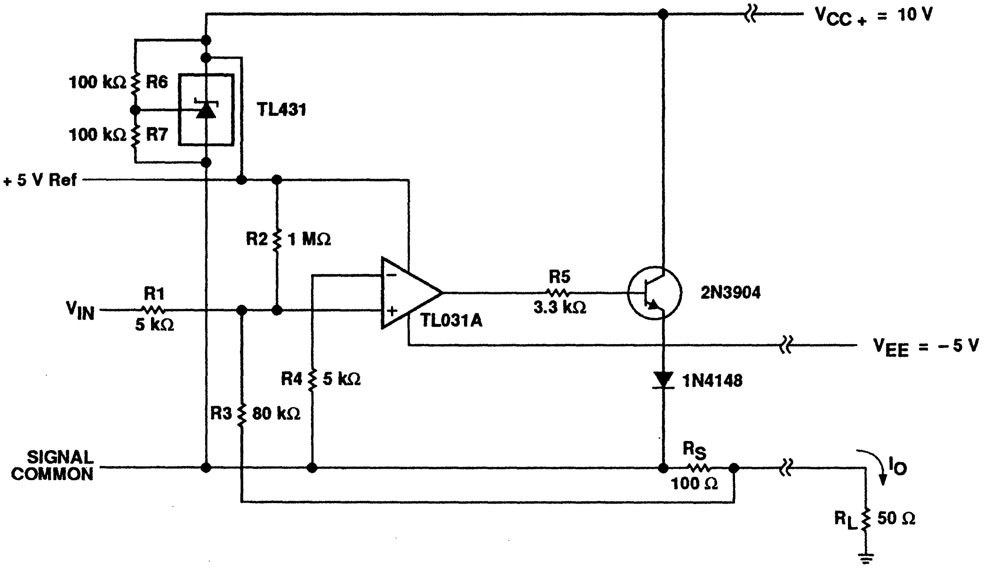


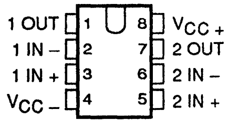
Figure 54. 3-Wire 4- to 20-mA Current Loop

TL032, TL032A
ENHANCED JFET LOW-POWER LOW-OFFSET DUAL OPERATIONAL AMPLIFIERS

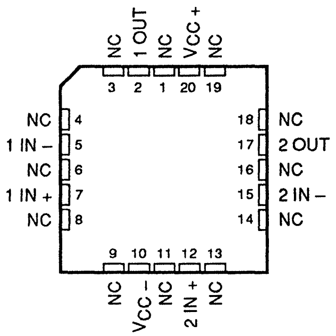
D3152, JULY 1988 – REVISED JANUARY 1991

- **Maximum Offset Voltage . . . 800 µV**
- **High Slew Rate . . . 2.9 V/µs Typ**
- **Low Input Bias Current . . . 2 pA Typ**
- **Very Low Power Consumption . . . 13 mW Typ**
- **Output Short-Circuit Protection**

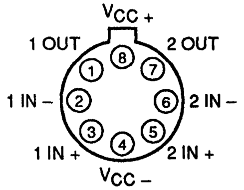
D, JG, or P PACKAGE
(TOP VIEW)



FK PACKAGE
(TOP VIEW)



L PACKAGE
(TOP VIEW)



Pin 4 (L Package) is in electrical contact with the case

NC – No internal connection

description

The TL032 and TL032A dual operational amplifiers incorporate well-matched, high-voltage JFET and bipolar transistors in a monolithic integrated circuit. These devices offer the significant advantages of Texas Instruments new enhanced JFET process. This process affords not only low initial offset voltage due to the on-chip zener trim capability but also stable offset voltage over time and temperature. In comparison, traditional JFET processes are plagued by significant offset voltage drift.

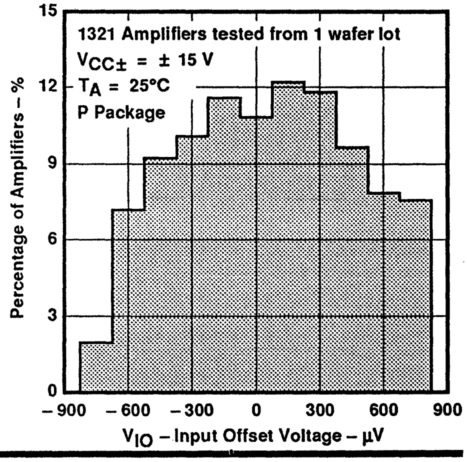
This new enhanced process still maintains the traditional JFET advantages of fast slew rates and low input bias and offset currents. These advantages coupled with low power consumption make the TL032 well-suited for new state-of-the-art designs as well as existing design upgrades. The TL032 has been designed to be functionally compatible and pin compatible with the TL062.

AVAILABLE OPTIONS

T_A	V_{IO} max AT 25°C	PACKAGE				
		SMALL-OUTLINE (D)	CHIP CARRIER (FK)	CERAMIC DIP (JG)	METAL CAN (L)	PLASTIC DIP (P)
0°C to 70°C	0.8 mV	TL032ACD	—	—	—	TL032ACP
	1.5 mV	TL032CD	—	—	—	TL032CP
– 40°C to 85°C	0.8 mV	TL032AID	—	—	—	TL032AIP
	1.5 mV	TL032ID	—	—	—	TL032IP
– 55°C to 125°C	0.8 mV	TL032AMD	TL032AMFK	TL032AMJG	TL032AML	TL032AMP
	1.5 mV	TL032MD	TL032MFK	TL032MJG	TL032ML	TL032MP

D packages are available taped and reeled. Add "R" suffix to device type, (e.g., TL032CDR).

DISTRIBUTION OF TL032A
INPUT OFFSET VOLTAGE



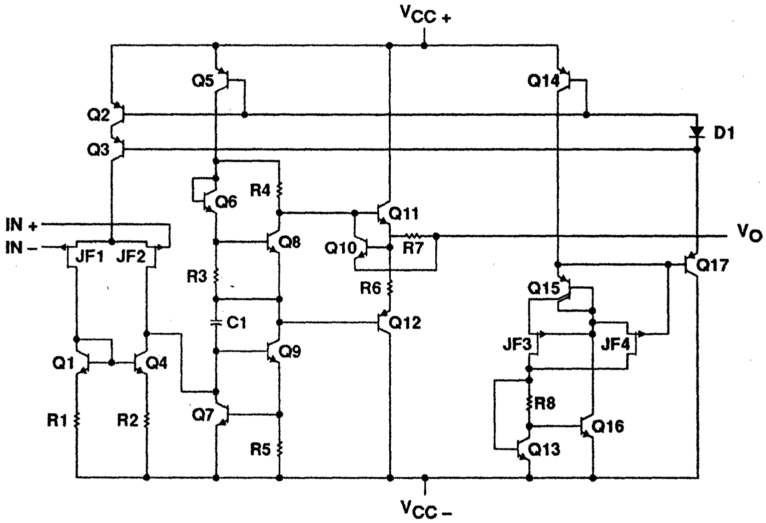
description (continued)

functionally compatible and pin compatible with the TL062. Two offset voltage grades are available: TL032 (1.5 mV max) and TL032A (800 µV max).

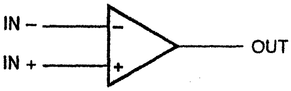
A variety of available packaging options includes small-outline and chip carrier versions for high density system applications.

The C-suffix devices are characterized for operation from 0°C to 70°C. The I-suffix devices are characterized for operation from – 40°C to 85°C. The M-suffix devices are characterized for operation over the full military temperature range of – 55°C to 125°C.

equivalent schematic (each amplifier)



symbol (each amplifier)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC+} (see Note 1)	18 V
Supply voltage, V_{CC-} (see Note 1)	– 18 V
Differential input voltage (see Note 2)	± 30 V
Input voltage range, V_I (any input, see Notes 1 and 3)	± 15 V
Input current, I_I (each input)	± 1 mA
Output current, I_O (each output)	± 40 mA
Total current into V_{CC+} terminal	160 mA
Total current out of V_{CC-} terminal	160 mA
Duration of short-circuit current at (or below) 25°C (see Note 4)	unlimited
Continuous total dissipation	See Dissipation Rating Table
Operating free-air temperature, T_A: C-suffix	0°C to 70°C
I-suffix	– 40°C to 85°C
M-suffix	– 55°C to 125°C
Storage temperature range	– 65°C to 150°C
Case temperature for 60 seconds: FK package	260°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D or P package	260°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: JG or L package	300°C

NOTES:
1. All voltage values, except differential voltages, are with respect to the midpoint between V_{CC+} and V_{CC-}.
2. Differential voltages are at the noninverting input with respect to the inverting input.
3. The magnitude of the input voltage must never exceed the magnitude of the supply voltage or 15 V, whichever is less.
4. The output may be shorted to either supply. Temperature and/or supply voltages must be limited to ensure that the maximum dissipation rating is not exceeded.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING	$T_A = 125°C$ POWER RATING
D	725 mW	5.8 mW/°C	464 mW	377 mW	145 mW
FK	1375 mW	11.0 mW/°C	880 mW	715 mW	275 mW
JG	1050 mW	8.4 mW/°C	672 mW	546 mW	210 mW
L	825 mW	6.6 mW/°C	528 mW	429 mW	165 mW
P	1000 mW	8.0 mW/°C	640 mW	520 mW	200 mW

recommended operating conditions

		C-SUFFIX			I-SUFFIX			M-SUFFIX			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		± 5		± 15	± 5		± 15	± 5		± 15	V
Common-mode input voltage, V_{IC}	$V_{CC\pm} = \pm 5$ V	– 1.5		4	– 1.5		4	– 1.5		4	V
	$V_{CC\pm} = \pm 15$ V	– 11.5		14	– 11.5		14	– 11.5		14	
Operating free-air temperature, T_A		0		70	– 40		85	– 55		125	°C

electrical characteristics

PARAMETER		TEST CONDITIONS		T_A†	$V_{CC\pm} = \pm 5$ V			$V_{CC\pm} = \pm 15$ V			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	$V_O = 0$, $V_{IC} = 0$, $R_S = 50\ \Omega$	TL032C	25°C		0.69	3.5		0.57	1.5	mV
				Full range			4.5			2.5	
			TL032AC	25°C		0.53	2.8		0.39	0.8	
				Full range			3.8			1.8	
α_{VIO}	Temperature coefficient of input offset voltage (see Note 8)		TL032C	25°C to 70°C		11.5			10.8		µV/°C
			TL032AC	25°C to 70°C		11.5			10.8	25	
	Input offset voltage long-term drift (see Note 5)			25°C		0.04			0.04		µV/mo
I_{IO}	Input offset current	$V_O = 0$, $V_{IC} = 0$, See Figure 5		25°C		1	100		1	100	pA
				70°C		9	200		12	200	
I_{IB}	Input bias current	$V_O = 0$, $V_{IC} = 0$, See Figure 5		25°C		2	200		2	200	pA
				70°C		50	400		80	400	
V_{ICR}	Common-mode input voltage range			25°C	−1.5 to 4	−3.4 to 5.4		−11.5 to 14	−13.4 to 15.4		V
				Full range	−1.5 to 4			−11.5 to 14			
V_{OM+}	Maximum positive peak output voltage swing	$R_L = 10\ k\Omega$		25°C	3	4.3		13	14		V
				0°C	3	4.2		13	14		
				70°C	3	4.3		13	14		
V_{OM-}	Maximum negative peak output voltage swing	$R_L = 10\ k\Omega$		25°C	−3	−4.2		−12.5	−13.9		V
				0°C	−3	−4.1		−12.5	−13.9		
				70°C	−3	−4.2		−12.5	−14		
A_{VD}	Large-signal differential voltage amplification	$R_L = 10\ k\Omega$, See Note 6		25°C	4	12		5	14.3		V/mV
				0°C	3	11.1		4	13.5		
				70°C	4	13.3		5	15.2		
r_i	Input resistance			25°C		10^{12}			10^{12}		Ω
C_i	Input capacitance			25°C		5			4		pF
CMRR	Common-mode rejection ratio	$V_{IC} = V_{ICR}$ min, $V_O = 0$, $R_S = 50\ \Omega$		25°C	70	87		75	94		dB
				0°C	70	87		75	94		
				70°C	70	87		75	94		
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm} / \Delta V_{IO}$)	$V_{CC\pm} = \pm 5$ V to ± 15 V, $V_O = 0$, $R_S = 50\ \Omega$		25°C	75	96		75	96		dB
				0°C	75	96		75	96		
				70°C	75	96		75	96		
P_D	Total power dissipation (two amplifiers)	No load, $V_O = 0$		25°C		3.8	5		13	17	mW
				0°C		3.7	5		12.7	17	
				70°C		3.8	5		12.6	17	
I_{CC}	Supply current (two amplifiers)	No load, $V_O = 0$		25°C		384	500		434	560	µA
				0°C		368	500		422	560	
				70°C		378	500		420	560	
V_{o1}/V_{o2}	Crosstalk attenuation	$A_{VD} = 100$		25°C		120			120		dB

† Full range is 0°C to 70°C.

NOTES: 5. Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at $T_A = 150°C$ extrapolated to $T_A = 25°C$ using the Arrhenius equation and assuming an activation energy of 0.96 eV.

6. At $V_{CC\pm} = \pm 5$ V, $V_O = \pm 2.3$ V; at $V_{CC\pm} = \pm 15$ V, $V_O = \pm 10$ V.

8. This parameter is tested on a sample basis for the TL032A. For other test requirements, please contact the factory. This statement has no bearing on testing or nontesting of other parameters.

operating characteristics

PARAMETER			TEST CONDITIONS		T_A	$V_{CC\pm} = \pm5$ V			$V_{CC\pm} = \pm15$ V			UNIT
						MIN	TYP	MAX	MIN	TYP	MAX	
SR +	Positive slew rate at unity gain		R_L = 10 kΩ, C_L = 100 pF, See Figure 1, See Note 7		25°C		2		2	2.9		V/μs
					0°C		1.8		1.5	2.6		
					70°C		2.2		2	3.2		
SR –	Negative slew rate at unity gain				25°C		3.9		3.5	5.1		V/μs
					0°C		3.7		3.2	5.0		
					70°C		4		3.2	5.0		
t_r	Rise time		V_{IPP} = ±10 mV, R_L = 10 kΩ, C_L = 100 pF, See Figures 1 and 2		25°C		138			132		ns
					0°C		134			127		
					70°C		150			142		
t_f	Fall time				25°C		138			132		ns
					0°C		134			127		
					70°C		150			142		
	Overshoot factor				25°C		11%			5%		
					0°C		10%			4%		
					70°C		12%			6%		
V_n	Equivalent input noise voltage (see Note 9)	TL032C	R_S = 100 Ω, See Figure 3	f = 10 Hz	25°C		49			49		nV/√Hz
				f = 1 kHz			41			41		
		TL032AC		f = 10 Hz	25°C		49			49		
				f = 1 kHz			41			41	60	
I_n	Equivalent input noise current		f = 1 kHz		25°C		0.003			0.003		pA/√Hz
B1	Unity-gain bandwidth		V_i = 10 mV, R_L = 10 kΩ, C_L = 25 pF, See Figure 4		25°C		1			1.1		MHz
					0°C		1			1.1		
					70°C		1			1		
ϕ_m	Phase margin at unity gain		V_i = 10 mV, R_L = 10 kΩ, C_L = 25 pF, See Figure 4		25°C		61°			65°		
					0°C		61°			65°		
					70°C		60°			64°		

NOTES: 7. For $V_{CC\pm} = \pm5$ V, $V_{IPP} = \pm1$ V; for $V_{CC\pm} = \pm15$ V, $V_{IPP} = \pm5$ V.

9. This parameter is tested on a sample basis. For other test requirements, please contact the factory. This statement has no bearing on testing or nontesting of other parameters.

electrical characteristics

PARAMETER		TEST CONDITIONS		T_A†	$V_{CC\pm} = \pm 5$ V			$V_{CC\pm} = \pm 15$ V			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	$V_O = 0$, $V_{IC} = 0$, $R_S = 50\ \Omega$	TL032I	25°C		0.69	3.5		0.57	1.5	mV
				Full range			5.3			3.3	
			TL032AI	25°C		0.53	2.8		0.39	0.8	
				Full range			4.6			2.6	
α_{VIO}	Temperature coefficient of input offset voltage (see Note 8)		TL032I	25°C to 85°C		11.4			10.8		µV/°C
			TL032AI	25°C to 85°C		11.4			10.8	25	
	Input offset voltage long-term drift (see Note 5)			25°C		0.04			0.04		µV/mo
I_{IO}	Input offset current	$V_O = 0$, $V_{IC} = 0$, See Figure 5		25°C		1	100		1	100	pA
				85°C		0.02	0.45		0.02	0.45	nA
I_{IB}	Input bias current	$V_O = 0$, $V_{IC} = 0$, See Figure 5		25°C		2	200		2	200	pA
				85°C		0.2	0.9		0.3	0.9	nA
V_{ICR}	Common-mode input voltage range			25°C	− 1.5 to 4	− 3.4 to 5.4		− 11.5 to 14	− 13.4 to 15.4		V
				Full range	− 1.5 to 4			− 11.5 to 14			
V_{OM+}	Maximum positive peak output voltage swing	$R_L = 10\ k\Omega$		25°C	3	4.3		13	14		V
				− 40°C	3	4.1		13	14		
				85°C	3	4.4		13	14		
V_{OM-}	Maximum negative peak output voltage swing	$R_L = 10\ k\Omega$		25°C	− 3	− 4.2		− 12.5	− 13.9		V
				− 40°C	− 3	− 4.1		− 12.5	− 13.8		
				85°C	− 3	− 4.2		− 12.5	− 14		
A_{VD}	Large-signal differential voltage amplification	$R_L = 10\ k\Omega$, See Note 6		25°C	4	12		5	14.3		V/mV
				− 40°C	3	8.4		4	11.6		
				85°C	4	13.5		5	15.3		
r_i	Input resistance			25°C		10^{12}			10^{12}		Ω
C_i	Input capacitance			25°C		5			4		pF
CMRR	Common-mode rejection ratio	$V_{IC} = V_{ICR}$ min, $V_O = 0$, $R_S = 50\ \Omega$		25°C	70	87		75	94		dB
				− 40°C	70	87		75	94		
				85°C	70	87		75	94		
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm} / \Delta V_{IO}$)	$V_{CC\pm} = \pm 5$ V to ± 15 V, $V_O = 0$, $R_S = 50\ \Omega$		25°C	75	96		75	96		dB
				− 40°C	75	96		75	96		
				85°C	75	96		75	96		
P_D	Total power dissipation (two amplifiers)	No load, $V_O = 0$		25°C		3.8	5		13	17	mW
				− 40°C		2.9	5		10.9	17	
				85°C		3.7	5		12.4	17	
I_{CC}	Supply current (two amplifiers)	No load, $V_O = 0$		25°C		384	500		434	560	µA
				− 40°C		288	500		362	560	
				85°C		372	500		414	560	
V_{o1}/V_{o2}	Crosstalk attenuation	$A_{VD} = 100$		25°C		120			120		dB

† Full range is –40°C to 85°C.

NOTES: 5. Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at $T_A = 150$°C extrapolated to $T_A = 25$°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

6. At $V_{CC\pm} = \pm 5$ V, $V_O = \pm 2.3$ V; at $V_{CC\pm} = \pm 15$ V, $V_O = \pm 10$ V.

8. This parameter is tested on a sample basis for the TL032A. For other test requirements, please contact the factory. This statement has no bearing on testing or nontesting of other parameters.

operating characteristics

PARAMETER			TEST CONDITIONS		T_A	$V_{CC\pm} = \pm5$ V			$V_{CC\pm} = \pm15$ V			UNIT
						MIN	TYP	MAX	MIN	TYP	MAX	
SR +	Positive slew rate at unity gain		R_L = 10 kΩ, C_L = 100 pF, See Figure 1, See Note 7		25°C		2		2	2.9		V/µs
					– 40°C		1.6		1.5	2.1		
					85°C		2.3		2	3.3		
SR –	Negative slew rate at unity gain				25°C		3.9		3.5	5.1		V/µs
					– 40°C		3.3		3.2	4.8		
					85°C		4.1		3.2	4.9		
t_r	Rise time		V_{IPP} = ± 10 mV, R_L = 10 kΩ, C_L = 100 pF, See Figures 1 and 2		25°C		138			132		ns
					– 40°C		132			123		
					85°C		154			146		
t_f	Fall time				25°C		138			132		ns
					– 40°C		132			123		
					85°C		154			146		
	Overshoot factor				25°C		11%			5%		
					– 40°C		12%			5%		
					85°C		13%			7%		
V_n	Equivalent input noise voltage (see Note 9)	TL032I	R_S = 100 Ω, See Figure 3	f = 10 Hz	25°C		49			49		nV/√Hz
				f = 1 kHz			41			41		
		TL032AI		f = 10 Hz	25°C		49			49		
				f = 1 kHz			41			41	60	
I_n	Equivalent input noise current		f = 1 kHz		25°C		0.003			0.003		pA/√Hz
B1	Unity-gain bandwidth		V_i = 10 mV, R_L = 10 kΩ, C_L = 25 pF, See Figure 4		25°C		1			1.1		MHz
					– 40°C		1			1.1		
					85°C		0.9			1		
ϕ_m	Phase margin at unity gain		V_i = 10 mV, R_L = 10 kΩ, C_L = 25 pF, See Figure 4		25°C		61°			65°		
					– 40°C		60°			65°		
					85°C		60°			64°		

NOTES: 7. For $V_{CC\pm} = \pm5$ V, $V_{IPP} = \pm1$ V; for $V_{CC\pm} = \pm15$ V, $V_{IPP} = \pm5$ V.

9. This parameter is tested on a sample basis. For other test requirements, please contact the factory. This statement has no bearing on testing or nontesting of other parameters.

electrical characteristics

PARAMETER		TEST CONDITIONS		T_A†	$V_{CC\pm} = \pm 5$ V			$V_{CC\pm} = \pm 15$ V			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	$V_O = 0$, $V_{IC} = 0$, $R_S = 50\ \Omega$	TL032M	25°C		0.69	3.5		0.57	1.5	mV
				Full range			6.5			4.5	
			TL032AM	25°C		0.53	2.8		0.39	0.8	
				Full range			5.8			3.8	
α_{VIO}	Temperature coefficient of input offset voltage		TL032M	25°C to 125°C		9.7			9.7		µV/°C
			TL032AM	25°C to 125°C		9.7			9.7		
	Input offset voltage long-term drift (see Note 5)			25°C		0.04			0.04		µV/mo
I_{IO}	Input offset current	$V_O = 0$, $V_{IC} = 0$, See Figure 5		25°C		1	100		1	100	pA
				125°C		0.2	10		0.2	10	nA
I_{IB}	Input bias current	$V_O = 0$, $V_{IC} = 0$, See Figure 5		25°C		2	200		2	200	pA
				125°C		7	20		8	20	nA
V_{ICR}	Common-mode input voltage range			25°C	−1.5 to 4	−3.4 to 5.4		−11.5 to 14	−13.4 to 15.4		V
				Full range	−1.5 to 4			−11.5 to 14			
V_{OM+}	Maximum positive peak output voltage swing	$R_L = 10\ k\Omega$		25°C	3	4.3		13	14		V
				−55°C	3	4.1		13	14		
				125°C	3	4.4		13	14		
V_{OM-}	Maximum negative peak output voltage swing	$R_L = 10\ k\Omega$		25°C	−3	−4.2		−12.5	−13.9		V
				−55°C	−3	−4		−12.5	−13.8		
				125°C	−3	−4.3		−12.5	−14		
A_{VD}	Large-signal differential voltage amplification	$R_L = 10\ k\Omega$, See Note 6		25°C	4	12		5	14.3		V/mV
				−55°C	3	7.1		4	10.4		
				125°C	3	12.9		4	15		
r_i	Input resistance			25°C		10^{12}			10^{12}		Ω
C_i	Input capacitance			25°C		5			4		pF
CMRR	Common-mode rejection ratio	$V_{IC} = V_{ICR}$ min, $V_O = 0$, $R_S = 50\ \Omega$		25°C	70	87		75	94		dB
				−55°C	70	87		70	94		
				125°C	70	87		70	94		
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm} / \Delta V_{IO}$)	$V_{CC\pm} = \pm 5$ V to ± 15 V, $V_O = 0$, $R_S = 50\ \Omega$		25°C	75	96		75	96		dB
				−55°C	75	95		75	95		
				125°C	75	96		75	96		
P_D	Total power dissipation (two amplifiers)	No load, $V_O = 0$		25°C		3.8	5		13	17	mW
				−55°C		2.3	5		9.4	17	
				125°C		3.6	5		11.8	17	
I_{CC}	Supply current (two amplifiers)	No load, $V_O = 0$		25°C		384	500		434	560	µA
				−55°C		228	500		312	560	
				125°C		356	500		394	560	
V_{o1}/V_{o2}	Crosstalk attenuation	$A_{VD} = 100$		25°C		120			120		dB

† Full range is − 55°C to 125°C.

NOTES: 5. Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at $T_A = 150$°C extrapolated to $T_A = 25$°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

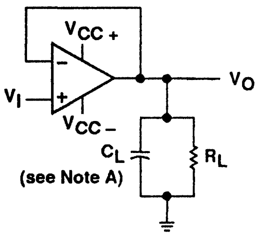
6. At $V_{CC\pm} = \pm 5$ V, $V_O = \pm 2.3$ V; at $V_{CC\pm} = \pm 15$ V, $V_O = \pm 10$ V.

operating characteristics

PARAMETER			TEST CONDITIONS		T_A	$V_{CC\pm} = \pm5$ V			$V_{CC\pm} = \pm15$ V			UNIT
						MIN	TYP	MAX	MIN	TYP	MAX	
SR +	Positive slew rate at unity gain		R_L = 10 kΩ, C_L = 100 pF, See Figure 1, See Note 7		25°C		2		2	2.9		V/μs
					– 55°C		1.4		1.2	1.9		
					125°C		2.4		1.2	3.5		
SR –	Negative slew rate at unity gain				25°C		3.9		3	5.1		V/μs
					– 55°C		3.2		2.5	4.6		
					125°C		4.1		2.5	4.7		
t_r	Rise time		V_{IPP} = ± 10 mV, R_L = 10 kΩ, C_L = 100 pF, See Figures 1 and 2		25°C		138			132		ns
					– 55°C		142			123		
					125°C		166			158		
t_f	Fall time				25°C		138			132		ns
					– 55°C		142			123		
					125°C		166			158		
	Overshoot factor				25°C		11%			5%		
					– 55°C		16%			6%		
					125°C		14%			8%		
V_n	Equivalent input noise voltage	TL032M	R_S = 100 Ω, See Figure 3	f = 10 Hz	25°C		49			49		nV/√Hz
				f = 1 kHz			41			41		
		TL032AM		f = 10 Hz	25°C		49			49		
				f = 1 kHz			41			41		
I_n	Equivalent input noise current		f = 1 kHz		25°C		0.003			0.003		pA/√Hz
B1	Unity-gain bandwidth		V_i = 10 mV, R_L = 10 kΩ, C_L = 25 pF, See Figure 4		25°C		1			1.1		MHz
					– 55°C		1			1.1		
					125°C		0.9			0.9		
ϕ_m	Phase margin at unity gain		V_i = 10 mV, R_L = 10 kΩ, C_L = 25 pF, See Figure 4		25°C		61°			65°		
					– 55°C		57°			64°		
					125°C		59°			62°		

NOTE 7: For $V_{CC\pm} = \pm5$ V, $V_{IPP} = \pm1$ V; for $V_{CC\pm} = \pm15$ V, $V_{IPP} = \pm5$ V.

PARAMETER MEASUREMENT INFORMATION



NOTE A: C_L includes fixture capacitance.

Figure 1. Slew Rate, Rise/Fall Time, and Overshoot Test Circuit

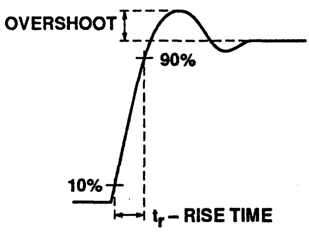


Figure 2. Rise Time and Overshoot Waveform

PARAMETER MEASUREMENT INFORMATION

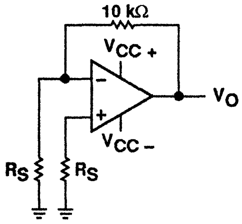
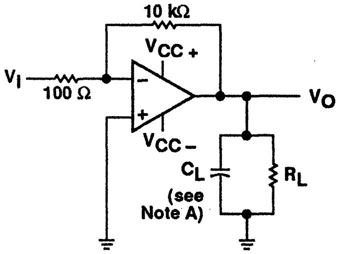


Figure 3. Noise Voltage Test Circuit



NOTE A: C_L includes fixture capacitance.

Figure 4. Unity-Gain Bandwidth and Phase Margin Test Circuit

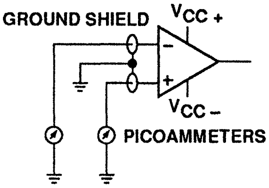


Figure 5. Input Bias and Offset Current Test Circuit

typical values

Typical values as presented in this data sheet represent the median (50% point) of device parametric performance.

input bias and offset current

At the picoamp bias current level typical of the TL032 and TL032A, accurate measurement of the bias current becomes difficult. Not only does this measurement require a picoammeter, but test socket leakages can easily exceed the actual device bias currents. To accurately measure these small currents Texas Instruments uses a two step process. The socket leakage is measured using picoammeters with bias voltages applied but with no device in the socket. The device is then inserted into the socket and a second test that measures both the socket leakage and the device input bias current is performed. The two measurements are then subtracted algebraically to determine the bias current of the device.

noise

Because of the increasing emphasis on low noise levels in many of today's applications, the input noise voltage density is sample-tested at f = 1 kHz. Texas Instruments also has additional noise testing capability to meet specific application requirements. Please contact the factory for details.

TYPICAL CHARACTERISTICS

table of graphs

			FIGURE
V_{IO}	Input offset voltage	Distribution	6
α_{VIO}	Temperature coefficient of input offset voltage	Distribution	7
I_{IO}	Input offset current	vs Temperature	8
I_{IB}	Input bias current	vs V_{IC} vs Temperature	9 8
V_I	Input voltage range	vs V_{CC} vs Temperature	10 11
V_{ID}	Differential input voltage	vs Output voltage	12, 13
V_{OM}	Maximum peak output voltage swing	vs V_{CC} vs Output current vs Frequency vs Temperature	14 16, 17 15 18, 19
A_{VD}	Differential voltage amplification	vs R_L vs Frequency vs Temperature	20 21 22
z_o	Output impedance	vs Frequency	23
CMRR	Common-mode rejection ratio	vs Frequency vs Temperature	24, 25 26
k_{SVR}	Supply-voltage rejection ratio	vs Temperature	27
I_{OS}	Short-circuit output current	vs V_{CC} vs Time vs Temperature	28 29 30
I_{CC}	Supply current	vs V_{CC} vs Temperature	32 33
SR	Slew rate	vs R_L vs Temperature	34, 35 36, 37
	Overshoot factor	vs C_L	38
V_n	Equivalent input noise voltage	vs Frequency	31
THD	Total harmonic distortion	vs Frequency	39
B_1	Unity-gain bandwidth	vs V_{CC} vs Temperature	40 41
ϕ_m	Phase margin	vs V_{CC} vs C_L vs Temperature	42 43 44
	Phase shift	vs Frequency	21
	Pulse response	Small-signal Large-signal	45 46, 47

TYPICAL CHARACTERISTICS†

DISTRIBUTION OF TL032
INPUT OFFSET VOLTAGE

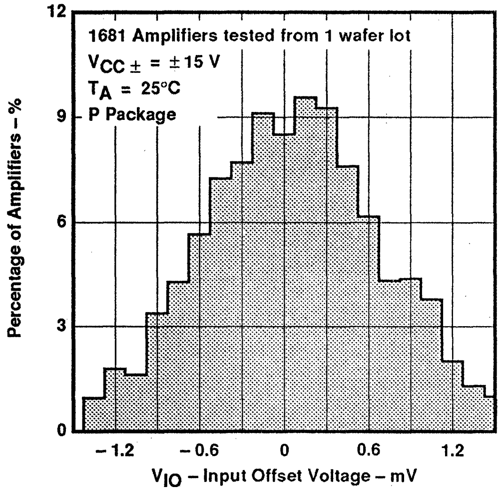


Figure 6

DISTRIBUTION OF TL032
INPUT OFFSET VOLTAGE
TEMPERATURE COEFFICIENT

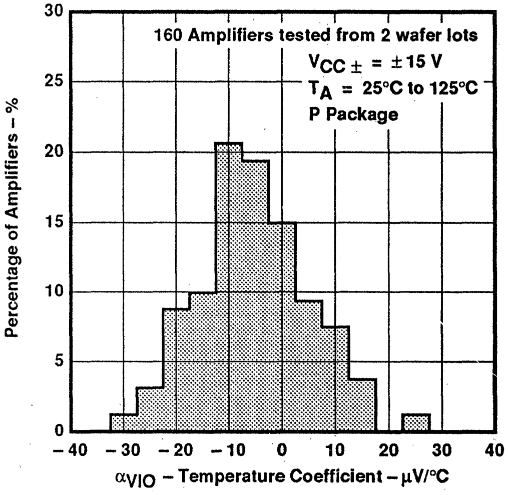


Figure 7

INPUT BIAS CURRENT AND
INPUT OFFSET CURRENT
vs
FREE-AIR TEMPERATURE

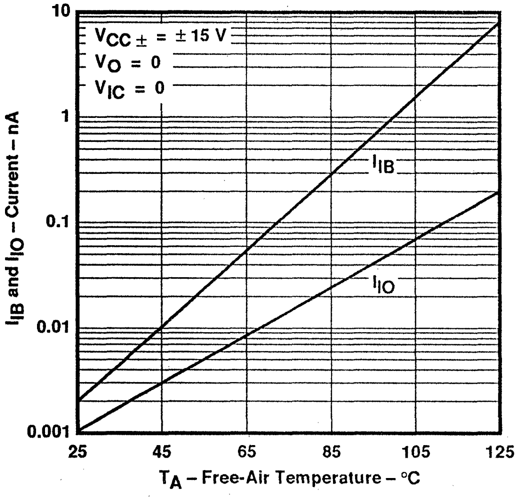


Figure 8

INPUT BIAS CURRENT
vs
COMMON-MODE INPUT VOLTAGE

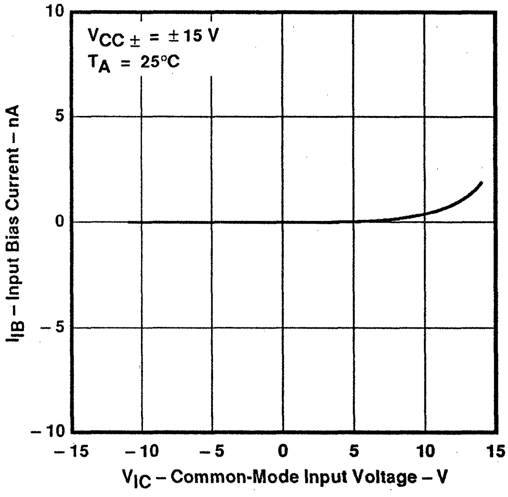


Figure 9

---

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

COMMON-MODE
INPUT VOLTAGE RANGE LIMITS
vs
SUPPLY VOLTAGE

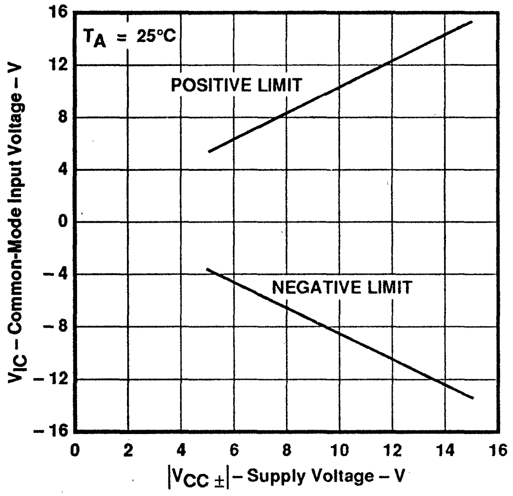


Figure 10

COMMON-MODE
INPUT VOLTAGE RANGE LIMITS
vs
FREE-AIR TEMPERATURE

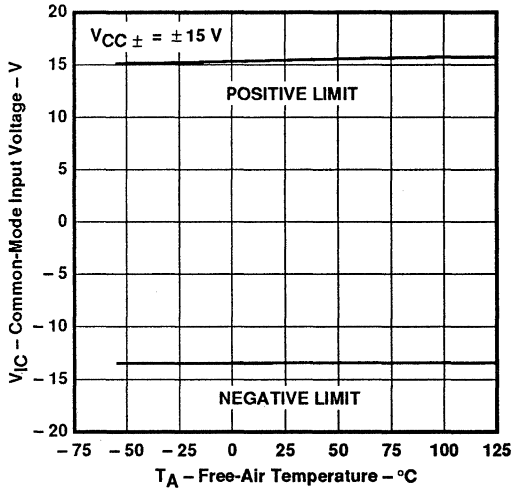


Figure 11

DIFFERENTIAL INPUT VOLTAGE
vs
OUTPUT VOLTAGE

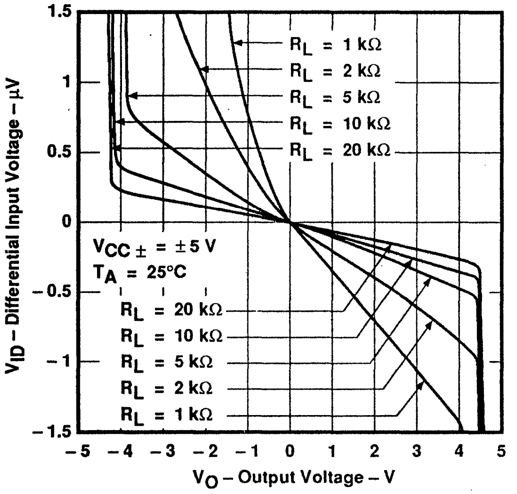


Figure 12

DIFFERENTIAL INPUT VOLTAGE
vs
OUTPUT VOLTAGE

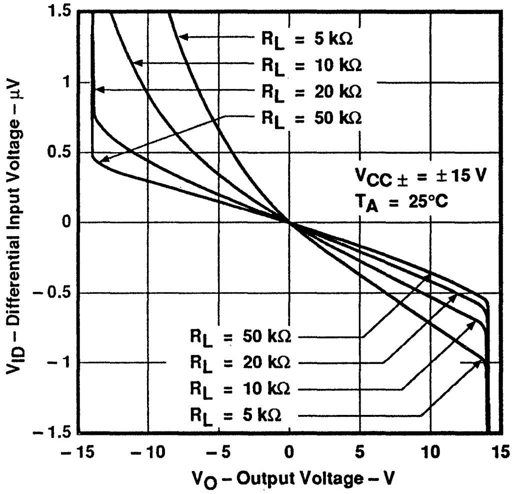


Figure 13

---

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS[†]

MAXIMUM PEAK OUTPUT VOLTAGE
vs
SUPPLY VOLTAGE

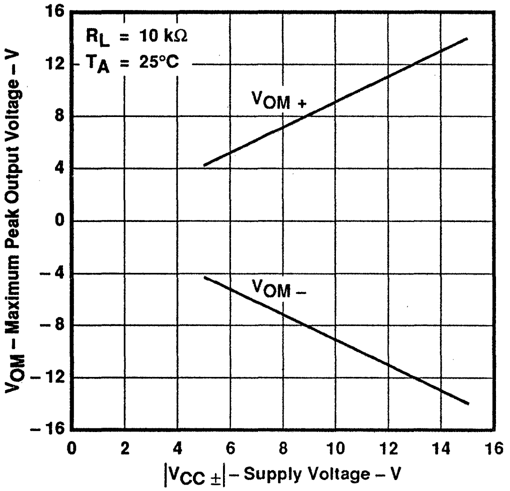


Figure 14

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE
vs
FREQUENCY

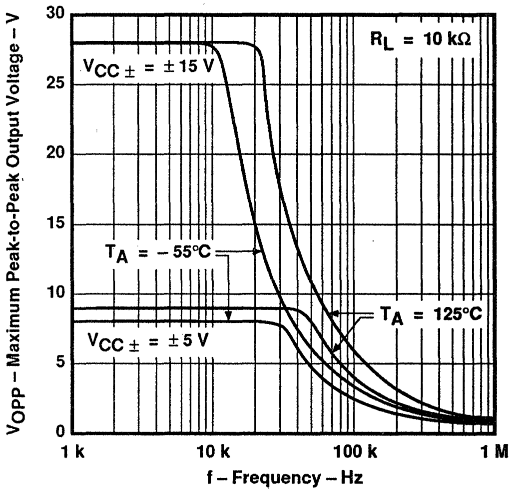


Figure 15

MAXIMUM PEAK OUTPUT VOLTAGE
vs
OUTPUT CURRENT

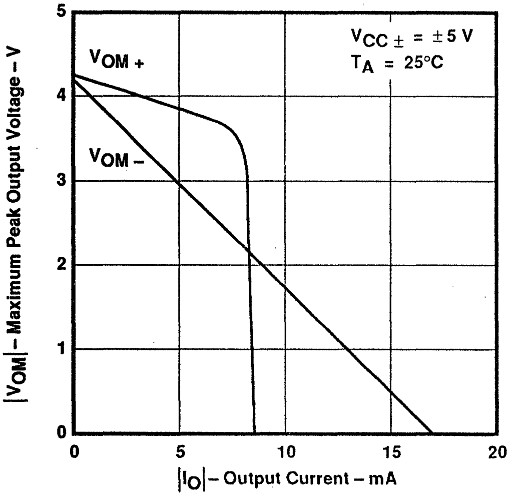


Figure 16

MAXIMUM PEAK OUTPUT VOLTAGE
vs
OUTPUT CURRENT

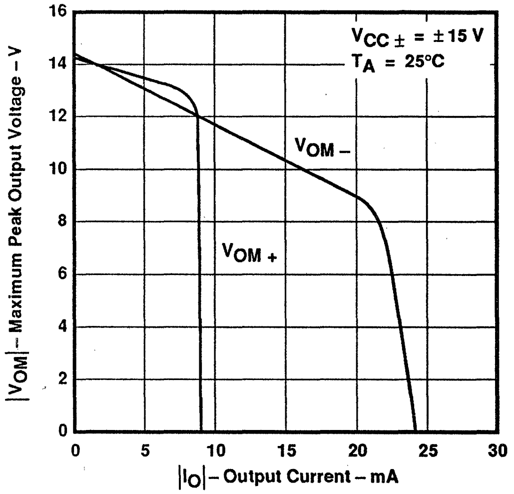


Figure 17

[†] Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

MAXIMUM PEAK OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

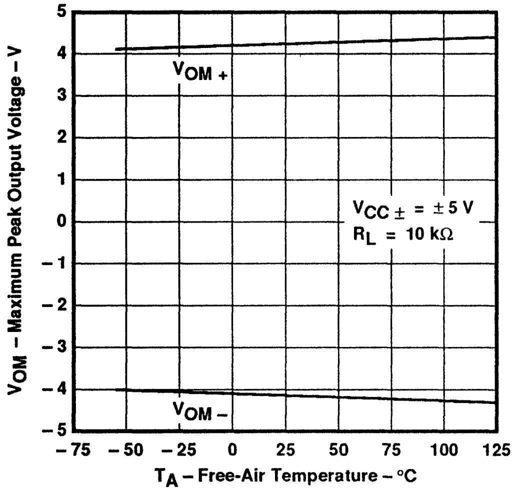


Figure 18

MAXIMUM PEAK OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

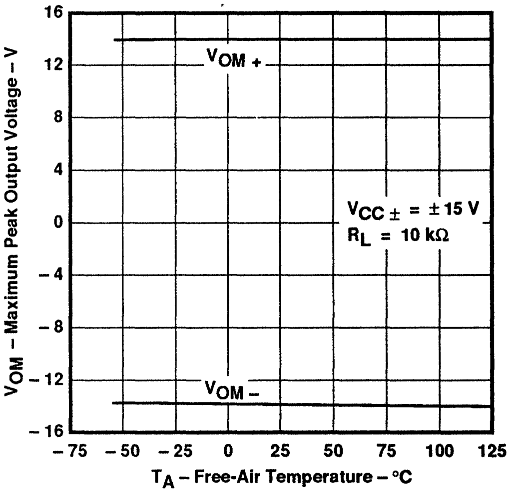


Figure 19

LARGE-SIGNAL VOLTAGE AMPLIFICATION
vs
LOAD RESISTANCE

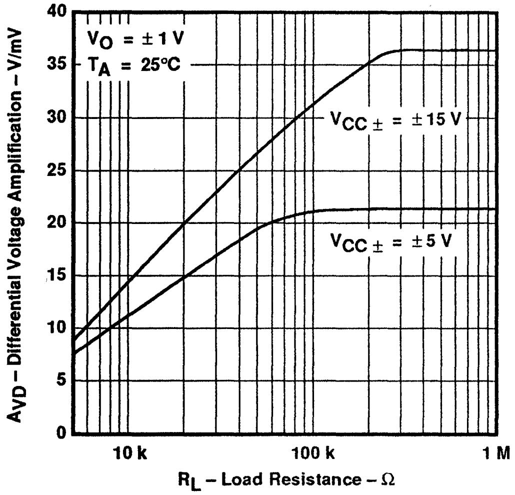


Figure 20

LARGE-SIGNAL DIFFERENTIAL VOLTAGE
AMPLIFICATION AND PHASE SHIFT
vs
FREQUENCY

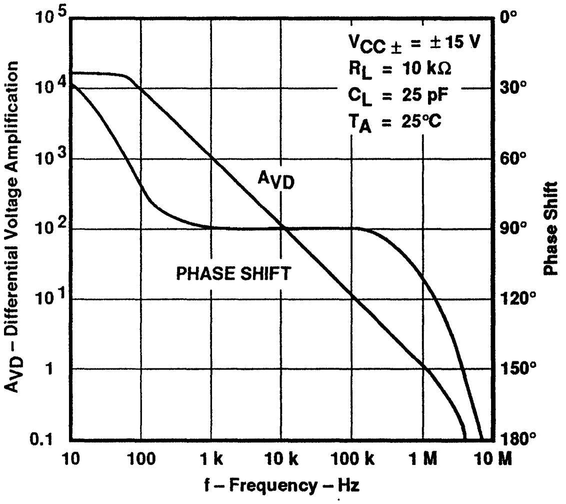


Figure 21

---

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

LARGE-SIGNAL VOLTAGE AMPLIFICATION
vs
FREE-AIR TEMPERATURE

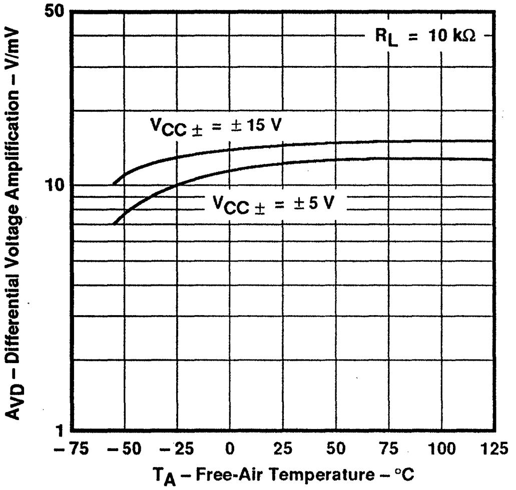


Figure 22

OUTPUT IMPEDANCE
vs
FREQUENCY

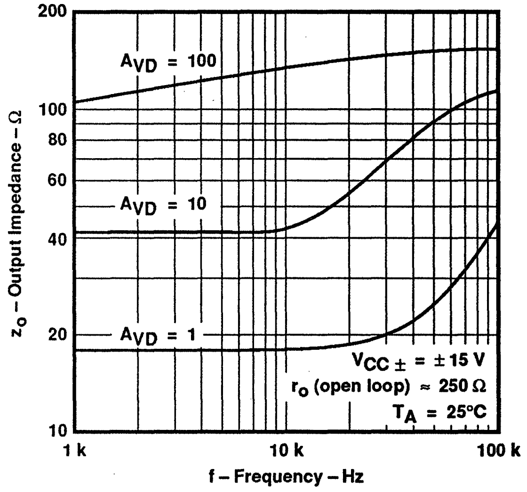


Figure 23

COMMON-MODE REJECTION RATIO
vs
FREQUENCY

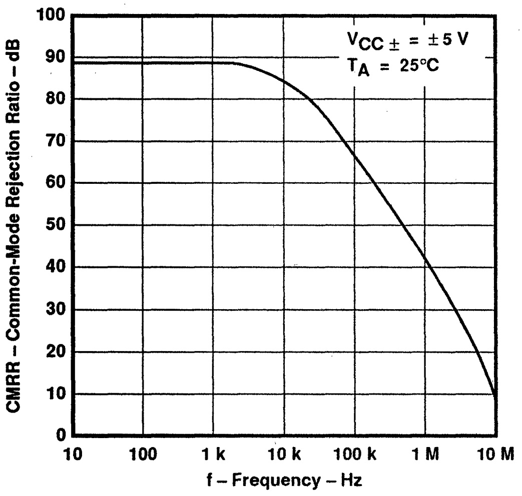


Figure 24

COMMON-MODE REJECTION RATIO
vs
FREQUENCY

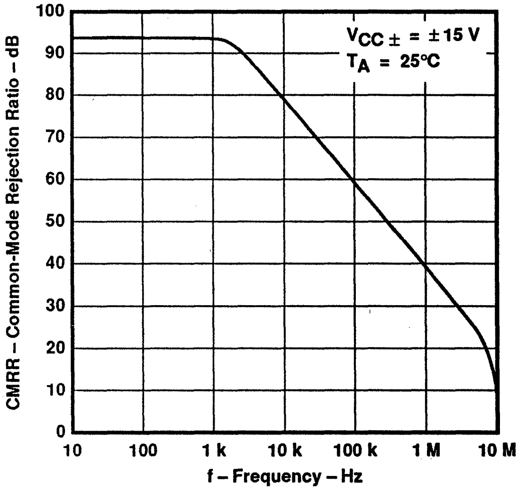


Figure 25

---

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS[†]

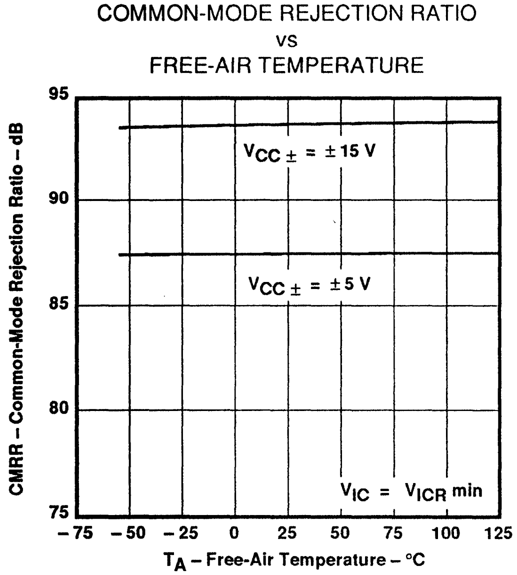


Figure 26

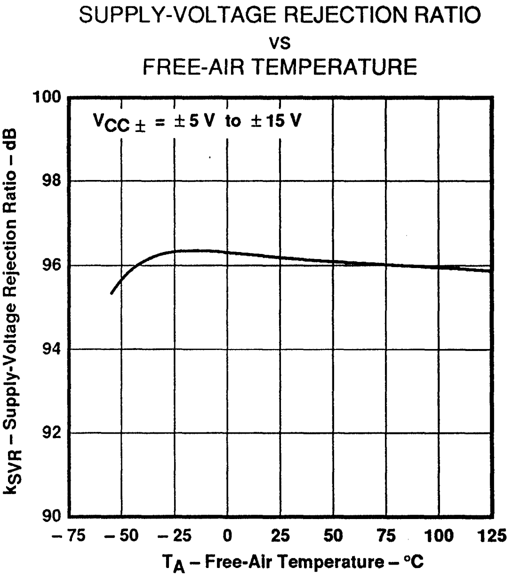


Figure 27

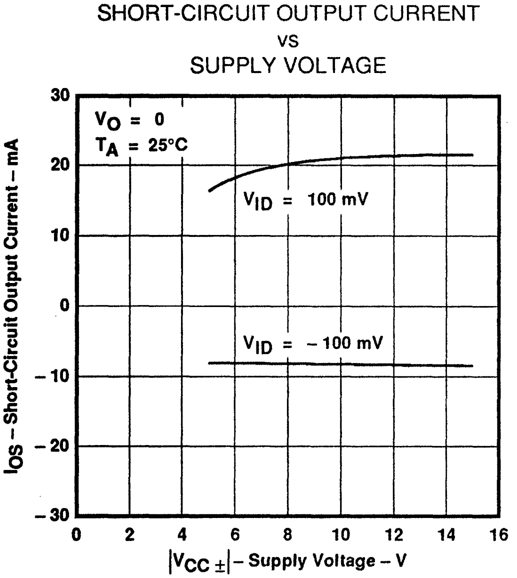


Figure 28

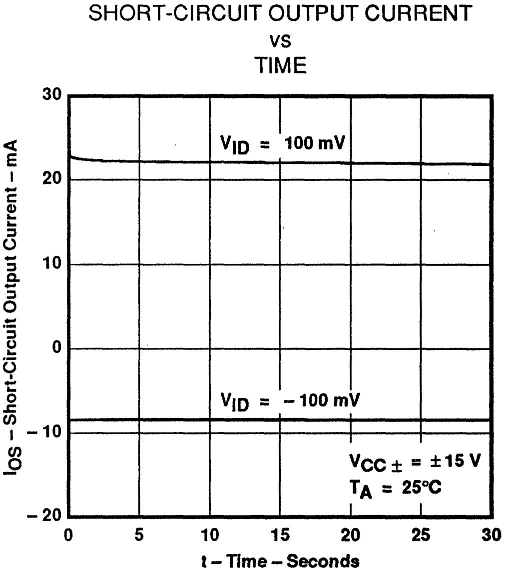


Figure 29

[†] Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

SHORT-CIRCUIT OUTPUT CURRENT
vs
FREE-AIR TEMPERATURE

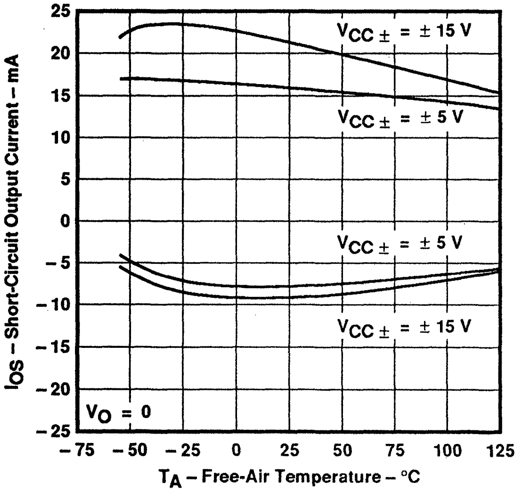


Figure 30

EQUIVALENT INPUT NOISE VOLTAGE
vs
FREQUENCY

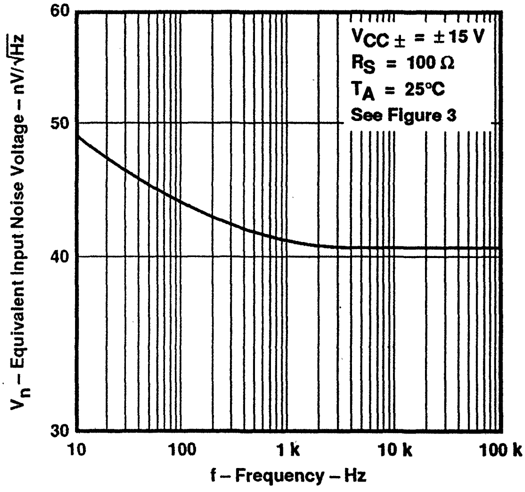


Figure 31

SUPPLY CURRENT
vs
SUPPLY VOLTAGE

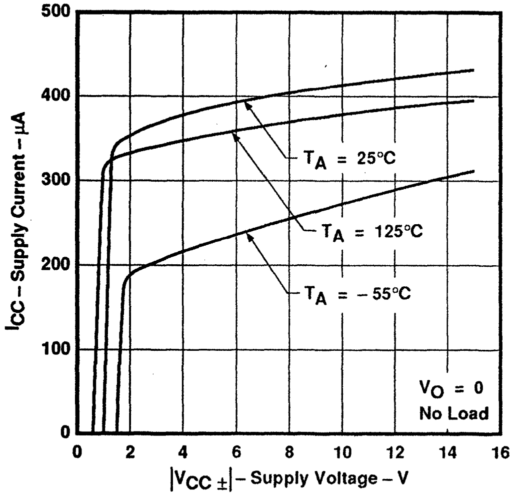


Figure 32

SUPPLY CURRENT
vs
FREE-AIR TEMPERATURE

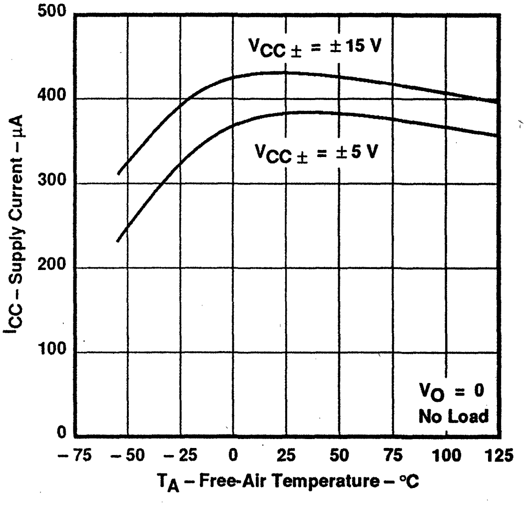


Figure 33

---

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

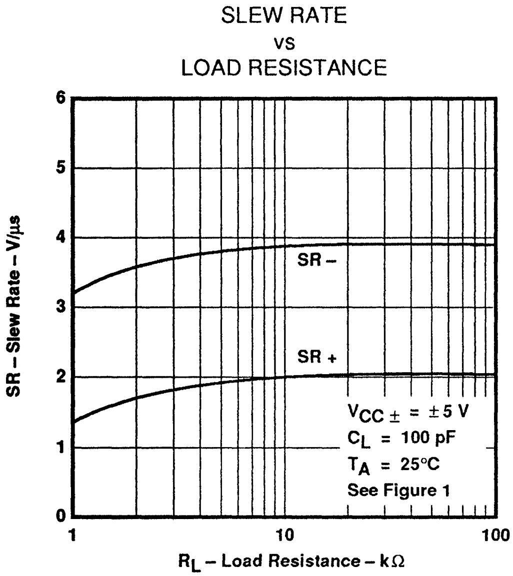


Figure 34

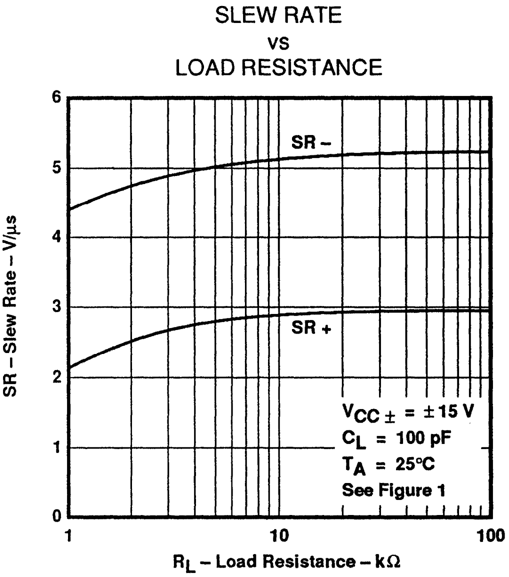


Figure 35

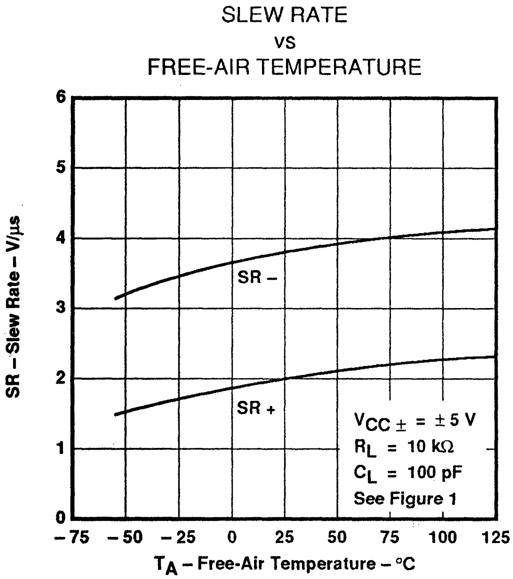


Figure 36

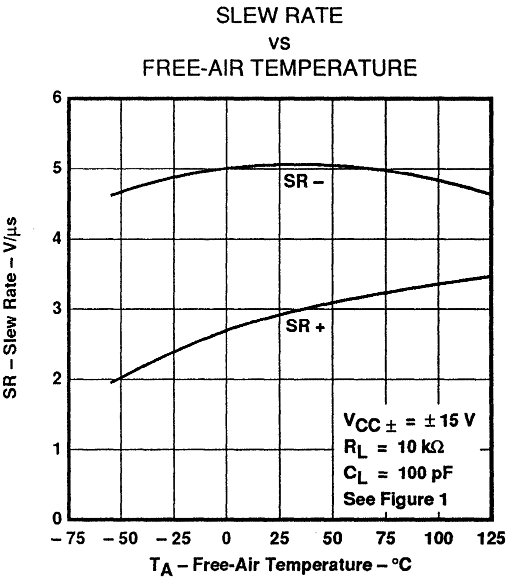


Figure 37

---

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

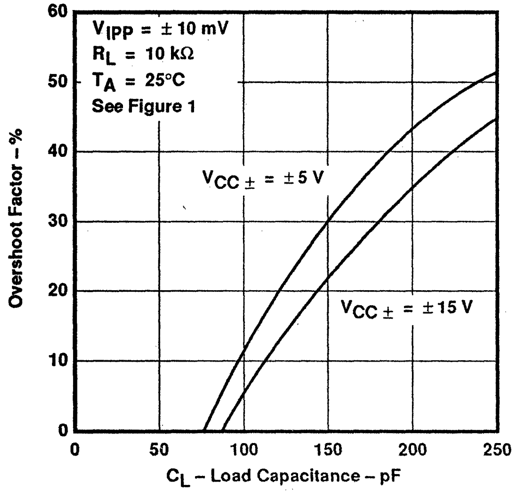

OVERSHOOT FACTOR
vs
LOAD CAPACITANCE

Figure 38

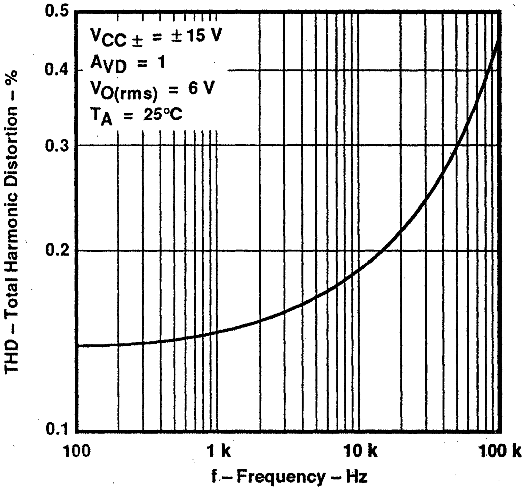

TOTAL HARMONIC DISTORTION
vs
FREQUENCY

Figure 39

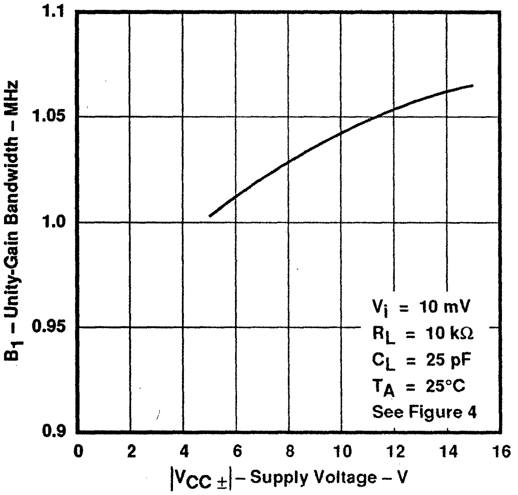

UNITY-GAIN BANDWIDTH
vs
SUPPLY VOLTAGE

Figure 40

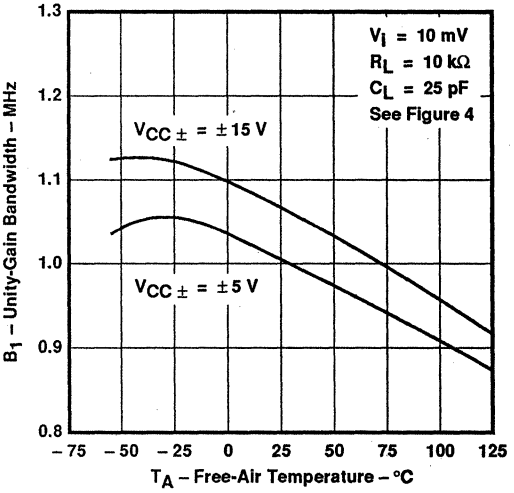

UNITY-GAIN BANDWIDTH
vs
FREE-AIR TEMPERATURE

Figure 41

---

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS[†]

PHASE MARGIN
vs
SUPPLY VOLTAGE

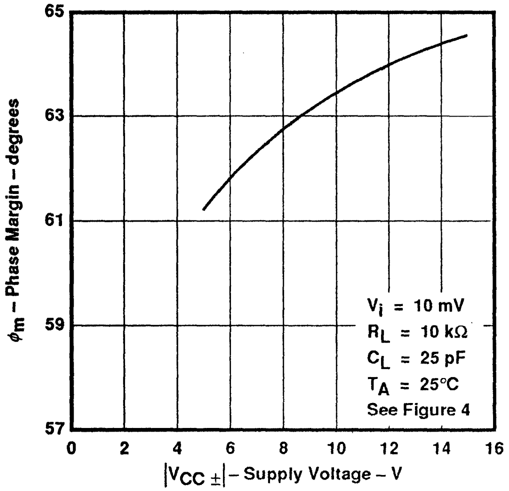


Figure 42

PHASE MARGIN
vs
LOAD CAPACITANCE

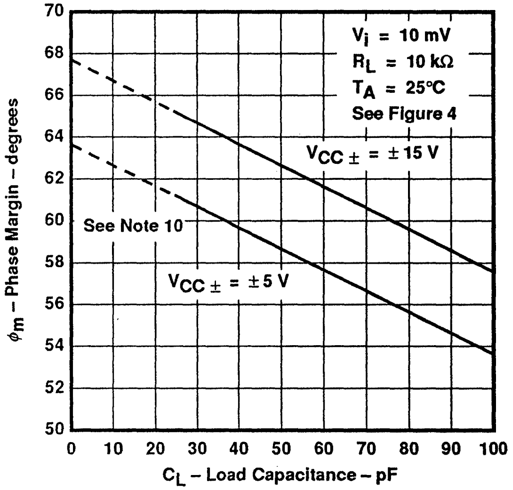


Figure 43

PHASE MARGIN
vs
FREE-AIR TEMPERATURE

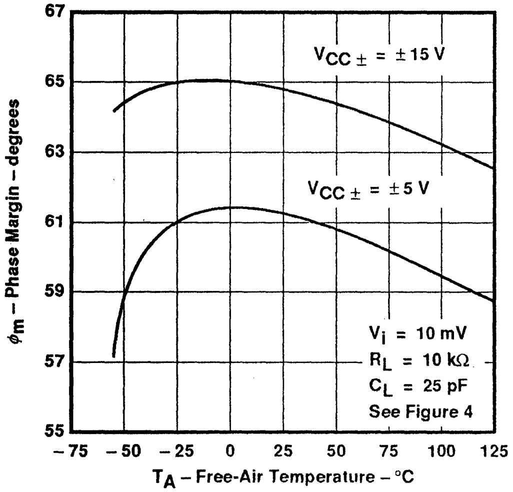


Figure 44

VOLTAGE-FOLLOWER
SMALL-SIGNAL
PULSE RESPONSE

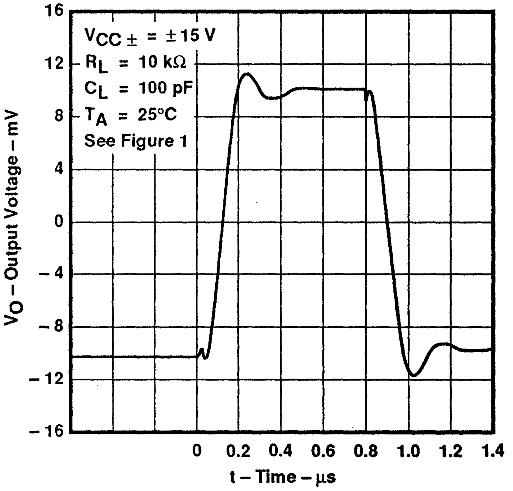


Figure 45

[†] Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

NOTE 10: Values of phase margin below a load capacitance of 25 pF were estimated.

TYPICAL CHARACTERISTICS

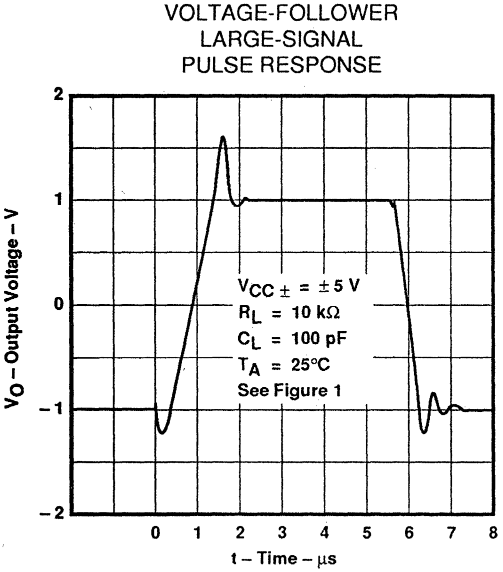


Figure 46

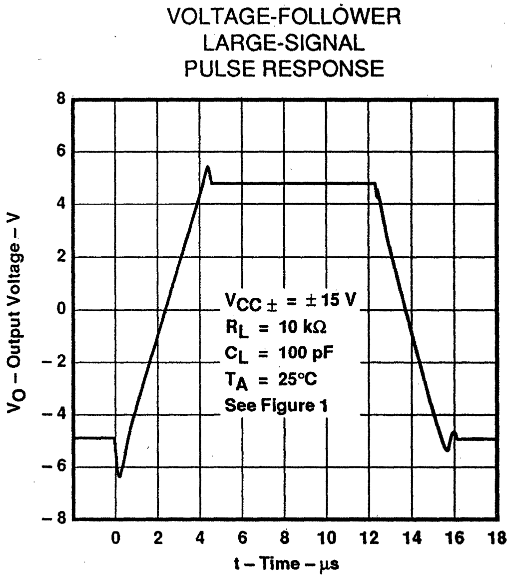


Figure 47

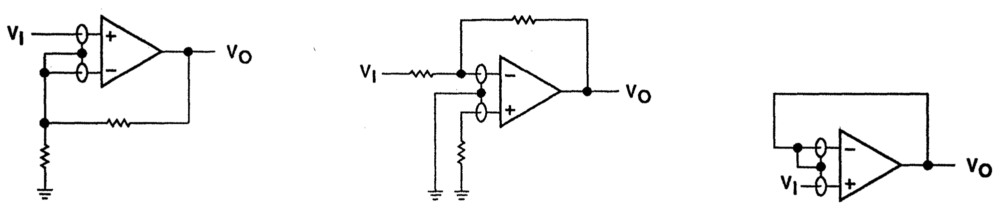
APPLICATION INFORMATION

input characteristics

The TL032 and TL032A are specified with a minimum and a maximum input voltage that, if exceeded at either input, could cause the device to malfunction.

Because of the extremely high input impedance and resulting low bias current requirements, the TL032 and TL032A are well-suited for low-level signal processing; however, leakage currents on printed circuit boards and sockets can easily exceed bias current requirements and cause degradation in system performance. It is a good practice to include guard rings around inputs (see Figure 48). These guards should be driven from a low-impedance source at the same voltage level as the common-mode input.

The inputs of any unused amplifiers should be tied to ground to avoid possible oscillation.



(a) NONINVERTING AMPLIFIER

(b) INVERTING AMPLIFIER

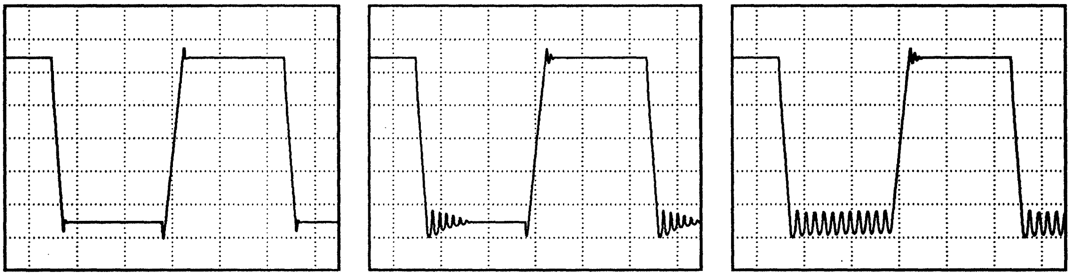
(c) UNITY-GAIN AMPLIFIER

Figure 48. Use of Guard Rings

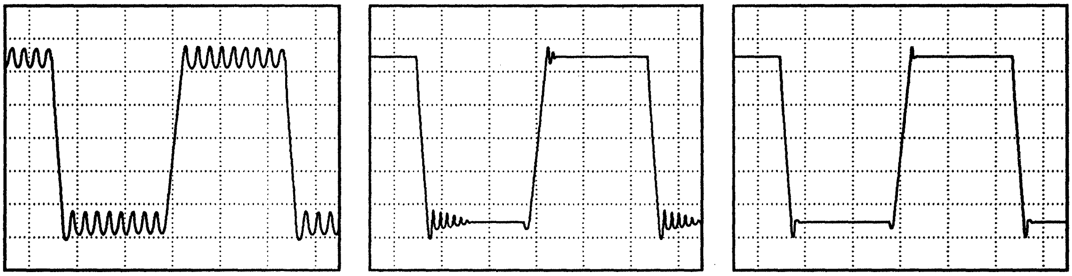
APPLICATION INFORMATION

output characteristics

All operating characteristics (except bandwidth and phase margin) are specified with 100 pF load capacitance. The TL032 and TL032A will drive higher capacitive loads; however, as the load capacitance increases, the resulting response pole occurs at lower frequencies, thereby causing ringing, peaking, or even oscillation. The value of the load capacitance at which oscillation occurs varies with production lots. If an application appears to be sensitive to oscillation due to load capacitance, adding a small resistance in series with the load should alleviate the problem. Capacitive loads of 1000 pF and larger may be driven if enough resistance is added in series with the output (see Figure 49).

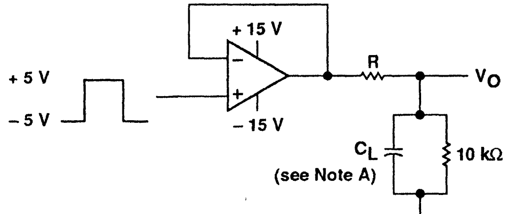


(a) C_L = 100 pF, R = 0 (b) C_L = 300 pF, R = 0 (c) C_L = 350 pF, R = 0



(d) C_L = 1000 pF, R = 0 (e) C_L = 1000 pF, R = 50 Ω (f) C_L = 1000 pF, R = 2 kΩ

Figure 49. Effect of Capacitive Loads



NOTE A: C_L includes fixture capacitance.

Figure 50. Test Circuit for Output Characteristics

APPLICATION INFORMATION

high-Q notch filter

In general, Texas Instruments enhanced JFET operational amplifiers serve as excellent filters. This circuit provides a narrow notch at a specific frequency. Notch filters are designed to eliminate frequencies that are interfering with the operation of an application. For this filter, the center frequency can be calculated as:

$$f_O = \frac{1}{2\pi R1C1}$$

With the resistors and capacitors shown below, the center frequency is 1 kHz. Note that C1 = C3 = C2 ÷ 2 and also that R1 = R3 = 2 × R2. The center frequency can be modified by varying these values. When adjusting the center frequency, be sure that the operational amplifier still has sufficient gain at the frequency of interest.

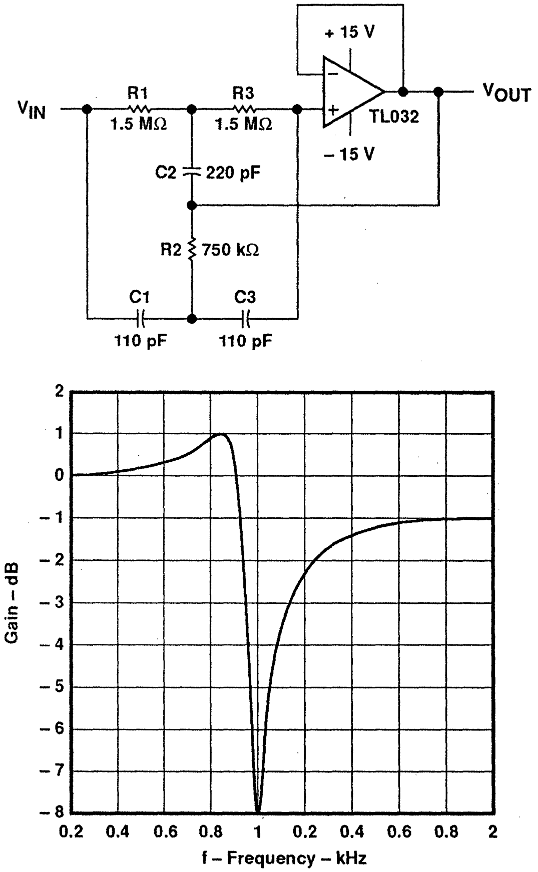


Figure 51. High-Q Notch Filter

APPLICATION INFORMATION

2-wire 4- to 20-mA current loop

Often information from an analog sensor must be sent over a distance to the receiving circuitry. For many applications, the most feasible method involves converting voltage information to a current before transmission. The following circuit benefits from the high input impedance of the TL032A since many inexpensive sensors do not have low output impedance.

Assuming that the voltage at the TL032A's non-inverting input is zero, the following equation determines the output current:

$$I_O = V_{IN}\left(\frac{R3}{R1 \times R_S}\right) + 5\,V\left(\frac{R3}{R2 \times R_S}\right) = 0.16 \times V_{IN} + 4\ \text{mA}$$

The current presently provides 4 to 20 mA output for an input voltage of 0 to 100 mV. By modifying R1, R2, and R3, the input voltage range or the output current range can be adjusted.

Including the offset voltage of the operational amplifier in the above equation clearly illustrates why the low offset TL032A was chosen:

$$I_O = V_{IN}\left(\frac{R3}{R1 \times R_S}\right) + 5\,V\left(\frac{R3}{R2 \times R_S}\right) - V_{IO}\left(\frac{R3}{R1 \times R_S} + \frac{R3}{R2 \times R_S} + \frac{R1}{R_S}\right) = 0.16 \times V_{IN} + 4\ \text{mA} - 0.17 \times V_{IO}$$

For example, an offset voltage of 1 mV decreases the output current by 0.17 mA.

Thanks to the low-power consumption of the TL032A, this circuit has at least 2 mA available to drive the actual sensor from the 5-V reference node.

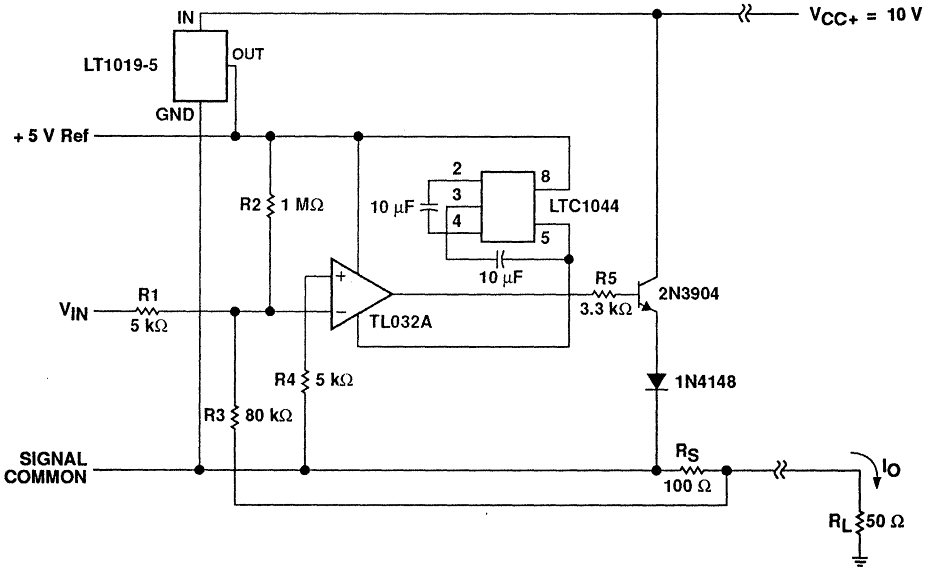


Figure 52. 2-Wire 4- to 20-mA Current Loop

APPLICATION INFORMATION

low-level light detector preamplifier

Applications that need to detect small currents require high input impedance operational amplifiers; otherwise, the bias currents of the operational amplifier camouflage the current being monitored. Phototransistors provide a current that is proportional to the light reaching the transistor. The TL032 allows even the small currents resulting from low-level light to be detected.

In this circuit, if there is no light, the phototransistor is off and the output is high. As light is detected, the operational amplifier output begins pulling low. Adjusting R4 both compensates for offset voltage of the amplifier and adjusts the point of light detection by the amplifier.

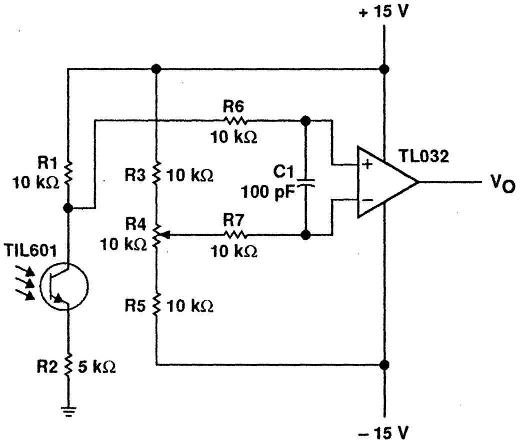


Figure 53. Low-Level Light Detector Preamplifier

TL034, TL034A
ENHANCED JFET LOW-POWER LOW-OFFSET QUAD OPERATIONAL AMPLIFIERS

D3153, JULY 1988 – REVISED FEBRUARY 1991

- **Maximum Offset Voltage . . . 1.5 mV**
- **High Slew Rate . . . 2.9 V/µs Typ**
- **Low Input Bias Current . . . 2 pA Typ**
- **Very Low Power Consumption . . . 26 mW Typ**
- **Output Short-Circuit Protection**
- **Monolithic Construction**

description

The TL034 and TL034A quadruple operational amplifiers incorporate well-matched, high-voltage JFET and bipolar transistors in a monolithic integrated circuit. These devices offer the significant advantages of Texas Instruments new enhanced JFET process. This process affords not only low initial offset voltage due to the on-chip zener trim capability but also stable offset voltage over time and temperature. In comparison, traditional JFET processes are plagued by significant offset voltage drift.

This new enhanced process still maintains the traditional JFET advantages of fast slew rates and low input bias and offset currents. These advantages, coupled with low power consumption, make the TL034 well-suited for new state-of-the-art designs as well as existing design upgrades. The TL034 has been designed to be functionally compatible and pin compatible with the TL064.

Two offset voltage grades are available:
TL034 (4 mV max) and TL034A (1.5 mV max).

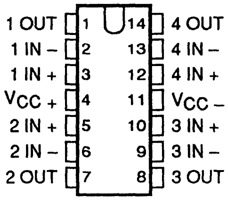
A variety of available packaging options includes small-outline and chip carrier versions for high density system applications.

AVAILABLE OPTIONS

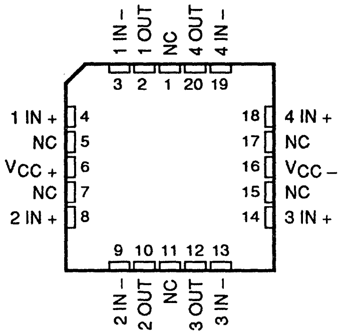
T_A	V_{IO} max AT 25°C	PACKAGE			
		SMALL-OUTLINE (D)	CHIP CARRIER (FK)	CERAMIC DIP (J)	PLASTIC DIP (N)
0°C to 70°C	1.5 mV	TL034ACD	——	——	TL034ACN
	4 mV	TL034CD	——	——	TL034CN
− 40°C to 85°C	1.5 mV	TL034AID	——	——	TL034AIN
	4 mV	TL034ID	——	——	TL034IN
− 55°C to 125°C	1.5 mV	TL034AMD	TL034AMFK	TL034AMJ	TL034AMN
	4 mV	TL034MD	TL034MFK	TL034MJ	TL034MN

D packages are available taped and reeled. Add "R" suffix to device type (e.g., TL034CDR).

D, J, or N PACKAGE
(TOP VIEW)

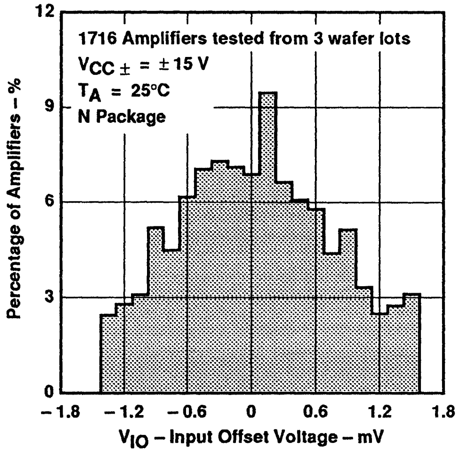


FK PACKAGE
(TOP VIEW)



NC – No internal connection

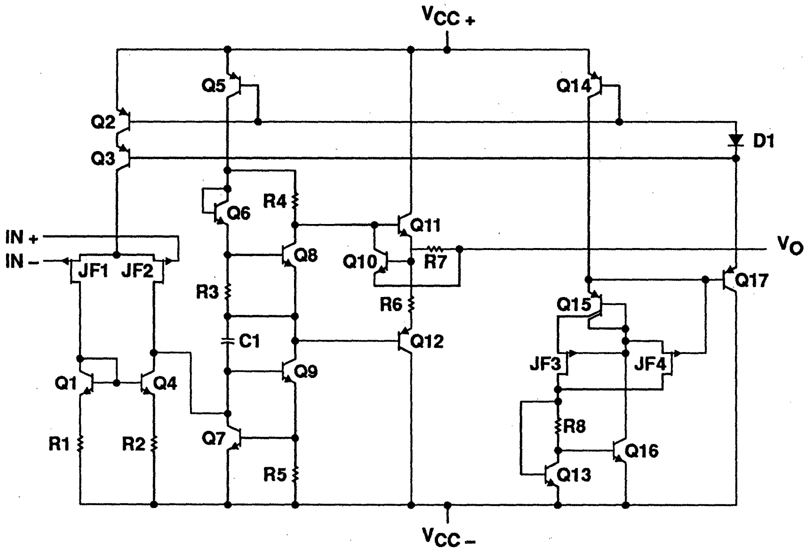
DISTRIBUTION OF TL034A
INPUT OFFSET VOLTAGE



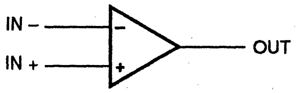
description (continued)

The C-suffix devices are characterized for operation from 0°C to 70°C. The I-suffix devices are characterized for operation from – 40°C to 85°C. The M-suffix devices are characterized for operation over the full military temperature range of – 55°C to 125°C.

equivalent schematic (each amplifier)



symbol (each amplifier)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC+} (see Note 1)	18 V
Supply voltage, V_{CC-} (see Note 1)	– 18 V
Differential input voltage (see Note 2)	± 30 V
Input voltage range, V_I (any input, see Notes 1 and 3)	± 15 V
Input current, I_I (each input)	± 1 mA
Output current, I_O (each output)	± 40 mA
Total current into V_{CC+} terminal	160 mA
Total current out of V_{CC-} terminal	160 mA
Duration of short-circuit current at (or below) 25°C (see Note 4)	unlimited
Continuous total dissipation	See Dissipation Rating Table
Operating free-air temperature range, T_A: C-suffix	0°C to 70°C
I-suffix	– 40°C to 85°C
M-suffix	– 55°C to 125°C
Storage temperature range	– 65°C to 150°C
Case temperature for 60 seconds: FK package	260°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D or N package	260°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: J package	300°C

NOTES:
1. All voltage values, except differential voltages, are with respect to the midpoint between V_{CC+} and V_{CC-}.
2. Differential voltages are at the noninverting input with respect to the inverting input.
3. The magnitude of the input voltage must never exceed the magnitude of the supply voltage or 15 V, whichever is less.
4. The output may be shorted to either supply. Temperature and/or supply voltages must be limited to ensure that the maximum dissipation rating is not exceeded.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING	$T_A = 125°C$ POWER RATING
D	950 mW	7.6 mW/°C	608 mW	494 mW	190 mW
FK	1375 mW	11.0 mW/°C	880 mW	715 mW	275 mW
J	1375 mW	11.0 mW/°C	880 mW	715 mW	275 mW
N	1150 mW	9.2 mW/°C	736 mW	598 mW	230 mW

recommended operating conditions

		C-SUFFIX			I-SUFFIX			M-SUFFIX			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		± 5		± 15	± 5		± 15	± 5		± 15	V
Common-mode input voltage, V_{IC}	$V_{CC\pm} = \pm 5$ V	– 1.5		4	– 1.5		4	– 1.5		4	V
	$V_{CC\pm} = \pm 15$ V	– 11.5		14	– 11.5		14	– 11.5		14	
Operating free-air temperature, T_A		0		70	– 40		85	– 55		125	°C

electrical characteristics

PARAMETER		TEST CONDITIONS		T_A†	$V_{CC\pm} = \pm5$ V			$V_{CC\pm} = \pm15$ V			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	$V_O = 0$, $V_{IC} = 0$, $R_S = 50\ \Omega$	TL034C	25°C		0.91	6		0.79	4	mV
				Full range			8.2			6.2	
			TL034AC	25°C		0.7	3.5		0.58	1.5	
				Full range			5.7			3.7	
α_{VIO}	Temperature coefficient of input offset voltage (see Note 7)		TL034C	25°C to 70°C		11.6			12		μV/°C
			TL034AC	25°C to 70°C		11.6			12	25	
	Input offset voltage long-term drift (see Note 5)			25°C		0.04			0.04		μV/mo
I_{IO}	Input offset current	$V_O = 0$, $V_{IC} = 0$, See Figure 5		25°C		1	100		1	100	pA
				70°C		9	200		12	200	
I_{IB}	Input bias current	$V_O = 0$, $V_{IC} = 0$, See Figure 5		25°C		2	200		2	200	pA
				70°C		50	400		80	400	
V_{ICR}	Common-mode input voltage range			25°C	− 1.5 to 4	− 3.4 to 5.4		− 11.5 to 14	− 13.4 to 15.4		V
				Full range	− 1.5 to 4			− 11.5 to 14			
V_{OM+}	Maximum positive peak output voltage swing	$R_L = 10\ k\Omega$		25°C	3	4.3		13	14		V
				0°C	3	4.2		13	14		
				70°C	3	4.3		13	14		
V_{OM-}	Maximum negative peak output voltage swing	$R_L = 10\ k\Omega$		25°C	− 3	− 4.2		− 12.5	− 13.9		V
				0°C	− 3	− 4.1		− 12.5	− 13.9		
				70°C	− 3	− 4.2		− 12.5	− 14		
A_{VD}	Large-signal differential voltage amplification	$R_L = 10\ k\Omega$, See Note 6		25°C	4	12		5	14.3		V/mV
				0°C	3	11.1		4	13.5		
				70°C	4	13.3		5	15.2		
r_i	Input resistance			25°C		10^{12}			10^{12}		Ω
C_i	Input capacitance			25°C		5			4		pF
CMRR	Common-mode rejection ratio	$V_{IC} = V_{ICR}$ min, $V_O = 0$, $R_S = 50\ \Omega$		25°C	70	87		75	94		dB
				0°C	70	87		75	94		
				70°C	70	87		75	94		
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm} / \Delta V_{IO}$)	$V_{CC\pm} = \pm5$ V to ± 15 V, $V_O = 0$, $R_S = 50\ \Omega$		25°C	75	96		75	96		dB
				0°C	75	96		75	96		
				70°C	75	96		75	96		
P_D	Total power dissipation (four amplifiers)	No load, $V_O = 0$		25°C		7.7	10		26	34	mW
				0°C		7.4	10		25.3	34	
				70°C		7.6	10		25.2	34	
I_{CC}	Supply current (four amplifiers)	No load, $V_O = 0$		25°C		0.77	1		0.87	1.12	mA
				0°C		0.74	1		0.85	1.12	
				70°C		0.76	1		0.84	1.12	
V_{o1}/V_{o2}	Crosstalk attenuation	$A_{VD} = 100$		25°C		120			120		dB

† Full range is 0°C to 70°C.

NOTES: 5. Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at $T_A = 150°C$ extrapolated to $T_A = 25°C$ using the Arrhenius equation and assuming an activation energy of 0.96 eV.

6. At $V_{CC\pm} = \pm5$ V, $V_O = \pm2.3$ V; at $V_{CC\pm} = \pm15$ V, $V_O = \pm10$ V.

7. This parameter is tested on a sample basis for the TL034A. For other test requirements, please contact the factory. This statement has no bearing on testing or nontesting of other parameters.

operating characteristics

PARAMETER			TEST CONDITIONS		T_A	$V_{CC\pm} = \pm 5$ V			$V_{CC\pm} = \pm 15$ V			UNIT
						MIN	TYP	MAX	MIN	TYP	MAX	
SR +	Positive slew rate at unity gain		$R_L = 10$ kΩ, $C_L = 100$ pF, See Figure 1, See Note 8		25°C		2		2	2.9		V/µs
					0°C		1.8		1.5	2.6		
					70°C		2.2		2	3.2		
SR –	Negative slew rate at unity gain				25°C		3.9		3.5	5.1		V/µs
					0°C		3.7		3.2	5.0		
					70°C		4		3.2	5.0		
t_r	Rise time		$V_{IPP} = \pm 10$ mV, $R_L = 10$ kΩ, $C_L = 100$ pF, See Figures 1 and 2		25°C		138			132		ns
					0°C		134			127		
					70°C		150			142		
t_f	Fall time				25°C		138			132		ns
					0°C		134			127		
					70°C		150			142		
	Overshoot factor				25°C		11%			5%		
					0°C		10%			4%		
					70°C		12%			6%		
V_n	Equivalent input noise voltage (see Note 9)	TL034C	$R_S = 100$ Ω, See Figure 3	f = 10 Hz	25°C		83			83		nV/√Hz
				f = 1 kHz			43			43		
		TL034AC		f = 10 Hz	25°C		83			83		
				f = 1 kHz			43			43	60	
I_n	Equivalent input noise current		f = 1 kHz		25°C		0.003			0.003		pA/√Hz
B1	Unity-gain bandwidth		$V_i = 10$ mV, $R_L = 10$ kΩ, $C_L = 25$ pF, See Figure 4		25°C		1			1.1		MHz
					0°C		1			1.1		
					70°C		1			1		
ϕ_m	Phase margin at unity gain		$V_i = 10$ mV, $R_L = 10$ kΩ, $C_L = 25$ pF, See Figure 4		25°C		61°			65°		
					0°C		61°			65°		
					70°C		60°			64°		

NOTES: 8. For $V_{CC\pm} = \pm 5$ V, $V_{IPP} = \pm 1$ V; for $V_{CC\pm} = \pm 15$ V, $V_{IPP} = \pm 5$ V.

9. This parameter is tested on a sample basis. For other test requirements, please contact the factory. This statement has no bearing on testing or nontesting of other parameters.

electrical characteristics

PARAMETER		TEST CONDITIONS		T_A†	$V_{CC\pm}$ = ±5 V			$V_{CC\pm}$ = ±15 V			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_O = 0, V_{IC} = 0, R_S = 50 Ω	TL034I	25°C		0.91	6		0.79	4	mV
				Full range			9.3			7.3	
			TL034AI	25°C		0.7	3.5		0.58	1.5	
				Full range			6.8			4.8	
α_{VIO}	Temperature coefficient of input offset voltage (see Note 7)		TL034I	25°C to 85°C		11.5			11.6		µV/°C
			TL034AI	25°C to 85°C		11.5			11.6	25	
	Input offset voltage long-term drift (see Note 5)			25°C		0.04			0.04		µV/mo
I_{IO}	Input offset current	V_O = 0, V_{IC} = 0, See Figure 5		25°C		1	100		1	100	pA
				85°C		0.02	0.45		0.02	0.45	nA
I_{IB}	Input bias current	V_O = 0, V_{IC} = 0, See Figure 5		25°C		2	200		2	200	pA
				85°C		0.2	0.9		0.3	0.9	nA
V_{ICR}	Common-mode input voltage range			25°C	− 1.5 to 4	− 3.4 to 5.4		− 11.5 to 14	− 13.4 to 15.4		V
				Full range	− 1.5 to 4			− 11.5 to 14			
V_{OM+}	Maximum positive peak output voltage swing	R_L = 10 kΩ		25°C	3	4.3		13	14		V
				− 40°C	3	4.1		13	14		
				85°C	3	4.4		13	14		
V_{OM-}	Maximum negative peak output voltage swing	R_L = 10 kΩ		25°C	− 3	− 4.2		− 12.5	− 13.9		V
				− 40°C	− 3	− 4.1		− 12.5	− 13.8		
				85°C	− 3	− 4.2		− 12.5	− 14		
A_{VD}	Large-signal differential voltage amplification	R_L = 10 kΩ, See Note 6		25°C	4	12		5	14.3		V/mV
				− 40°C	3	8.4		4	11.6		
				85°C	4	13.5		5	15.3		
r_i	Input resistance			25°C		10^{12}			10^{12}		Ω
C_i	Input capacitance			25°C		5			4		pF
CMRR	Common-mode rejection ratio	V_{IC} = V_{ICR} min, V_O = 0, R_S = 50 Ω		25°C	70	87		75	94		dB
				− 40°C	70	87		75	94		
				85°C	70	87		75	94		
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm} / \Delta V_{IO}$)	$V_{CC\pm}$ = ± 5 V to ± 15 V, V_O = 0, R_S = 50 Ω		25°C	75	96		75	96		dB
				− 40°C	75	96		75	96		
				85°C	75	96		75	96		
P_D	Total power dissipation (four amplifiers)	No load, V_O = 0		25°C		7.7	10		26	34	mW
				− 40°C		5.8	10		21.7	34	
				85°C		7.4	10		24.8	34	
I_{CC}	Supply current (four amplifiers)	No load, V_O = 0		25°C		0.77	1		0.87	1.12	mA
				− 40°C		0.58	1		0.72	1.12	
				85°C		0.74	1		0.83	1.12	
V_{O1}/V_{O2}	Crosstalk attenuation	A_{VD} = 100		25°C		120			120		dB

† Full range is − 40°C to 85°C.

NOTES: 5. Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at T_A = 150°C extrapolated to T_A = 25°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

6. At $V_{CC\pm}$ = ± 5 V, V_O = ± 2.3 V; at $V_{CC\pm}$ = ± 15 V, V_O = ± 10 V.

7. This parameter is tested on a sample basis for the TL034A. For other test requirements, please contact the factory. This statement has no bearing on testing or nontesting of other parameters.

operating characteristics

PARAMETER			TEST CONDITIONS		T_A	$V_{CC\pm} = \pm5$ V			$V_{CC\pm} = \pm15$ V			UNIT
						MIN	TYP	MAX	MIN	TYP	MAX	
SR +	Positive slew rate at unity gain		R_L = 10 kΩ, C_L = 100 pF, See Figure 1, See Note 8		25°C		2		2	2.9		V/µs
					−40°C		1.6		1.5	2.1		
					85°C		2.3		2	3.3		
SR −	Negative slew rate at unity gain				25°C		3.9		3.5	5.1		V/µs
					−40°C		3.3		3.2	4.8		
					85°C		4.1		3.2	4.9		
t_r	Rise time		V_{IPP} = ±10 mV, R_L = 10 kΩ, C_L = 100 pF, See Figures 1 and 2		25°C		138			132		ns
					−40°C		132			123		
					85°C		154			146		
t_f	Fall time				25°C		138			132		ns
					−40°C		132			123		
					85°C		154			146		
	Overshoot factor				25°C		11%			5%		
					−40°C		12%			5%		
					85°C		13%			7%		
V_n	Equivalent input noise voltage (see Note 9)	TL034I	R_S = 100 Ω, See Figure 3	f = 10 Hz	25°C		83			83		nV/√Hz
				f = 1 kHz			43			43		
		TL034AI		f = 10 Hz	25°C		83			83		
				f = 1 kHz			43			43	60	
I_n	Equivalent input noise current		f = 1 kHz		25°C		0.003			0.003		pA/√Hz
B1	Unity-gain bandwidth		V_i = 10 mV, R_L = 10 kΩ, C_L = 25 pF, See Figure 4		25°C		1			1.1		MHz
					−40°C		1			1.1		
					85°C		0.9			1		
ϕ_m	Phase margin at unity gain		V_i = 10 mV, R_L = 10 kΩ, C_L = 25 pF, See Figure 4		25°C		61°			65°		
					−40°C		60°			65°		
					85°C		60°			64°		

NOTES: 8. For $V_{CC\pm} = \pm5$ V, $V_{IPP} = \pm1$ V; for $V_{CC\pm} = \pm15$ V, $V_{IPP} = \pm5$ V.

9. This parameter is tested on a sample basis. For other test requirements, please contact the factory. This statement has no bearing on testing or nontesting of other parameters.

electrical characteristics

PARAMETER		TEST CONDITIONS		T_A†	$V_{CC\pm} = \pm 5$ V			$V_{CC\pm} = \pm 15$ V			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	$V_O = 0$, $V_{IC} = 0$, $R_S = 50\ \Omega$	TL034M	25°C		0.91	6		0.78	4	mV
				Full range			11			9	
			TL034AM	25°C		0.7	3.5		0.58	1.5	
				Full range			8.5			6.5	
α_{VIO}	Temperature coefficient of input offset voltage		TL034M	25°C to 125°C		10.6			10.9		µV/°C
			TL034AM	25°C to 125°C		10.6			10.9		
	Input offset voltage long-term drift (see Note 5)			25°C		0.04			0.04		µV/mo
I_{IO}	Input offset current	$V_O = 0$, $V_{IC} = 0$, See Figure 5		25°C		1	100		1	100	pA
				125°C		0.2	10		0.2	10	nA
I_{IB}	Input bias current	$V_O = 0$, $V_{IC} = 0$, See Figure 5		25°C		2	200		2	200	pA
				125°C		7	20		8	20	nA
V_{ICR}	Common-mode input voltage range			25°C	− 1.5 to 4	− 3.4 to 5.4		− 11.5 to 14	− 13.4 to 15.4		V
				Full range	− 1.5 to 4			− 11.5 to 14			
V_{OM+}	Maximum positive peak output voltage swing	$R_L = 10$ kΩ		25°C	3	4.3		13	14		V
				− 55°C	3	4.1		13	14		
				125°C	3	4.4		13	14		
V_{OM-}	Maximum negative peak output voltage swing	$R_L = 10$ kΩ		25°C	− 3	− 4.2		− 12.5	− 13.9		V
				− 55°C	− 3	− 4		− 12.5	− 13.8		
				125°C	− 3	− 4.3		− 12.5	− 14		
A_{VD}	Large-signal differential voltage amplification	$R_L = 10$ kΩ, See Note 6		25°C	4	12		5	14.3		V/mV
				− 55°C	3	7.1		4	10.4		
				125°C	3	12.9		4	15		
r_i	Input resistance			25°C		10^{12}			10^{12}		Ω
C_i	Input capacitance			25°C		5			4		pF
CMRR	Common-mode rejection ratio	$V_{IC} = V_{ICR}$ min, $V_O = 0$, $R_S = 50\ \Omega$		25°C	70	87		75	94		dB
				− 55°C	70	87		70	94		
				125°C	70	87		70	94		
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm} / \Delta V_{IO}$)	$V_{CC\pm} = \pm 5$ V to ± 15 V, $V_O = 0$, $R_S = 50\ \Omega$		25°C	75	96		75	96		dB
				− 55°C	75	95		75	95		
				125°C	75	96		75	96		
P_D	Total power dissipation (four amplifiers)	No load, $V_O = 0$		25°C		7.7	10		26	34	mW
				− 55°C		4.6	12		18.7	45	
				125°C		7.1	12		23.6	45	
I_{CC}	Supply current (four amplifiers)	No load, $V_O = 0$		25°C		0.77	1		0.87	1.12	mA
				− 55°C		0.46	1.2		0.62	1.5	
				125°C		0.71	1.2		0.79	1.5	
V_{O1}/V_{O2}	Crosstalk attenuation	$A_{VD} = 100$		25°C		120			120		dB

† Full range is − 55°C to 125°C.

NOTES: 5. Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at $T_A = 150°C$ extrapolated to $T_A = 25°C$ using the Arrhenius equation and assuming an activation energy of 0.96 eV.

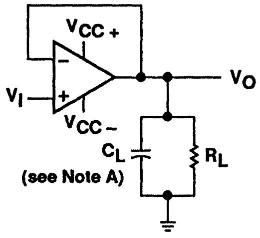
6. At $V_{CC\pm} = \pm 5$ V, $V_O = \pm 2.3$ V; at $V_{CC\pm} = \pm 15$ V, $V_O = \pm 10$ V.

operating characteristics

PARAMETER			TEST CONDITIONS		T_A	$V_{CC\pm} = \pm5$ V MIN	$V_{CC\pm} = \pm5$ V TYP	$V_{CC\pm} = \pm5$ V MAX	$V_{CC\pm} = \pm15$ V MIN	$V_{CC\pm} = \pm15$ V TYP	$V_{CC\pm} = \pm15$ V MAX	UNIT
SR +	Positive slew rate at unity gain		R_L = 10 kΩ, C_L = 100 pF, See Figure 1, See Note 8		25°C		2		2	2.9		V/µs
					−55°C		1.4		1.2	1.9		
					125°C		2.4		1.2	3.5		
SR −	Negative slew rate at unity gain				25°C		3.9		3	5.1		V/µs
					−55°C		3.2		2.5	4.6		
					125°C		4.1		2.5	4.7		
t_r	Rise time		V_{IPP} = ±10 mV, R_L = 10 kΩ, C_L = 100 pF, See Figures 1 and 2		25°C		138			132		ns
					−55°C		142			123		
					125°C		166			158		
t_f	Fall time				25°C		138			132		ns
					−55°C		142			123		
					125°C		166			158		
	Overshoot factor				25°C		11%			5%		
					−55°C		16%			6%		
					125°C		14%			8%		
V_n	Equivalent input noise voltage	TL034M	R_S = 100 Ω, See Figure 3	f = 10 Hz	25°C		83			83		nV/√Hz
				f = 1 kHz			43			43		
		TL034AM		f = 10 Hz	25°C		83			83		
				f = 1 kHz			43			43		
I_n	Equivalent input noise current		f = 1 kHz		25°C		0.003			0.003		pA/√Hz
B1	Unity-gain bandwidth		V_i = 10 mV, R_L = 10 kΩ, C_L = 25 pF, See Figure 4		25°C		1			1.1		MHz
					−55°C		1			1.1		
					125°C		0.9			0.9		
ϕ_m	Phase margin at unity gain		V_i = 10 mV, R_L = 10 kΩ, C_L = 25 pF, See Figure 4		25°C		61°			65°		
					−55°C		57°			64°		
					125°C		59°			62°		

NOTE 8: For $V_{CC\pm} = \pm5$ V, $V_{IPP} = \pm1$ V; for $V_{CC\pm} = \pm15$ V, $V_{IPP} = \pm5$ V.

PARAMETER MEASUREMENT INFORMATION



NOTE A: C_L includes fixture capacitance.

Figure 1. Slew Rate, Rise/Fall Time, and Overshoot Test Circuit

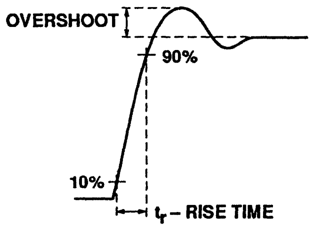


Figure 2. Rise Time and Overshoot Waveform

PARAMETER MEASUREMENT INFORMATION

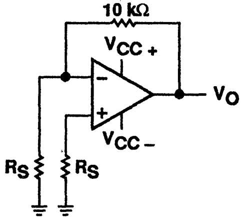
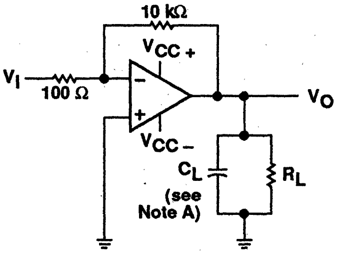


Figure 3. Noise Voltage Test Circuit



NOTE A: C_L includes fixture capacitance.

Figure 4. Unity-Gain Bandwidth and Phase Margin Test Circuit

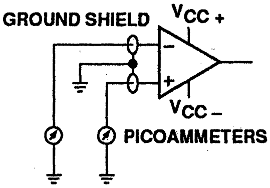


Figure 5. Input Bias and Offset Current Test Circuit

typical values

Typical values as presented in this data sheet represent the median (50% point) of device parametric performance.

input bias and offset current

At the picoamp bias current level typical of the TL034 and TL034A, accurate measurement of the bias current becomes difficult. Not only does this measurement require a picoammeter, but test socket leakages can easily exceed the actual device bias currents. To accurately measure these small currents, Texas Instruments uses a two step process. The socket leakage is measured using picoammeters with bias voltages applied but with no device in the socket. The device is then inserted into the socket and a second test that measures both the socket leakage and the device input bias current is performed. The two measurements are then subtracted algebraically to determine the bias current of the device.

noise

Because of the increasing emphasis on low noise levels in many of today's applications, the input noise voltage density is sample-tested at f = 1 kHz. Texas Instruments also has additional noise testing capability to meet specific application requirements. Please contact the factory for details.

TYPICAL CHARACTERISTICS

table of graphs

			FIGURE
V_{IO}	Input offset voltage	Distribution	6
α_{VIO}	Temperature coefficient of input offset voltage	Distribution	7
I_{IO}	Input offset current	vs Temperature	8
I_{IB}	Input bias current	vs V_{IC}	9
		vs Temperature	8
V_I	Input voltage range	vs V_{CC}	10
		vs Temperature	11
V_{ID}	Differential input voltage	vs Output voltage	12, 13
V_{OM}	Maximum peak output voltage swing	vs V_{CC}	14
		vs Output current	16, 17
		vs Frequency	15
		vs Temperature	18, 19
A_{VD}	Differential voltage amplification	vs R_L	20
		vs Frequency	21
		vs Temperature	22
z_o	Output impedance	vs Frequency	23
CMRR	Common-mode rejection ratio	vs Frequency	24, 25
		vs Temperature	26
k_{SVR}	Supply-voltage rejection ratio	vs Temperature	27
I_{OS}	Short-circuit output current	vs V_{CC}	28
		vs Time	29
		vs Temperature	30
I_{CC}	Supply current	vs V_{CC}	32
		vs Temperature	33
SR	Slew rate	vs R_L	34, 35
		vs Temperature	36, 37
	Overshoot factor	vs C_L	38
V_n	Equivalent input noise voltage	vs Frequency	31
THD	Total harmonic distortion	vs Frequency	39
B_1	Unity-gain bandwidth	vs V_{CC}	40
		vs Temperature	41
ϕ_m	Phase margin	vs V_{CC}	42
		vs C_L	43
		vs Temperature	44
	Phase shift	vs Frequency	21
	Pulse response	Small-signal	45
		Large-signal	46, 47

TYPICAL CHARACTERISTICS†

DISTRIBUTION OF TL034
INPUT OFFSET VOLTAGE

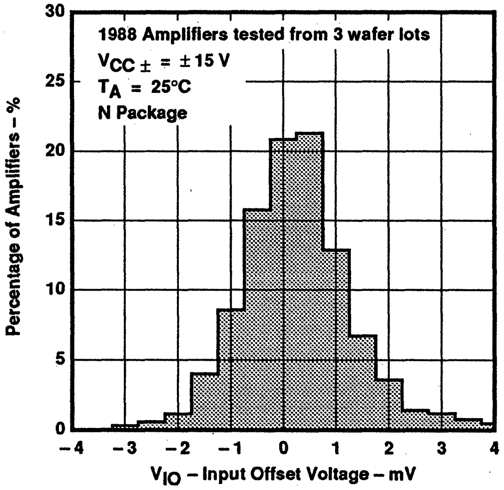


Figure 6

DISTRIBUTION OF TL034
INPUT OFFSET VOLTAGE
TEMPERATURE COEFFICIENT

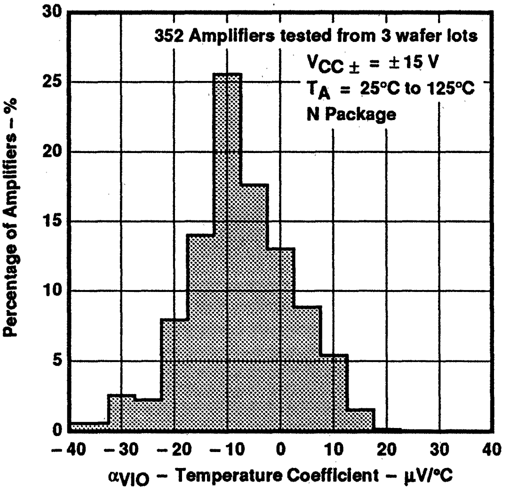


Figure 7

INPUT BIAS CURRENT AND
INPUT OFFSET CURRENT
vs
FREE-AIR TEMPERATURE

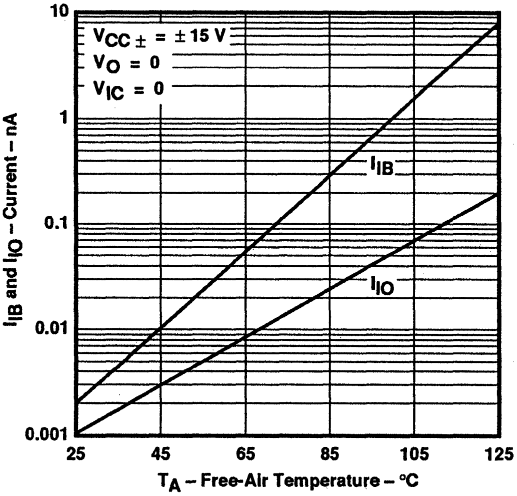


Figure 8

INPUT BIAS CURRENT
vs
COMMON-MODE INPUT VOLTAGE

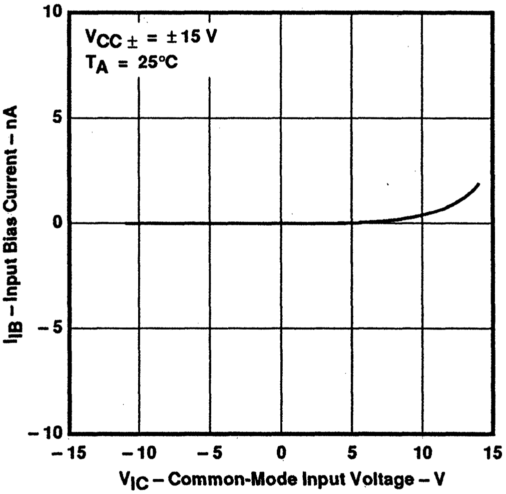


Figure 9

---

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

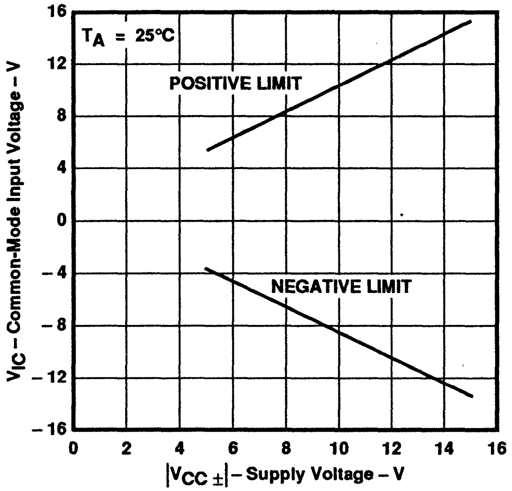

COMMON-MODE
INPUT VOLTAGE RANGE LIMITS
vs
SUPPLY VOLTAGE

Figure 10

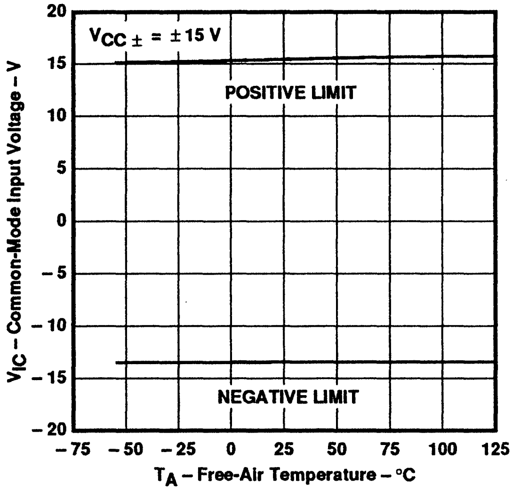

COMMON-MODE
INPUT VOLTAGE RANGE LIMITS
vs
FREE-AIR TEMPERATURE

Figure 11

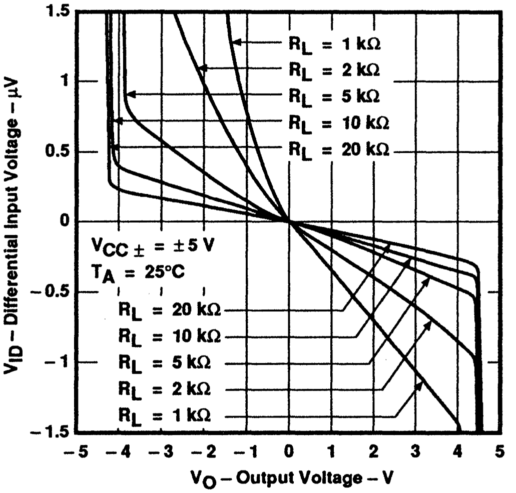

DIFFERENTIAL INPUT VOLTAGE
vs
OUTPUT VOLTAGE

Figure 12

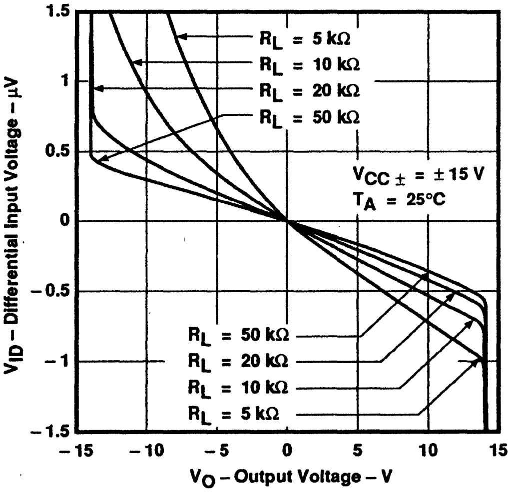

DIFFERENTIAL INPUT VOLTAGE
vs
OUTPUT VOLTAGE

Figure 13

---

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS[†]

MAXIMUM PEAK OUTPUT VOLTAGE
vs
SUPPLY VOLTAGE

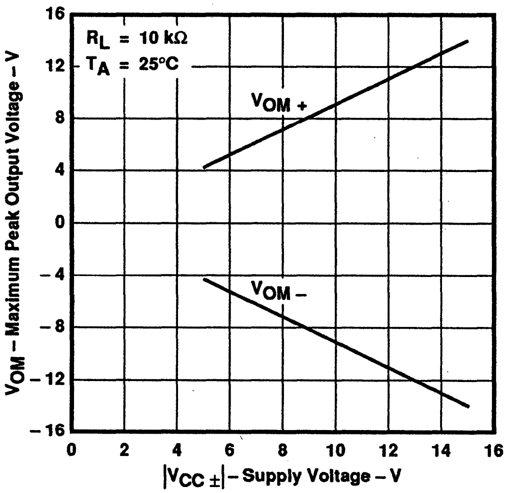


Figure 14

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE
vs
FREQUENCY

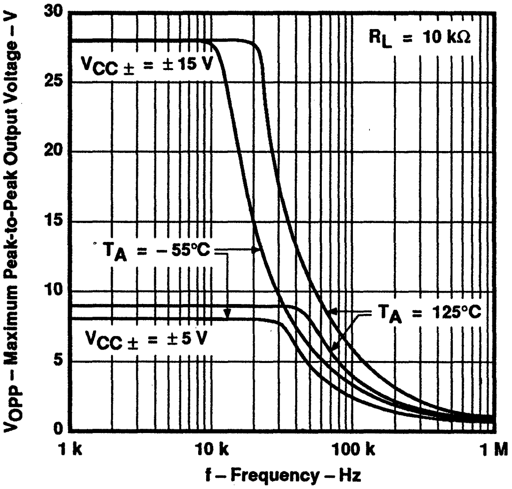


Figure 15

MAXIMUM PEAK OUTPUT VOLTAGE
vs
OUTPUT CURRENT

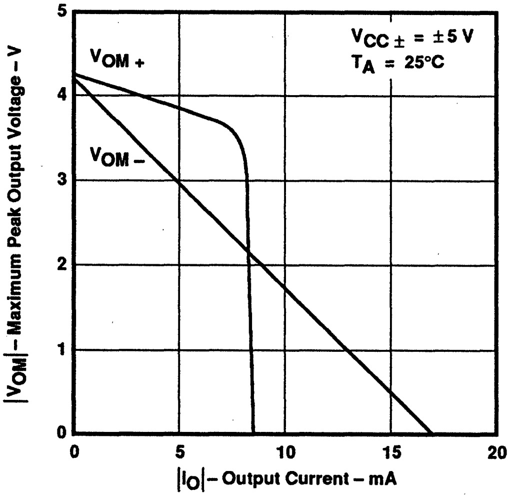


Figure 16

MAXIMUM PEAK OUTPUT VOLTAGE
vs
OUTPUT CURRENT

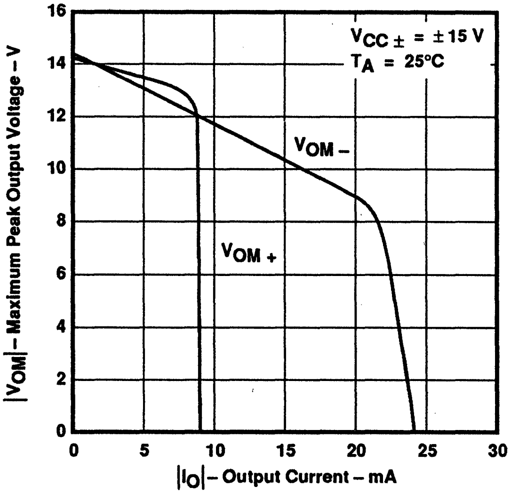


Figure 17

[†] Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS[†]

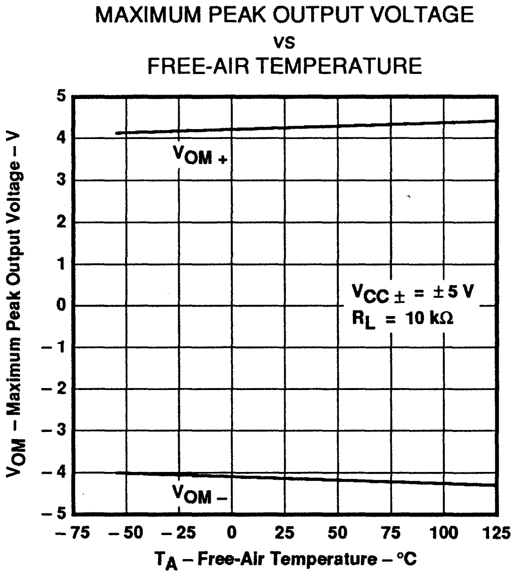


Figure 18

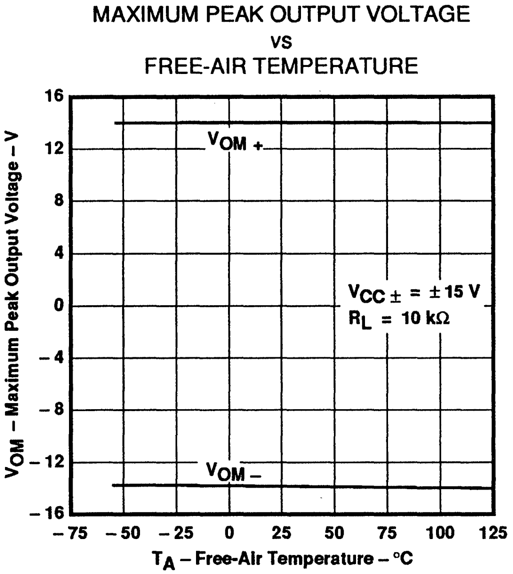


Figure 19

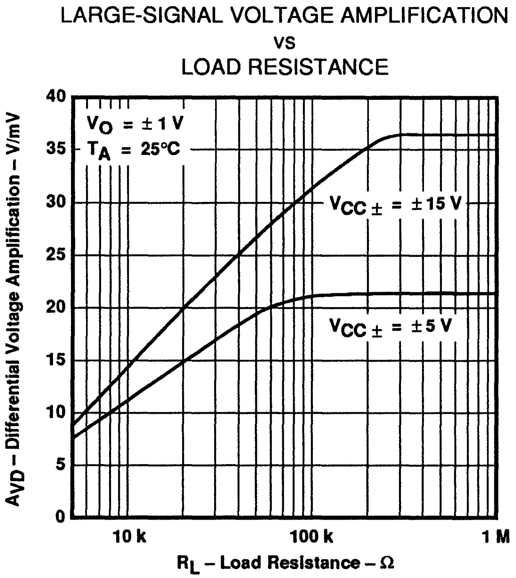


Figure 20

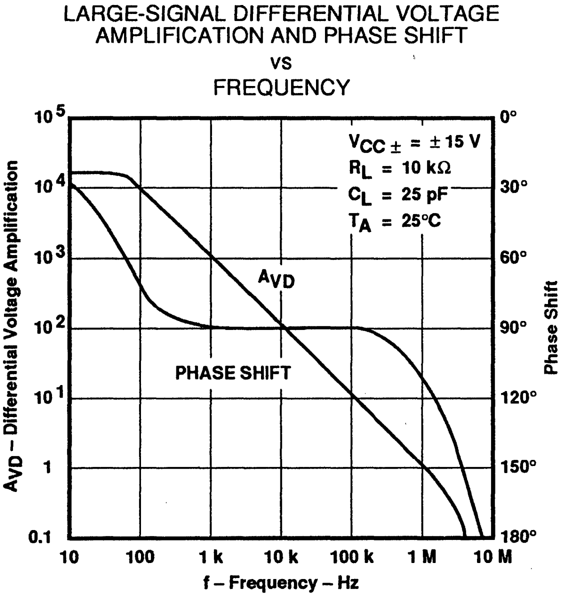


Figure 21

[†] Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

LARGE-SIGNAL VOLTAGE AMPLIFICATION
vs
FREE-AIR TEMPERATURE

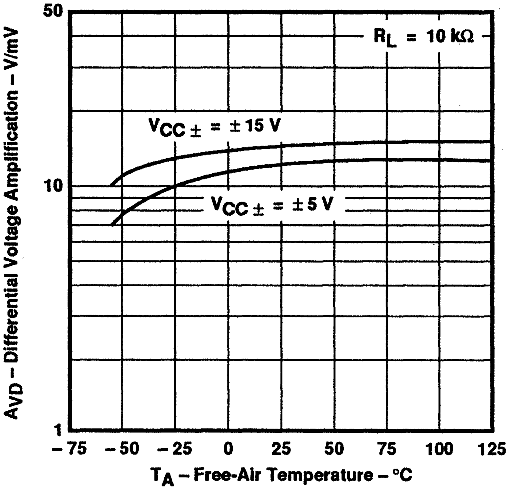


Figure 22

OUTPUT IMPEDANCE
vs
FREQUENCY

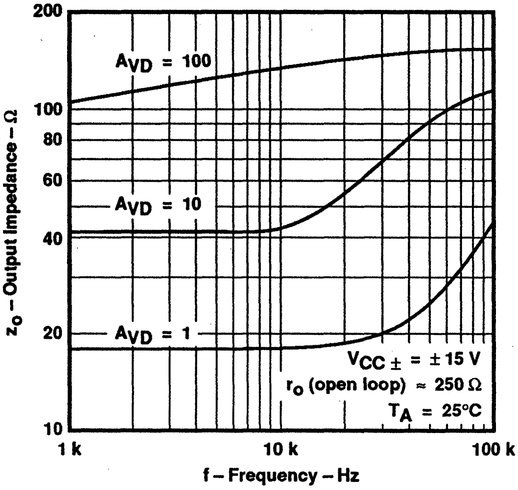


Figure 23

COMMON-MODE REJECTION RATIO
vs
FREQUENCY

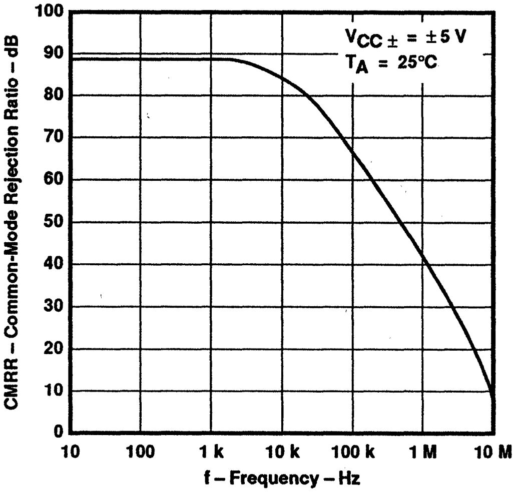


Figure 24

COMMON-MODE REJECTION RATIO
vs
FREQUENCY

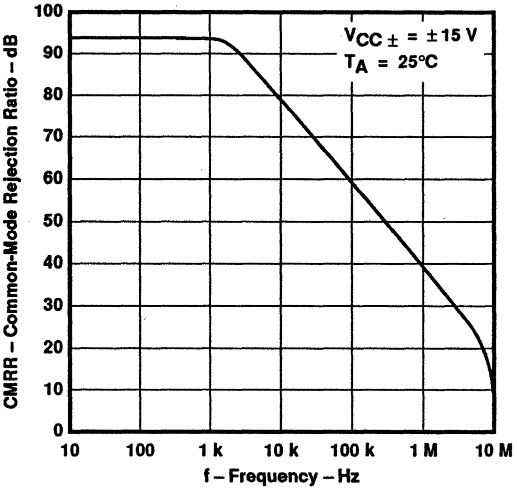


Figure 25

---

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

COMMON-MODE REJECTION RATIO vs FREE-AIR TEMPERATURE

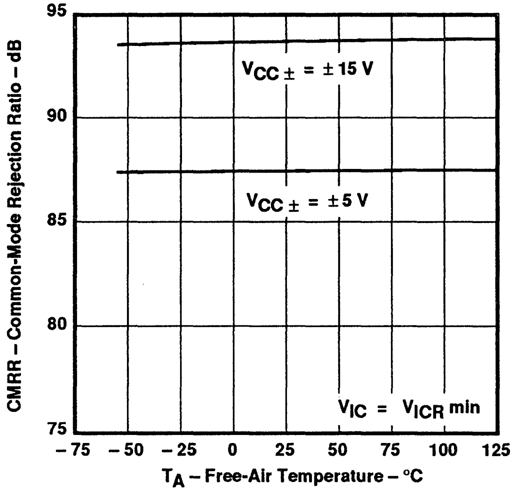


Figure 26

SUPPLY-VOLTAGE REJECTION RATIO vs FREE-AIR TEMPERATURE

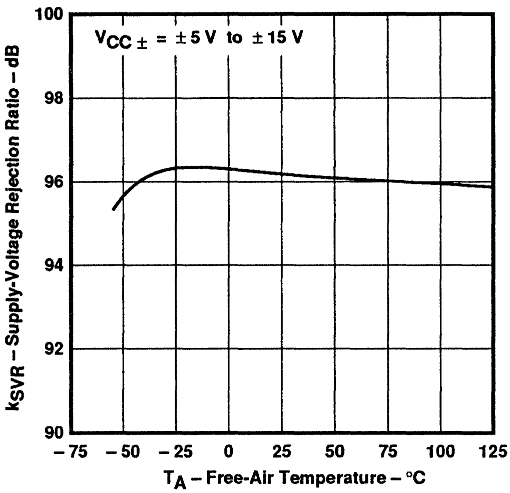


Figure 27

SHORT-CIRCUIT OUTPUT CURRENT vs SUPPLY VOLTAGE

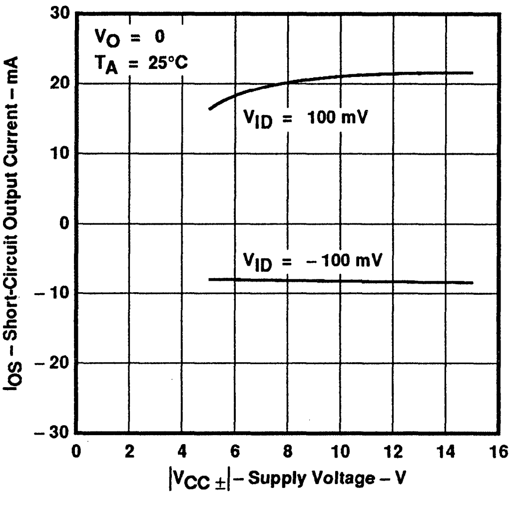


Figure 28

SHORT-CIRCUIT OUTPUT CURRENT vs TIME

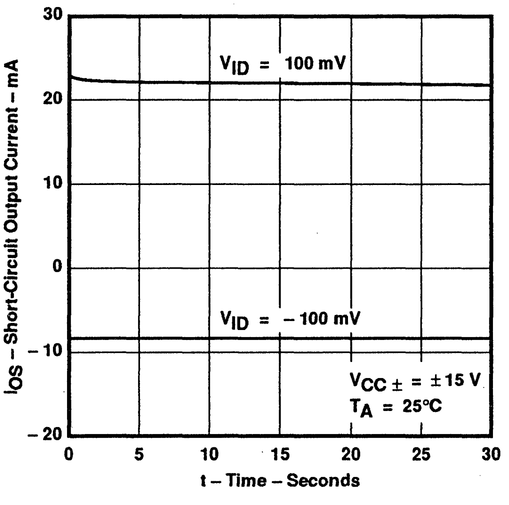


Figure 29

---

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

SHORT-CIRCUIT OUTPUT CURRENT
vs
FREE-AIR TEMPERATURE

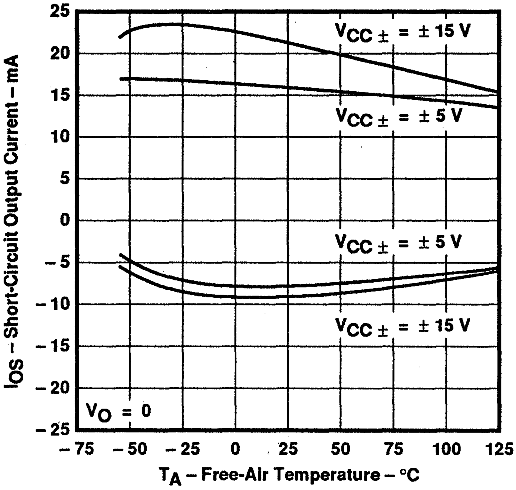


Figure 30

EQUIVALENT INPUT NOISE VOLTAGE
vs
FREQUENCY

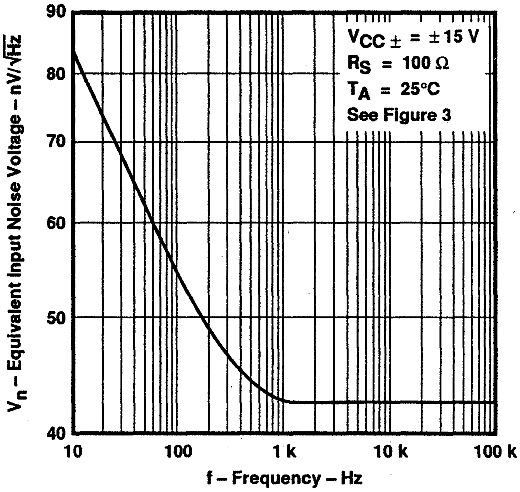


Figure 31

SUPPLY CURRENT
vs
SUPPLY VOLTAGE

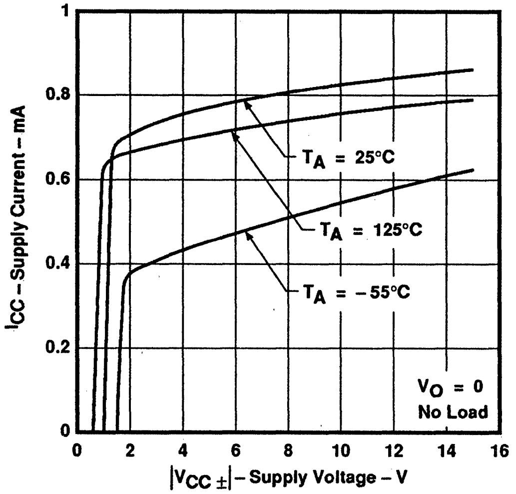


Figure 32

SUPPLY CURRENT
vs
FREE-AIR TEMPERATURE

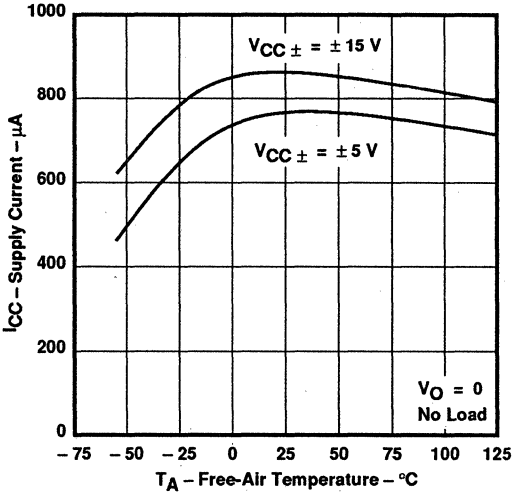


Figure 33

---

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

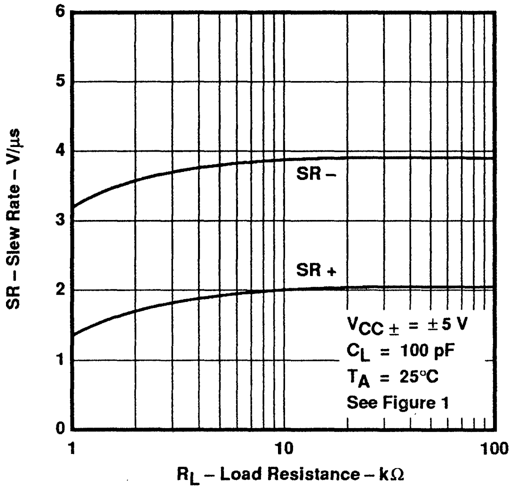

SLEW RATE
vs
LOAD RESISTANCE

Figure 34

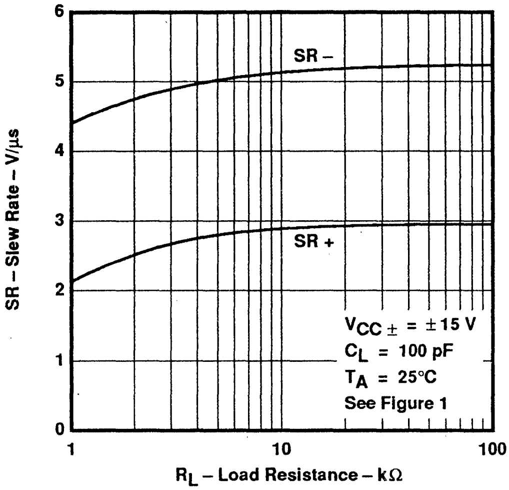

SLEW RATE
vs
LOAD RESISTANCE

Figure 35

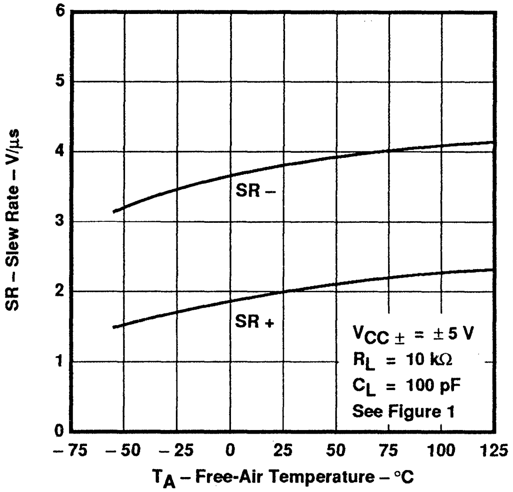

SLEW RATE
vs
FREE-AIR TEMPERATURE

Figure 36

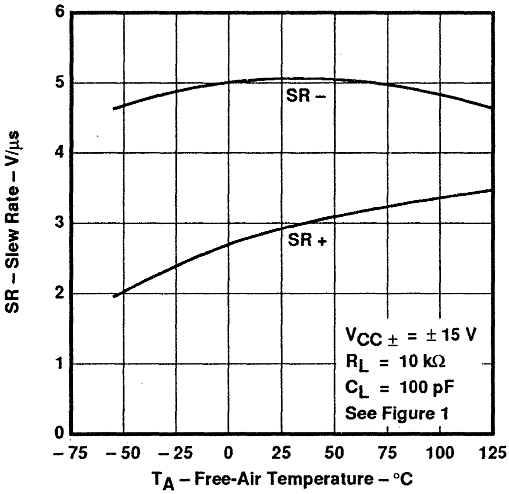

SLEW RATE
vs
FREE-AIR TEMPERATURE

Figure 37

---

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS[†]

OVERSHOOT FACTOR
vs
LOAD CAPACITANCE

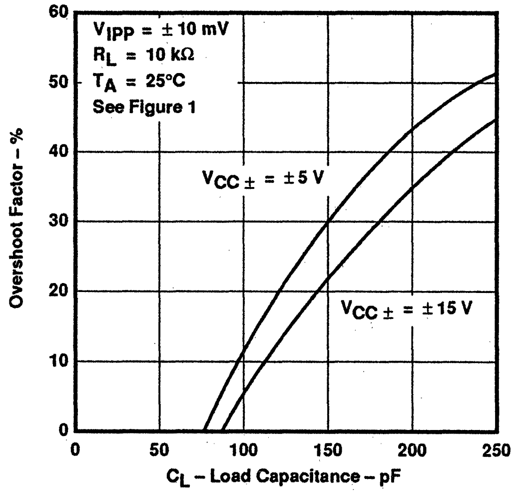


Figure 38

TOTAL HARMONIC DISTORTION
vs
FREQUENCY

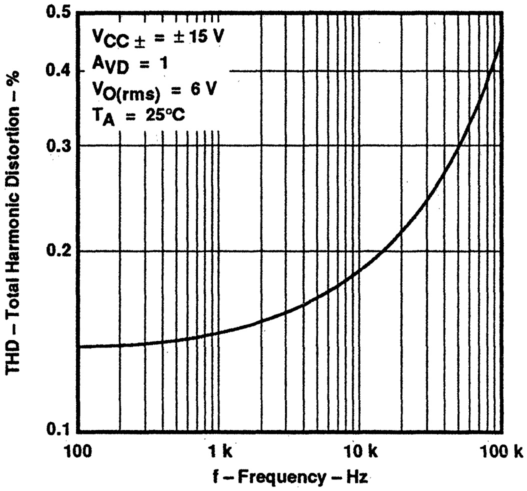


Figure 39

UNITY-GAIN BANDWIDTH
vs
SUPPLY VOLTAGE

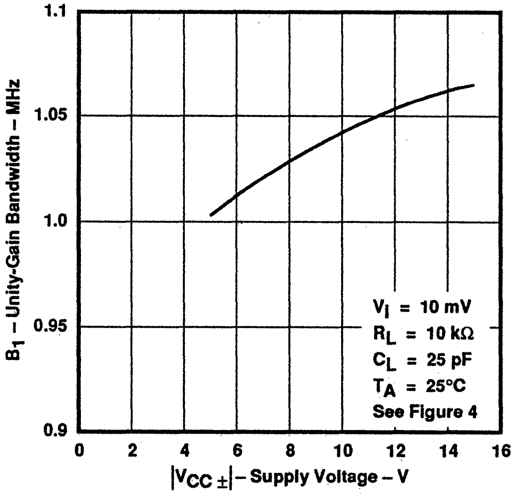


Figure 40

UNITY-GAIN BANDWIDTH
vs
FREE-AIR TEMPERATURE

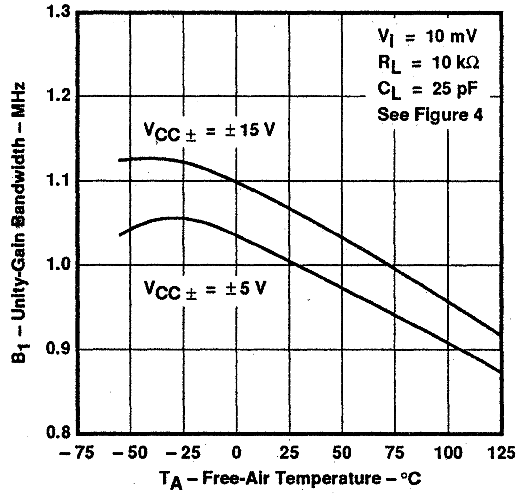


Figure 41

[†] Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

PHASE MARGIN
vs
SUPPLY VOLTAGE

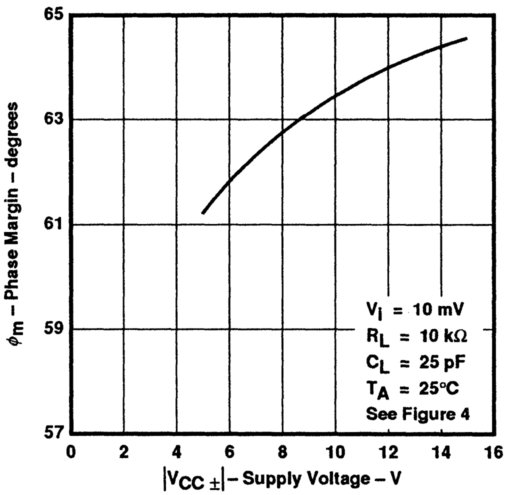


Figure 42

PHASE MARGIN
vs
LOAD CAPACITANCE

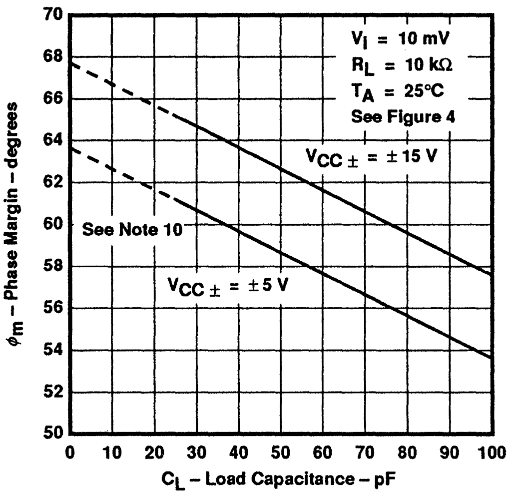


Figure 43

PHASE MARGIN
vs
FREE-AIR TEMPERATURE

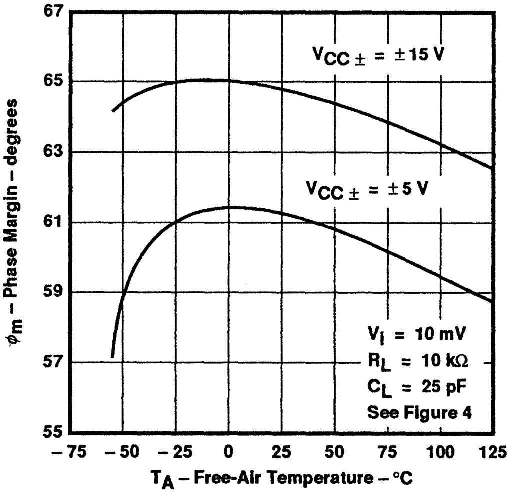


Figure 44

VOLTAGE-FOLLOWER
SMALL-SIGNAL
PULSE RESPONSE

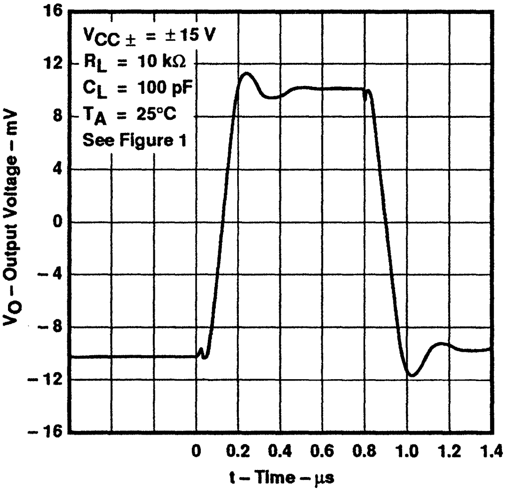
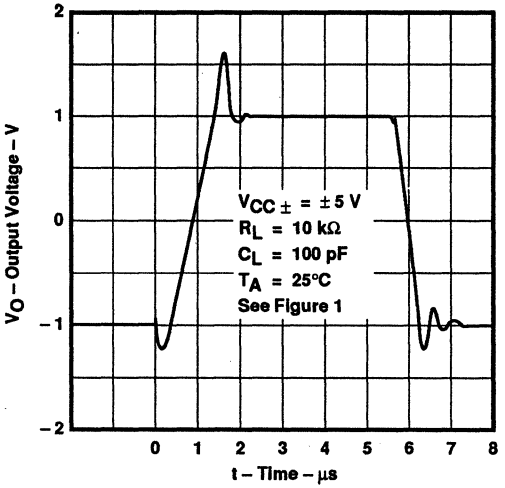


Figure 45

NOTE 10: Values of phase margin below a load capacitance of 25 pF were estimated.

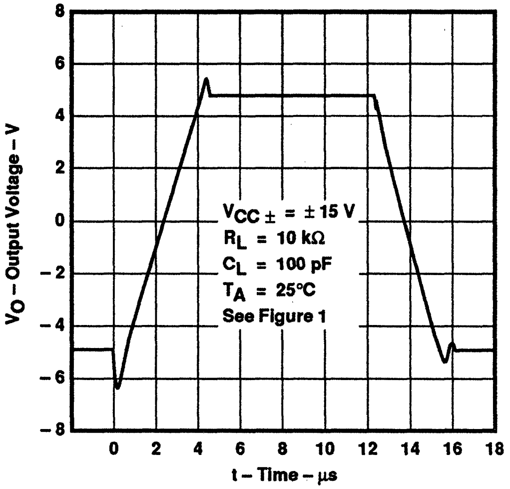
† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS



VOLTAGE-FOLLOWER
LARGE-SIGNAL
PULSE RESPONSE

Figure 46



VOLTAGE-FOLLOWER
LARGE-SIGNAL
PULSE RESPONSE

Figure 47

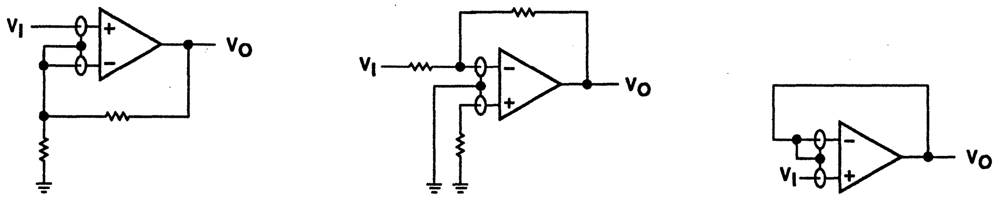
APPLICATION INFORMATION

input characteristics

The TL034 and TL034A are specified with a minimum and a maximum input voltage that, if exceeded at either input, could cause the device to malfunction.

Because of the extremely high input impedance and resulting low bias current requirements, the TL034 and TL034A are well-suited for low-level signal processing; however, leakage currents on printed circuit boards and sockets can easily exceed bias current requirements and cause degradation in system performance. It is a good practice to include guard rings around inputs (see Figure 48). These guards should be driven from a low-impedance source at the same voltage level as the common-mode input.

The inputs of any unused amplifiers should be tied to ground to avoid possible oscillation.



(a) NONINVERTING AMPLIFIER

(b) INVERTING AMPLIFIER

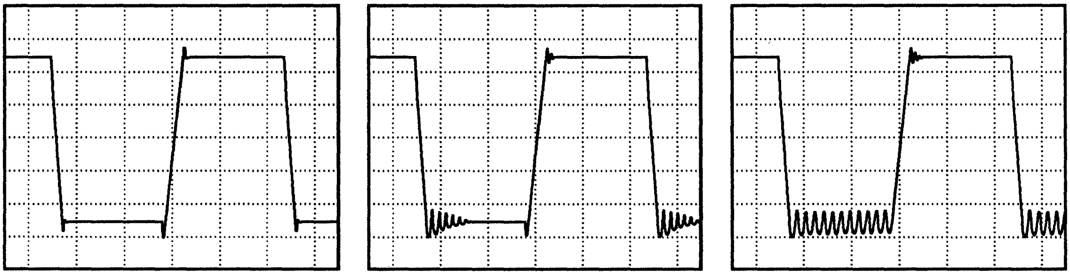
(c) UNITY-GAIN AMPLIFIER

Figure 48. Use of Guard Rings

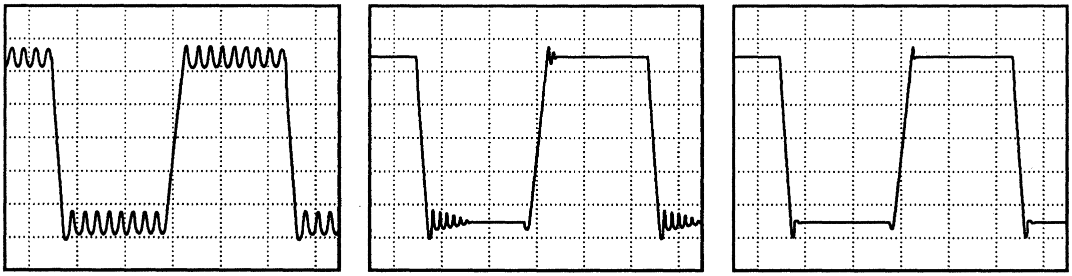
APPLICATION INFORMATION

output characteristics

All operating characteristics (except bandwidth and phase margin) are specified with 100 pF load capacitance. The TL034 and TL034A will drive higher capacitive loads; however, as the load capacitance increases, the resulting response pole occurs at lower frequencies, thereby causing ringing, peaking, or even oscillation. The value of the load capacitance at which oscillation occurs varies with production lots. If an application appears to be sensitive to oscillation due to load capacitance, adding a small resistance in series with the load should alleviate the problem. Capacitive loads of 1000 pF and larger may be driven if enough resistance is added in series with the output (see Figure 49).

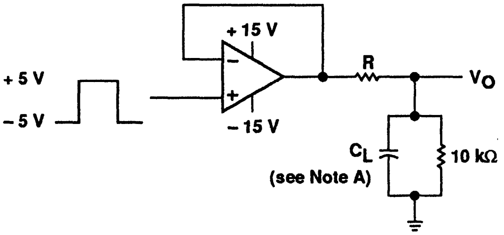


(a) C_L = 100 pF, R = 0 (b) C_L = 300 pF, R = 0 (c) C_L = 350 pF, R = 0



(d) C_L = 1000 pF, R = 0 (e) C_L = 1000 pF, R = 50 Ω (f) C_L = 1000 pF, R = 2 kΩ

Figure 49. Effect of Capacitive Loads



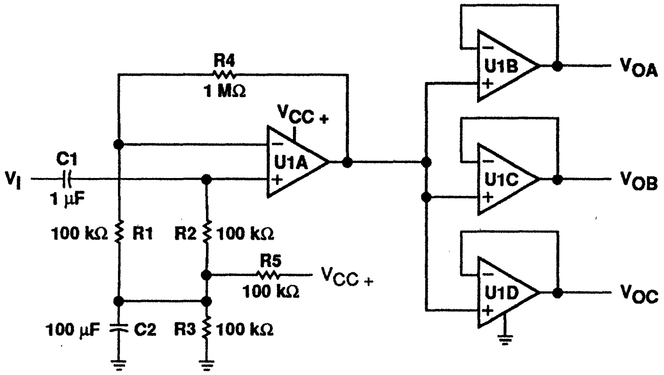
NOTE A: C_L includes fixture capacitance.

Figure 50. Test Circuit for Output Characteristics

APPLICATION INFORMATION

audio distribution amplifier

This audio distribution amplifier feeds the input signal to three separate output channels. U1A amplifies the input signal with a gain of 10 while U1B, U1C, and U1D serve as buffers to the output channels. The gain response of this circuit is very flat from 20 Hz to 20 kHz. The TL034 allows quick response to the input signal while maintaining low power consumption.



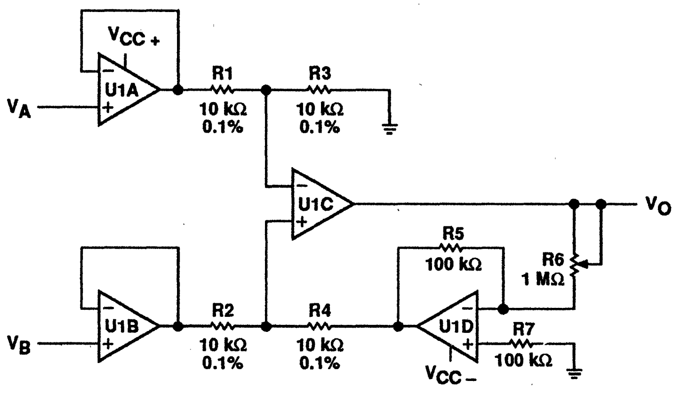
NOTE : U1A through U1D = TL034; V_{CC+} = 5 V.

instrumentation amplifier with linear gain adjust

The TL034 low-offset voltage and low-power consumption provides an accurate but inexpensive instrumentation amplifier. This particular configuration offers the advantage that the gain can be linearly set by one resistor:

$$V_O = \frac{R6}{R5} \times (V_B - V_A)$$

Adjusting R6 varies the gain. The value of R6 should always be greater or equal to the value of R5 in order to ensure stability. The disadvantage of this instrumentation amplifier topology is the high degree of CMRR degradation resulting from mismatches between R1, R2, R3, and R4. For this reason, these four resistors should be 0.1% tolerance resistors.



NOTE : U1A through U1D = TL034; $V_{CC\pm}$ = ±15 V.

TL044M, TL044C
QUAD LOW-POWER OPERATIONAL AMPLIFIERS

D1662, SEPTEMBER 1973—REVISED JUNE 1988

- **Very Low Power Consumption**
- **Typical Power Dissipation with ±2-V Supplies . . . 340 μW**
- **Low Input Bias and Offset Currents**
- **Output Short-Circuit Protection**
- **Low Input Offset Voltage**
- **Internal Frequency Compensation**
- **Latch-Up-Free Operation**
- **Power Applied in Pairs**

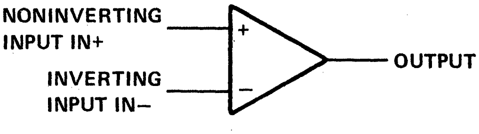
TL044M IS NOT RECOMMENDED FOR NEW DESIGNS.

description

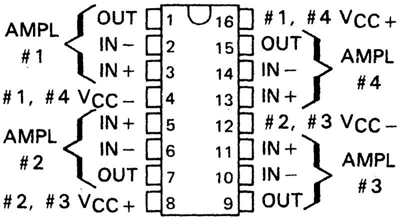
The TL044 is a quad low-power operational amplifier designed to replace higher-power devices in many applications without sacrificing system performance. High input impedance, low supply currents, and low equivalent input noise voltage over a wide range of operating supply voltages result in an extremely versatile operational amplifier for use in a variety of analog applications including battery-operated circuits. Internal frequency compensation, absence of latch-up, high slew rate, and output short-circuit protection assure ease of use. Power may be applied separately to Section A (amplifiers 1 and 4) or Section B (amplifiers 2 and 3) while the other pair remains unpowered.

The TL044M is characterized for operation over the full military temperature range of −55°C to 125°C; the TL044C is characterized for operation from 0°C to 70°C.

symbol (each amplifier)

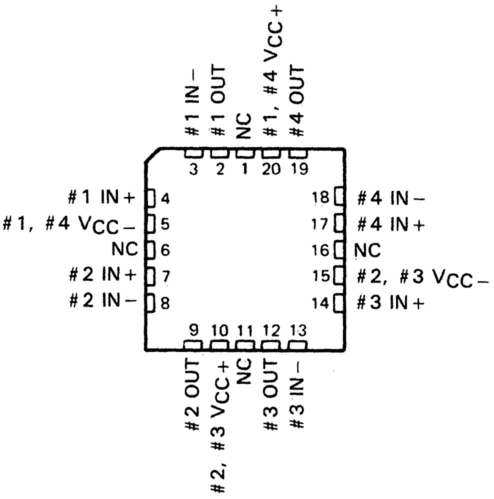


TL044M . . . J OR W DUAL-IN-LINE PACKAGE
TL044C . . . J OR N PACKAGE
(TOP VIEW)



Pins 4 and 12 are internally connected together in the N package only.

TL044M . . . FK PACKAGE
(TOP VIEW)



NC—No internal connection

TEXAS INSTRUMENTS
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

AVAILABLE OPTIONS

T_A	V_{IO} MAX AT 25°C	PACKAGE			
		CHIP CARRIER (FK)	CERAMIC DIP (J)	PLASTIC DIP (N)	FLAT PACK (W)
0°C to 70°C	5 mV	—	TL044CJ	TL044CN	—
−55°C to 125°C	5 mV	TL044MFK	TL044MJ	—	TL044MW

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

		TL044M	TL044C	UNIT
Supply voltage V_{CC+} (see Note 1)		22	18	V
Supply voltage V_{CC-} (see Note 1)		−22	−18	V
Differential input voltage (see Note 2)		±30	±30	V
Input voltage (any input, see Notes 1 and 3)		±15	±15	V
Duration of output short-circuit (see Note 4)		unlimited	unlimited	
Continuous total dissipation		See Dissipation Rating Table		
Operating free-air temperature range		−55 to 125	0 to 70	°C
Storage temperature range		−65 to 150	−65 to 150	°C
Case temperature for 60 seconds	FK package	260		°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds	J or W package	300	300	°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	N package		260	°C

NOTES: 1. All voltage values, unless otherwise noted, are with respect to the midpoint between V_{CC+} and V_{CC-}.
2. Differential voltages are at the noninverting input terminal with respect to the inverting input terminal.
3. The magnitude of the input voltage must never exceed the magnitude of the supply voltage or 15 V, whichever is less.
4. The output may be shorted to ground or either power supply. For the TL044M only, the unlimited duration of the short-circuit applies at (or below) 125°C case temperature or 85°C free-air temperature.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR	DERATE ABOVE T_A	$T_A = 70°C$ POWER RATING	$T_A = 125°C$ POWER RATING
FK	680 mW	11.0 mW/°C	88°C	680 mW	275 mW
J (TL044M)	680 mW	11.0 mW/°C	88°C	680 mW	275 mW
J (TL044C)	680 mW	8.2 mW/°C	67°C	656 mW	—
N	680 mW	N/A	N/A	680 mW	—
W	680 mW	8.0 mW/°C	65°C	640 mW	200 mW

electrical characteristics at specified free-air temperature, V_{CC+} = 15 V, V_{CC-} = −15 V

PARAMETER		TEST CONDITIONS†		TL044M			TL044C			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_O = 0,	25°C		1	5		1	5	mV
		R_S = 50 Ω	Full range			6			7.5	
I_{IO}	Input offset current	V_O = 0	25°C		5	40		15	80	nA
			Full range			100			200	
I_{IB}	Input bias current	V_O = 0	25°C		50	100		100	250	nA
			Full range			250			400	
V_{ICR}	Common-mode input voltage range		25°C	±12	±13		±12	±13		V
			Full range	±12			±12			
V_{OPP}	Maximum peak-to-peak output voltage swing	R_L = 10 kΩ	25°C	20	26		20	26		V
		R_L ≥ 10 kΩ	Full range	20			20			
A_{VD}	Large-signal differential voltage amplification	R_L ≥ 10 kΩ,	25°C	72	86		60	80		dB
		V_O = ±10 V	Full range	66			60			
B_1	Unity-gain bandwidth		25°C		0.5			0.5		MHz
CMRR	Common-mode rejection ratio	V_{IC} = V_{ICR} min,	25°C	60	72		60	72		dB
		V_O = 0, R_S = 50 Ω	Full range	60			60			
k_{SVS}	Supply voltage sensitivity ($\Delta V_{IO}/\Delta V_{CC}$)	V_{CC} = ±9 V to ±15 V,	25°C		30	150		30	200	μV/V
		V_O = 0, R_S = 50 Ω	Full range			150			200	
V_n	Equivalent input noise voltage	A_{VD} = 20 dB, B = 1 Hz, f = 1 kHz	25°C		50			50		nV/√Hz
I_{OS}	Short-circuit output current		25°C		±6			±6		mA
I_{CC}	Supply current (four amplifiers)	No load,	25°C		250	400		250	500	μA
		V_O = 0 V	Full range			400			500	
P_D	Total dissipation (four amplifiers)	No load,	25°C		7.5	12		7.5	15	mW
		V_O = 0 V	Full range			12			15	

† All characteristics are measured under open-loop conditions with zero common-mode input voltage, unless otherwise specified. Full range for TL044M is −55°C to 125°C and for TL044C is 0°C to 70°C.

operating characteristics, V_{CC+} = 15 V, V_{CC-} = −15 V, T_A = 25°C

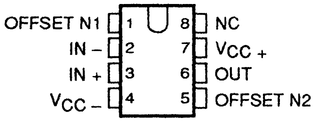
PARAMETER		TEST CONDITIONS		TL044M			TL044C			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
t_r	Rise time	V_I = 20 mV,	R_L = 10 kΩ,		0.3			0.3		μs
	Overshoot factor	C_L = 100 pF,	See Figure 1		5%			5%		
SR	Slew rate at unity gain	V_I = 10 V, C_L = 100 pF,	R_L = 10 kΩ, See Figure 1		0.5			0.5		V/μs

TL051, TL051A
ENHANCED JFET PRECISION OPERATIONAL AMPLIFIERS

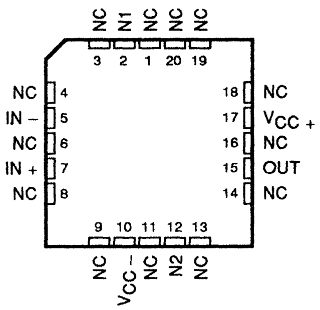
D3234, JUNE 1988 – REVISED NOVEMBER 1990

- **Maximum Offset Voltage . . . 800 µV (TL051A)**
- **High Slew Rate . . . 19.8 V/µs Typ at 25°C**
- **Low Total Harmonic Distortion . . . 0.003% Typ at R_L = 2 kΩ**
- **Low Noise Voltage . . . 18 nV/√Hz Typ at f = 1 kHz**
- **Low Input Bias Currents . . . 30 pA Typ**

D, JG, or P PACKAGE
(TOP VIEW)

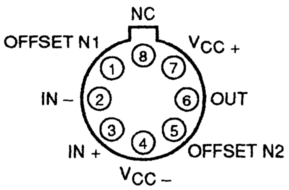


FK PACKAGE
(TOP VIEW)



NC – No internal connection

L PACKAGE
(TOP VIEW)



Pin 4 is in electrical contact with the case

description

The TL051 and TL051A operational amplifiers incorporate well-matched, high-voltage JFET and bipolar transistors in a monolithic integrated circuit. These devices offer the significant advantages of Texas Instruments new enhanced JFET process. This process affords not only low initial offset voltage due to the on-chip zener trim capability but also stable offset voltage over time and temperature. In comparison, traditional JFET processes are plagued by significant offset voltage drift.

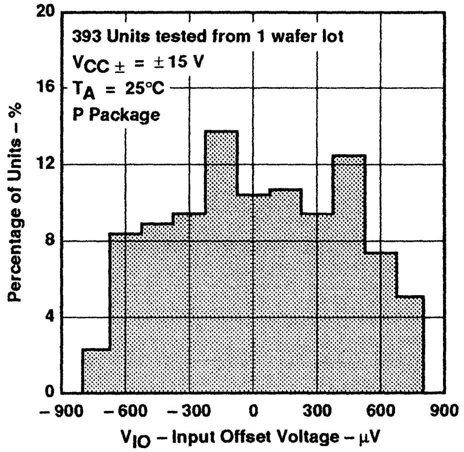
This new enhanced process still maintains the traditional JFET advantages of fast slew rates and low input bias and offset currents. These advantages coupled with low noise and low harmonic distortion make the TL051 well-suited for new state-of-the-art designs as well as existing design upgrades. The TL051 has been

AVAILABLE OPTIONS

T_A	V_{IO} max AT 25°C	PACKAGE				
		SMALL-OUTLINE (D)	CHIP CARRIER (FK)	CERAMIC DIP (JG)	METAL CAN (L)	PLASTIC DIP (P)
0°C to 70°C	800 µV	TL051ACD	——	——	——	TL051ACP
	1500 µV	TL051CD	——	——	——	TL051CP
– 40°C to 85°C	800 µV	TL051AID	——	——	——	TL051AIP
	1500 µV	TL051ID	——	——	——	TL051IP
– 55°C to 125°C	800 µV	TL051AMD	TL051AMFK	TL051AMJG	TL051AML	TL051AMP
	1500 µV	TL051MD	TL051MFK	TL051MJG	TL051ML	TL051MP

D packages are available taped-and-reeled. Add "R" suffix to device type (e.g., TL051CDR).

DISTRIBUTION OF TL051A
INPUT OFFSET VOLTAGE



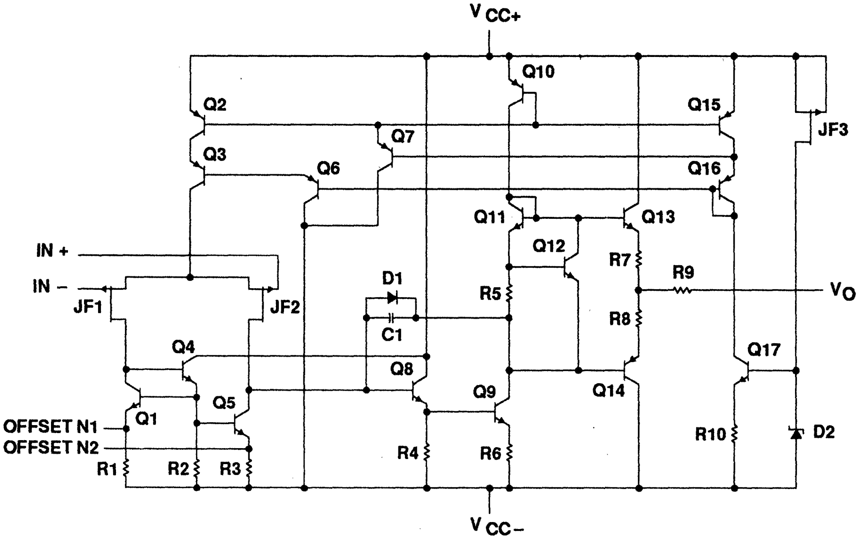
description (continued)

designed to be functionally compatible, as well as pin compatible, with the TL071 and TL081. Two offset voltage grades are available: TL051 (1.5 mV max) and TL051A (800 µV max).

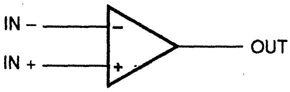
A variety of available packaging options includes small-outline and chip carrier versions for high-density system applications.

The C-suffix devices are characterized for operation from 0°C to 70°C. The I-suffix devices are characterized for operation from – 40°C to 85°C. The M-suffix devices are characterized for operation over the full military temperature range of – 55°C to 125°C.

equivalent schematic (each amplifier)



symbol (each amplifier)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC+} (see Note 1)	18 V
Supply voltage, V_{CC-} (see Note 1)	– 18 V
Differential input voltage (see Note 2)	± 30 V
Input voltage range, V_I (any input, see Notes 1 and 3)	± 15 V
Input current, I_I (each input)	± 1 mA
Output current, I_O (each output)	± 80 mA
Total current into V_{CC+} terminal	160 mA
Total current out of V_{CC-} terminal	160 mA
Duration of short-circuit current at (or below) 25°C (see Note 4)	unlimited
Continuous total dissipation	See Dissipation Rating Table
Operating free-air temperature range, T_A: C-suffix	0°C to 70°C
I-suffix	– 40°C to 85°C
M-suffix	– 55°C to 125°C
Storage temperature range	– 65°C to 150°C
Case temperature for 60 seconds: FK package	260°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D or P package	260°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: JG or L package	300°C

NOTES: 1. All voltage values, except differential voltages, are with respect to the midpoint between V_{CC+} and V_{CC-}.
2. Differential voltages are at the noninverting input with respect to the inverting input.
3. The magnitude of the input voltage must never exceed the magnitude of the supply voltage or 15 V, whichever is less.
4. The output may be shorted to either supply. Temperature and/or supply voltages must be limited to ensure that the maximum dissipation rating is not exceeded.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING	$T_A = 125°C$ POWER RATING
D	725 mW	5.8 mW/°C	464 mW	377 mW	145 mW
FK	1375 mW	11.0 mW/°C	880 mW	715 mW	275 mW
JG	1050 mW	8.4 mW/°C	672 mW	546 mW	210 mW
L	825 mW	6.6 mW/°C	528 mW	429 mW	165 mW
P	1000 mW	8.0 mW/°C	640 mW	520 mW	200 mW

recommended operating conditions

		C-SUFFIX			I-SUFFIX			M-SUFFIX			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		± 5		± 15	± 5		± 15	± 5		± 15	V
Common-mode input voltage, V_{IC}	$V_{CC\pm} = \pm 5$ V	– 1		4	– 1		4	– 1		4	V
	$V_{CC\pm} = \pm 15$ V	– 11		11	– 11		11	– 11		11	
Operating free-air temperature, T_A		0		70	– 40		85	– 55		125	°C

electrical characteristics

PARAMETER		TEST CONDITIONS		T_A†	$V_{CC\pm} = \pm 5$ V			$V_{CC\pm} = \pm 15$ V			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	$V_O = 0$, $V_{IC} = 0$, $R_S = 50\ \Omega$	TL051C	25°C		0.75	3.5		0.59	1.5	mV
				Full range			4.5			2.5	
			TL051AC	25°C		0.55	2.8		0.35	0.8	
				Full range			3.8			1.8	
α_{VIO}	Temperature coefficient of input offset voltage (see Note 9)		TL051C	25°C to 70°C		8			8		µV/°C
			TL051AC	25°C to 70°C		8			8	25	
	Input offset voltage long-term drift (see Note 5)			25°C		0.04			0.04		µV/mo
I_{IO}	Input offset current	$V_O = 0$, $V_{IC} = 0$, See Figure 5		25°C		4	100		5	100	pA
				70°C		0.02	1		0.025	1	nA
I_{IB}	Input bias current	$V_O = 0$, $V_{IC} = 0$, See Figure 5		25°C		20	200		30	200	pA
				70°C		0.15	4		0.2	4	nA
V_{ICR}	Common-mode input voltage range			25°C	−1 to 4	−2.3 to 5.6		−11 to 11	−12.3 to 15.6		V
				Full range	−1 to 4			−11 to 11			
V_{OM+}	Maximum positive peak output voltage swing	$R_L = 10\ k\Omega$		25°C	3	4.2		13	13.9		V
				Full range	3			13			
		$R_L = 2\ k\Omega$		25°C	2.5	3.8		11.5	12.7		
				Full range	2.5			11.5			
V_{OM-}	Maximum negative peak output voltage swing	$R_L = 10\ k\Omega$		25°C	−2.5	−3.5		−12	−13.2		V
				Full range	−2.5			−12			
		$R_L = 2\ k\Omega$		25°C	−2.3	−3.2		−11	−12		
				Full range	−2.3			−11			
A_{VD}	Large-signal differential voltage amplification	$R_L = 2\ k\Omega$, See Note 6		25°C	25	59		50	105		V/mV
				0°C	30	65		60	129		
				70°C	20	46		30	85		
r_i	Input resistance			25°C		10^{12}			10^{12}		Ω
C_i	Input capacitance			25°C		10			12		pF
CMRR	Common-mode rejection ratio	$V_{IC} = V_{ICR}$ min, $V_O = 0$, $R_S = 50\ \Omega$		25°C	65	85		75	93		dB
				0°C	65	84		75	92		
				70°C	65	84		75	91		
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm} / \Delta V_{IO}$)	$V_{CC\pm} = \pm 5$ V to ± 15 V, $V_O = 0$, $R_S = 50\ \Omega$		25°C	75	99		75	99		dB
				0°C	75	98		75	98		
				70°C	75	97		75	97		
I_{CC}	Supply current (four amplifiers)	No load, $V_O = 0$		25°C		2.6	3.2		2.7	3.2	mA
				0°C		2.7	3.2		2.8	3.2	
				70°C		2.6	3.2		2.7	3.2	

† Full range is 0°C to 70°C.

NOTES: 5. Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at $T_A = 150°C$ extrapolated to $T_A = 25°C$ using the Arrhenius equation and assuming an activation energy of 0.96 eV.

6. For $V_{CC\pm} = \pm 5$ V, $V_O = \pm 2.3$ V; at $V_{CC\pm} = \pm 15$ V, $V_O = \pm 10$ V.

9. This parameter is tested on a sample basis for the TL051A. For other test requirements, please contact the factory. This statement has no bearing on testing or nontesting of other parameters.

operating characteristics

PARAMETER		TEST CONDITIONS		T_A†	$V_{CC\pm} = \pm 5$ V			$V_{CC\pm} = \pm 15$ V			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
SR +	Positive slew rate at unity gain	R_L = 2 kΩ, C_L = 100 pF, See Figure 1 and Note 7		25°C		18.2		15	23.7		V/µs
				0°C		19.5		13	24.1		
				70°C		16.4		13	22.6		
SR –	Negative slew rate at unity gain			25°C		16.5		15	19.8		
				0°C		16.8		13	19.9		
				70°C		16		13	19.3		
t_r	Rise time	V_{IPP} = ± 10 mV, R_L = 2 kΩ, C_L = 100 pF, See Figures 1 and 2		25°C		55			56		ns
				0°C		54			55		
				70°C		63			63		
t_f	Fall time			25°C		55			57		
				0°C		54			56		
				70°C		62			64		
	Overshoot factor			25°C		24%			19%		
				0°C		24%			19%		
				70°C		24%			19%		
V_n	Equivalent input noise voltage (see Note 10)	R_S = 100 Ω, See Figure 3	f = 10 Hz	25°C		75			75		nV/√Hz
			f = 1 kHz	25°C		18			18	30	
V_{NPP}	Peak-to-peak equivalent input noise voltage		f = 10 Hz to 10 kHz	25°C		4			4		µV
I_n	Equivalent input noise current	f = 1 kHz		25°C		0.01			0.01		pA/√Hz
THD	Total harmonic distortion	R_S = 1 kΩ, R_L = 2 kΩ, f = 1 kHz, See Note 8		25°C		0.003%			0.003%		
B_1	Unity-gain bandwidth	V_i = 10 mV, R_L = 2 kΩ, C_L = 25 pF, See Figure 4		25°C		3			3.1		MHz
				0°C		3.2			3.3		
				70°C		2.7			2.8		
ϕ_m	Phase margin at unity gain	V_i = 10 mV, R_L = 2 kΩ, C_L = 25 pF, See Figure 4		25°C		59°			62°		
				0°C		58°			62°		
				70°C		59°			62°		

† Full range is 0°C to 70°C.

NOTES: 7. For $V_{CC\pm} = \pm 5$ V, $V_{IPP} = \pm 1$ V; for $V_{CC\pm} = \pm 15$ V, $V_{IPP} = \pm 5$ V.

8. For $V_{CC\pm} = \pm 5$ V, $V_{o(rms)} = 1$ V; for $V_{CC\pm} = \pm 15$ V, $V_{o(rms)} = 6$ V.

10. This parameter is tested on a sample basis. For other test requirements, please contact the factory. This statement has no bearing on testing or nontesting of other parameters.

electrical characteristics

PARAMETER		TEST CONDITIONS		T_A†	$V_{CC\pm} = \pm 5$ V			$V_{CC\pm} = \pm 15$ V			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	$V_O = 0$, $V_{IC} = 0$, $R_S = 50\ \Omega$	TL051I	25°C		0.75	3.5		0.59	1.5	mV
				Full range			5.3			3.3	
			TL051AI	25°C		0.55	2.8		0.35	0.8	
				Full range			4.6			2.6	
α_{VIO}	Temperature coefficient of input offset voltage (see Note 9)		TL051I	25°C to 85°C		7			8		µV/°C
			TL051AI	25°C to 85°C		8			8	25	
	Input offset voltage long-term drift (see Note 5)			25°C		0.04			0.04		µV/mo
I_{IO}	Input offset current	$V_O = 0$, $V_{IC} = 0$, See Figure 5		25°C		4	100		5	100	pA
				85°C		0.06	10		0.07	10	nA
I_{IB}	Input bias current	$V_O = 0$, $V_{IC} = 0$, See Figure 5		25°C		20	200		30	200	pA
				85°C		0.6	20		0.7	20	nA
V_{ICR}	Common-mode input voltage range			25°C	−1 to 4	−2.3 to 5.6		−11 to 11	−12.3 to 15.6		V
				Full range	−1 to 4			−11 to 11			
V_{OM+}	Maximum positive peak output voltage swing	$R_L = 10\ k\Omega$		25°C	3	4.2		13	13.9		V
				Full range	3			13			
		$R_L = 2\ k\Omega$		25°C	2.5	3.8		11.5	12.7		
				Full range	2.5			11.5			
V_{OM-}	Maximum negative peak output voltage swing	$R_L = 10\ k\Omega$		25°C	−2.5	−3.5		−12	−13.2		V
				Full range	−2.5			−12			
		$R_L = 2\ k\Omega$		25°C	−2.3	−3.2		−11	−12		
				Full range	−2.3			−11			
A_{VD}	Large-signal differential voltage amplification	$R_L = 2\ k\Omega$, See Note 6		25°C	25	59		50	105		V/mV
				−40°C	30	74		60	145		
				85°C	20	43		30	76		
r_i	Input resistance			25°C		10^{12}			10^{12}		Ω
C_i	Input capacitance			25°C		10			12		pF
CMRR	Common-mode rejection ratio	$V_{IC} = V_{ICR}$ min, $V_O = 0$, $R_S = 50\ \Omega$		25°C	65	85		75	93		dB
				−40°C	65	83		75	90		
				85°C	65	84		75	93		
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm} / \Delta V_{IO}$)	$V_{CC\pm} = \pm 5$ V to ± 15 V, $V_O = 0$, $R_S = 50\ \Omega$		25°C	75	99		75	99		dB
				−40°C	75	98		75	98		
				85°C	75	99		75	99		
I_{CC}	Supply current (four amplifiers)	No load, $V_O = 0$		25°C		2.6	3.2		2.7	3.2	mA
				−40°C		2.4	3.2		2.6	3.2	
				85°C		2.5	3.2		2.6	3.2	

† Full range is − 40°C to 85°C.

NOTES: 5. Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at $T_A = 150$°C extrapolated to $T_A = 25$°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

6. For $V_{CC\pm} = \pm 5$ V, $V_O = \pm 2.3$ V; at $V_{CC\pm} = \pm 15$ V, $V_O = \pm 10$ V.

9. This parameter is tested on a sample basis for the TL051A. For other test requirements, please contact the factory. This statement has no bearing on testing or nontesting of other parameters.

operating characteristics

PARAMETER		TEST CONDITIONS		T_A†	$V_{CC\pm}$ = ±5 V			$V_{CC\pm}$ = ±15 V			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
SR +	Positive slew rate at unity gain	R_L = 2 kΩ, C_L = 100 pF, See Figure 1 and Note 7		25°C		18.2		15	23.7		V/µs
				– 40°C		20.1		13	23		
				85°C		16.1		13	21.9		
SR –	Negative slew rate at unity gain			25°C		16.5		15	19.8		
				– 40°C		16.6		13	19.4		
				85°C		15.7		13	19.1		
t_r	Rise time	V_{IPP} = ± 10 mV, R_L = 2 kΩ, C_L = 100 pF, See Figures 1 and 2		25°C		55			56		ns
				– 40°C		52			53		
				85°C		64			65		
t_f	Fall time			25°C		55			57		
				– 40°C		51			53		
				85°C		64			65		
	Overshoot factor			25°C		24%			19%		
				– 40°C		24%			19%		
				85°C		24%			19%		
V_n	Equivalent input noise voltage (see Note 10)	R_S = 100 Ω, See Figure 3	f = 10 Hz	25°C		75			75		nV/√Hz
			f = 1 kHz	25°C		18			18	30	
V_{NPP}	Peak-to-peak equivalent input noise voltage		f = 10 Hz to 10 kHz	25°C		4			4		µV
I_n	Equivalent input noise current	f = 1 kHz		25°C		0.01			0.01		pA/√Hz
THD	Total harmonic distortion	R_S = 1 kΩ, R_L = 2 kΩ, f = 1 kHz, See Note 8		25°C		0.003%			0.003%		
B_1	Unity-gain bandwidth	V_i = 10 mV, R_L = 2 kΩ, C_L = 25 pF, See Figure 4		25°C		3			3.1		MHz
				– 40°C		3.5			3.6		
				85°C		2.6			2.7		
ϕ_m	Phase margin at unity gain	V_i = 10 mV, R_L = 2 kΩ, C_L = 25 pF, See Figure 4		25°C		59°			62°		
				– 40°C		58°			61°		
				85°C		59°			62°		

† Full range is – 40°C to 85°C.

NOTES: 7. For $V_{CC\pm}$ = ± 5 V, V_{IPP} = ± 1 V; for $V_{CC\pm}$ = ± 15 V, V_{IPP} = ± 5 V.

8. For $V_{CC\pm}$ = ± 5 V, $V_{o(rms)}$ = 1 V; for $V_{CC\pm}$ = ± 15 V, $V_{o(rms)}$ = 6 V.

10. This parameter is tested on a sample basis. For other test requirements, please contact the factory. This statement has no bearing on testing or nontesting of other parameters.

electrical characteristics

PARAMETER		TEST CONDITIONS		T_A†	$V_{CC\pm} = \pm 5$ V			$V_{CC\pm} = \pm 15$ V			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	$V_O = 0$, $V_{IC} = 0$, $R_S = 50\ \Omega$	TL051M	25°C		0.75	3.5		0.59	1.5	mV
				Full range			6.5			4.5	
			TL051AM	25°C		0.55	2.8		0.35	0.8	
				Full range			5.8			3.8	
α_{VIO}	Temperature coefficient of input offset voltage		TL051M	25°C to 125°C		8			8		µV/°C
			TL051AM	25°C to 125°C		8			8		
	Input offset voltage long-term drift (see Note 5)			25°C		0.04			0.04		µV/mo
I_{IO}	Input offset current	$V_O = 0$, $V_{IC} = 0$, See Figure 5		25°C		4	100		5	100	pA
				125°C		1	20		2	20	nA
I_{IB}	Input bias current	$V_O = 0$, $V_{IC} = 0$, See Figure 5		25°C		20	200		30	200	pA
				125°C		10	50		20	50	nA
V_{ICR}	Common-mode input voltage range			25°C	−1 to 4	− 2.3 to 5.6		− 11 to 11	− 12.3 to 15.6		V
				Full range	− 1 to 4			− 11 to 11			
V_{OM+}	Maximum positive peak output voltage swing	$R_L = 10\ \mathrm{k\Omega}$		25°C	3	4.2		13	13.9		V
				Full range	3			13			
		$R_L = 2\ \mathrm{k\Omega}$		25°C	2.5	3.8		11.5	12.7		
				Full range	2.5			11.5			
V_{OM-}	Maximum negative peak output voltage swing	$R_L = 10\ \mathrm{k\Omega}$		25°C	− 2.5	− 3.5		− 12	− 13.2		V
				Full range	− 2.5			− 12			
		$R_L = 2\ \mathrm{k\Omega}$		25°C	− 2.3	− 3.2		− 11	− 12		
				Full range	− 2.3			− 11			
A_{VD}	Large-signal differential voltage amplification	$R_L = 2\ \mathrm{k\Omega}$, See Note 6		25°C	25	59		50	105		V/mV
				− 55°C	30	76		60	149		
				125°C	10	32		15	49		
r_i	Input resistance			25°C		10^{12}			10^{12}		Ω
C_i	Input capacitance			25°C		10			12		pF
CMRR	Common-mode rejection ratio	$V_{IC} = V_{ICR}$ min, $V_O = 0$, $R_S = 50\ \Omega$		25°C	65	85		75	93		dB
				− 55°C	65	83		75	92		
				125°C	65	84		75	94		
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm} / \Delta V_{IO}$)	$V_{CC\pm} = \pm 5$ V to ± 15 V, $V_O = 0$, $R_S = 50\ \Omega$		25°C	75	99		75	99		dB
				− 55°C	75	98		75	98		
				125°C	75	100		75	100		
I_{CC}	Supply current (four amplifiers)	No load, $V_O = 0$		25°C		2.6	3.2		2.7	3.2	mA
				− 55°C		2.3	3.2		2.4	3.2	
				125°C		2.4	3.2		2.5	3.2	

† Full range is − 55°C to 125°C.

NOTES: 5. Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at $T_A = 150°C$ extrapolated to $T_A = 25°C$ using the Arrhenius equation and assuming an activation energy of 0.96 eV.

6. For $V_{CC\pm} = \pm 5$ V, $V_O = \pm 2.3$ V; at $V_{CC\pm} = \pm 15$ V, $V_O = \pm 10$ V.

operating characteristics

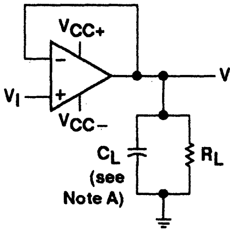
PARAMETER		TEST CONDITIONS		T_A†	$V_{CC\pm} = \pm 5$ V			$V_{CC\pm} = \pm 15$ V			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
SR +	Positive slew rate at unity gain	R_L = 2 kΩ, C_L = 100 pF, See Figure 1 and Note 7		25°C		18.2		15	23.7		V/µs
				– 55°C		17.5			20		
				125°C		15			21.2		
SR –	Negative slew rate at unity gain			25°C		16.5		15	19.8		
				– 55°C		15.1			17		
				125°C		14.8			18.2		
t_r	Rise time	V_{IPP} = ± 10 mV, R_L = 2 kΩ, C_L = 100 pF, See Figures 1 and 2		25°C		55			56		ns
				– 55°C		51			52		
				125°C		68			68		
t_f	Fall time			25°C		55			57		
				– 55°C		51			52		
				125°C		68			69		
	Overshoot factor			25°C		24%			19%		
				– 55°C		25%			19%		
				125°C		25%			19%		
V_n	Equivalent input noise voltage	R_S = 100 Ω, See Figure 3	f = 10 Hz	25°C		75			75		nV/√Hz
			f = 1 kHz	25°C		18			19		
V_{NPP}	Peak-to-peak equivalent input noise voltage		f = 10 Hz to 10 kHz	25°C		4			4		µV
I_n	Equivalent input noise current	f = 1 kHz		25°C		0.01			0.01		pA/√Hz
THD	Total harmonic distortion	R_S = 1 kΩ, R_L = 2 kΩ, f = 1 kHz, See Note 8		25°C		0.003%			0.003%		
B_1	Unity-gain bandwidth	V_i = 10 mV, R_L = 2 kΩ, C_L = 25 pF, See Figure 4		25°C		3			3.1		MHz
				– 55°C		3.6			3.7		
				125°C		2.3			2.4		
ϕ_m	Phase margin at unity gain	V_i = 10 mV, R_L = 2 kΩ, C_L = 25 pF, See Figure 4		25°C		59°			62°		
				– 55°C		57°			61°		
				125°C		59°			62°		

† Full range is – 55°C to 125°C.

NOTES: 7. For $V_{CC\pm} = \pm 5$ V, $V_{IPP} = \pm 1$ V; for $V_{CC\pm} = \pm 15$ V, $V_{IPP} = \pm 5$ V.

8. For $V_{CC\pm} = \pm 5$ V, $V_{o(rms)} = 1$ V; for $V_{CC\pm} = \pm 15$ V, $V_{o(rms)} = 6$ V.

PARAMETER MEASUREMENT INFORMATION



NOTE A: C_L includes fixture capacitance.

FIGURE 1. SLEW RATE, RISE/FALL TIME, AND OVERSHOOT TEST CIRCUIT

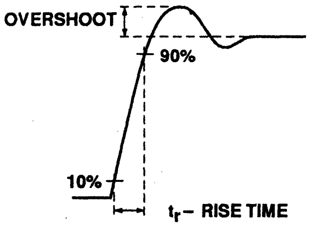


FIGURE 2. RISE TIME AND OVERSHOOT WAVEFORM

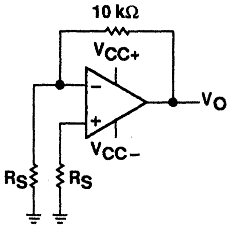
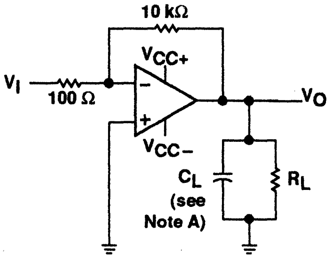


FIGURE 3. NOISE VOLTAGE TEST CIRCUIT



NOTE A: C_L includes fixture capacitance.

FIGURE 4. UNITY-GAIN BANDWIDTH AND PHASE MARGIN TEST CIRCUIT

typical values

Typical values as presented in this data sheet represent the median (50% point) of device parametric performance.

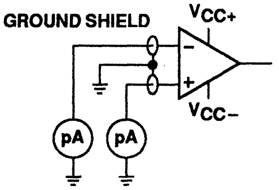


FIGURE 5. INPUT BIAS AND OFFSET CURRENT TEST CIRCUIT

input bias and offset current

At the picoamp-bias-current level typical of the TL051 and TL051A, accurate measurement of the bias current becomes difficult. Not only does this measurement require a picoammeter, but test socket leakages can easily exceed the actual device bias currents. To accurately measure these small currents, Texas Instruments uses a two-step process. The socket leakage is measured using picoammeters with bias voltages applied but with no device in the socket. The device is then inserted in the socket and a second test that measures both the socket leakage and the device input bias current is performed. The two measurements are then subtracted algebraically to determine the bias current of the device.

noise

Because of the increasing emphasis on low noise levels in many of today's applications, the input noise voltage density is sample-tested at f = 1 kHz. Texas Instruments also has additional noise testing capability to meet specific application requirements. Please contact the factory for details.

TYPICAL CHARACTERISTICS

table of graphs

			FIGURE
V_{IO}	Input offset voltage	Distribution	6
α_{VIO}	Temperature coefficient of input offset voltage	Distribution	7
I_{IO}	Input offset current	vs Temperature	8
I_{IB}	Input bias current	vs V_{IC} vs Temperature	9 8
V_I	Input voltage range	vs V_{CC} vs Temperature	10 11
V_O	Output voltage	vs Differential input voltage	12, 13
V_{OM}	Maximum peak output voltage swing	vs V_{CC} vs Output current vs Frequency vs Temperature	14 18, 19 15, 16, 17 20, 21
A_{VD}	Differential voltage amplification	vs R_L vs Frequency vs Temperature	22 23 24, 25
z_o	Output impedance	vs Frequency	29
CMRR	Common-mode rejection ratio	vs Frequency vs Temperature	26, 27 28
k_{SVR}	Supply-voltage rejection ratio	vs Temperature	30
I_{OS}	Short-circuit output current	vs V_{CC} vs Time vs Temperature	31 32 33
I_{CC}	Supply current	vs V_{CC} vs Temperature	34 35
SR	Slew rate	vs R_L vs Temperature	36, 37 38, 39
	Overshoot factor	vs C_L	40
V_n	Equivalent input noise voltage	vs Frequency	41
THD	Total harmonic distortion	vs Frequency	42
B_1	Unity-gain bandwidth	vs V_{CC} vs Temperature	43 44
ϕ_m	Phase margin	vs V_{CC} vs C_L vs Temperature	45 46 47
	Phase shift	vs Frequency	23
	Pulse response	Small-signal Large-signal	48 49

TYPICAL CHARACTERISTICS[†]

DISTRIBUTION OF TL051
INPUT OFFSET VOLTAGE

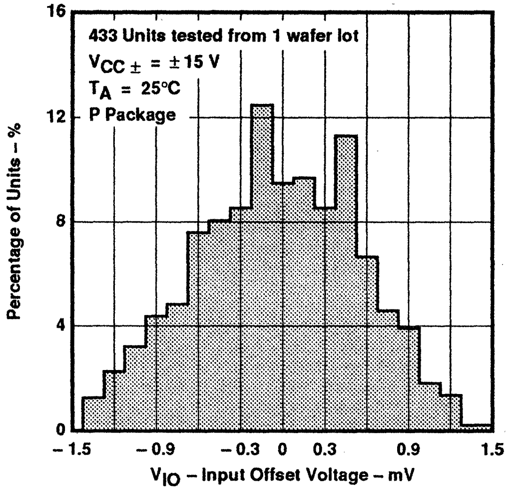


FIGURE 6

DISTRIBUTION OF TL051
INPUT OFFSET VOLTAGE
TEMPERATURE COEFFICIENT

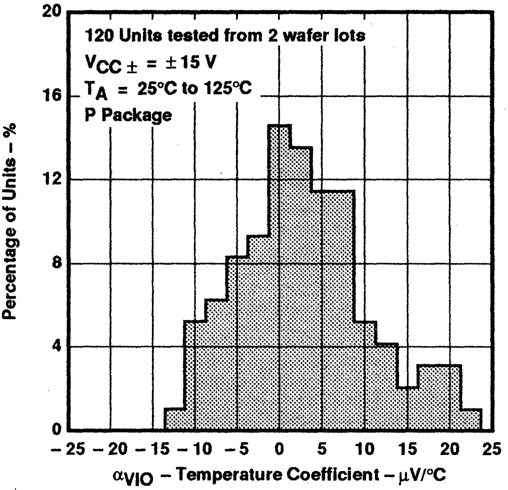


FIGURE 7

INPUT BIAS CURRENT AND
INPUT OFFSET CURRENT
vs
FREE-AIR TEMPERATURE

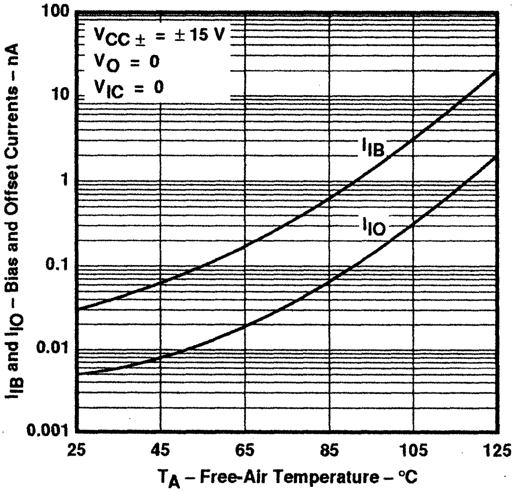


FIGURE 8

INPUT BIAS CURRENT
vs
COMMON-MODE INPUT VOLTAGE

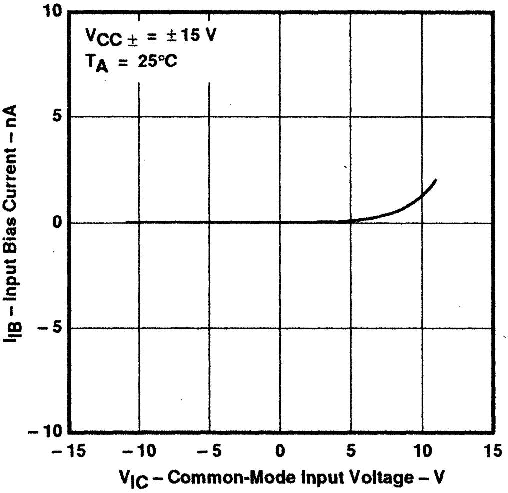


FIGURE 9

[†] Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

COMMON-MODE
INPUT VOLTAGE RANGE LIMITS
vs
SUPPLY VOLTAGE

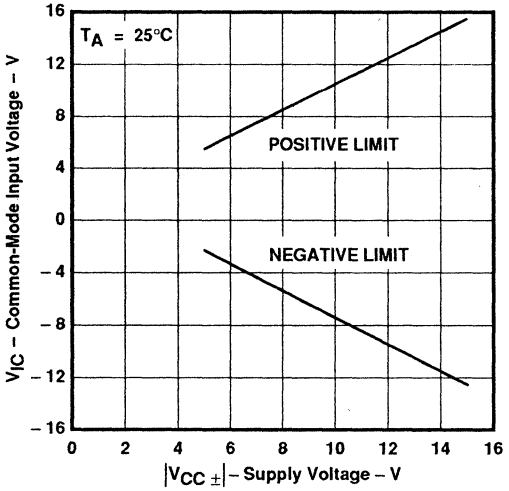


FIGURE 10

COMMON-MODE
INPUT VOLTAGE RANGE LIMITS
vs
FREE-AIR TEMPERATURE

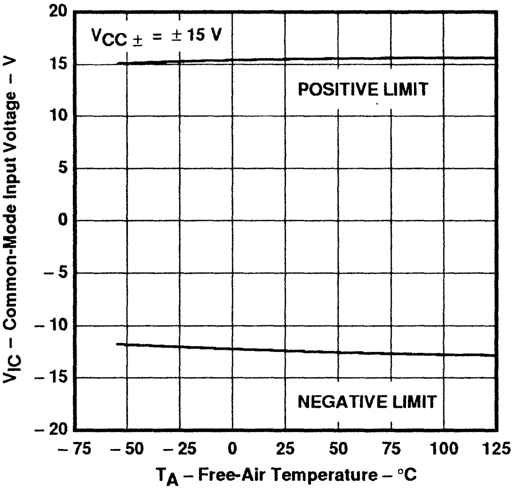


FIGURE 11

OUTPUT VOLTAGE
vs
DIFFERENTIAL INPUT VOLTAGE

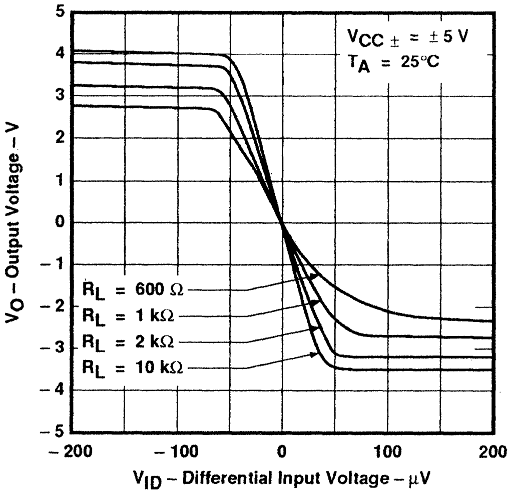


FIGURE 12

OUTPUT VOLTAGE
vs
DIFFERENTIAL INPUT VOLTAGE

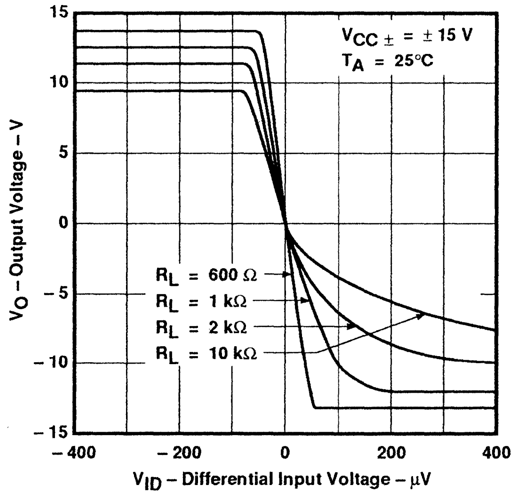


FIGURE 13

---

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

MAXIMUM PEAK OUTPUT VOLTAGE
vs
SUPPLY VOLTAGE

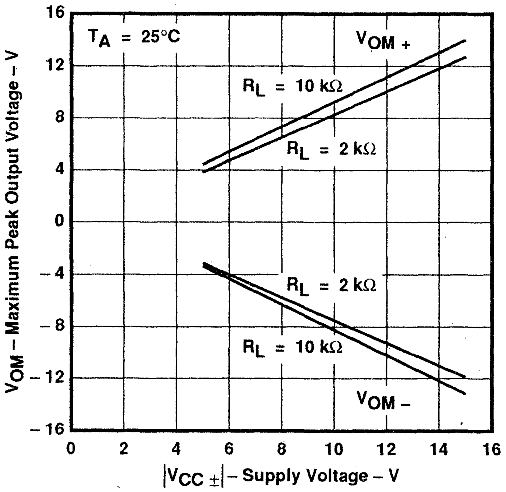


FIGURE 14

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE
vs
FREQUENCY

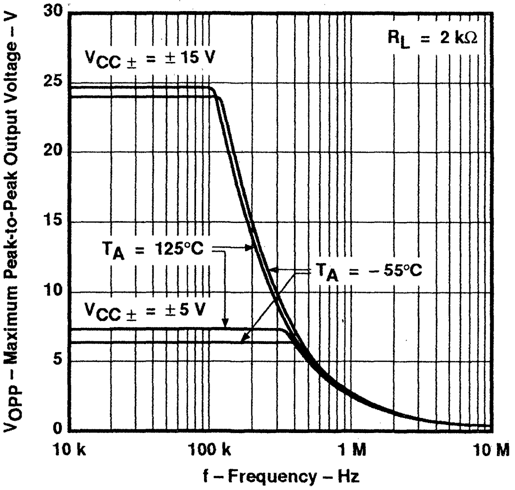


FIGURE 15

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE
vs
FREQUENCY

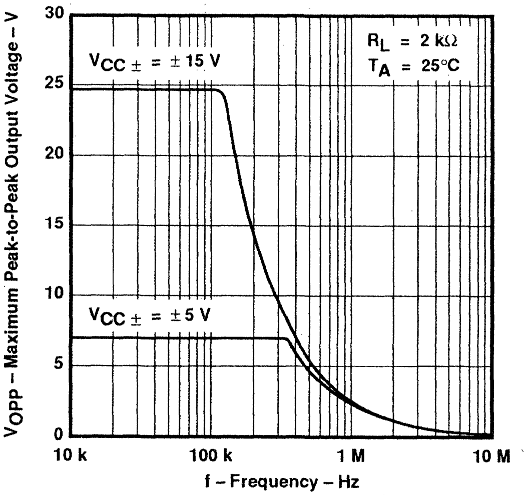


FIGURE 16

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE
vs
FREQUENCY

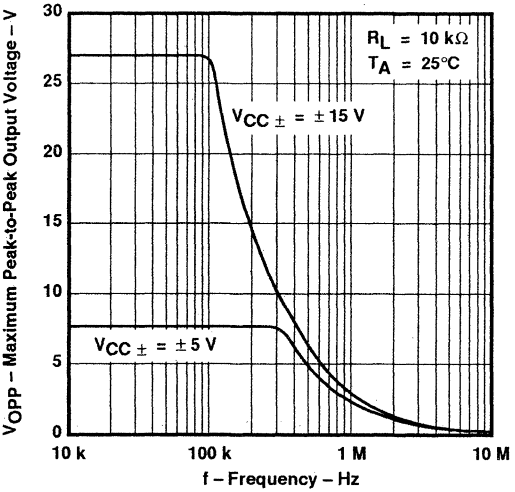


FIGURE 17

---

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

MAXIMUM PEAK OUTPUT VOLTAGE
vs
OUTPUT CURRENT

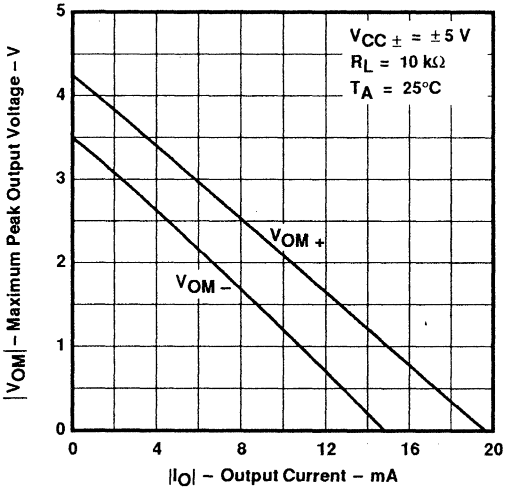


FIGURE 18

MAXIMUM PEAK OUTPUT VOLTAGE
vs
OUTPUT CURRENT

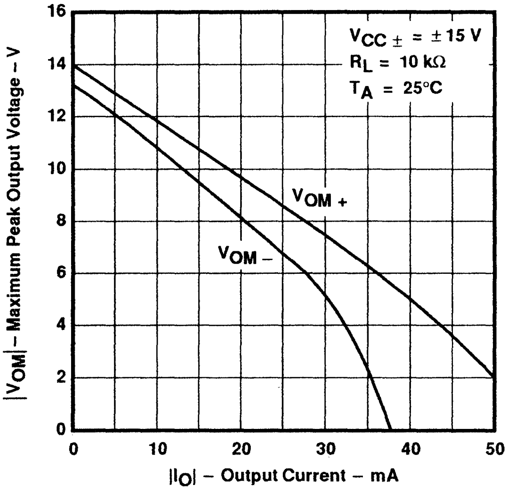


FIGURE 19

MAXIMUM PEAK OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

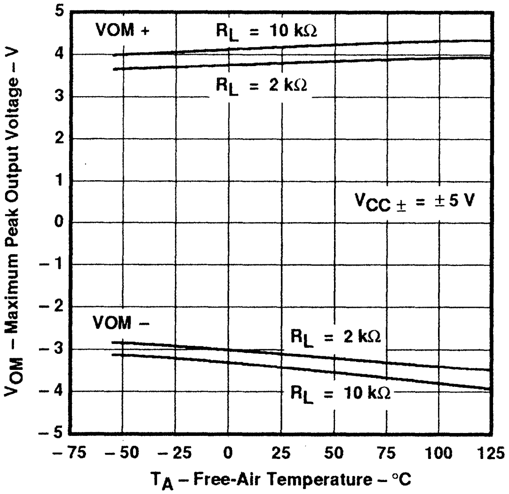


FIGURE 20

MAXIMUM PEAK OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

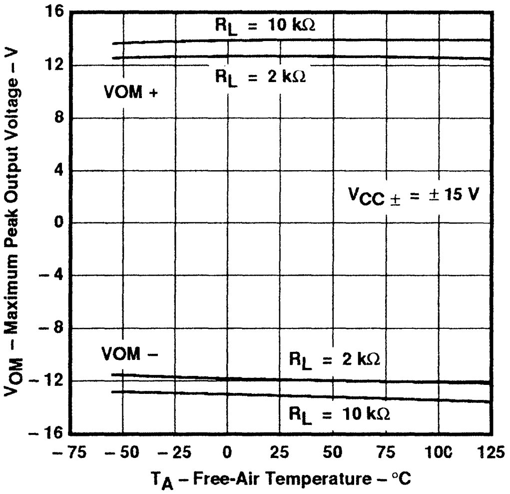


FIGURE 21

---

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS[†]

LARGE-SIGNAL VOLTAGE AMPLIFICATION vs LOAD RESISTANCE

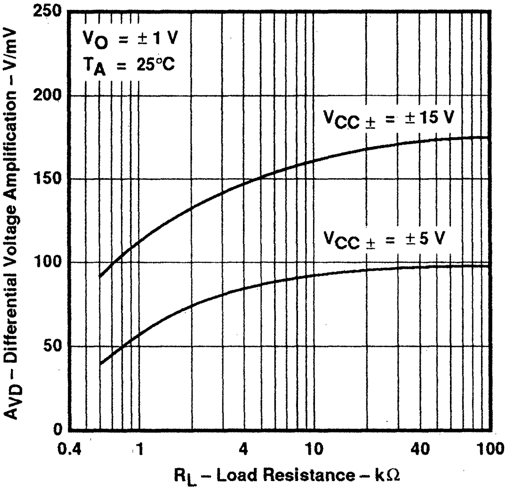


FIGURE 22

LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION AND PHASE SHIFT vs FREQUENCY

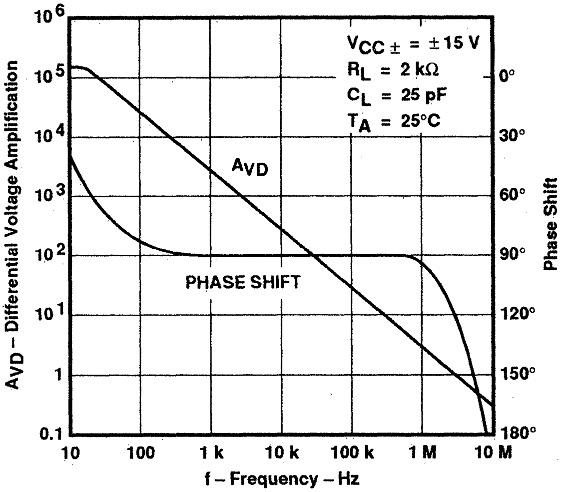


FIGURE 23

LARGE-SIGNAL VOLTAGE AMPLIFICATION vs FREE-AIR TEMPERATURE

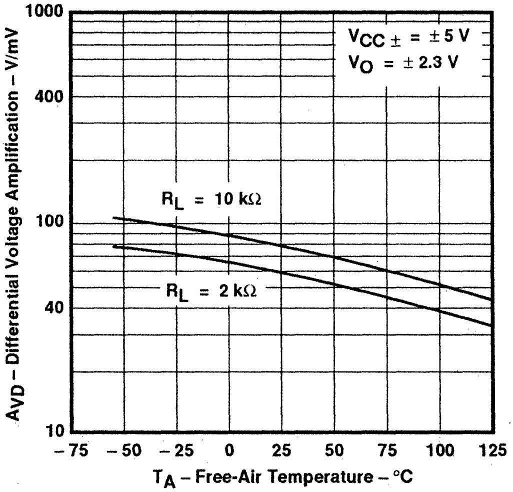


FIGURE 24

LARGE-SIGNAL VOLTAGE AMPLIFICATION vs FREE-AIR TEMPERATURE

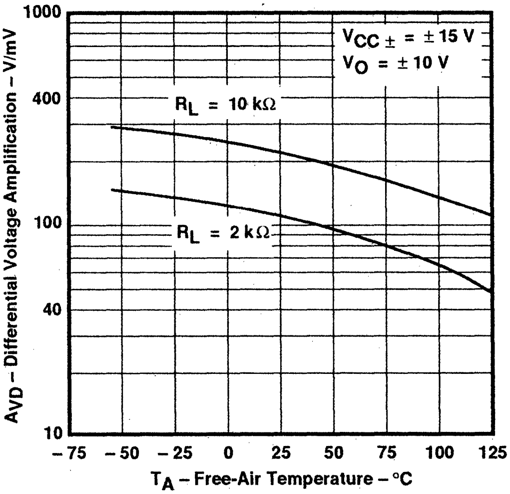


FIGURE 25

[†] Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

COMMON-MODE REJECTION RATIO
vs
FREQUENCY

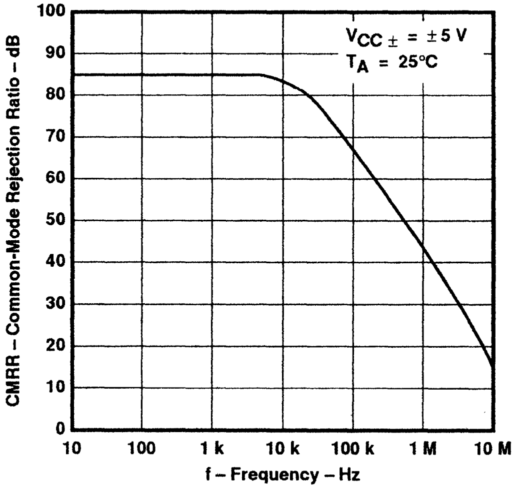


FIGURE 26

COMMON-MODE REJECTION RATIO
vs
FREQUENCY

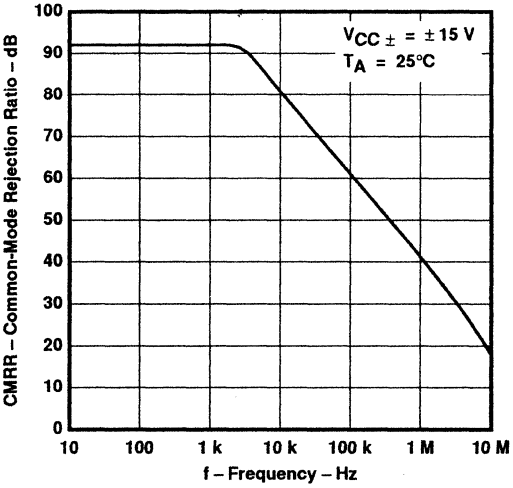


FIGURE 27

COMMON-MODE REJECTION RATIO
vs
FREE-AIR TEMPERATURE

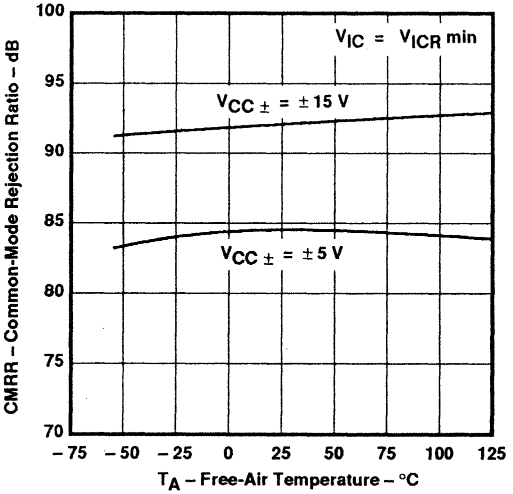


FIGURE 28

OUTPUT IMPEDANCE
vs
FREQUENCY

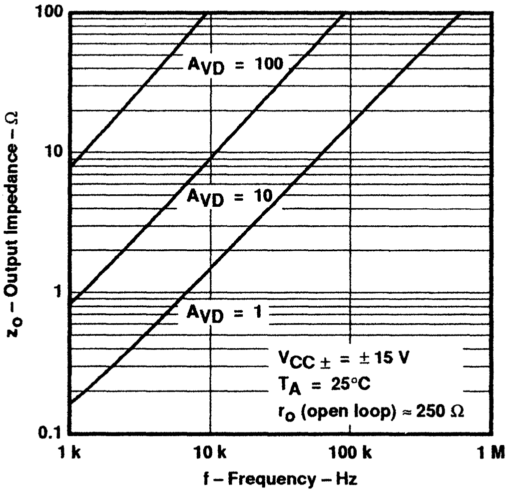


FIGURE 29

---

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

SUPPLY-VOLTAGE REJECTION RATIO
vs
FREE-AIR TEMPERATURE

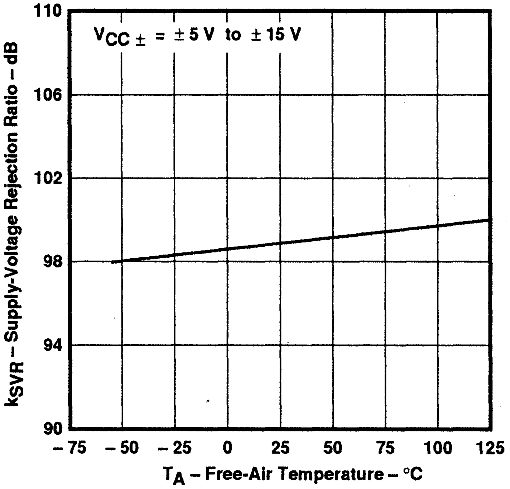


FIGURE 30

SHORT-CIRCUIT OUTPUT CURRENT
vs
SUPPLY VOLTAGE

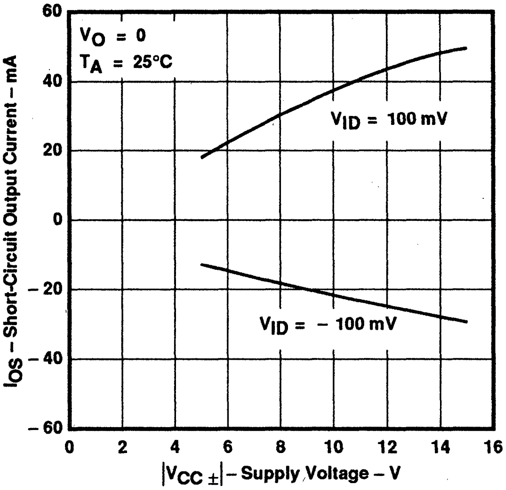


FIGURE 31

SHORT-CIRCUIT OUTPUT CURRENT
vs
TIME

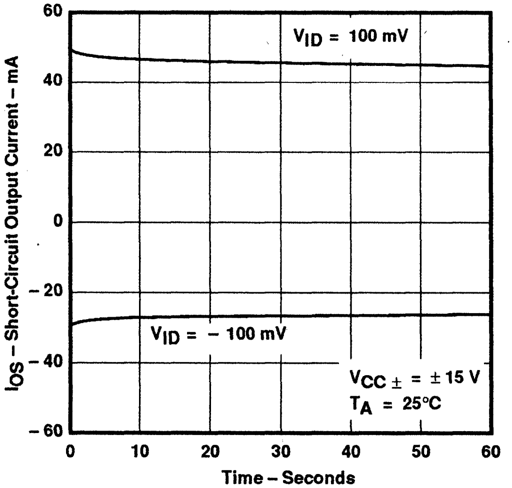


FIGURE 32

SHORT-CIRCUIT OUTPUT CURRENT
vs
FREE-AIR TEMPERATURE

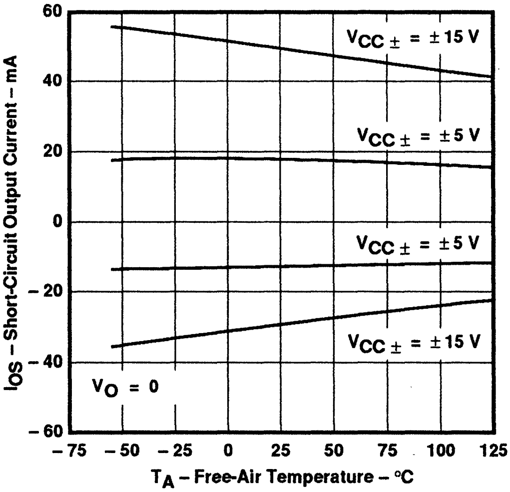


FIGURE 33

---

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

SUPPLY CURRENT
vs
SUPPLY VOLTAGE

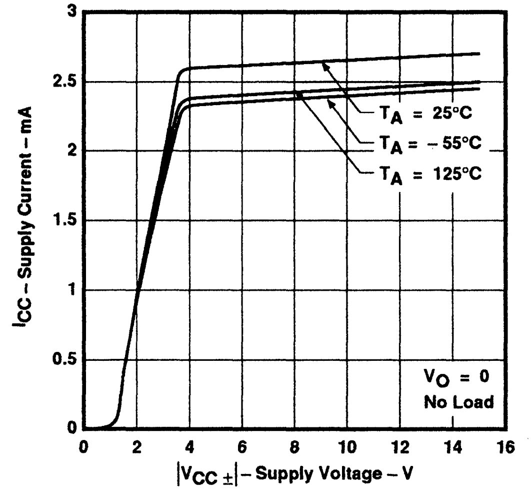


FIGURE 34

SUPPLY CURRENT
vs
FREE-AIR TEMPERATURE

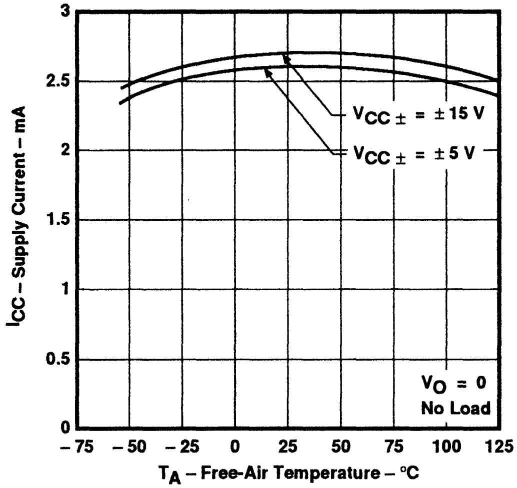


FIGURE 35

SLEW RATE
vs
LOAD RESISTANCE

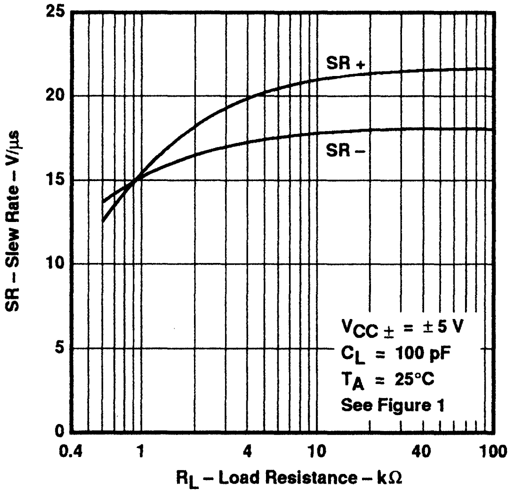


FIGURE 36

SLEW RATE
vs
LOAD RESISTANCE

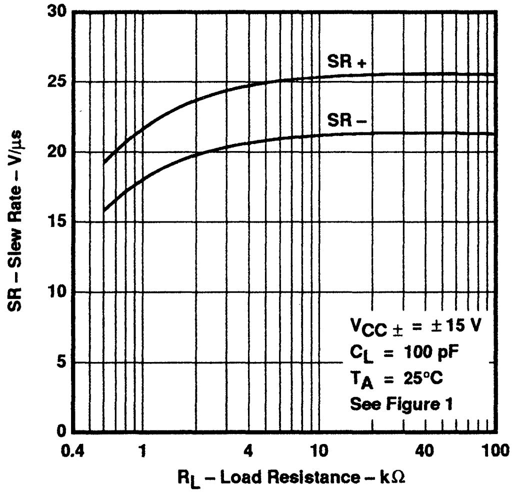


FIGURE 37

---

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS[†]

SLEW RATE
vs
FREE-AIR TEMPERATURE

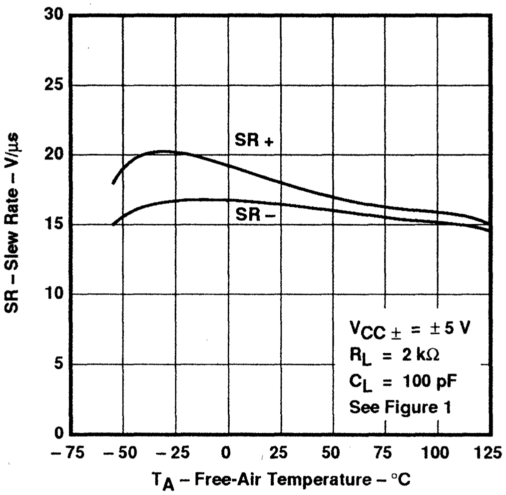


FIGURE 38

SLEW RATE
vs
FREE-AIR TEMPERATURE

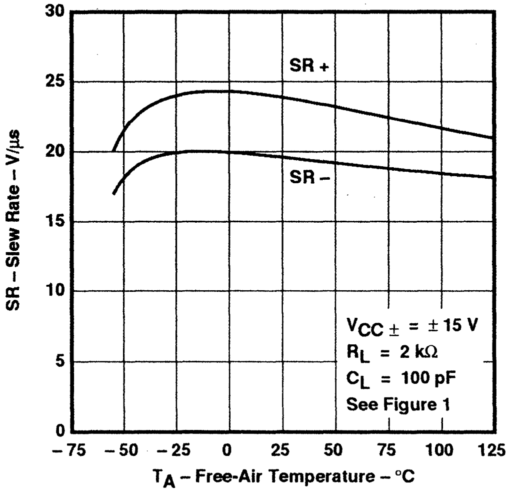


FIGURE 39

OVERSHOOT FACTOR
vs
LOAD CAPACITANCE

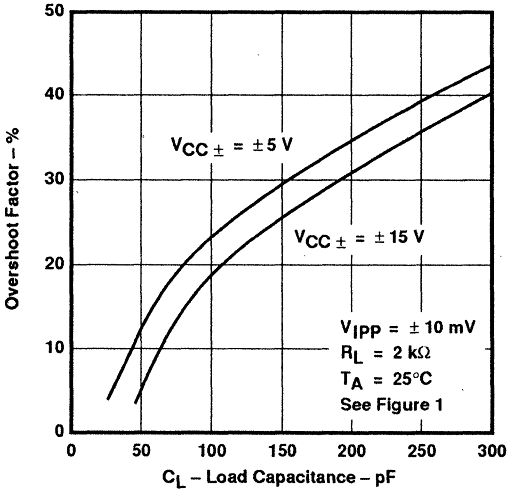


FIGURE 40

EQUIVALENT INPUT NOISE VOLTAGE
vs
FREQUENCY

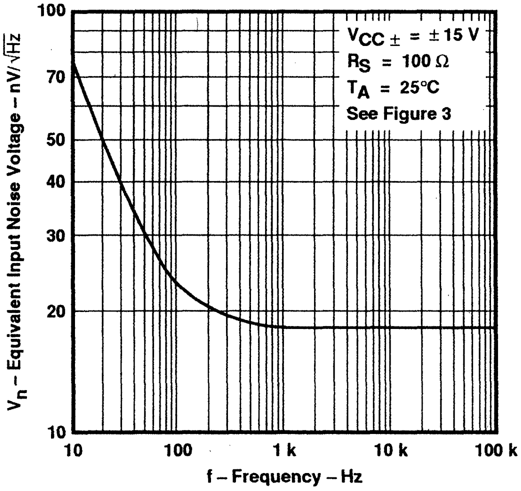


FIGURE 41

[†] Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

TOTAL HARMONIC DISTORTION
vs
FREQUENCY

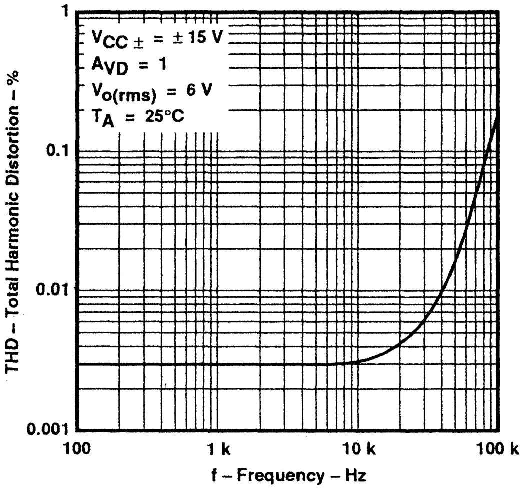


FIGURE 42

UNITY-GAIN BANDWIDTH
vs
SUPPLY VOLTAGE

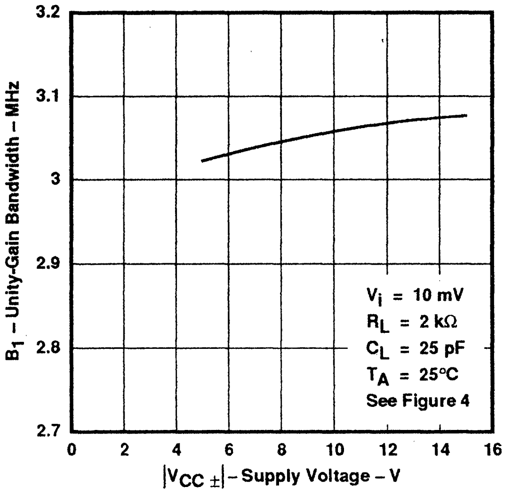


FIGURE 43

UNITY-GAIN BANDWIDTH
vs
FREE-AIR TEMPERATURE

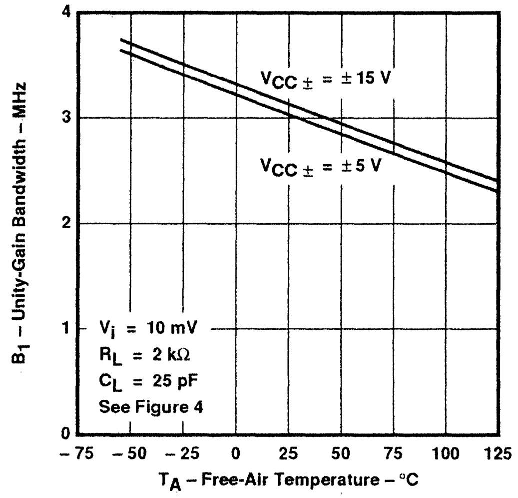


FIGURE 44

PHASE MARGIN
vs
SUPPLY VOLTAGE

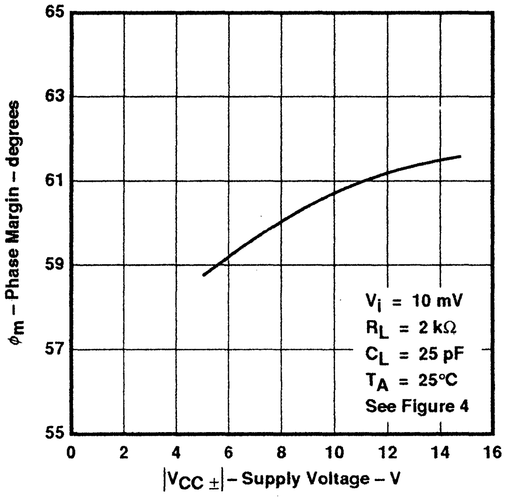


FIGURE 45

---

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

PHASE MARGIN
vs
LOAD CAPACITANCE

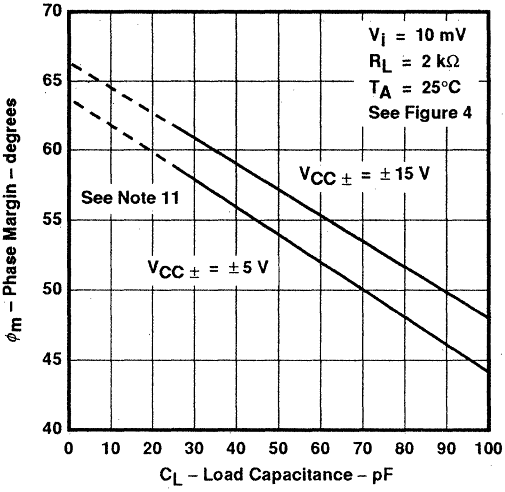


FIGURE 46

PHASE MARGIN
vs
FREE-AIR TEMPERATURE

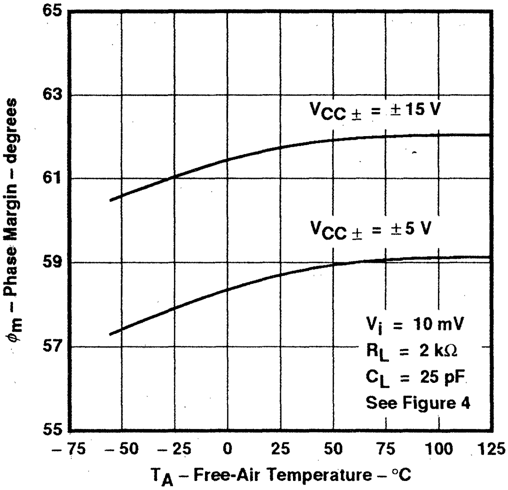


FIGURE 47

VOLTAGE-FOLLOWER
SMALL-SIGNAL
PULSE RESPONSE

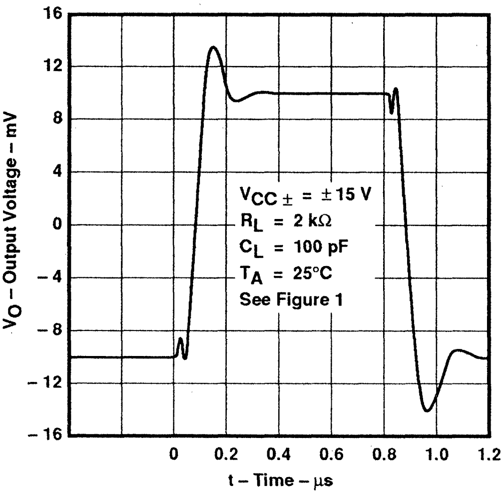


FIGURE 48

VOLTAGE-FOLLOWER
LARGE-SIGNAL
PULSE RESPONSE

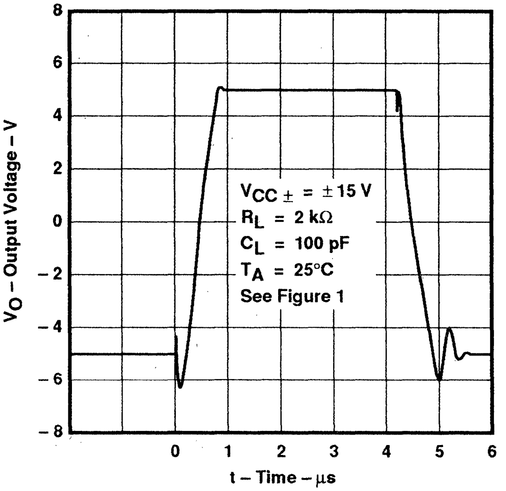


FIGURE 49

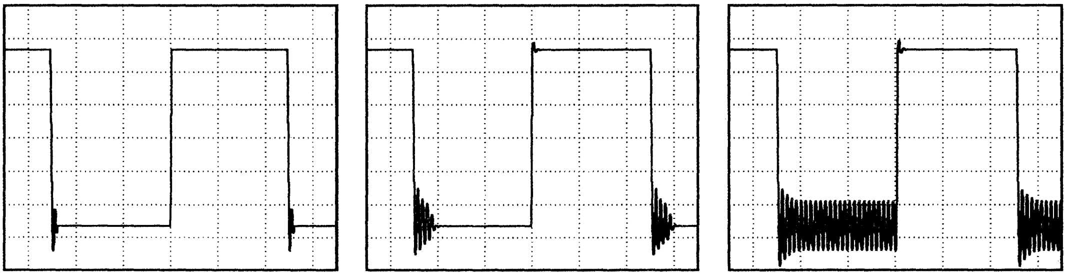
---

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.
NOTE 11: Values of phase margin below a load capacitance of 25 pF were estimated.

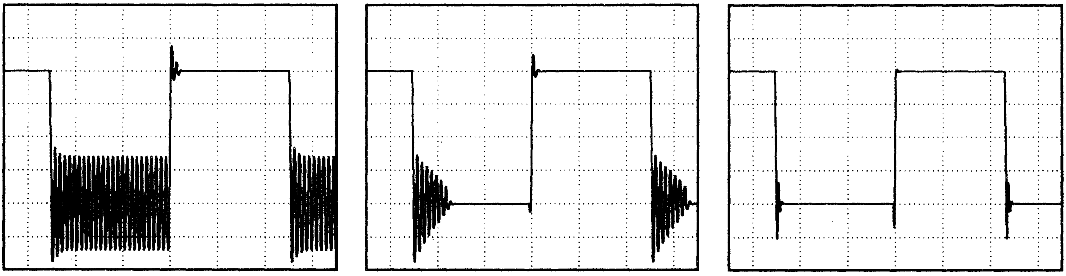
TYPICAL APPLICATION DATA

output characteristics

All operating characteristics (except bandwidth and phase margin) are specified with 100-pF load capacitance. The TL051 and TL051A will drive higher capacitive loads; however, as the load capacitance increases, the resulting response pole occurs at lower frequencies, thereby causing ringing, peaking, or even oscillation. The value of the load capacitance at which oscillation occurs varies with production lots. If an application appears to be sensitive to oscillation due to load capacitance, adding a small resistance in series with the load should alleviate the problem. Capacitive loads of 1000 pF and larger may be driven if enough resistance is added in series with the output (see Figure 50).

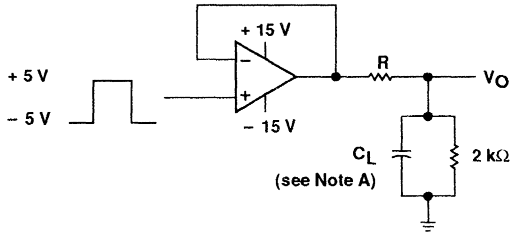


(a) C_L = 100 pF, R = 0 (b) C_L = 300 pF, R = 0 (c) C_L = 350 pF, R = 0



(d) C_L = 1000 pF, R = 0 (e) C_L 1000 pF, R = 50 Ω (f) C_L = 1000 pF, R = 2 kΩ

FIGURE 50. EFFECT OF CAPACITIVE LOADS



NOTE A: C_L includes fixture capacitance.

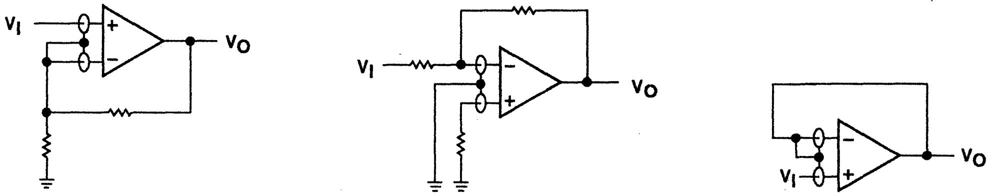
FIGURE 51. TEST CIRCUIT FOR OUTPUT CHARACTERISTICS

TYPICAL APPLICATION DATA

input characteristics

The TL051 and TL051A are specified with a minimum and a maximum input voltage that, if exceeded at either input, could cause the device to malfunction.

Because of the extremely high input impedance and resulting low bias current requirements, the TL051 and TL051A are well suited for low-level signal processing; however, leakage currents on printed circuit boards and sockets can easily exceed bias current requirements and cause degradation in system performance. It is good practice to include guard rings around inputs (see Figure 52). These guards should be driven from a low-impedance source at the same voltage level as the common-mode input.



(a) NONINVERTING AMPLIFIER (b) INVERTING AMPLIFIER (c) UNITY-GAIN AMPLIFIER

FIGURE 52. USE OF GUARD RINGS

noise performance

The noise specifications in op amp circuits are greatly dependent on the current in the first-stage differential amplifier. The low input bias current requirements of the TL051 and TL051A result in a very low current noise. This feature makes the devices especially favorable over bipolar devices when using values of circuit impedance greater than 50 kΩ.

TYPICAL APPLICATION DATA

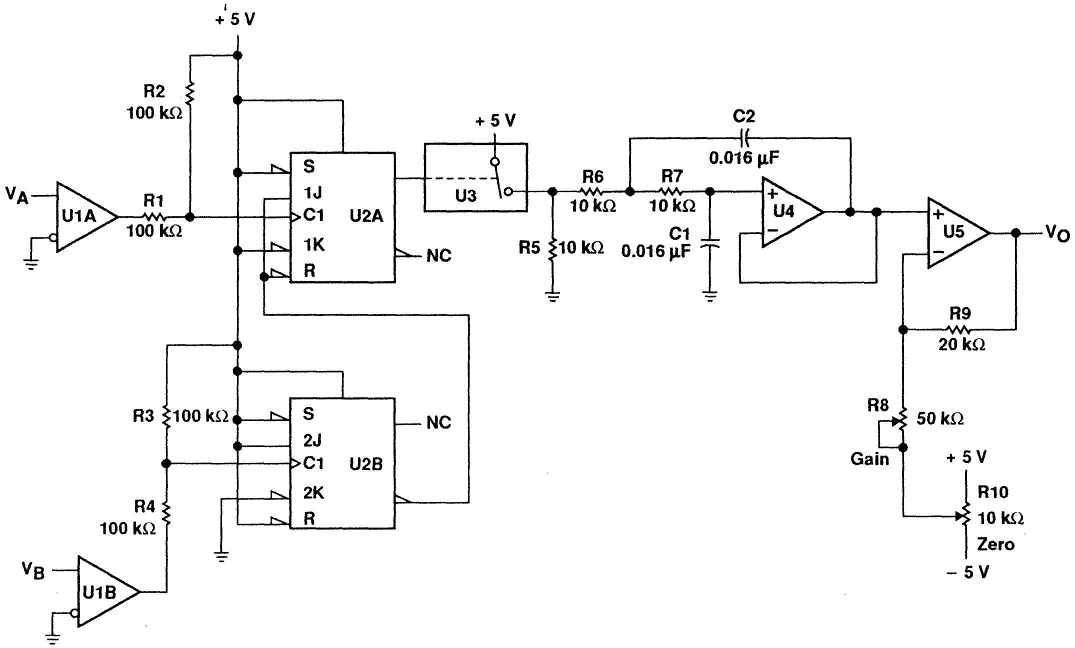
phase meter

The phase meter in Figure 53 produces an output voltage of 10 mV per degree of phase delay between the two input signals V_A and V_B. The reference signal V_A must be the same frequency as V_B. The TLC3702 comparators (U1) convert these two input sine waves into ± 5-V square waves. Then R1 and R4 provide level shifting prior to the SN74HC109 dual J-K flip flop.

Flip-flop U2B is connected as a toggle flip-flop and generates a square wave at half the frequency of V_B. Flip-flop U2A also produces a square wave at half the input frequency. The pulse duration of U2A varies from zero to half the period, where zero corresponds to zero phase delay between V_A and V_B, and half the period corresponds to V_B lagging V_A by 360 degrees.

The output pulse from U2A causes the TLC4066 (U3) switch to charge the TL051 (U4) integrator capacitors C1 and C2. As the phase delay approaches 360 degrees, the output of U2A approximates a square wave, and U4 has an output of almost 2.5 V. U5 acts as a noninverting amplifier with a gain of 1.44 in order to scale the 0- to 2.5-V integrator output to a 0- to 3.6-V output range.

R8 and R10 provide output gain and zero-level calibration. This circuit operates over a 100-Hz to 10-kHz frequency range.



NOTES: U1 = TLC3702; $V_{CC\pm}$ = ±5 V.
U2 = SN74HC109.
U3 = TLC4066.
U4,U5 = TL051; $V_{CC\pm}$ = ±5 V.

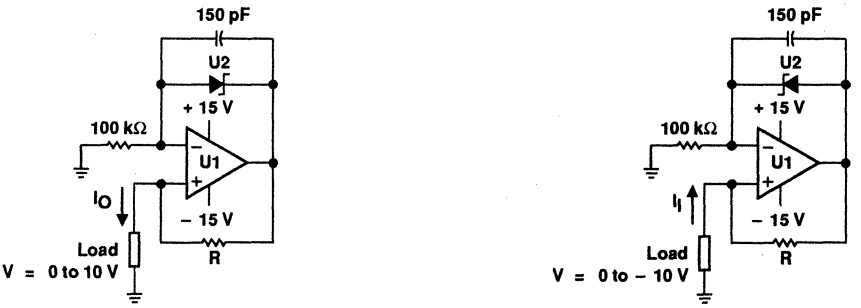
FIGURE 53. PHASE METER

TYPICAL APPLICATION DATA

precision constant-current source over temperature

A precision current source benefits from the high input impedance and stability of Texas Instruments enhanced JFET process. A low-current shunt regulator maintains 2.5 V between the inverting input and the output of the TL051. The negative feedback then forces 2.5 V across the current setting resistor R; therefore, the current to the load is simply 2.5 V divided by R.

Possible choices for the shunt regulator include the LT1004, LT1009, and LM385. Note that if the regulator's cathode connects to the op amp output, this circuit will source load current. Similarly, if the cathode connects to the inverting input, the circuit will sink current from the load. To minimize output current change with temperature, R should be a metal film resistor with a low temperature coefficient. Also, this circuit must be operated with split voltage supplies.



(a) SOURCE CURRENT LOAD

(b) SINK CURRENT LOAD

NOTES: U1 = TL051.
U2 = LM385, LT1004, or LT1009 voltage reference.
$I = \frac{2.5\ \text{V}}{R}$, R = Low temperature coefficient metal film resistor.

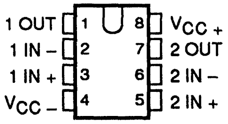
FIGURE 54. PRECISION CONSTANT-CURRENT SOURCE

TL052, TL052A
ENHANCED JFET PRECISION DUAL OPERATIONAL AMPLIFIERS

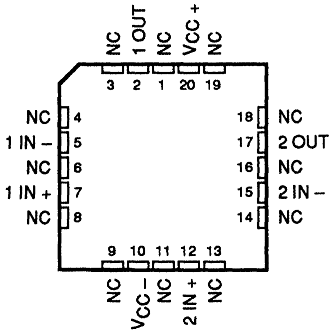
D3235, JUNE 1988 – REVISED FEBRUARY 1991

- **Maximum Offset Voltage . . . 800 µV (TL052A)**
- **High Slew Rate . . . 17.8 V/µs Typ at 25°C**
- **Low Total Harmonic Distortion . . . 0.003% Typ at R_L = 2 kΩ**
- **Low Noise Voltage . . . 19 nV/√Hz Typ at f = 1 kHz**
- **Low Input Bias Currents . . . 30 pA Typ**

D, JG, or P PACKAGE
(TOP VIEW)

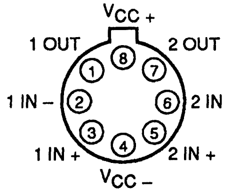


FK PACKAGE
(TOP VIEW)



NC – No internal connection

L PACKAGE
(TOP VIEW)



Pin 4 is in electrical contact with the case

description

The TL052 and TL052A dual operational amplifiers incorporate well-matched, high-voltage JFET and bipolar transistors in a monolithic integrated circuit. These devices offer the significant advantages of Texas Instruments new enhanced JFET process. This process affords not only low initial offset voltage due to the on-chip zener trim capability but also stable offset voltage over time and temperature. In comparison, traditional JFET processes are plagued by significant offset voltage drift.

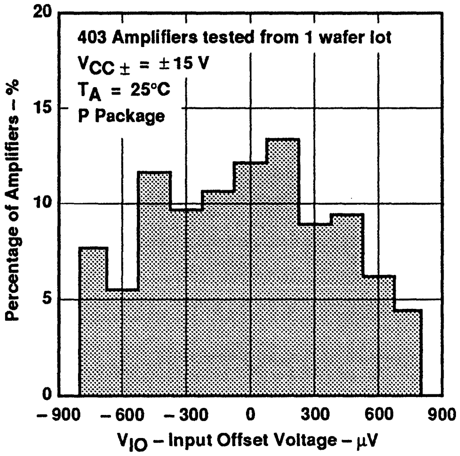
This new enhanced process still maintains the traditional JFET advantages of fast slew rates and low input bias and offset currents. These advantages coupled with low noise and low harmonic distortion make the TL052 well-suited for new state-of-the-art designs as well as existing design upgrades. The TL052 has been

AVAILABLE OPTIONS

T_A	V_{IO} max AT 25°C	PACKAGE				
		SMALL-OUTLINE (D)	CHIP CARRIER (FK)	CERAMIC DIP (JG)	METAL CAN (L)	PLASTIC DIP (P)
0°C to 70°C	800 µV	TL052ACD	——	——	——	TL052ACP
	1500 µV	TL052CD	——	——	——	TL052CP
– 40°C to 85°C	800 µV	TL052AID	——	——	——	TL052AIP
	1500 µV	TL052ID	——	——	——	TL052IP
– 55°C to 125°C	800 µV	TL052AMD	TL052AMFK	TL052AMJG	TL052AML	TL052AMP
	1500 µV	TL052MD	TL052MFK	TL052MJG	TL052ML	TL052MP

D packages are available taped and reeled. Add "R" suffix to device type, (e.g., TL052CDR).

DISTRIBUTION OF TL052A
INPUT OFFSET VOLTAGE



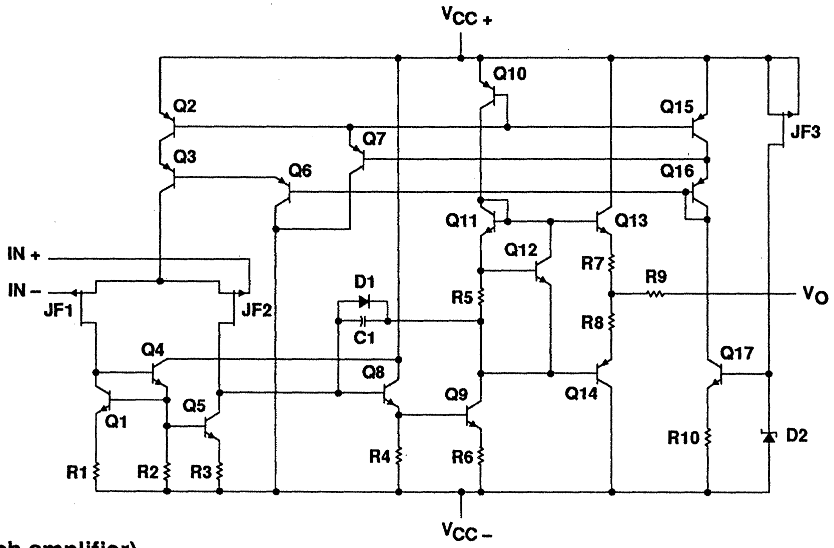
description (continued)

designed to be functionally compatible, as well as pin compatible, with the TL072 and TL082. Two offset voltage grades are available: TL052 (1.5 mV max) and TL052A (800 µV max).

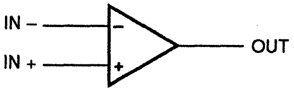
A variety of available packaging options includes small-outline and chip carrier versions for high-density system applications.

The C-suffix devices are characterized for operation from 0°C to 70°C. The I-suffix devices are characterized for operation from – 40°C to 85°C. The M-suffix devices are characterized for operation over the full military temperature range of – 55°C to 125°C.

equivalent schematic (each amplifier)



symbol (each amplifier)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC+} (see Note 1)	18 V
Supply voltage, V_{CC-} (see Note 1)	– 18 V
Differential input voltage (see Note 2)	± 30 V
Input voltage range, V_I (any input, see Notes 1 and 3)	± 15 V
Input current, I_I (each input)	± 1 mA
Output current, I_O (each output)	± 80 mA
Total current into V_{CC+} terminal	160 mA
Total current out of V_{CC-} terminal	160 mA
Duration of short-circuit current at (or below) 25°C (see Note 4)	unlimited
Continuous total dissipation	See Dissipation Rating Table
Operating free-air temperature range, T_A: C-suffix	0°C to 70°C
I-suffix	– 40°C to 85°C
M-suffix	– 55°C to 125°C
Storage temperature range	– 65°C to 150°C
Case temperature for 60 seconds: FK package	260°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D or P package	260°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: JG or L package	300°C

NOTES:
1. All voltage values, except differential voltages, are with respect to the midpoint between V_{CC+} and V_{CC-}.
2. Differential voltages are at the noninverting input with respect to the inverting input.
3. The magnitude of the input voltage must never exceed the magnitude of the supply voltage or 15 V, whichever is less.
4. The output may be shorted to either supply. Temperature and/or supply voltages must be limited to ensure that the maximum dissipation rating is not exceeded.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING	$T_A = 125°C$ POWER RATING
D	725 mW	5.8 mW/°C	464 mW	377 mW	145 mW
FK	1375 mW	11.0 mW/°C	880 mW	715 mW	275 mW
JG	1050 mW	8.4 mW/°C	672 mW	546 mW	210 mW
L	825 mW	6.6 mW/°C	528 mW	429 mW	165 mW
P	1000 mW	8.0 mW/°C	640 mW	520 mW	200 mW

recommended operating conditions

		C-SUFFIX			I-SUFFIX			M-SUFFIX			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		± 5		± 15	± 5		± 15	± 5		± 15	V
Common-mode input voltage, V_{IC}	$V_{CC\pm} = \pm 5$ V	– 1		4	– 1		4	– 1		4	V
	$V_{CC\pm} = \pm 15$ V	– 11		11	– 11		11	– 11		11	
Operating free-air temperature, T_A		0		70	– 40		85	– 55		125	°C

electrical characteristics

PARAMETER		TEST CONDITIONS		T_A†	$V_{CC\pm} = \pm 5$ V			$V_{CC\pm} = \pm 15$ V			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	$V_O = 0$, $V_{IC} = 0$, $R_S = 50\ \Omega$	TL052C	25°C		0.73	3.5		0.65	1.5	mV
				Full range			4.5			2.5	
			TL052AC	25°C		0.51	2.8		0.4	0.8	
				Full range			3.8			1.8	
α_{VIO}	Temperature coefficient of input offset voltage (see Note 9)		TL052C	25°C to 70°C		8			8		µV/°C
			TL052AC	25°C to 70°C		8			6	25	
	Input offset voltage long-term drift (see Note 5)			25°C		0.04			0.04		µV/mo
I_{IO}	Input offset current	$V_O = 0$, $V_{IC} = 0$, See Figure 5		25°C		4	100		5	100	pA
				70°C		0.02	1		0.025	1	nA
I_{IB}	Input bias current	$V_O = 0$, $V_{IC} = 0$, See Figure 5		25°C		20	200		30	200	pA
				70°C		0.15	4		0.2	4	nA
V_{ICR}	Common-mode input voltage range			25°C	−1 to 4	−2.3 to 5.6		−11 to 11	−12.3 to 15.6		V
				Full range	−1 to 4			−11 to 11			
V_{OM+}	Maximum positive peak output voltage swing	$R_L = 10\ k\Omega$		25°C	3	4.2		13	13.9		V
				Full range	3			13			
		$R_L = 2\ k\Omega$		25°C	2.5	3.8		11.5	12.7		
				Full range	2.5			11.5			
V_{OM-}	Maximum negative peak output voltage swing	$R_L = 10\ k\Omega$		25°C	−2.5	−3.5		−12	−13.2		V
				Full range	−2.5			−12			
		$R_L = 2\ k\Omega$		25°C	−2.3	−3.2		−11	−12		
				Full range	−2.3			−11			
A_{VD}	Large-signal differential voltage amplification	$R_L = 2\ k\Omega$, See Note 6		25°C	25	59		50	105		V/mV
				0°C	30	65		60	129		
				70°C	20	46		30	85		
r_i	Input resistance			25°C		10^{12}			10^{12}		Ω
C_i	Input capacitance			25°C		10			12		pF
CMRR	Common-mode rejection ratio	$V_{IC} = V_{ICR}$ min, $V_O = 0$, $R_S = 50\ \Omega$		25°C	65	85		75	93		dB
				0°C	65	84		75	92		
				70°C	65	84		75	91		
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm} / \Delta V_{IO}$)	$V_{CC\pm} = \pm 5$ V to ± 15 V, $V_O = 0$, $R_S = 50\ \Omega$		25°C	75	99		75	99		dB
				0°C	75	98		75	98		
				70°C	75	97		75	97		
I_{CC}	Supply current (four amplifiers)	No load, $V_O = 0$		25°C		4.6	5.6		4.8	5.6	mA
				0°C		4.7	6.4		4.8	6.4	
				70°C		4.4	6.4		4.6	6.4	
V_{o1}/V_{o2}	Crosstalk attenuation	$A_{VD} = 100$		25°C		120			120		dB

† Full range is 0°C to 70°C.

NOTES: 5. Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at $T_A = 150$°C extrapolated to $T_A = 25$°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

6. For $V_{CC\pm} = \pm 5$ V, $V_O = \pm 2.3$ V; at $V_{CC\pm} = \pm 15$ V, $V_O = \pm 10$ V.

9. This parameter is tested on a sample basis for the TL052A. For other test requirements, please contact the factory. This statement has no bearing on testing or nontesting of other parameters.

operating characteristics

PARAMETER		TEST CONDITIONS		T_A†	$V_{CC\pm} = \pm5$ V			$V_{CC\pm} = \pm15$ V			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
SR +	Positive slew rate at unity gain	R_L = 2 kΩ, C_L = 100 pF, See Figure 1 and Note 7		25°C		17.8		13	20.7		V/µs
				0°C		18.5		11	20.9		
				70°C		16.5		11	20.8		
SR –	Negative slew rate at unity gain			25°C		15.4		13	17.8		
				0°C		15.7		11	18.5		
				70°C		14.7		11	16.5		
t_r	Rise time	V_{IPP} = ± 10 mV, R_L = 2 kΩ, C_L = 100 pF, See Figures 1 and 2		25°C		55			56		ns
				0°C		54			55		
				70°C		63			63		
t_f	Fall time			25°C		55			57		
				0°C		54			56		
				70°C		62			64		
	Overshoot factor			25°C		24%			19%		
				0°C		24%			19%		
				70°C		24%			19%		
V_n	Equivalent input noise voltage (see Note 10)	R_S = 100 Ω, See Figure 3	f = 10 Hz	25°C		71			71		nV/√Hz
			f = 1 kHz	25°C		19			19	30	
V_{NPP}	Peak-to-peak equivalent input noise voltage		f = 10 Hz to 10 kHz	25°C		4			4		µV
I_n	Equivalent input noise current	f = 1 kHz		25°C		0.01			0.01		pA/√Hz
THD	Total harmonic distortion	R_S = 1 kΩ, R_L = 2 kΩ, f = 1 kHz, See Note 8		25°C		0.003%			0.003%		
B_1	Unity-gain bandwidth	V_i = 10 mV, R_L = 2 kΩ, C_L = 25 pF, See Figure 4		25°C		3			3		MHz
				0°C		3.2			3.2		
				70°C		2.6			2.7		
ϕ_m	Phase margin at unity gain	V_i = 10 mV, R_L = 2 kΩ, C_L = 25 pF, See Figure 4		25°C		60°			63°		
				0°C		59°			63°		
				70°C		60°			63°		

† Full range is 0°C to 70°C.

NOTES: 7. For $V_{CC\pm} = \pm5$ V, $V_{IPP} = \pm1$ V; for $V_{CC\pm} = \pm15$ V, $V_{IPP} = \pm5$ V.

8. For $V_{CC\pm} = \pm5$ V, $V_{O(rms)} = 1$ V; for $V_{CC\pm} = \pm15$ V, $V_{O(rms)} = 6$ V.

10. This parameter is tested on a sample basis. For other test requirements, please contact the factory. This statement has no bearing on testing or nontesting of other parameters.

electrical characteristics

PARAMETER		TEST CONDITIONS		T_A†	$V_{CC\pm} = \pm 5$ V			$V_{CC\pm} = \pm 15$ V			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	$V_O = 0$, $V_{IC} = 0$, $R_S = 50\ \Omega$	TL052I	25°C		0.73	3.5		0.65	1.5	mV
				Full range			5.3			3.3	
			TL052AI	25°C		0.51	2.8		0.4	0.8	
				Full range			4.6			2.6	
α_{VIO}	Temperature coefficient of input offset voltage (see Note 9)		TL052I	25°C to 85°C		7			6		μV/°C
			TL052AI	25°C to 85°C		6			6	25	
	Input offset voltage long-term drift (see Note 5)			25°C		0.04			0.04		μV/mo
I_{IO}	Input offset current	$V_O = 0$, $V_{IC} = 0$, See Figure 5		25°C		4	100		5	100	pA
				85°C		0.06	10		0.07	10	nA
I_{IB}	Input bias current	$V_O = 0$, $V_{IC} = 0$, See Figure 5		25°C		20	200		30	200	pA
				85°C		0.6	20		0.7	20	nA
V_{ICR}	Common-mode input voltage range			25°C	−1 to 4	−2.3 to 5.6		−11 to 11	−12.3 to 15.6		V
				Full range	−1 to 4			−11 to 11			
V_{OM+}	Maximum positive peak output voltage swing	$R_L = 10\ k\Omega$		25°C	3	4.2		13	13.9		V
				Full range	3			13			
		$R_L = 2\ k\Omega$		25°C	2.5	3.8		11.5	12.7		
				Full range	2.5			11.5			
V_{OM-}	Maximum negative peak output voltage swing	$R_L = 10\ k\Omega$		25°C	−2.5	−3.5		−12	−13.2		V
				Full range	−2.5			−12			
		$R_L = 2\ k\Omega$		25°C	−2.3	−3.2		−11	−12		
				Full range	−2.3			−11			
A_{VD}	Large-signal differential voltage amplification	$R_L = 2\ k\Omega$, See Note 6		25°C	25	59		50	105		V/mV
				−40°C	30	74		60	145		
				85°C	20	43		30	76		
r_i	Input resistance			25°C		10^{12}			10^{12}		Ω
C_i	Input capacitance			25°C		10			12		pF
CMRR	Common-mode rejection ratio	$V_{IC} = V_{ICR}$ min, $V_O = 0$, $R_S = 50\ \Omega$		25°C	65	85		75	93		dB
				−40°C	65	83		75	90		
				85°C	65	84		75	93		
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm} / \Delta V_{IO}$)	$V_{CC\pm} = \pm 5$ V to ± 15 V, $V_O = 0$, $R_S = 50\ \Omega$		25°C	75	99		75	99		dB
				−40°C	75	98		75	98		
				85°C	75	99		75	99		
I_{CC}	Supply current (four amplifiers)	No load, $V_O = 0$		25°C		4.6	5.6		4.8	5.6	mA
				−40°C		4.5	6.4		4.7	6.4	
				85°C		4.4	6.4		4.6	6.4	
V_{o1}/V_{o2}	Crosstalk attenuation	$A_{VD} = 100$		25°C		120			120		dB

† Full range is − 40°C to 85°C.

NOTES: 5. Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at $T_A = 150°C$ extrapolated to $T_A = 25°C$ using the Arrhenius equation and assuming an activation energy of 0.96 eV.

6. For $V_{CC\pm} = \pm 5$ V, $V_O = \pm 2.3$ V; at $V_{CC\pm} = \pm 15$ V, $V_O = \pm 10$ V.

9. This parameter is tested on a sample basis for the TL052A. For other test requirements, please contact the factory. This statement has no bearing on testing or nontesting of other parameters.

operating characteristics

PARAMETER		TEST CONDITIONS		T_A†	$V_{CC\pm}$ = ±5 V			$V_{CC\pm}$ = ±15 V			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
SR +	Positive slew rate at unity gain	R_L = 2 kΩ, C_L = 100 pF, See Figure 1 and Note 7		25°C		17.8		13	20.7		V/µs
				– 40°C		18.8		11	20.6		
				85°C		16		11	20.7		
SR –	Negative slew rate at unity gain			25°C		15.4		13	17.8		
				– 40°C		16		11	17.8		
				85°C		14.5		11	17.2		
t_r	Rise time	V_{IPP} = ± 10 mV, R_L = 2 kΩ, C_L = 100 pF, See Figures 1 and 2		25°C		55			56		ns
				– 40°C		52			53		
				85°C		64			65		
t_f	Fall time			25°C		55			57		
				– 40°C		51			53		
				85°C		64			65		
	Overshoot factor			25°C		24%			19%		
				– 40°C		24%			19%		
				85°C		24%			19%		
V_n	Equivalent input noise voltage (see Note 10)	R_S = 100 Ω, See Figure 3	f = 10 Hz	25°C		71			71		nV/√Hz
			f = 1 kHz	25°C		19			19	30	
V_{NPP}	Peak-to-peak equivalent input noise voltage		f = 10 Hz to 10 kHz	25°C		4			4		µV
I_n	Equivalent input noise current	f = 1 kHz		25°C		0.01			0.01		pA/√Hz
THD	Total harmonic distortion	R_S = 1 kΩ, R_L = 2 kΩ, f = 1 kHz, See Note 8		25°C		0.003%			0.003%		
B_1	Unity-gain bandwidth	V_i = 10 mV, R_L = 2 kΩ, C_L = 25 pF, See Figure 4		25°C		3			3		MHz
				– 40°C		3.5			3.6		
				85°C		2.5			2.6		
ϕ_m	Phase margin at unity gain	V_i = 10 mV, R_L = 2 kΩ, C_L = 25 pF, See Figure 4		25°C		60°			63°		
				– 40°C		58°			61°		
				85°C		60°			63°		

† Full range is – 40°C to 85°C.

NOTES: 7. For $V_{CC\pm}$ = ±5 V, V_{IPP} = ± 1 V; for $V_{CC\pm}$ = ± 15 V, V_{IPP} = ±5 V.

8. For $V_{CC\pm}$ = ±5 V, $V_{O(rms)}$ = 1 V; for $V_{CC\pm}$ = ± 15 V, $V_{O(rms)}$ = 6 V.

10. This parameter is tested on a sample basis. For other test requirements, please contact the factory. This statement has no bearing on testing or nontesting of other parameters.

electrical characteristics

PARAMETER		TEST CONDITIONS		T_A†	$V_{CC\pm}$ = ±5 V			$V_{CC\pm}$ = ±15 V			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_O = 0, V_{IC} = 0, R_S = 50 Ω	TL052M	25°C		0.73	3.5		0.65	1.5	mV
				Full range			6.5			4.5	
			TL052AM	25°C		0.51	2.8		0.4	0.8	
				Full range			5.8			3.8	
α_{VIO}	Temperature coefficient of input offset voltage		TL052M	25°C to 125°C		10			9		µV/°C
			TL052AM	25°C to 125°C		9			8		
	Input offset voltage long-term drift (see Note 5)			25°C		0.04			0.04		µV/mo
I_{IO}	Input offset current	V_O = 0, V_{IC} = 0, See Figure 5		25°C		4	100		5	100	pA
				125°C		1	20		2	20	nA
I_{IB}	Input bias current	V_O = 0, V_{IC} = 0, See Figure 5		25°C		20	200		30	200	pA
				125°C		10	50		20	50	nA
V_{ICR}	Common-mode input voltage range			25°C	−1 to 4	−2.3 to 5.6		−11 to 11	−12.3 to 15.6		V
				Full range	−1 to 4			−11 to 11			
V_{OM+}	Maximum positive peak output voltage swing	R_L = 10 kΩ		25°C	3	4.2		13	13.9		V
				Full range	3			13			
		R_L = 2 kΩ		25°C	2.5	3.8		11.5	12.7		
				Full range	2.5			11.5			
V_{OM-}	Maximum negative peak output voltage swing	R_L = 10 kΩ		25°C	−2.5	−3.5		−12	−13.2		V
				Full range	−2.5			−12			
		R_L = 2 kΩ		25°C	−2.3	−3.2		−11	−12		
				Full range	−2.3			−11			
A_{VD}	Large-signal differential voltage amplification	R_L = 2 kΩ, See Note 6		25°C	25	59		50	105		V/mV
				−55°C	30	76		60	149		
				125°C	10	32		15	49		
r_i	Input resistance			25°C		10^{12}			10^{12}		Ω
C_i	Input capacitance			25°C		10			12		pF
CMRR	Common-mode rejection ratio	V_{IC} = V_{ICR} min, V_O = 0, R_S = 50 Ω		25°C	65	85		75	93		dB
				−55°C	65	83		75	92		
				125°C	65	84		75	94		
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm} / \Delta V_{IO}$)	$V_{CC\pm}$ = ±5 V to ±15 V, V_O = 0, R_S = 50 Ω		25°C	75	99		75	99		dB
				−55°C	75	98		75	98		
				125°C	75	100		75	100		
I_{CC}	Supply current (four amplifiers)	No load, V_O = 0		25°C		4.6	5.6		4.8	5.6	mA
				−55°C		4.4	6.4		4.5	6.4	
				125°C		4.2	6.4		4.4	6.4	
V_{o1}/V_{o2}	Crosstalk attenuation	A_{VD} = 100		25°C		120			120		dB

† Full range is −55°C to 125°C.

NOTES: 5. Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at T_A = 150°C extrapolated to T_A = 25°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

6. For $V_{CC\pm}$ = ±5 V, V_O = ±2.3 V; at $V_{CC\pm}$ = ±15 V, V_O = ±10 V.

operating characteristics

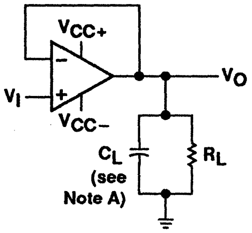
PARAMETER		TEST CONDITIONS		T_A†	$V_{CC\pm} = \pm5$ V			$V_{CC\pm} = \pm15$ V			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
SR +	Positive slew rate at unity gain	R_L = 2 kΩ, C_L = 100 pF, See Figure 1 and Note 7		25°C		17.8		13	20.7		V/µs
				– 55°C		18.8			20.3		
				125°C		14.5			20.2		
SR –	Negative slew rate at unity gain			25°C		15.4		13	17.8		
				– 55°C		15.7			17.6		
				125°C		13.8			16.5		
t_r	Rise time	V_{IPP} = ± 10 mV, R_L = 2 kΩ, C_L = 100 pF, See Figures 1 and 2		25°C		55			56		ns
				– 55°C		51			52		
				125°C		68			68		
t_f	Fall time			25°C		55			57		
				– 55°C		51			52		
				125°C		68			69		
	Overshoot factor			25°C		24%			19%		
				– 55°C		25%			19%		
				125°C		25%			19%		
V_n	Equivalent input noise voltage	R_S = 100 Ω, See Figure 3	f = 10 Hz	25°C		71			71		nV/√Hz
			f = 1 kHz	25°C		19			19		
V_{NPP}	Peak-to-peak equivalent input noise voltage		f = 10 Hz to 10 kHz	25°C		4			4		µV
I_n	Equivalent input noise current	f = 1 kHz		25°C		0.01			0.01		pA/√Hz
THD	Total harmonic distortion	R_S = 1 kΩ, R_L = 2 kΩ, f = 1 kHz, See Note 8		25°C		0.003%			0.003%		
B_1	Unity-gain bandwidth	V_i = 10 mV, R_L = 2 kΩ, C_L = 25 pF, See Figure 4		25°C		3			3		MHz
				– 55°C		3.6			3.7		
				125°C		2.3			2.4		
ϕ_m	Phase margin at unity gain	V_i = 10 mV, R_L = 2 kΩ, C_L = 25 pF, See Figure 4		25°C		60°			63°		
				– 55°C		57°			61°		
				125°C		60°			63°		

† Full range is – 55°C to 125°C.

NOTES: 7. For $V_{CC\pm} = \pm5$ V, $V_{IPP} = \pm1$ V; for $V_{CC\pm} = \pm15$ V, $V_{IPP} = \pm5$ V.

8. For $V_{CC\pm} = \pm5$ V, $V_{o(rms)} = 1$ V; for $V_{CC\pm} = \pm15$ V, $V_{o(rms)} = 6$ V.

PARAMETER MEASUREMENT INFORMATION



NOTE A: C_L includes fixture capacitance.

Figure 1. Slew Rate, Rise/Fall Time, and Overshoot Test Circuit

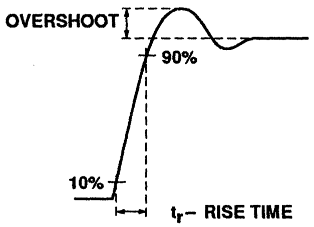


Figure 2. Rise Time and Overshoot Waveform

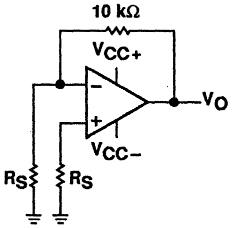
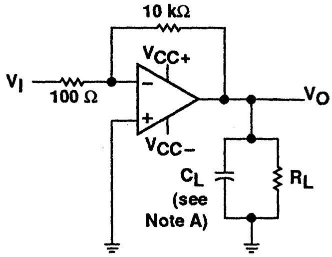


Figure 3. Noise Voltage Test Circuit



NOTE A: C_L includes fixture capacitance.

Figure 4. Unity-Gain Bandwidth and Phase Margin Test Circuit

typical values

Typical values as presented in this data sheet represent the median (50% point) of device parametric performance.

input bias and offset current

At the picoamp-bias-current level typical of the TL052 and TL052A, accurate measurement of the bias current becomes difficult. Not only does this measurement require a picoammeter, but test socket leakages can easily exceed the actual device bias currents. To accurately measure these small currents, Texas Instruments uses a two-step process. The socket leakage is measured using picoammeters with bias voltages applied, but with no device in the socket. The device is then inserted in the socket and a second test that measures both the socket leakage and the device input bias current is performed. The two measurements are then subtracted algebraically to determine the bias current of the device.

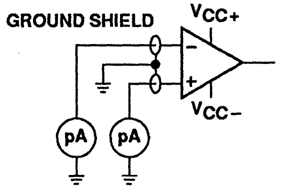


Figure 5. Input Bias and Offset Current Test Circuit

noise

Because of the increasing emphasis on low noise levels in many of today's applications, the input noise voltage density is sample-tested at f = 1 kHz. Texas Instruments also has additional noise testing capability to meet specific application requirements. Please contact the factory for details.

TYPICAL CHARACTERISTICS

table of graphs

			FIGURE
V_{IO}	Input offset voltage	Distribution	6
α_{VIO}	Temperature coefficient of input offset voltage	Distribution	7
I_{IO}	Input offset current	vs Temperature	8
I_{IB}	Input bias current	vs V_{IC} vs Temperature	9 8
V_I	Input voltage range	vs V_{CC} vs Temperature	10 11
V_O	Output voltage	vs Differential input voltage	12, 13
V_{OM}	Maximum peak output voltage swing	vs V_{CC} vs Output current vs Frequency vs Temperature	14 18, 19 15, 16, 17 20, 21
A_{VD}	Differential voltage amplification	vs R_L vs Frequency vs Temperature	22 23 24, 25
z_o	Output impedance	vs Frequency	29
CMRR	Common-mode rejection ratio	vs Frequency vs Temperature	26, 27 28
k_{SVR}	Supply-voltage rejection ratio	vs Temperature	30
I_{OS}	Short-circuit output current	vs V_{CC} vs Time vs Temperature	31 32 33
I_{CC}	Supply current	vs V_{CC} vs Temperature	34 35
SR	Slew rate	vs R_L vs Temperature	36, 37 38, 39
	Overshoot factor	vs C_L	40
V_n	Equivalent input noise voltage	vs Frequency	41
THD	Total harmonic distortion	vs Frequency	42
B_1	Unity-gain bandwidth	vs V_{CC} vs Temperature	43 44
ϕ_m	Phase margin	vs V_{CC} vs C_L vs Temperature	45 46 47
	Phase shift	vs Frequency	23
	Pulse response	Small-signal Large-signal	48 49

TYPICAL CHARACTERISTICS†

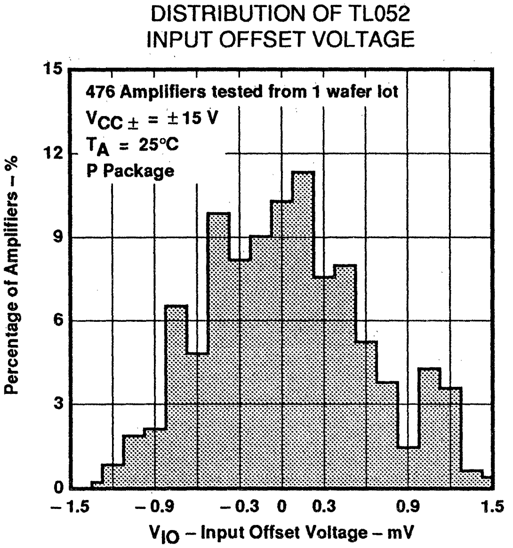


Figure 6

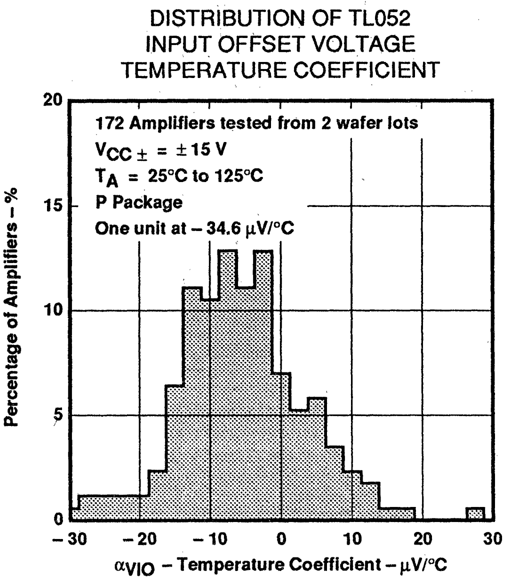


Figure 7

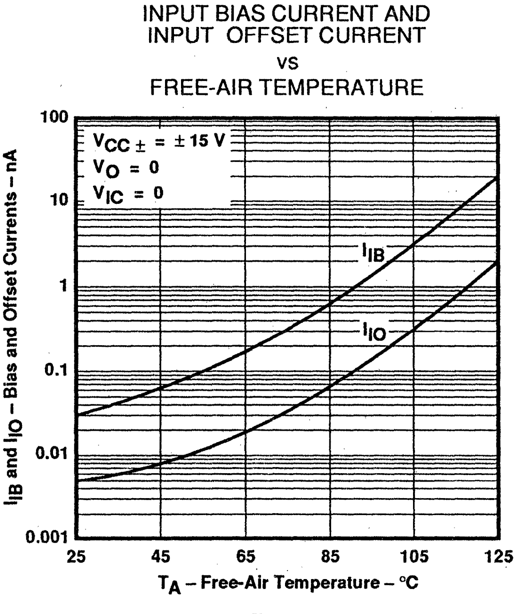


Figure 8

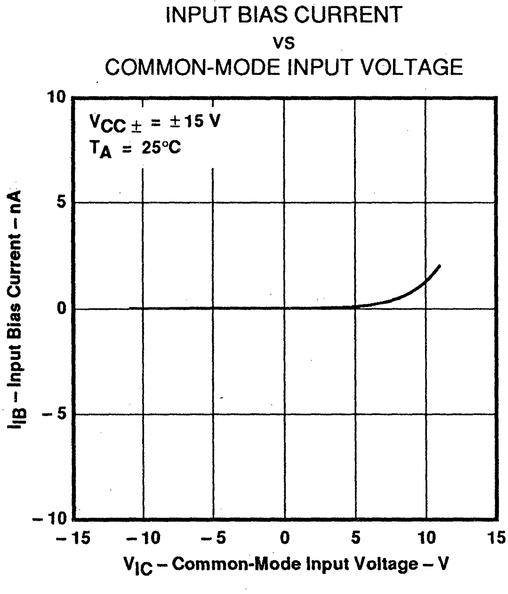


Figure 9

---

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

COMMON-MODE
INPUT VOLTAGE RANGE LIMITS
vs
SUPPLY VOLTAGE

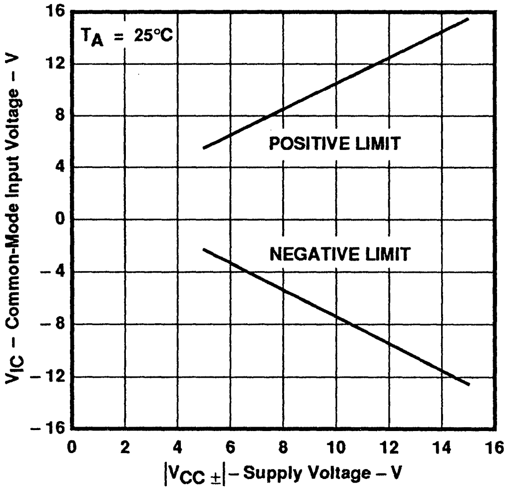


Figure 10

COMMON-MODE
INPUT VOLTAGE RANGE LIMITS
vs
FREE-AIR TEMPERATURE

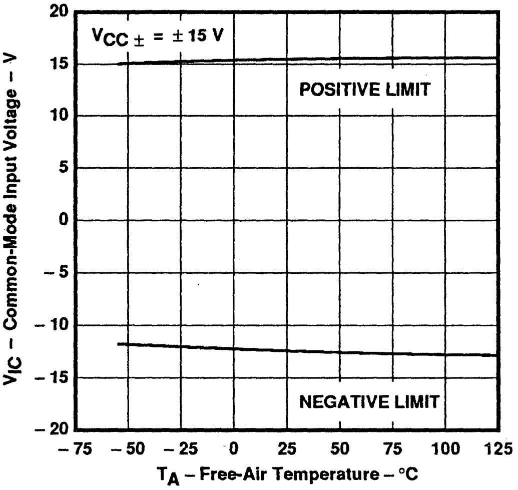


Figure 11

OUTPUT VOLTAGE
vs
DIFFERENTIAL INPUT VOLTAGE

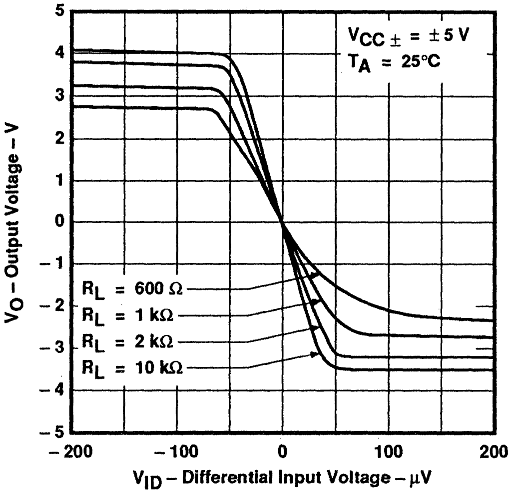


Figure 12

OUTPUT VOLTAGE
vs
DIFFERENTIAL INPUT VOLTAGE

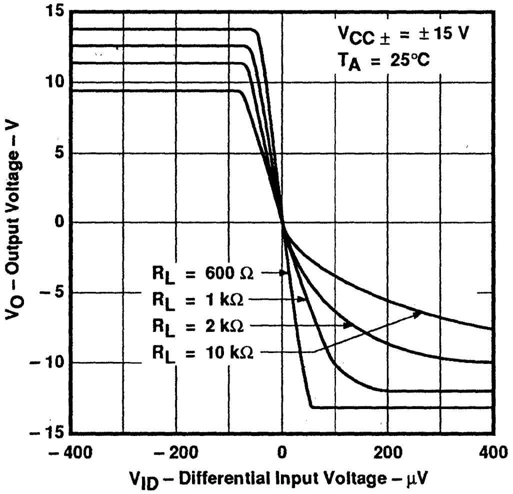


Figure 13

---

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

MAXIMUM PEAK OUTPUT VOLTAGE
vs
SUPPLY VOLTAGE

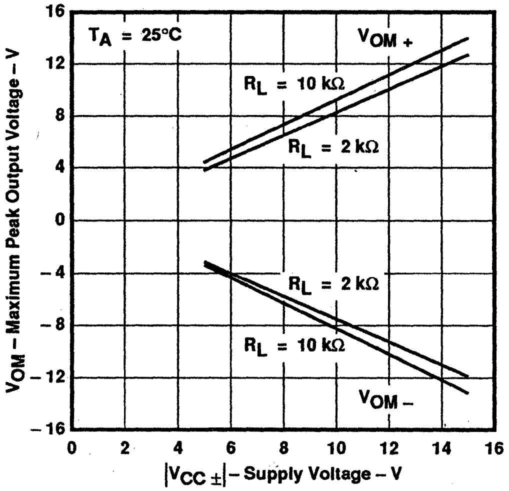


Figure 14

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE
vs
FREQUENCY

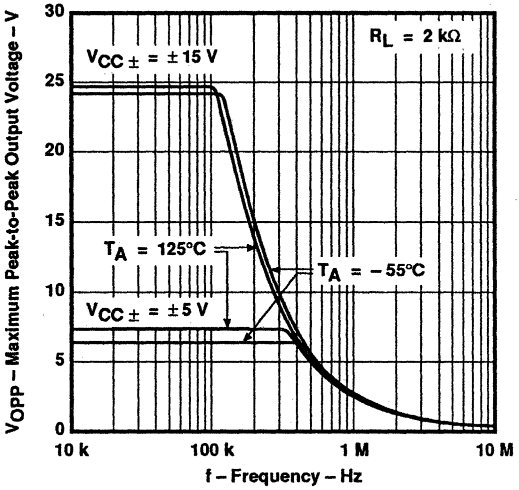


Figure 15

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE
vs
FREQUENCY

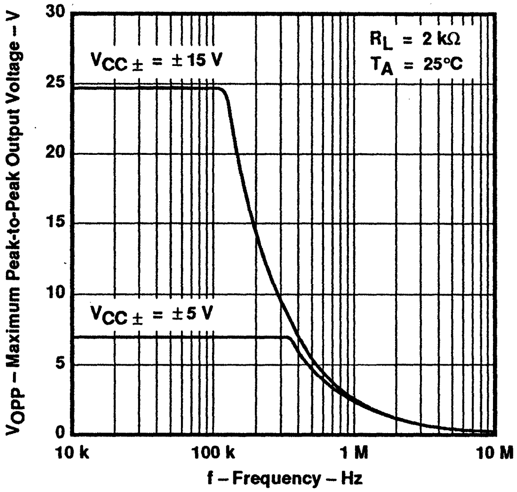


Figure 16

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE
vs
FREQUENCY

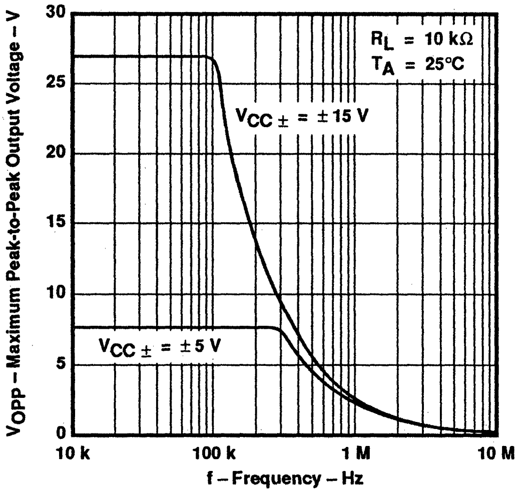
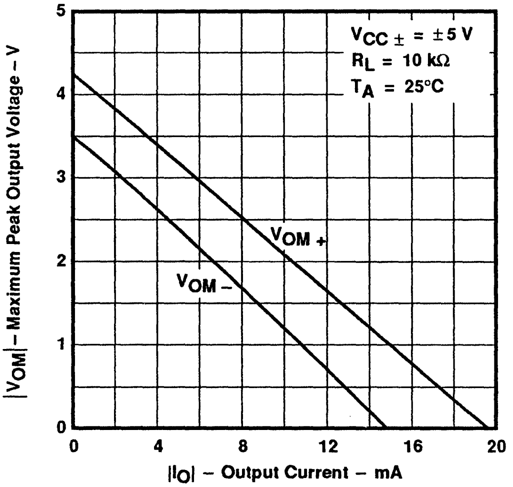


Figure 17

---

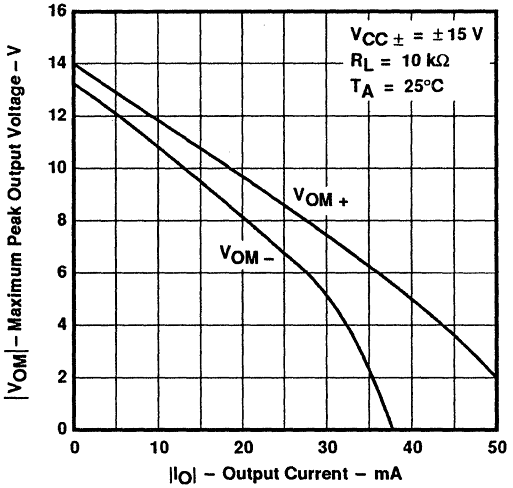
†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†



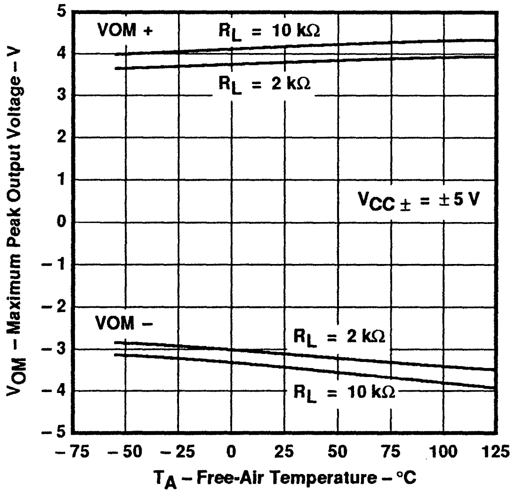
MAXIMUM PEAK OUTPUT VOLTAGE
vs
OUTPUT CURRENT

Figure 18



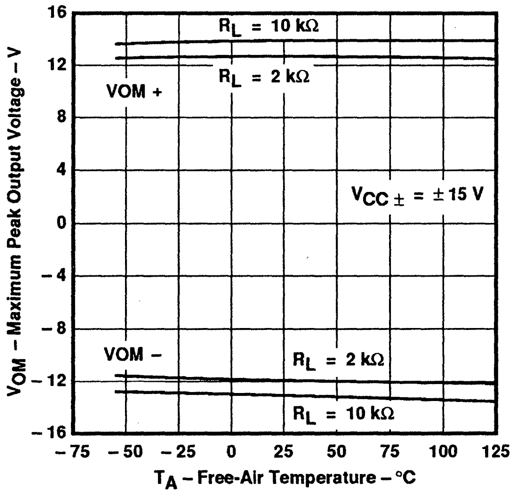
MAXIMUM PEAK OUTPUT VOLTAGE
vs
OUTPUT CURRENT

Figure 19



MAXIMUM PEAK OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

Figure 20



MAXIMUM PEAK OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

Figure 21

---

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

LARGE-SIGNAL VOLTAGE AMPLIFICATION
vs
LOAD RESISTANCE

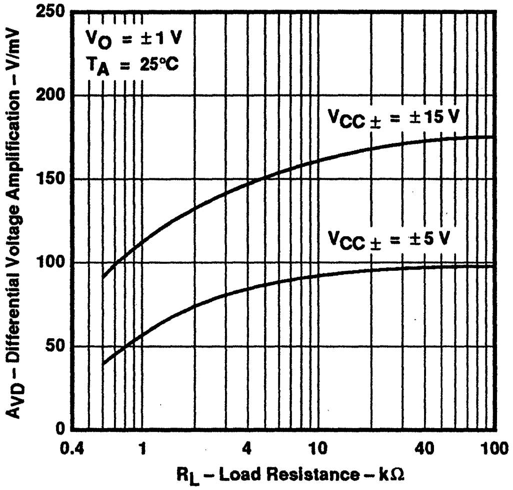


Figure 22

LARGE-SIGNAL DIFFERENTIAL VOLTAGE
AMPLIFICATION AND PHASE SHIFT
vs
FREQUENCY

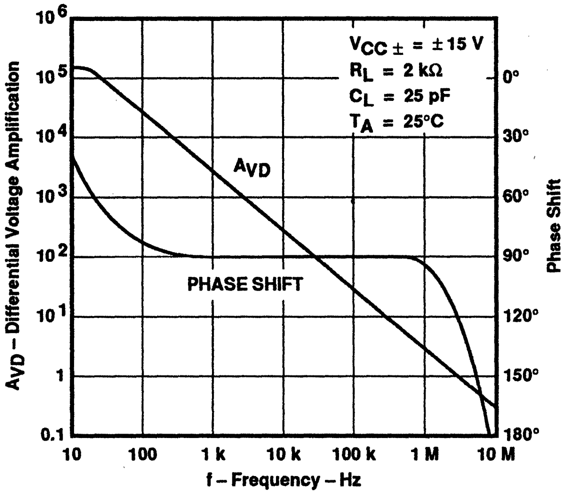


Figure 23

LARGE-SIGNAL VOLTAGE AMPLIFICATION
vs
FREE-AIR TEMPERATURE

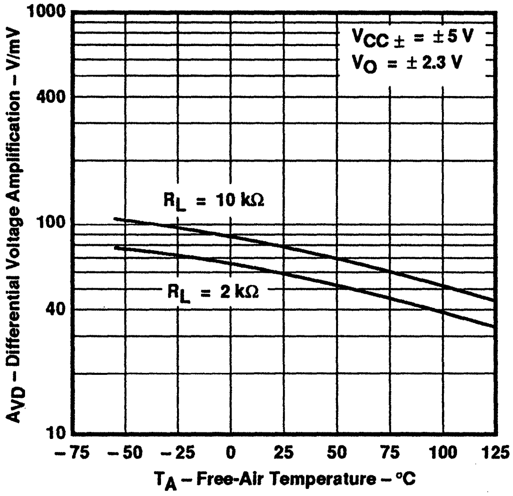


Figure 24

LARGE-SIGNAL VOLTAGE AMPLIFICATION
vs
FREE-AIR TEMPERATURE

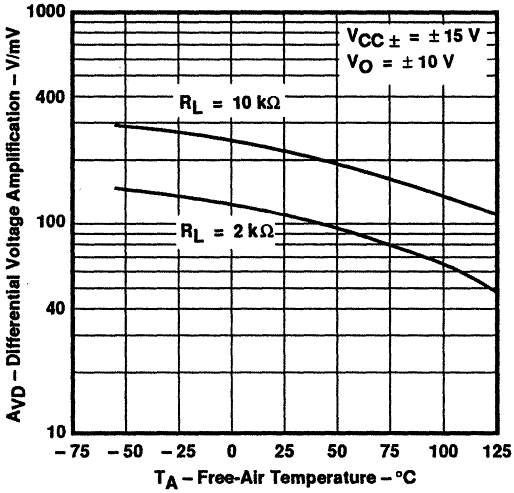


Figure 25

---

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS[†]

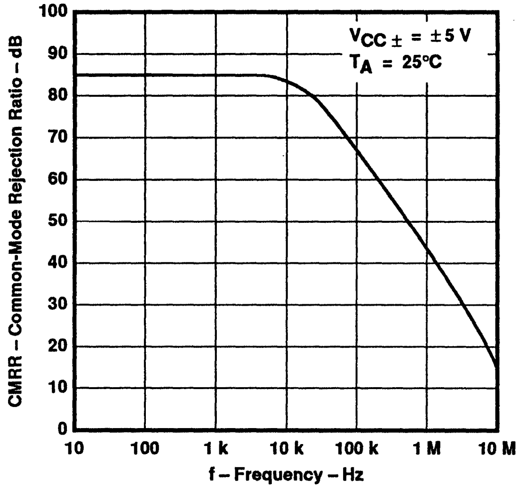

COMMON-MODE REJECTION RATIO
vs
FREQUENCY

Figure 26

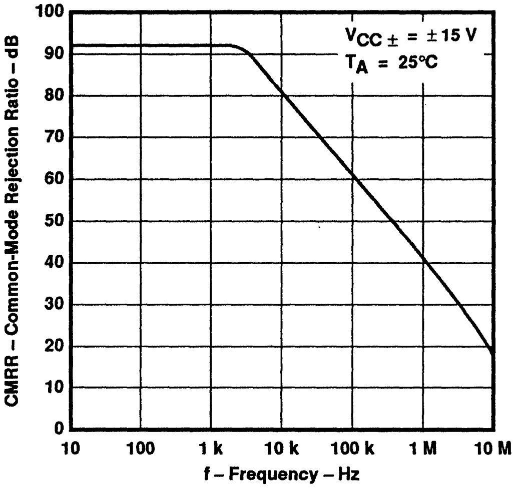

COMMON-MODE REJECTION RATIO
vs
FREQUENCY

Figure 27

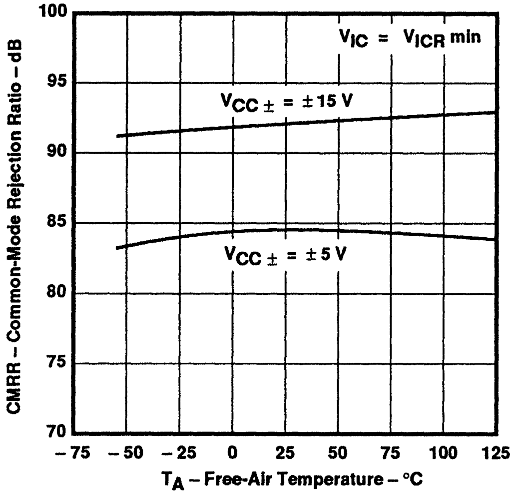

COMMON-MODE REJECTION RATIO
vs
FREE-AIR TEMPERATURE

Figure 28

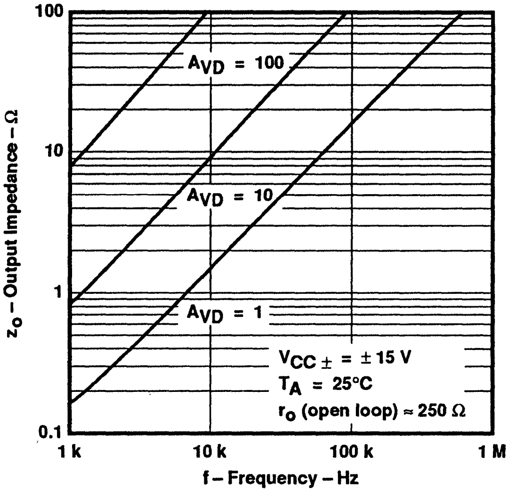

OUTPUT IMPEDANCE
vs
FREQUENCY

Figure 29

[†] Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS[†]

SUPPLY-VOLTAGE REJECTION RATIO
vs
FREE-AIR TEMPERATURE

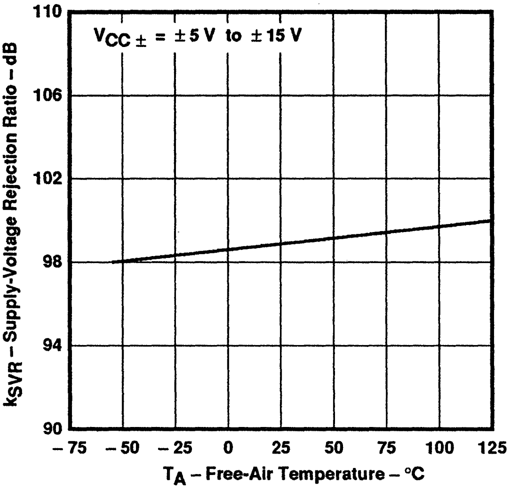


Figure 30

SHORT-CIRCUIT OUTPUT CURRENT
vs
SUPPLY VOLTAGE

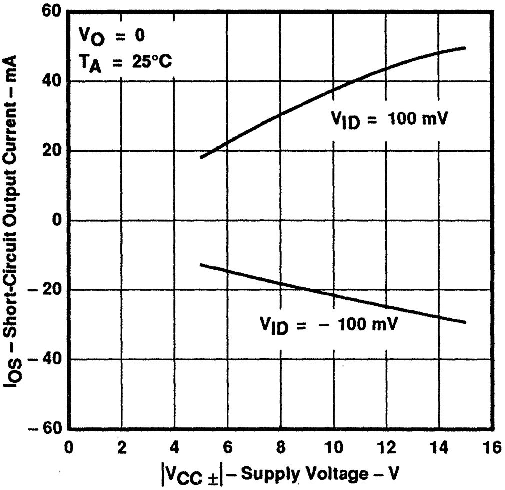


Figure 31

SHORT-CIRCUIT OUTPUT CURRENT
vs
TIME

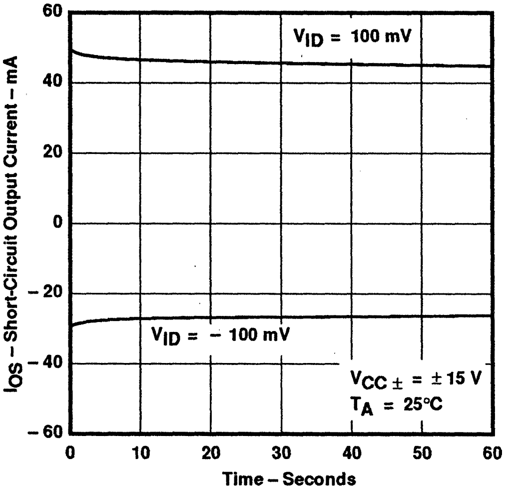


Figure 32

SHORT-CIRCUIT OUTPUT CURRENT
vs
FREE-AIR TEMPERATURE

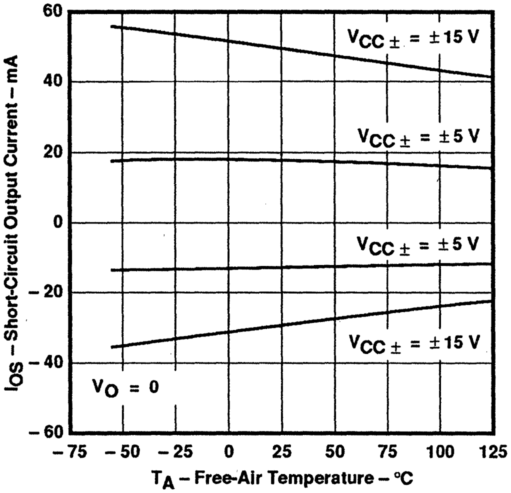


Figure 33

[†] Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS[†]

SUPPLY CURRENT
vs
SUPPLY VOLTAGE

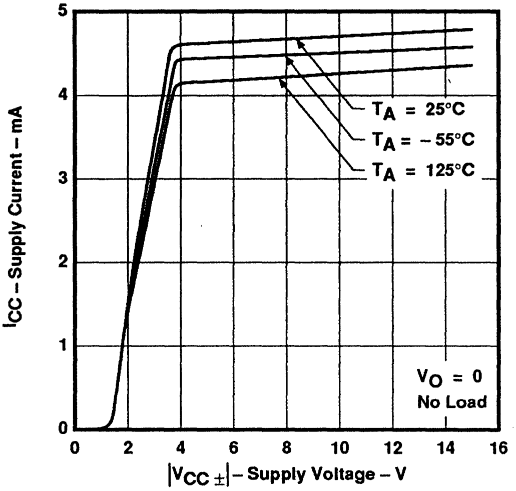


Figure 34

SUPPLY CURRENT
vs
FREE-AIR TEMPERATURE

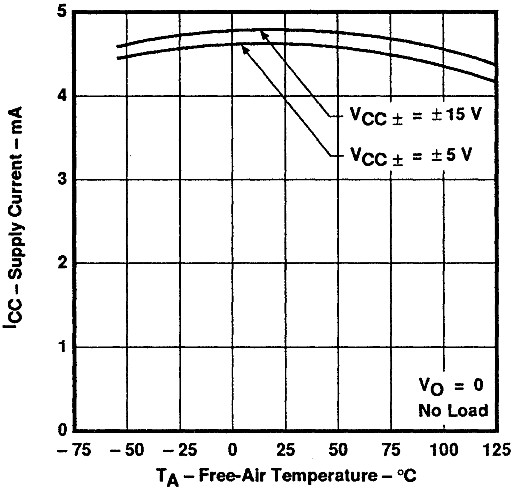


Figure 35

SLEW RATE
vs
LOAD RESISTANCE

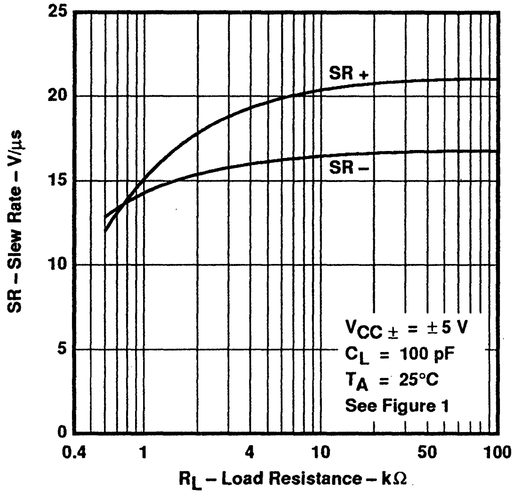


Figure 36

SLEW RATE
vs
LOAD RESISTANCE

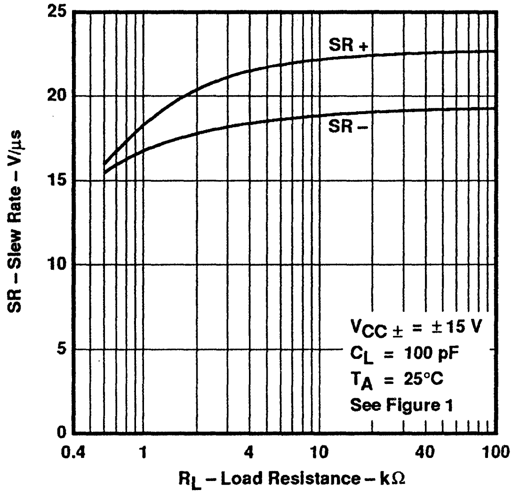


Figure 37

[†] Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

SLEW RATE
vs
FREE-AIR TEMPERATURE

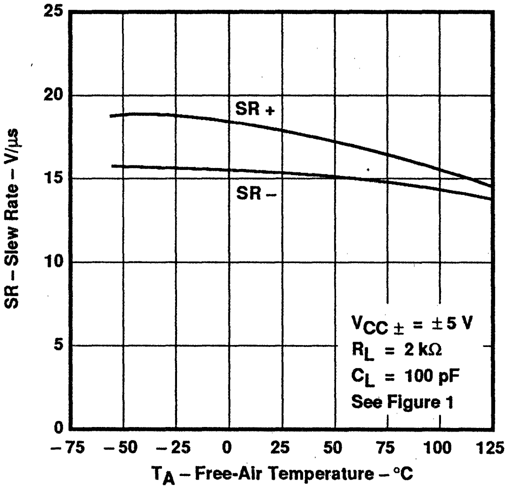


Figure 38

SLEW RATE
vs
FREE-AIR TEMPERATURE

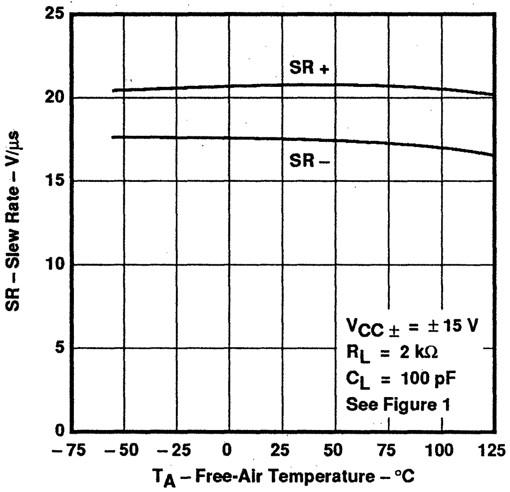


Figure 39

OVERSHOOT FACTOR
vs
LOAD CAPACITANCE

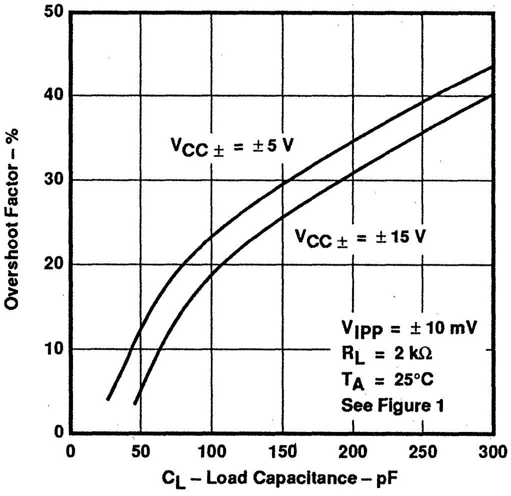


Figure 40

EQUIVALENT INPUT NOISE VOLTAGE
vs
FREQUENCY

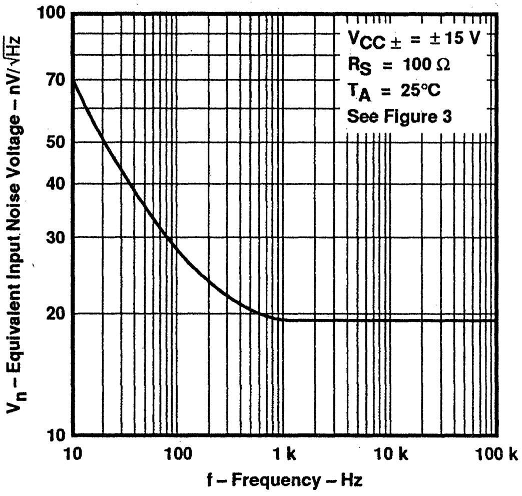


Figure 41

---

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

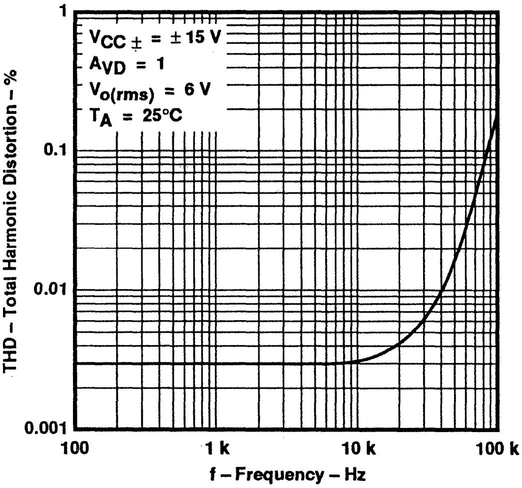

TOTAL HARMONIC DISTORTION
vs
FREQUENCY

Figure 42

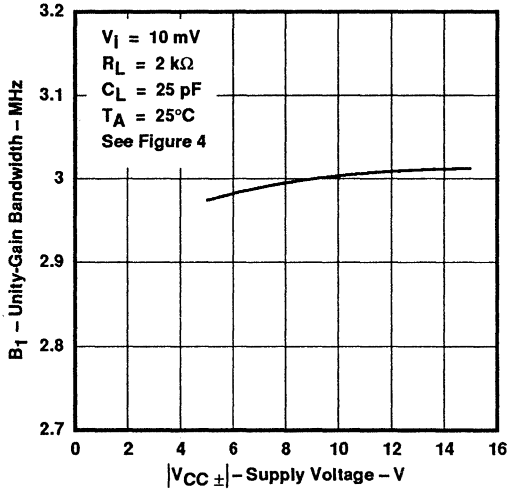

UNITY-GAIN BANDWIDTH
vs
SUPPLY VOLTAGE

Figure 43

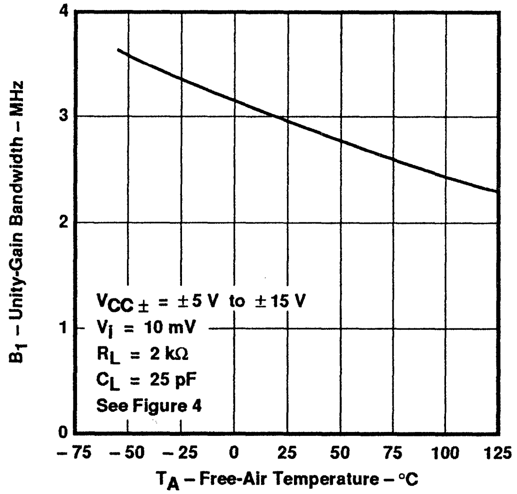

UNITY-GAIN BANDWIDTH
vs
FREE-AIR TEMPERATURE

Figure 44

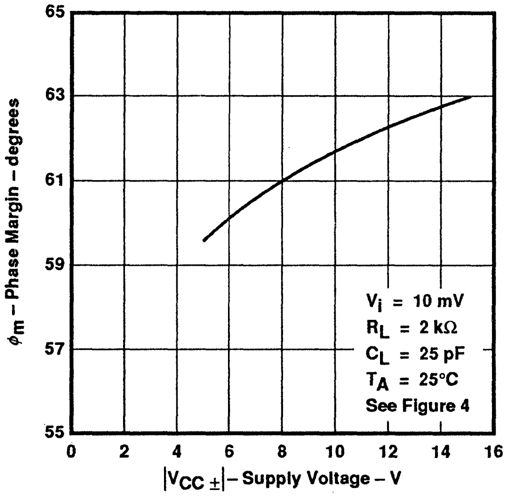

PHASE MARGIN
vs
SUPPLY VOLTAGE

Figure 45

---

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

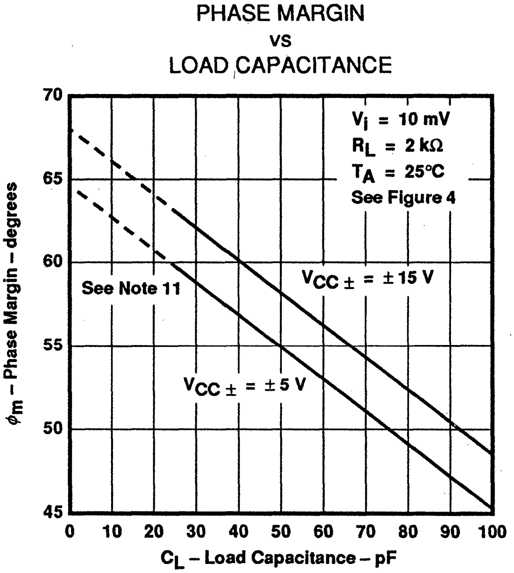


Figure 46

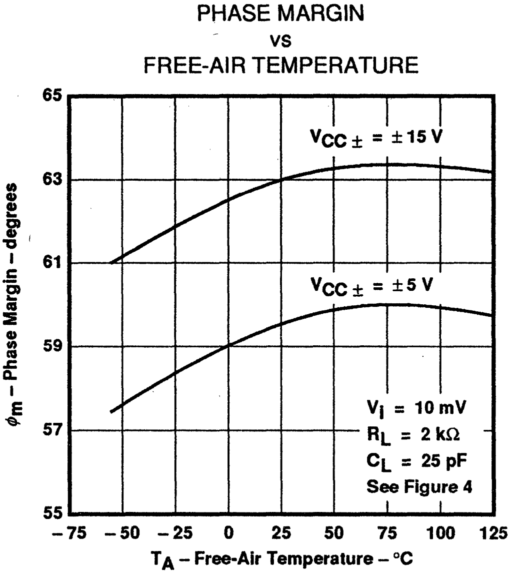


Figure 47

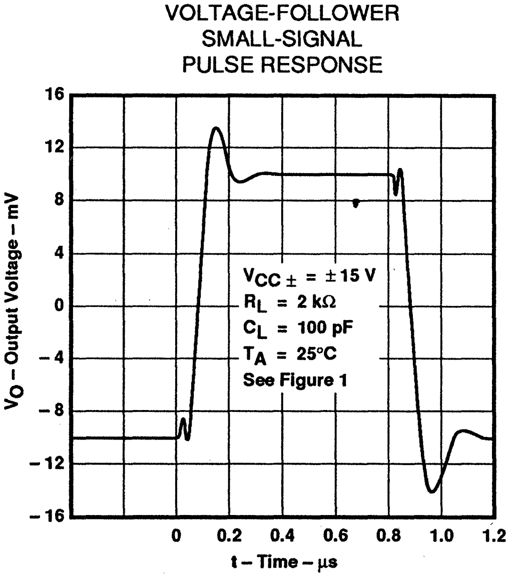


Figure 48

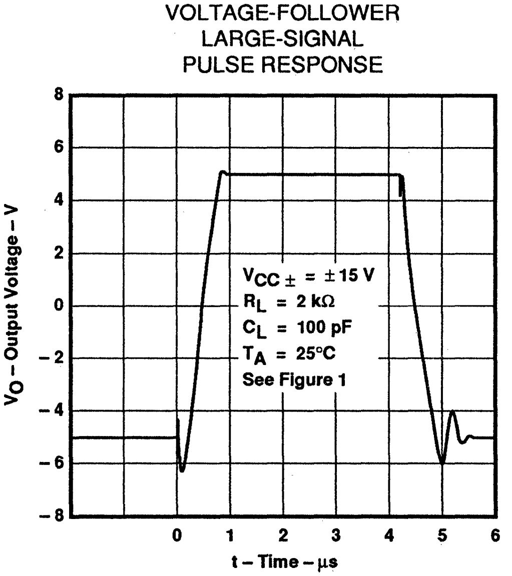


Figure 49

---

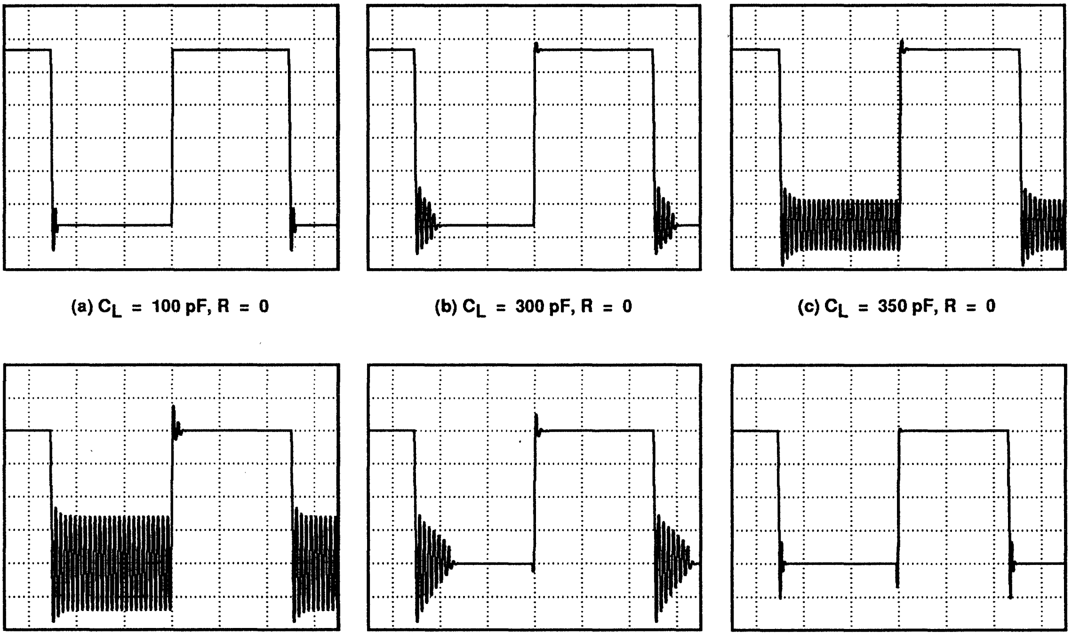
†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

NOTE 11: Values of phase margin below a load capacitance of 25 pF were estimated.

APPLICATION INFORMATION

output characteristics

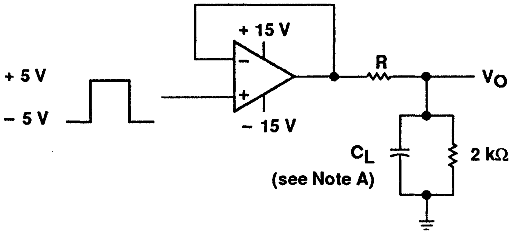
All operating characteristics (except bandwidth and phase margin) are specified with 100-pF load capacitance. The TL052 and TL052A will drive higher capacitive loads; however, as the load capacitance increases, the resulting response pole occurs at lower frequencies, thereby causing ringing, peaking, or even oscillation. The value of the load capacitance at which oscillation occurs varies with production lots. If an application appears to be sensitive to oscillation due to load capacitance, adding a small resistance in series with the load should alleviate the problem. Capacitive loads of 1000 pF and larger may be driven if enough resistance is added in series with the output (see Figure 50).



(a) C_L = 100 pF, R = 0 (b) C_L = 300 pF, R = 0 (c) C_L = 350 pF, R = 0

(d) C_L = 1000 pF, R = 0 (e) C_L 1000 pF, R = 50 Ω (f) C_L = 1000 pF, R = 2 kΩ

Figure 50. Effect of Capacitive Loads



NOTE A: C_L includes fixture capacitance.

Figure 51. Test Circuit for Output Characteristics

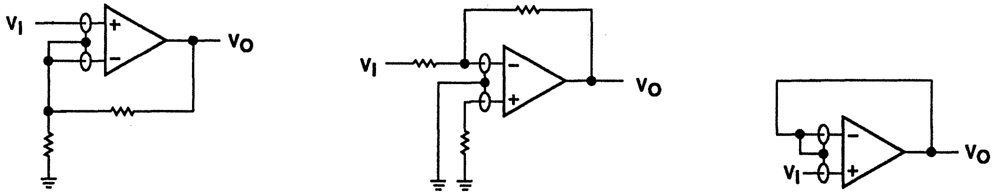
APPLICATION INFORMATION

input characteristics

The TL052 and TL052A are specified with a minimum and a maximum input voltage that, if exceeded at either input, could cause the device to malfunction.

Because of the extremely high input impedance and resulting low bias current requirements, the TL052 and TL052A are well suited for low-level signal processing; however, leakage currents on printed circuit boards and sockets can easily exceed bias current requirements and cause degradation in system performance. It is good practice to include guard rings around inputs (see Figure 52). These guards should be driven from a low-impedance source at the same voltage level as the common-mode input.

The inputs of any unused amplifiers should be tied to ground to avoid possible oscillation.



(a) NONINVERTING AMPLIFIER **(b) INVERTING AMPLIFIER--** **(c) UNITY-GAIN AMPLIFIER**

Figure 52. Use of Guard Rings

noise performance

The noise specifications in op amp circuits are greatly dependent on the current in the first-stage differential amplifier. The low input bias current requirements of the TL052 and TL052A result in a very low current noise. This feature makes the devices especially favorable over bipolar devices when using values of circuit impedance greater than 50 kΩ.

APPLICATION INFORMATION

Instrumentation amplifier with adjustable gain/null

The instrumentation amplifier in Figure 53 benefits greatly from the high input impedance and stable input offset voltage of the TL052A. Amplifiers U1A, U1B, and U2A form the actual instrumentation amplifier, while U2B provides offset null. Potentiometer R1 provides gain adjust. With R1 = 2 kΩ, the circuit gain equals 100, while with R1 = 200 kΩ, the circuit gain equals two. The following equation shows the instrumentation amplifier gain as a function of R1:

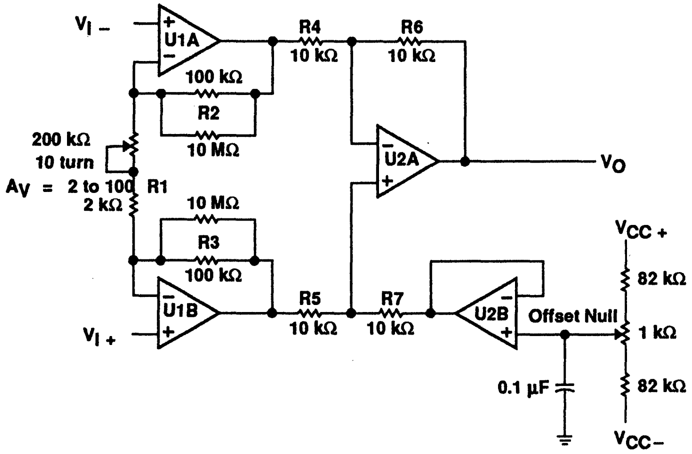
$$A_V = 1 + \left(\frac{R2 + R3}{R1}\right)$$

Readjusting the offset null is necessary whenever the circuit gain is changed. Note that if U2B is needed for another application, R7 can be terminated at ground. The low input offset voltage of the TL052A minimizes the dc error of the circuit. For best matching, all resistors should be one percent tolerance. The matching between R4, R5, R6, and R7 controls the CMRR of this application.

The following equation shows the output voltages when the input voltage equals zero. This dc error can be nulled by adjusting the offset null potentiometer; however, any change in offset voltage over time or temperature also creates an error. To calculate the error from changes in offset, consider the three offset components in the equation as delta offsets rather than initial offsets. The improved stability of Texas Instruments enhanced JFETs minimizes the error resulting from change in input offset voltage with time. Assuming V_{IN} equals zero, V_O can be shown as a function of the offset voltage:

$$V_O = V_{IO2}\left[\left(1 + \frac{R3}{R1}\right)\left(\frac{R7}{R5 + R7}\right)\left(1 + \frac{R6}{R4}\right) + \frac{R2}{R1}\left(\frac{R6}{R4}\right)\right]$$

$$- V_{IO1}\left[\frac{R3}{R1}\left(\frac{R7}{R5 + R7}\right)\left(1 + \frac{R6}{R4}\right) + \frac{R6}{R4}\left(1 + \frac{R2}{R1}\right)\right] + V_{IO3}\left(1 + \frac{R6}{R4}\right)$$



NOTE: U1A through U2B = TL052A; $V_{CC\pm}$ = ± 15 V.

Figure 53. Instrumentation Amplifier

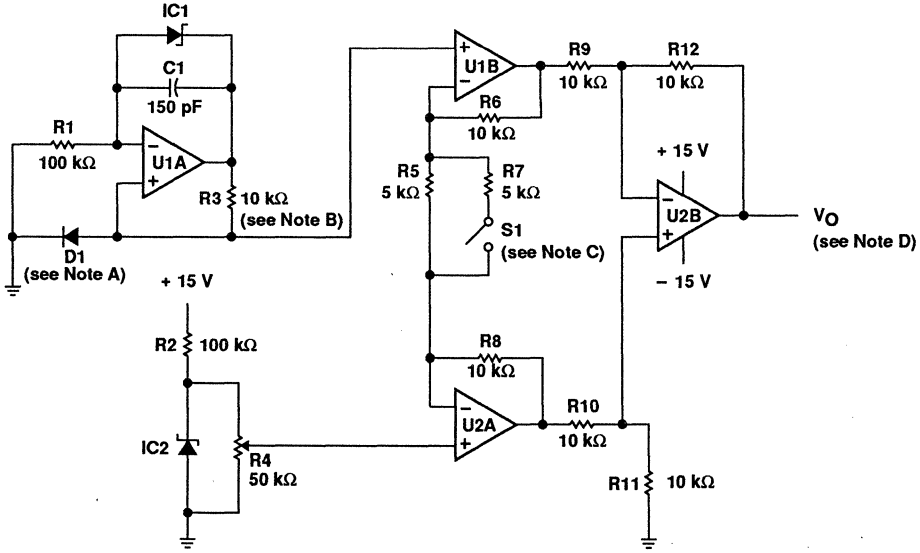
APPLICATION INFORMATION

analog thermometer

By combining a current source that does not vary over temperature with an instrumentation amplifier, a precise analog thermometer can be built (see Figure 54). Amplifier U1A and IC1 establish a constant current through the temperature sensing diode D1. For this section of the circuit to operate correctly, the TL052 must use split supplies and R3 must be a metal film resistor with a low temperature coefficient.

The temperature-sensitive voltage from the diode is compared to a temperature-stable voltage reference set by IC2. R4 should be adjusted to provide the correct output voltage when the diode is at a known temperature. Although this potentiometer resistance varies with temperature, the divider ratio of the potentiometer remains constant.

Amplifiers U1B, U2A, and U2B form the instrumentation amplifier that converts the difference between the diode and reference voltage to a voltage proportional to the temperature. With switch S1 closed, the amplifier gain equals 5, and the output voltage is proportional to temperature in degrees Celsius. With S1 open, the amplifier gain is 9, and the output is proportional to temperature in degrees Fahrenheit. Every time that S1 is changed, R4 must be recalibrated. By setting S1 correctly, the output voltage equals 10 mV per degree (C or F).



NOTES: A. Temperature sensing diode ≈ (− 2 mV/°C).
B. Metal film (low temperature coefficient).
C. Switch open for °F and closed for °C.
D. $V_O \propto$ Temperature; 10 mV/°C or 10 mV/°F.
E. U1A through U2B = TL052. IC1, IC2 = LM385, LT1004, or LT1009 voltage reference.

Figure 54. Analog Thermometer

APPLICATION INFORMATION

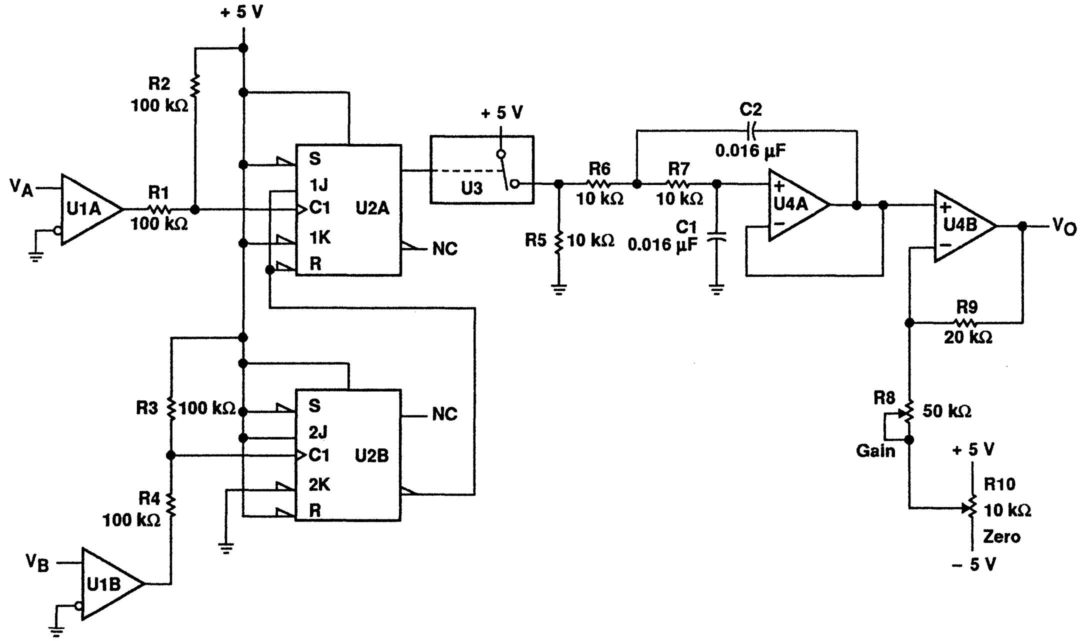
phase meter

The phase meter in Figure 55 produces an output voltage of 10 mV per degree of phase delay between the two input signals V_A and V_B. The reference signal V_A must be the same frequency as V_B. The TLC3702 comparators (U1) convert these two input sine waves into ± 5 V square waves. Then R1 and R4 provide level shifting prior to the SN74HC109 dual J-K flip flops.

Flip-flop U2B is connected as a toggle flip-flop and generates a square wave at half the frequency of V_B. Flip-flop U2A also produces a square wave at half the input frequency. The pulse duration of U2A varies from zero to half the period, where zero corresponds to zero phase delay between V_A and V_B, and half the period corresponds to V_B lagging V_A by 360 degrees.

The output pulse from U2A causes the TLC4066 (U3) switch to charge the TL052 (U4) integrator capacitors C1 and C2. As the phase delay approaches 360 degrees, the output of U4A approximates a square wave, and U2A has an output of almost 2.5 V. U4B acts as a noninverting amplifier with a gain of 1.44 in order to scale the 0- to 2.5-V integrator output to a 0-to 3.6-V output range.

R8 and R10 provide output gain and zero-level calibration. This circuit operates over a 100-Hz to 10-kHz frequency range.



NOTES: U1 = TLC3702; $V_{CC\pm}$ = ±5 V.
U2 = SN74HC109.
U3 = TLC4066.
U4 = TL052; $V_{CC\pm}$ = ±5 V.

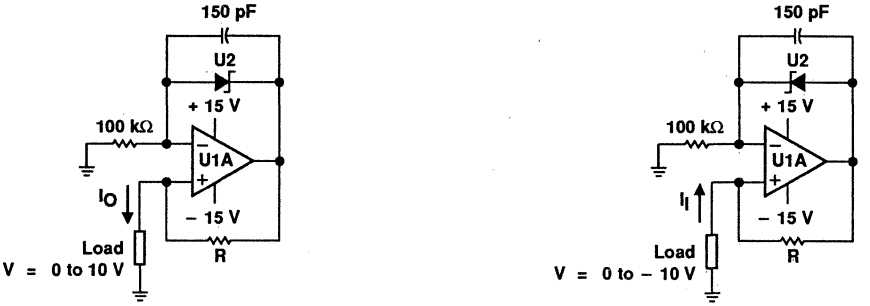
Figure 55. Phase Meter

APPLICATION INFORMATION

precision constant-current source over temperature

A precision current source benefits from the high input impedance and stability of Texas Instruments enhanced JFET process. A low-current shunt regulator maintains 2.5 V between the inverting input and the output of the TL052. The negative feedback then forces 2.5 V across the current setting resistor R; therefore, the current to the load is simply 2.5 V divided by R.

Possible choices for the shunt regulator include the LT1004, LT1009, and LM385. Note that if the regulator's cathode connects to the op amp output, this circuit will source load current. Similarly, if the cathode connects to the inverting input, the circuit will sink current from the load. To minimize output current change with temperature, R should be a metal film resistor with a low temperature coefficient. Also, this circuit must be operated with split voltage supplies.



(a) SOURCE CURRENT LOAD

(b) SINK CURRENT LOAD

NOTES: IC1 = LM385, LT1004, or LT1009 voltage reference.
U1A = TL052.
$I = \frac{2.5\ V}{R}$, R = Low temperature coefficient metal film resistor.

Figure 56. Precision Constant-Current Source

TL054, TL054A
ENHANCED JFET PRECISION QUAD OPERATIONAL AMPLIFIERS

D3236, JUNE 1988 – REVISED JANUARY 1991

- **Maximum Offset Voltage . . . 1.5 mV (TL054A)**
- **High Slew Rate . . . 15.9 V/µs Typ at 25°C**
- **Low Total Harmonic Distortion . . . 0.003% Typ at R_L = 2 kΩ**
- **Low Noise Voltage . . . 21 nV/√Hz Typ at f = 1 kHz**
- **Low Input Bias Currents . . . 30 pA Typ**
- **Monolithic Construction**

description

The TL054 and TL054A quad operational amplifiers incorporate well-matched, high-voltage JFET and bipolar transistors in a monolithic integrated circuit. These devices offer the significant advantages of Texas Instruments new enhanced JFET process. This process affords not only low initial offset voltage due to the on-chip zener trim capability but also stable offset voltage over time and temperature. In comparison, traditional JFET processes are plagued by significant offset voltage drift.

This new enhanced process still maintains the traditional JFET advantages of fast slew rates and low input bias and offset currents. These advantages coupled with low noise and low harmonic distortion make the TL054 well-suited for new state-of-the-art designs as well as existing design upgrades. The TL054 has been designed to be functionally compatible, as well as pin compatible, with the TL074 and TL084.

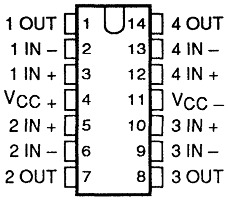
Two offset voltage grades are available:
TL054 (4 mV max) and TL054A (1.5 mV max).

AVAILABLE OPTIONS

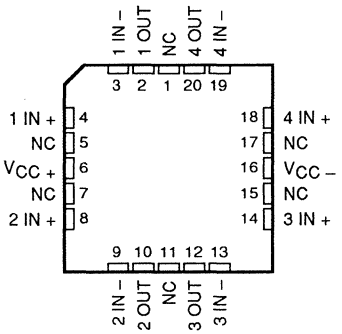
T_A	V_{IO} max AT 25°C	PACKAGE			
		SMALL-OUTLINE (D)	CHIP CARRIER (FK)	CERAMIC DIP (J)	PLASTIC DIP (N)
0°C to 70°C	1.5 mV	TL054ACD	——	——	TL054ACN
	4 mV	TL054CD	——	——	TL054CN
– 40°C to 85°C	1.5 mV	TL054AID	——	——	TL054AIN
	4 mV	TL054ID	——	——	TL054IN
– 55°C to 125°C	1.5 mV	TL054AMD	TL054AMFK	TL054AMJ	TL054AMN
	4 mV	TL054MD	TL054MFK	TL054MJ	TL054MN

D packages are available taped and reeled. Add "R" suffix to device type, (e.g., TL054CDR).

D, J, or N PACKAGE
(TOP VIEW)

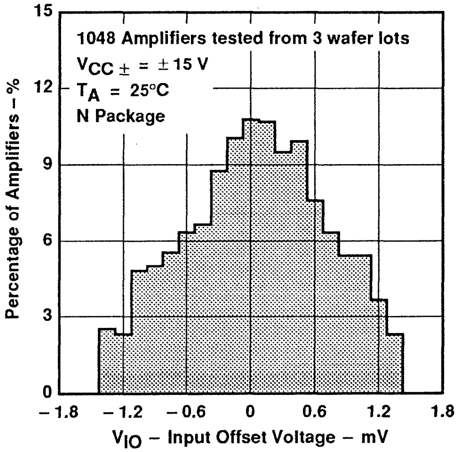


FK PACKAGE
(TOP VIEW)



NC – No internal connection

DISTRIBUTION OF TL054A
INPUT OFFSET VOLTAGE

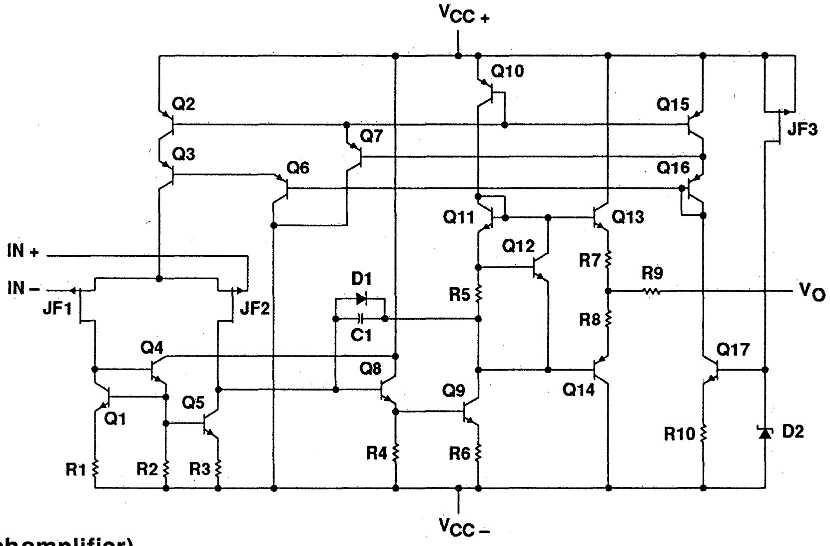


description (continued)

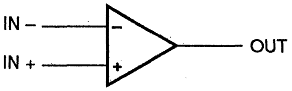
A variety of available packaging options includes small-outline and chip carrier versions for high-density system applications.

The C-suffix devices are characterized for operation from 0°C to 70°C. The I-suffix devices are characterized for operation from – 40°C to 85°C, and the M-suffix devices are characterized for operation over the full military temperature range of – 55°C to 125°C.

equivalent schematic (each amplifier)



symbol (each amplifier)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC+} (see Note 1)	18 V
Supply voltage, V_{CC-} (see Note 1)	– 18 V
Differential input voltage (see Note 2)	± 30 V
Input voltage range, V_I (any input, see Notes 1 and 3)	± 15 V
Input current, I_I (each input)	± 1 mA
Output current, I_O (each output)	± 80 mA
Total current into V_{CC+} terminal	160 mA
Total current out of V_{CC-} terminal	160 mA
Duration of short-circuit current at (or below) 25°C (see Note 4)	unlimited
Continuous total dissipation	See Dissipation Rating Table
Operating free-air temperature range, T_A: C-suffix	0°C to 70°C
I-suffix	– 40°C to 85°C
M-suffix	– 55°C to 125°C
Storage temperature range	– 65°C to 150°C
Case temperature for 60 seconds: FK package	260°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D or N package	260°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: J package	300°C

NOTES:
1. All voltage values, except differential voltages, are with respect to the midpoint between V_{CC+} and V_{CC-}.
2. Differential voltages are at the noninverting input with respect to the inverting input.
3. The magnitude of the input voltage must never exceed the magnitude of the supply voltage or 15 V, whichever is less.
4. The output may be shorted to either supply. Temperature and/or supply voltages must be limited to ensure that the maximum dissipation rating is not exceeded.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING	$T_A = 125°C$ POWER RATING
D	950 mW	7.6 mW/°C	608 mW	494 mW	190 mW
FK	1375 mW	11.0 mW/°C	880 mW	715 mW	275 mW
J	1375 mW	11.0 mW/°C	880 mW	715 mW	275 mW
N	1575 mW	12.6 mW/°C	1008 mW	819 mW	230 mW

recommended operating conditions

		C-SUFFIX			I-SUFFIX			M-SUFFIX			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		±5		±15	±5		±15	±5		±15	V
Common-mode input voltage, V_{IC}	$V_{CC\pm} = \pm 5$ V	–1		4	–1		4	–1		4	V
	$V_{CC\pm} = \pm 15$ V	–11		11	–11		11	–11		11	
Operating free-air temperature, T_A		0		70	–40		85	–55		125	°C

electrical characteristics

PARAMETER		TEST CONDITIONS		T_A†	$V_{CC\pm} = \pm 5$ V			$V_{CC\pm} = \pm 15$ V			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	$V_O = 0$, $V_{IC} = 0$, $R_S = 50\ \Omega$	TL054C	25°C		0.64	5.5		0.56	4	mV
				Full range			7.7			6.2	
			TL054AC	25°C		0.57	3.5		0.5	1.5	
				Full range			5.7			3.7	
α_{VIO}	Temperature coefficient of input offset voltage		TL054C	25°C to 70°C		25			23		µV/°C
			TL054AC	25°C to 70°C		24			23		
	Input offset voltage long-term drift (see Note 5)			25°C		0.04			0.04		µV/mo
I_{IO}	Input offset current	$V_O = 0$, $V_{IC} = 0$, See Figure 5		25°C		4	100		5	100	pA
				70°C		0.02	1		0.025	1	nA
I_{IB}	Input bias current	$V_O = 0$, $V_{IC} = 0$, See Figure 5		25°C		20	200		30	200	pA
				70°C		0.15	4		0.2	4	nA
V_{ICR}	Common-mode input voltage range			25°C	−1 to 4	−2.3 to 5.6		−11 to 11	−12.3 to 15.6		V
				Full range	−1 to 4			−11 to 11			
V_{OM+}	Maximum positive peak output voltage swing	$R_L = 10\ k\Omega$		25°C	3	4.2		13	13.9		V
				Full range	3			13			
		$R_L = 2\ k\Omega$		25°C	2.5	3.8		11.5	12.7		
				Full range	2.5			11.5			
V_{OM-}	Maximum negative peak output voltage swing	$R_L = 10\ k\Omega$		25°C	−2.5	−3.5		−12	−13.2		V
				Full range	−2.5			−12			
		$R_L = 2\ k\Omega$		25°C	−2.3	−3.2		−11	−12		
				Full range	−2.3			−11			
A_{VD}	Large-signal differential voltage amplification	$R_L = 2\ k\Omega$, See Note 6		25°C	25	72		50	133		V/mV
				0°C	30	88		60	173		
				70°C	20	57		30	85		
r_i	Input resistance			25°C		10^{12}			10^{12}		Ω
C_i	Input capacitance			25°C		10			12		pF
CMRR	Common-mode rejection ratio	$V_{IC} = V_{ICR}$ min, $V_O = 0$, $R_S = 50\ \Omega$		25°C	65	84		75	92		dB
				0°C	65	84		75	92		
				70°C	65	84		75	93		
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm} / \Delta V_{IO}$)	$V_{CC\pm} = \pm 5$ V to ± 15 V, $V_O = 0$, $R_S = 50\ \Omega$		25°C	75	99		75	99		dB
				0°C	75	99		75	99		
				70°C	75	99		75	99		
I_{CC}	Supply current (four amplifiers)	No load, $V_O = 0$		25°C		8.1	11.2		8.4	11.2	mA
				0°C		8.2	12.8		8.5	12.8	
				70°C		7.9	11.2		8.2	11.2	
V_{O1}/V_{O2}	Crosstalk attenuation	$A_{VD} = 100$		25°C		120			120		dB

† Full range is 0°C to 70°C.

NOTES: 5. Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at $T_A = 150$°C extrapolated to $T_A = 25$°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

6. For $V_{CC\pm} = \pm 5$ V, $V_O = \pm 2.3$ V; at $V_{CC\pm} = \pm 15$ V, $V_O = \pm 10$ V.

operating characteristics

PARAMETER		TEST CONDITIONS		T_A†	$V_{CC\pm}$ = ±5 V			$V_{CC\pm}$ = ±15 V			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
SR +	Positive slew rate at unity gain	R_L = 2 kΩ, C_L = 100 pF, See Figure 1 and Note 7		25°C		15.4		10	17.8		V/μs
				0°C		15.7		8	17.9		
				70°C		14.4		8	17.5		
SR −	Negative slew rate at unity gain			25°C		13.9		10	15.9		
				0°C		14.3		8	16.1		
				70°C		13.3		8	15.5		
t_r	Rise time	V_{IPP} = ±10 mV, R_L = 2 kΩ, C_L = 100 pF, See Figures 1 and 2		25°C		55			56		ns
				0°C		54			55		
				70°C		63			63		
t_f	Fall time			25°C		55			57		
				0°C		54			56		
				70°C		62			64		
	Overshoot factor			25°C		24%			19%		
				0°C		24%			19%		
				70°C		24%			19%		
V_n	Equivalent input noise voltage (see Note 9)	R_S = 100 Ω, See Figure 3	f = 10 Hz	25°C		75			75		nV/√Hz
			f = 1 kHz	25°C		21			21	45	
V_{NPP}	Peak-to-peak equivalent input noise voltage		f = 10 Hz to 10 kHz	25°C		4			4		μV
I_n	Equivalent input noise current	f = 1 kHz		25°C		0.01			0.01		pA/√Hz
THD	Total harmonic distortion	R_S = 1 kΩ, R_L = 2 kΩ, f = 1 kHz, See Note 8		25°C		0.003%			0.003%		
B_1	Unity-gain bandwidth	V_i = 10 mV, R_L = 2 kΩ, C_L = 25 pF, See Figure 4		25°C		2.7			2.7		MHz
				0°C		3			3		
				70°C		2.4			2.4		
ϕ_m	Phase margin at unity gain	V_i = 10 mV, R_L = 2 kΩ, C_L = 25 pF, See Figure 4		25°C		61°			64°		
				0°C		60°			64°		
				70°C		61°			63°		

† Full range is 0°C to 70°C.

NOTES: 7. For $V_{CC\pm}$ = ±5 V, V_{IPP} = ±1 V; for $V_{CC\pm}$ = ±15 V, V_{IPP} = ±5 V.

8. For $V_{CC\pm}$ = ±5 V, $V_{o(rms)}$ = 1 V; for $V_{CC\pm}$ = ±15 V, $V_{o(rms)}$ = 6 V.

9. This parameter is tested on a sample basis. For other test requirements, please contact the factory. This statement has no bearing on testing or nontesting of other parameters.

electrical characteristics

PARAMETER		TEST CONDITIONS		T_A†	$V_{CC\pm} = \pm 5$ V			$V_{CC\pm} = \pm 15$ V			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	$V_O = 0$, $V_{IC} = 0$, $R_S = 50\ \Omega$	TL054I	25°C		0.64	5.5		0.56	4	mV
				Full range			8.8			7.3	
			TL054AI	25°C		0.57	3.5		0.5	1.5	
				Full range			6.8			4.8	
α_{VIO}	Temperature coefficient of input offset voltage		TL054I	25°C to 85°C		25			24		µV/°C
			TL054AI	25°C to 85°C		25			23		
	Input offset voltage long-term drift (see Note 5)			25°C		0.04			0.04		µV/mo
I_{IO}	Input offset current	$V_O = 0$, $V_{IC} = 0$, See Figure 5		25°C		4	100		5	100	pA
				85°C		0.06	10		0.07	10	nA
I_{IB}	Input bias current	$V_O = 0$, $V_{IC} = 0$, See Figure 5		25°C		20	200		30	200	pA
				85°C		0.6	20		0.7	20	nA
V_{ICR}	Common-mode input voltage range			25°C	−1 to 4	−2.3 to 5.6		−11 to 11	−12.3 to 15.6		V
				Full range	−1 to 4			−11 to 11			
V_{OM+}	Maximum positive peak output voltage swing	$R_L = 10\ k\Omega$		25°C	3	4.2		13	13.9		V
				Full range	3			13			
		$R_L = 2\ k\Omega$		25°C	2.5	3.8		11.5	12.7		
				Full range	2.5			11.5			
V_{OM-}	Maximum negative peak output voltage swing	$R_L = 10\ k\Omega$		25°C	−2.5	−3.5		−12	−13.2		V
				Full range	−2.5			−12			
		$R_L = 2\ k\Omega$		25°C	−2.3	−3.2		−11	−12		
				Full range	−2.3			−11			
A_{VD}	Large-signal differential voltage amplification	$R_L = 2\ k\Omega$, See Note 6		25°C	25	72		50	133		V/mV
				−40°C	30	101		60	212		
				85°C	20	50		30	70		
r_i	Input resistance			25°C		10^{12}			10^{12}		Ω
C_i	Input capacitance			25°C		10			12		pF
CMRR	Common-mode rejection ratio	$V_{IC} = V_{ICR}$ min, $V_O = 0$, $R_S = 50\ \Omega$		25°C	65	84		75	92		dB
				−40°C	65	83		75	92		
				85°C	65	84		75	93		
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm} / \Delta V_{IO}$)	$V_{CC\pm} = \pm 5$ V to ± 15 V, $V_O = 0$, $R_S = 50\ \Omega$		25°C	75	99		75	99		dB
				−40°C	75	98		75	99		
				85°C	75	99		75	99		
I_{CC}	Supply current (four amplifiers)	No load, $V_O = 0$		25°C		8.1	11.2		8.4	11.2	mA
				−40°C		7.9	12.8		8.2	12.8	
				85°C		7.6	11.2		7.9	11.2	
V_{O1}/V_{O2}	Crosstalk attenuation	$A_{VD} = 100$		25°C		120			120		dB

† Full range is − 40°C to 85°C.

NOTES: 5. Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at $T_A = 150°C$ extrapolated to $T_A = 25°C$ using the Arrhenius equation and assuming an activation energy of 0.96 eV.

6. For $V_{CC\pm} = \pm 5$ V, $V_O = \pm 2.3$ V; at $V_{CC\pm} = \pm 15$ V, $V_O = \pm 10$ V.

operating characteristics

PARAMETER		TEST CONDITIONS		T_A†	$V_{CC\pm}$ = ±5 V			$V_{CC\pm}$ = ±15 V			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
SR +	Positive slew rate at unity gain	R_L = 2 kΩ, C_L = 100 pF, See Figure 1 and Note 7		25°C		15.4		10	17.8		V/µs
				– 40°C		16.4		8	18		
				85°C		14		8	17.3		
SR –	Negative slew rate at unity gain			25°C		13.9		10	15.9		
				– 40°C		14.7		8	16.1		
				85°C		13		8	15.3		
t_r	Rise time	V_{IPP} = ± 10 mV, R_L = 2 kΩ, C_L = 100 pF, See Figures 1 and 2		25°C		55			56		ns
				– 40°C		52			53		
				85°C		64			65		
t_f	Fall time			25°C		55			57		
				– 40°C		51			53		
				85°C		64			65		
	Overshoot factor			25°C		24%			19%		
				– 40°C		24%			19%		
				85°C		24%			19%		
V_n	Equivalent input noise voltage (see Note 9)	R_S = 100 Ω, See Figure 3	f = 10 Hz	25°C		75			75		nV/√Hz
			f = 1 kHz	25°C		21			21	45	
V_{NPP}	Peak-to-peak equivalent input noise voltage		f = 10 Hz to 10 kHz	25°C		4			4		µV
I_n	Equivalent input noise current	f = 1 kHz		25°C		0.01			0.01		pA/√Hz
THD	Total harmonic distortion	R_S = 1 kΩ, R_L = 2 kΩ, f = 1 kHz, See Note 8		25°C		0.003%			0.003%		
B_1	Unity-gain bandwidth	V_i = 10 mV, R_L = 2 kΩ, C_L = 25 pF, See Figure 4		25°C		2.7			2.7		MHz
				– 40°C		3.3			3.3		
				85°C		2.3			2.4		
ϕ_m	Phase margin at unity gain	V_i = 10 mV, R_L = 2 kΩ, C_L = 25 pF, See Figure 4		25°C		61°			64°		
				– 40°C		59°			62°		
				85°C		61°			64°		

† Full range is – 40°C to 85°C.

NOTES: 7. For $V_{CC\pm}$ = ±5 V, V_{IPP} = ± 1 V; for $V_{CC\pm}$ = ± 15 V, V_{IPP} = ±5 V.

8. For $V_{CC\pm}$ = ± 5 V, $V_{o(rms)}$ = 1 V; for $V_{CC\pm}$ = ± 15 V, $V_{o(rms)}$ = 6 V.

9. This parameter is tested on a sample basis. For other test requirements, please contact the factory. This statement has no bearing on testing or nontesting of other parameters.

electrical characteristics

PARAMETER		TEST CONDITIONS		T_A†	$V_{CC\pm} = \pm5$ V			$V_{CC\pm} = \pm15$ V			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	$V_O = 0$, $V_{IC} = 0$, $R_S = 50\ \Omega$	TL054M	25°C		0.64	5.5		0.56	4	mV
				Full range			10.5			9	
			TL054AM	25°C		0.57	3.5		0.5	1.5	
				Full range			8.5			6.5	
α_{VIO}	Temperature coefficient of input offset voltage		TL054M	25°C to 125°C		21			20		µV/°C
			TL054AM	25°C to 125°C		21			20		
	Input offset voltage long-term drift (see Note 5)			25°C		0.04			0.04		µV/mo
I_{IO}	Input offset current	$V_O = 0$, $V_{IC} = 0$, See Figure 5		25°C		4	100		5	100	pA
				125°C		1	20		2	20	nA
I_{IB}	Input bias current	$V_O = 0$, $V_{IC} = 0$, See Figure 5		25°C		20	200		30	200	pA
				125°C		10	50		20	50	nA
V_{ICR}	Common-mode input voltage range			25°C	−1 to 4	−2.3 to 5.6		−11 to 11	−12.3 to 15.6		V
				Full range	−1 to 4			−11 to 11			
V_{OM+}	Maximum positive peak output voltage swing	$R_L = 10$ kΩ		25°C	3	4.2		13	13.9		V
				Full range	3			13			
		$R_L = 2$ kΩ		25°C	2.5	3.8		11.5	12.7		
				Full range	2.5			11.5			
V_{OM-}	Maximum negative peak output voltage swing	$R_L = 10$ kΩ		25°C	−2.5	−3.5		−12	−13.2		V
				Full range	−2.5			−12			
		$R_L = 2$ kΩ		25°C	−2.3	−3.2		−11	−12		
				Full range	−2.3			−11			
A_{VD}	Large-signal differential voltage amplification	$R_L = 2$ kΩ, See Note 6		25°C	25	72		50	133		V/mV
				−55°C	30	99		60	209		
				125°C	10	35		15	35		
r_i	Input resistance			25°C		10^{12}			10^{12}		Ω
C_i	Input capacitance			25°C		10			12		pF
CMRR	Common-mode rejection ratio	$V_{IC} = V_{ICR}$min, $V_O = 0$, $R_S = 50\ \Omega$		25°C	65	84		75	92		dB
				−55°C	65	83		75	92		
				125°C	65	84		75	93		
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm} / \Delta V_{IO}$)	$V_{CC\pm} = \pm5$ V to ±15 V, $V_O = 0$, $R_S = 50\ \Omega$		25°C	75	99		75	99		dB
				−55°C	75	98		75	98		
				125°C	75	100		75	100		
I_{CC}	Supply current (four amplifiers)	No load, $V_O = 0$		25°C		8.1	11.2		8.4	11.2	mA
				−55°C		7.8	12.8		8.1	12.8	
				125°C		7.1	11.2		7.5	11.2	
V_{O1}/V_{O2}	Crosstalk attenuation	$A_{VD} = 100$		25°C		120			120		dB

† Full range is – 55°C to 125°C.

NOTES: 5. Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at $T_A = 150$°C extrapolated to $T_A = 25$°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

6. For $V_{CC\pm} = \pm5$ V, $V_O = \pm2.3$ V; at $V_{CC\pm} = \pm15$ V, $V_O = \pm10$ V.

operating characteristics

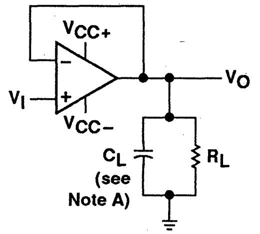
PARAMETER		TEST CONDITIONS		T_A†	$V_{CC\pm}$ = ±5 V			$V_{CC\pm}$ = ±15 V			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
SR+	Positive slew rate at unity gain	R_L = 2 kΩ, C_L = 100 pF, See Figure 1 and Note 7		25°C		15.4		10	17.8		V/µs
				−55°C		16.7			18.3		
				125°C		12.9			16.7		
SR−	Negative slew rate at unity gain			25°C		13.9		10	15.9		
				−55°C		14.7			16.3		
				125°C		12.2			14.5		
t_r	Rise time	V_{IPP} = ±10 mV, R_L = 2 kΩ, C_L = 100 pF, See Figures 1 and 2		25°C		55			56		ns
				−55°C		51			52		
				125°C		68			68		
t_f	Fall time			25°C		55			57		
				−55°C		51			52		
				125°C		68			69		
	Overshoot factor			25°C		24%			19%		
				−55°C		25%			19%		
				125°C		25%			19%		
V_n	Equivalent input noise voltage	R_S = 100 Ω, See Figure 3	f = 10 Hz	25°C		75			75		nV/√Hz
			f = 1 kHz	25°C		21			21		
V_{NPP}	Peak-to-peak equivalent input noise voltage		f = 10 Hz to 10 kHz	25°C		4			4		µV
I_n	Equivalent input noise current	f = 1 kHz		25°C		0.01			0.01		pA/√Hz
THD	Total harmonic distortion	R_S = 1 kΩ, R_L = 2 kΩ, f = 1 kHz, See Note 8		25°C		0.003%			0.003%		
B_1	Unity-gain bandwidth	V_i = 10 mV, R_L = 2 kΩ, C_L = 25 pF, See Figure 4		25°C		2.7			2.7		MHz
				−55°C		3.4			3.4		
				125°C		2.1			2.1		
ϕ_m	Phase margin at unity gain	V_i = 10 mV, R_L = 2 kΩ, C_L = 25 pF, See Figure 4		25°C		61°			64°		
				−55°C		58°			62°		
				125°C		60°			64°		

† Full range is − 55°C to 125°C.

NOTES: 7. For $V_{CC\pm}$ = ±5 V, V_{IPP} = ±1 V; for $V_{CC\pm}$ = ±15 V, V_{IPP} = ±5 V.

8. For $V_{CC\pm}$ = ±5 V, $V_{o(rms)}$ = 1 V; for $V_{CC\pm}$ = ±15 V, $V_{o(rms)}$ = 6 V.

PARAMETER MEASUREMENT INFORMATION



NOTE A: C_L includes fixture capacitance.

Figure 1. Slew Rate, Rise/Fall Time, and Overshoot Test Circuit

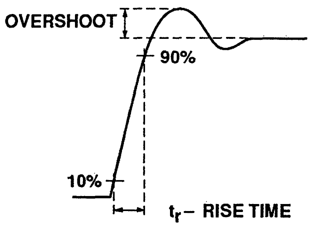


Figure 2. Rise Time and Overshoot Waveform

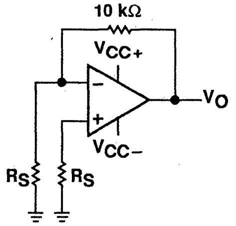
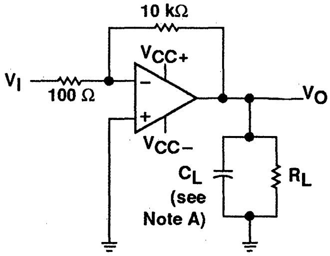


Figure 3. Noise Voltage Test Circuit



NOTE A: C_L includes fixture capacitance.

Figure 4. Unity-Gain Bandwidth and Phase Margin Test Circuit

typical values

Typical values as presented in this data sheet represent the median (50% point) of device parametric performance.

input bias and offset current

At the picoamp-bias-current level typical of the TL054 and TL054A, accurate measurement of the bias current becomes difficult. Not only does this measurement require a picoammeter, but test socket leakages can easily exceed the actual device bias currents. To accurately measure these small currents, Texas Instruments uses a two-step process. The socket leakage is measured using picoammeters with bias voltages applied, but with no device in the socket. The device is then inserted in the socket and a second test that measures both the socket leakage and the device input bias current is performed. The two measurements are then subtracted algebraically to determine the bias current of the device.

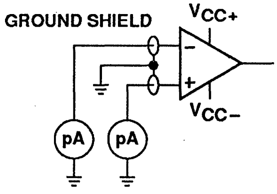


Figure 5. Input Bias and Offset Current Test Circuit

noise

Because of the increasing emphasis on low noise levels in many of today's applications, the input noise voltage density is sample-tested at f = 1 kHz. Texas Instruments also has additional noise testing capability to meet specific application requirements. Please contact the factory for details.

TYPICAL CHARACTERISTICS

table of graphs

			FIGURE
V_{IO}	Input offset voltage	Distribution	6
α_{VIO}	Temperature coefficient of input offset voltage	Distribution	7
I_{IO}	Input offset current	vs Temperature	8
I_{IB}	Input bias current	vs V_{IC}	9
		vs Temperature	8
V_I	Input voltage range	vs V_{CC}	10
		vs Temperature	11
V_O	Output voltage	vs Differential input voltage	12, 13
V_{OM}	Maximum peak output voltage swing	vs V_{CC}	14
		vs Output current	18, 19
		vs Frequency	15, 16, 17
		vs Temperature	20, 21
A_{VD}	Differential voltage amplification	vs R_L	22
		vs Frequency	23
		vs Temperature	24, 25
z_o	Output impedance	vs Frequency	29
CMRR	Common-mode rejection ratio	vs Frequency	26, 27
		vs Temperature	28
k_{SVR}	Supply-voltage rejection ratio	vs Temperature	30
I_{OS}	Short-circuit output current	vs V_{CC}	31
		vs Time	32
		vs Temperature	33
I_{CC}	Supply current	vs V_{CC}	34
		vs Temperature	35
SR	Slew rate	vs R_L	36, 37
		vs Temperature	38, 39
	Overshoot factor	vs C_L	40
V_n	Equivalent input noise voltage	vs Frequency	41
THD	Total harmonic distortion	vs Frequency	42
B_1	Unity-gain bandwidth	vs V_{CC}	43
		vs Temperature	44
ϕ_m	Phase margin	vs V_{CC}	45
		vs C_L	46
		vs Temperature	47
	Phase shift	vs Frequency	23
	Pulse response	Small-signal	48
		Large-signal	49

TYPICAL CHARACTERISTICS[†]

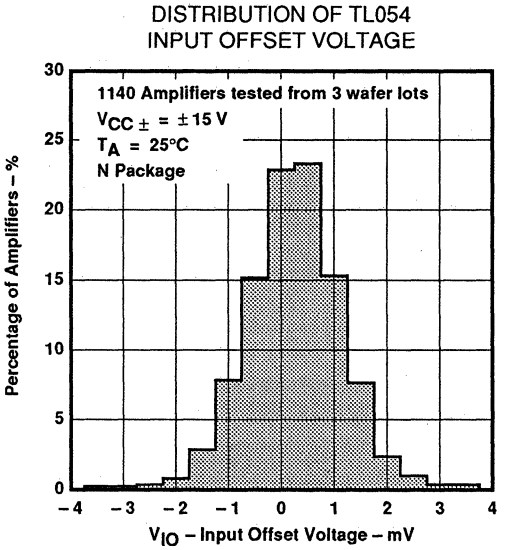


Figure 6

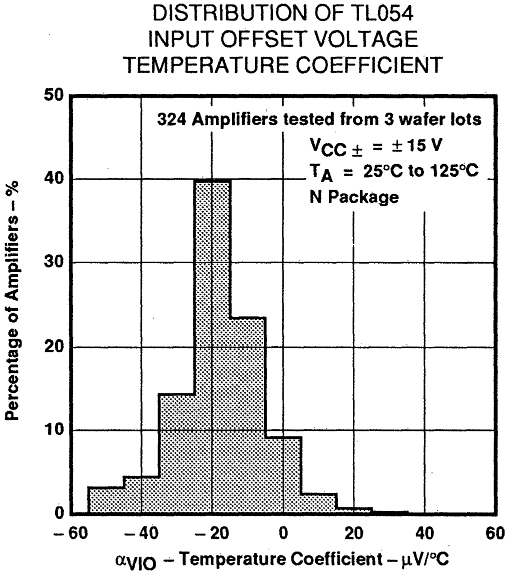


Figure 7

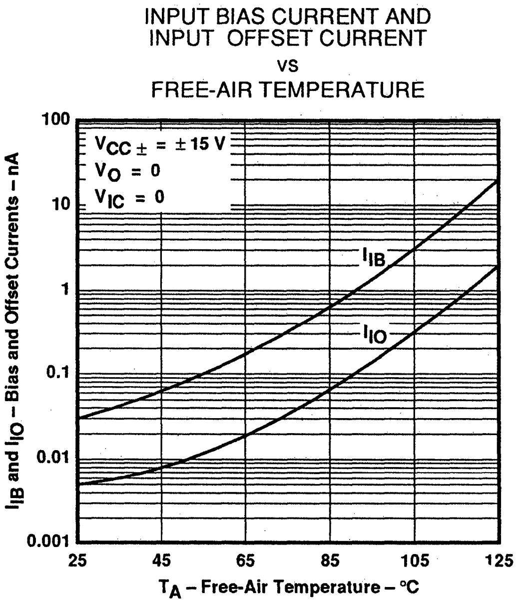


Figure 8

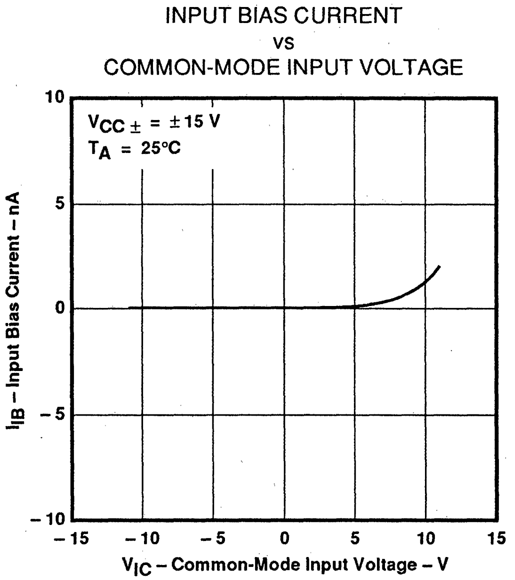


Figure 9

[†] Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

COMMON-MODE
INPUT VOLTAGE RANGE LIMITS
vs
SUPPLY VOLTAGE

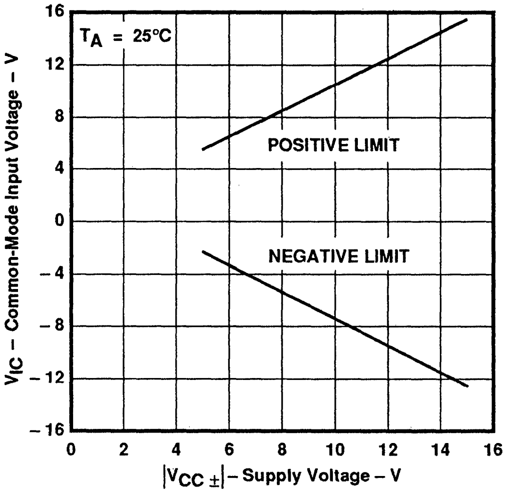


Figure 10

COMMON-MODE
INPUT VOLTAGE RANGE LIMITS
vs
FREE-AIR TEMPERATURE

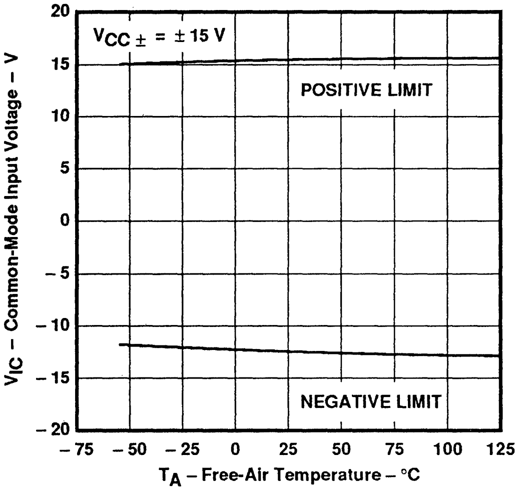


Figure 11

OUTPUT VOLTAGE
vs
DIFFERENTIAL INPUT VOLTAGE

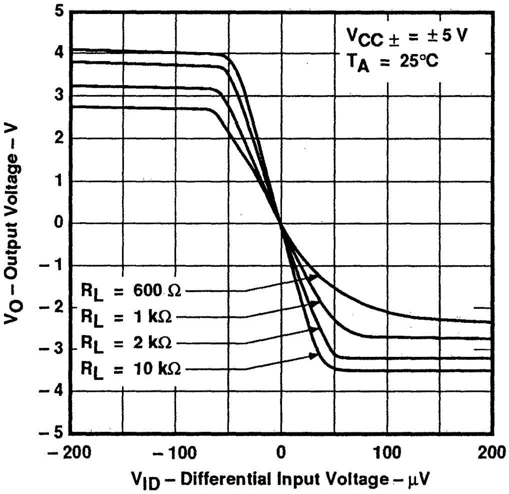


Figure 12

OUTPUT VOLTAGE
vs
DIFFERENTIAL INPUT VOLTAGE

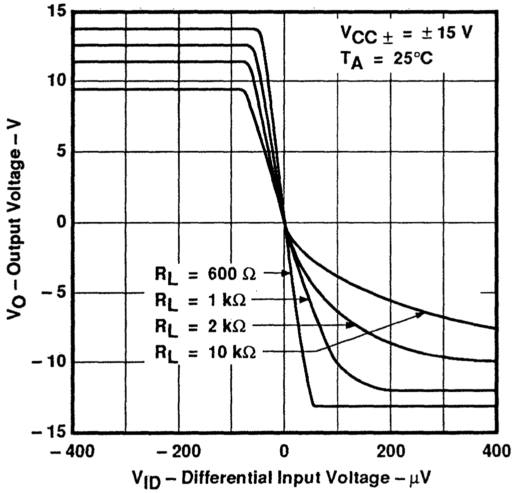


Figure 13

---

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

MAXIMUM PEAK OUTPUT VOLTAGE
vs
SUPPLY VOLTAGE

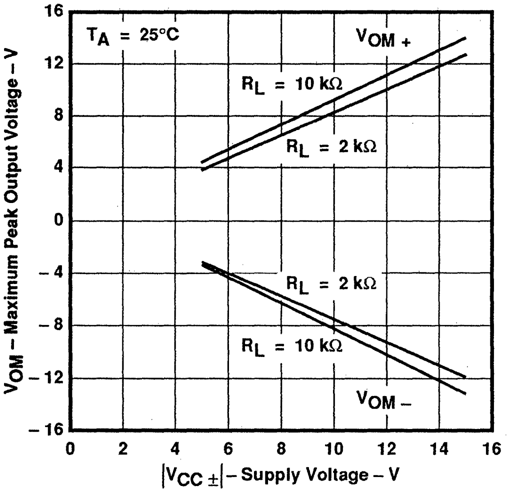


Figure 14

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE
vs
FREQUENCY

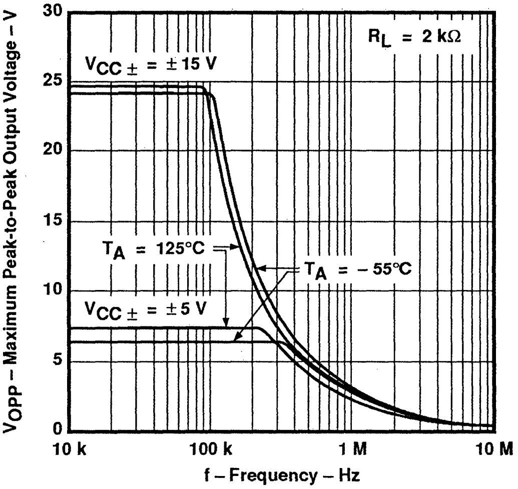


Figure 15

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE
vs
FREQUENCY

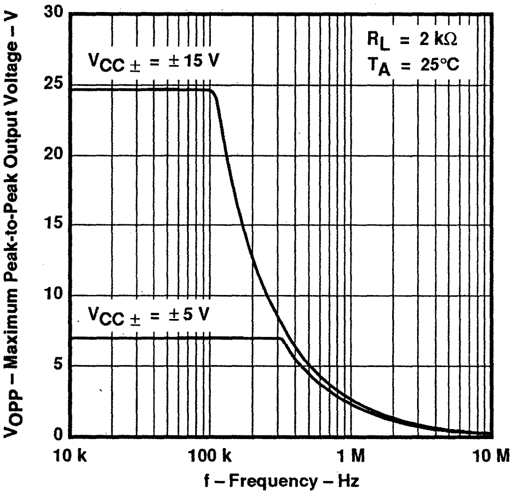


Figure 16

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE
vs
FREQUENCY

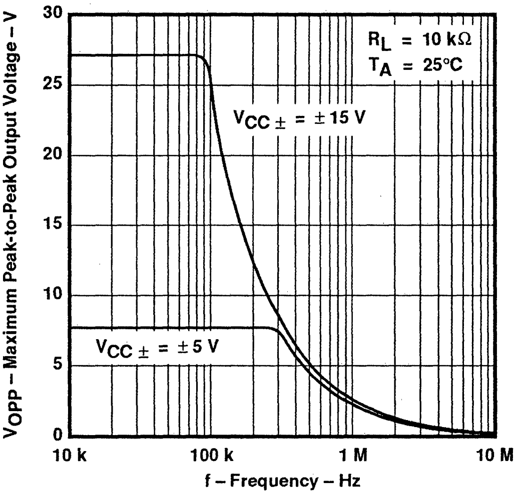


Figure 17

---

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS[†]

MAXIMUM PEAK OUTPUT VOLTAGE
vs
OUTPUT CURRENT

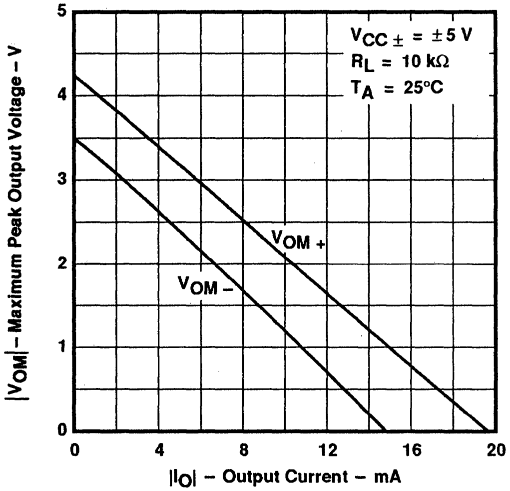


Figure 18

MAXIMUM PEAK OUTPUT VOLTAGE
vs
OUTPUT CURRENT

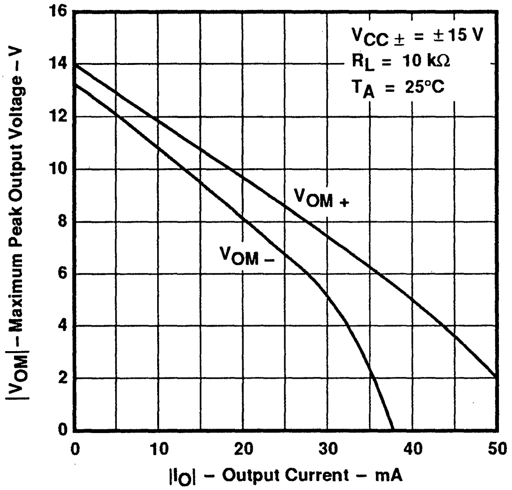


Figure 19

MAXIMUM PEAK OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

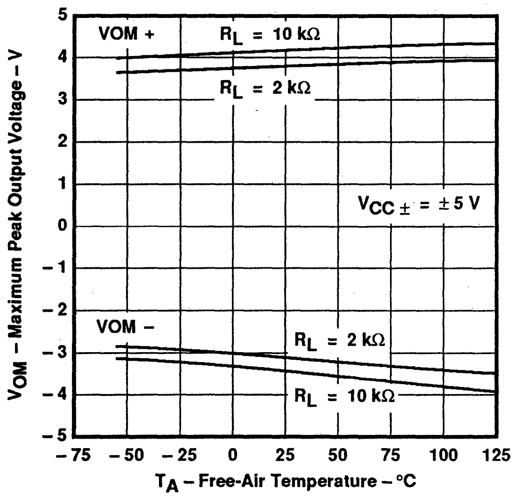


Figure 20

MAXIMUM PEAK OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

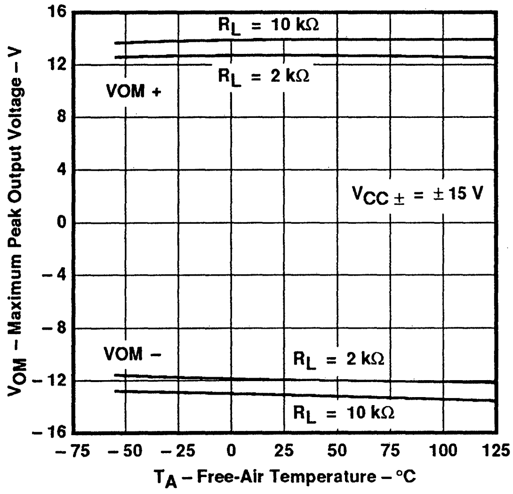


Figure 21

[†] Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

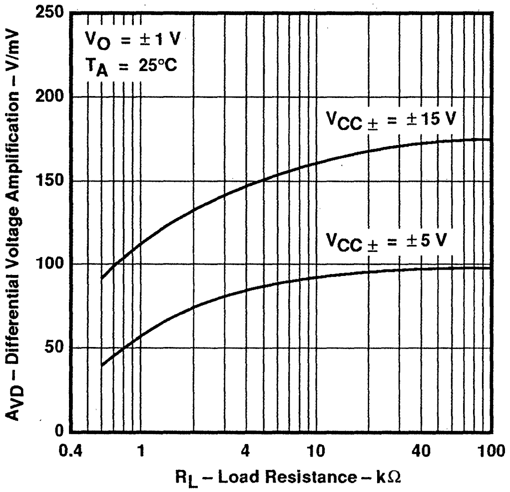

LARGE-SIGNAL VOLTAGE AMPLIFICATION
vs
LOAD RESISTANCE

Figure 22

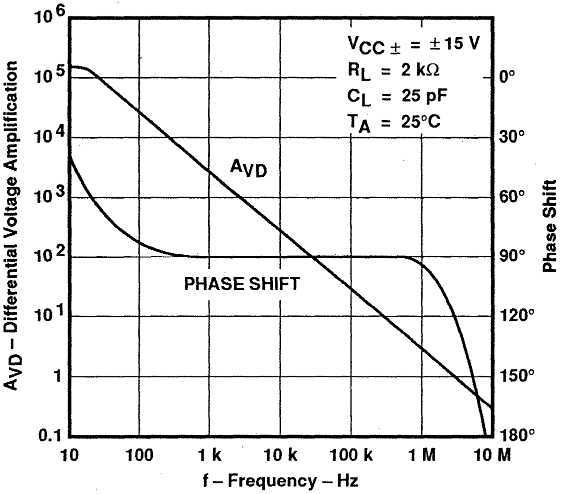

LARGE-SIGNAL DIFFERENTIAL VOLTAGE
AMPLIFICATION AND PHASE SHIFT
vs
FREQUENCY

Figure 23

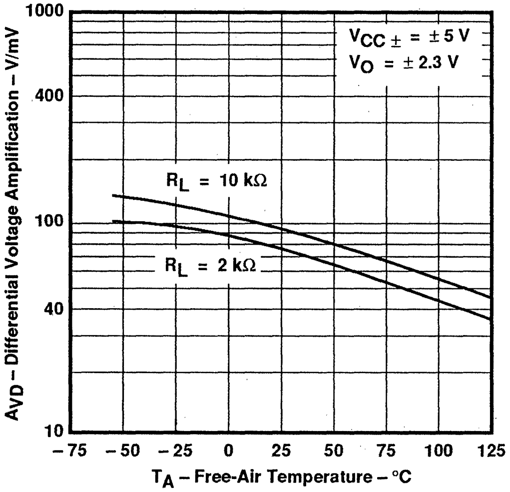

LARGE-SIGNAL VOLTAGE AMPLIFICATION
vs
FREE-AIR TEMPERATURE

Figure 24

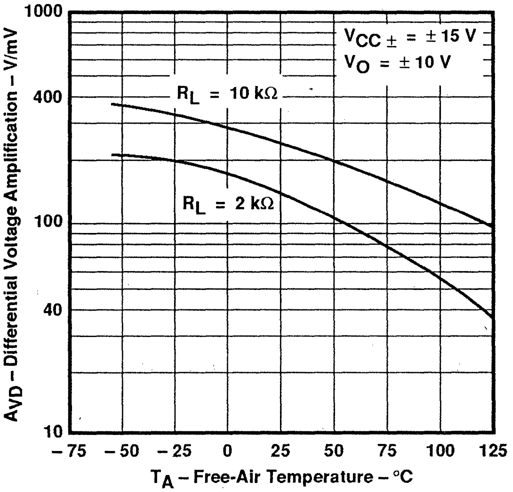

LARGE-SIGNAL VOLTAGE AMPLIFICATION
vs
FREE-AIR TEMPERATURE

Figure 25

---

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS[†]

COMMON-MODE REJECTION RATIO
vs
FREQUENCY

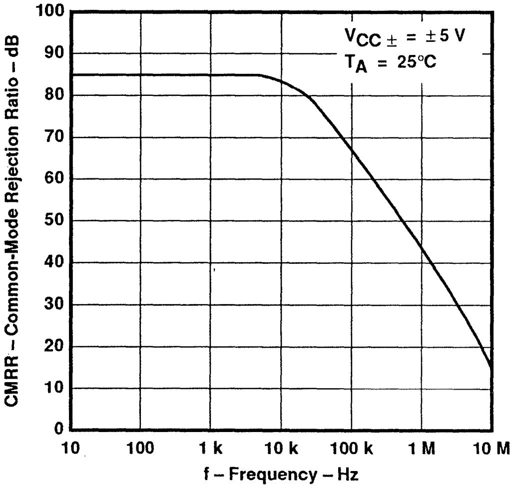


Figure 26

COMMON-MODE REJECTION RATIO
vs
FREQUENCY

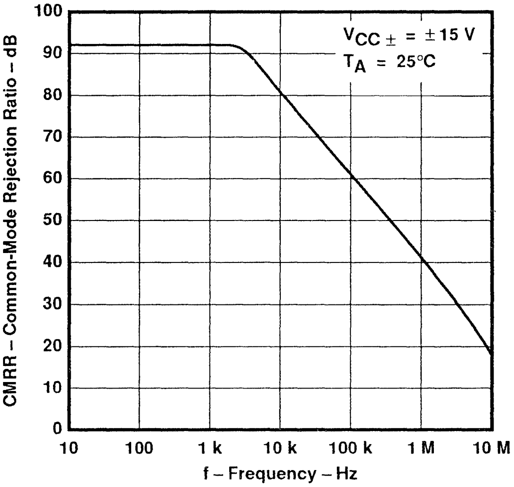


Figure 27

COMMON-MODE REJECTION RATIO
vs
FREQUENCY-AIR TEMPERATURE

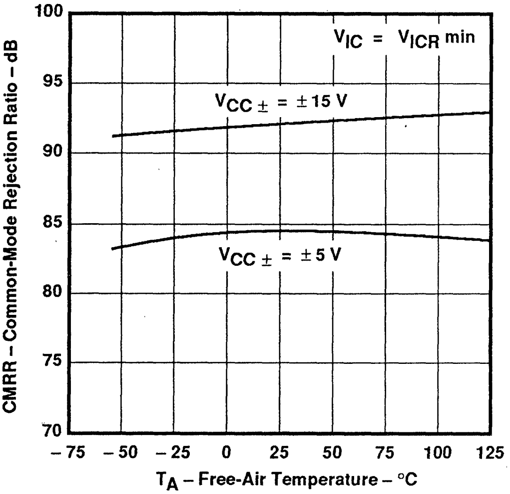


Figure 28

OUTPUT IMPEDANCE
vs
FREQUENCY

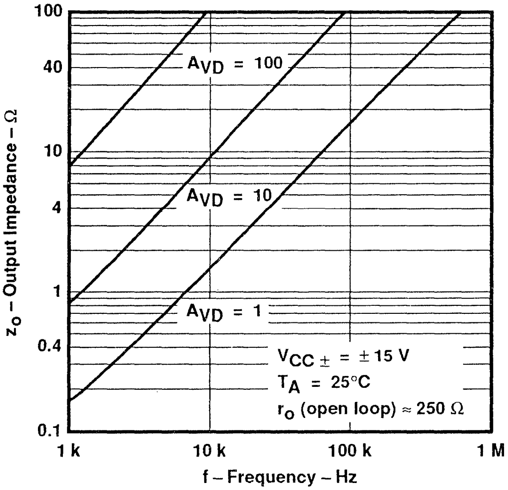


Figure 29

[†]Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

SUPPLY-VOLTAGE REJECTION RATIO
vs
FREE-AIR TEMPERATURE

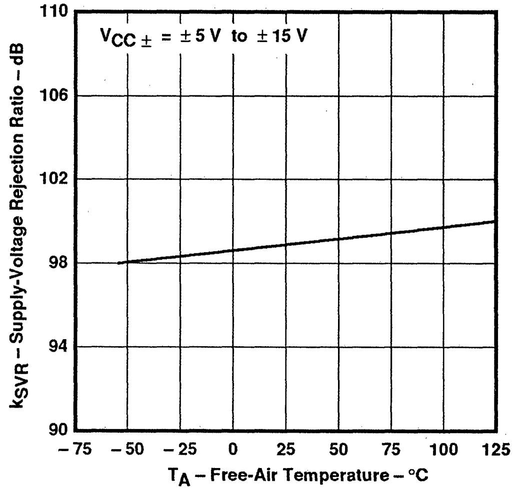


Figure 30

SHORT-CIRCUIT OUTPUT CURRENT
vs
SUPPLY VOLTAGE

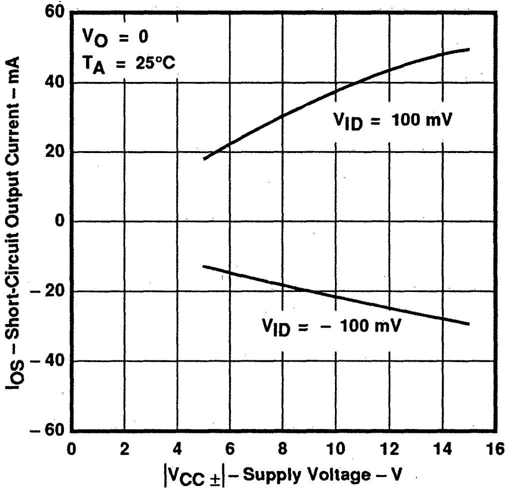


Figure 31

SHORT-CIRCUIT OUTPUT CURRENT
vs
TIME

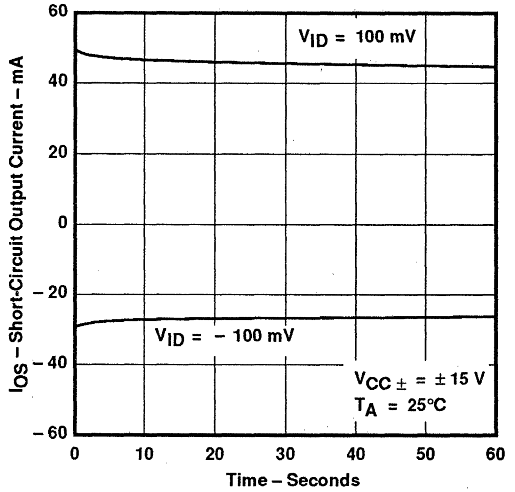


Figure 32

SHORT-CIRCUIT OUTPUT CURRENT
vs
FREE-AIR TEMPERATURE

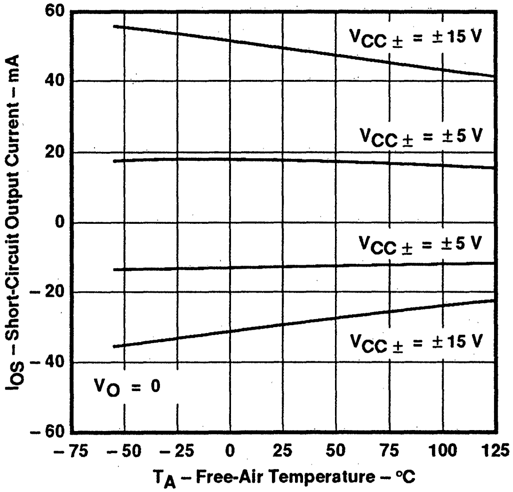


Figure 33

---

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS[†]

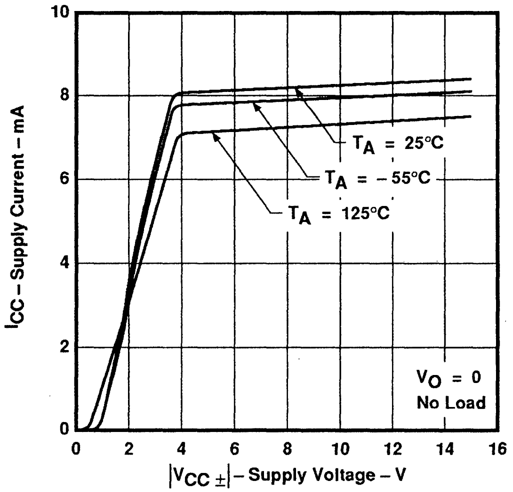

SUPPLY CURRENT
vs
SUPPLY VOLTAGE

Figure 34

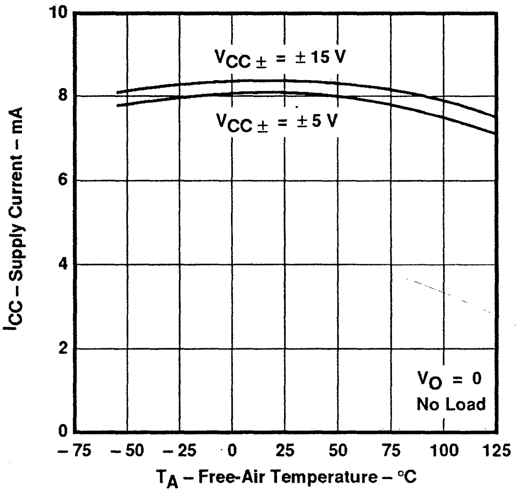

SUPPLY CURRENT
vs
FREE-AIR TEMPERATURE

Figure 35

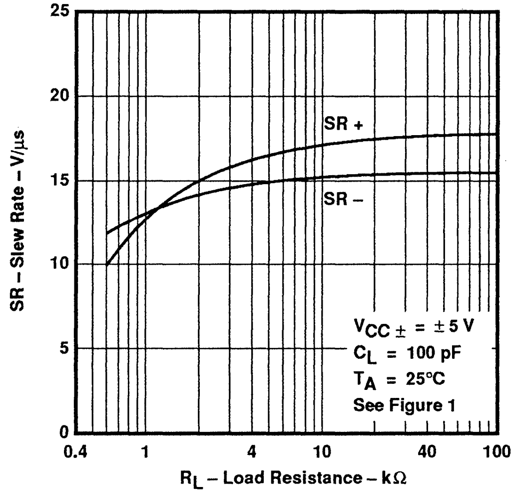

SLEW RATE
vs
LOAD RESISTANCE

Figure 36

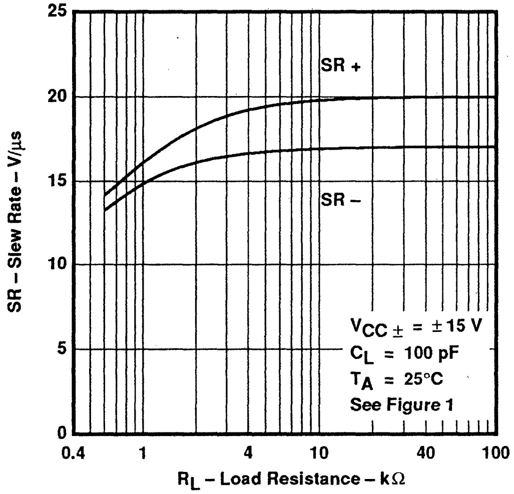

SLEW RATE
vs
LOAD RESISTANCE

Figure 37

[†] Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS[†]

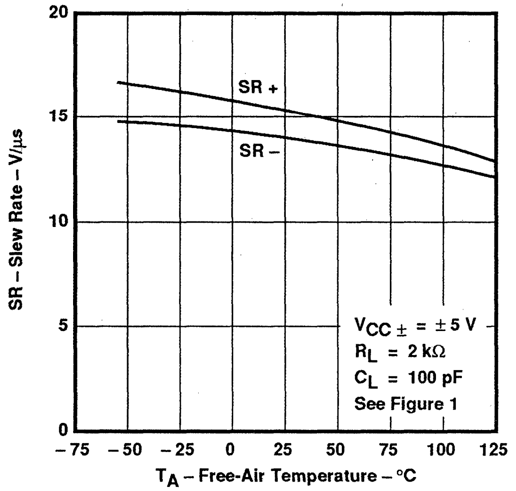

SLEW RATE
vs
FREE-AIR TEMPERATURE

Figure 38

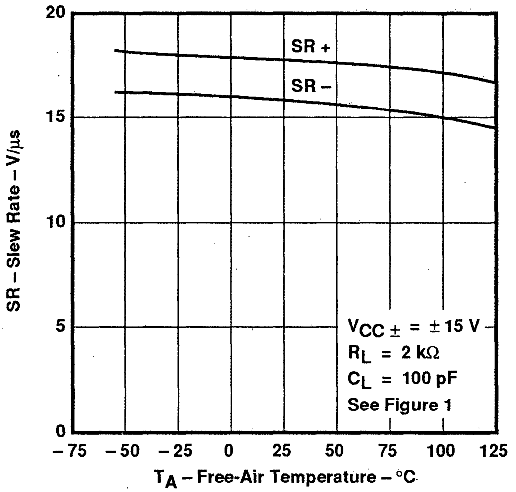

SLEW RATE
vs
FREE-AIR TEMPERATURE

Figure 39

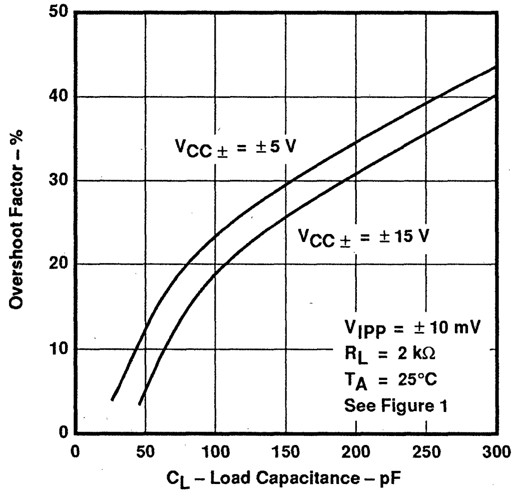

OVERSHOOT FACTOR
vs
LOAD CAPACITANCE

Figure 40

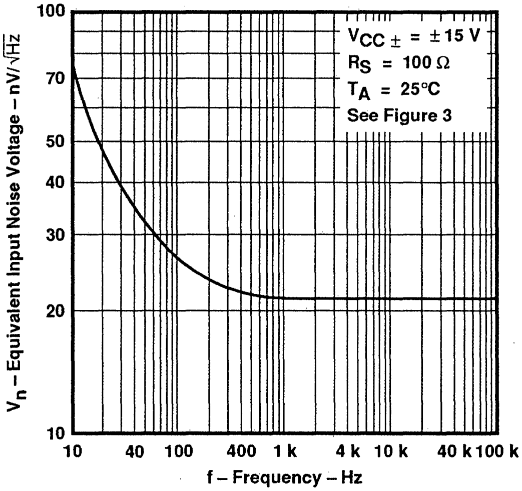

EQUIVALENT INPUT NOISE VOLTAGE
vs
FREQUENCY

Figure 41

[†] Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

TOTAL HARMONIC DISTORTION
vs
FREQUENCY

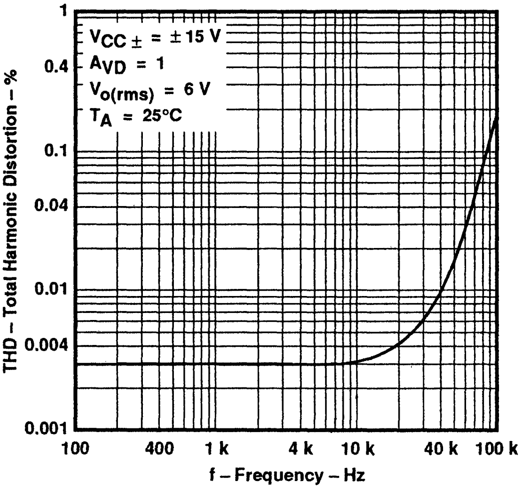


Figure 42

UNITY-GAIN BANDWIDTH
vs
SUPPLY VOLTAGE

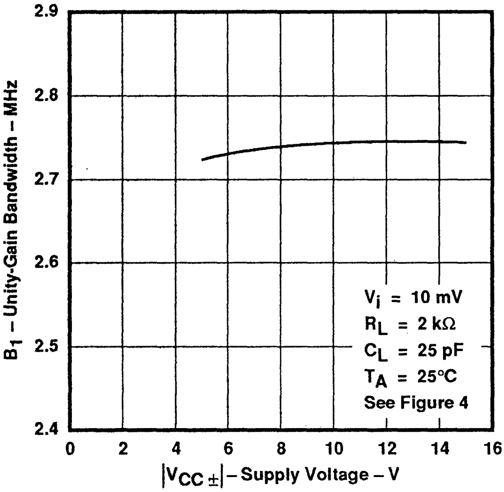


Figure 43

UNITY-GAIN BANDWIDTH
vs
FREE-AIR TEMPERATURE

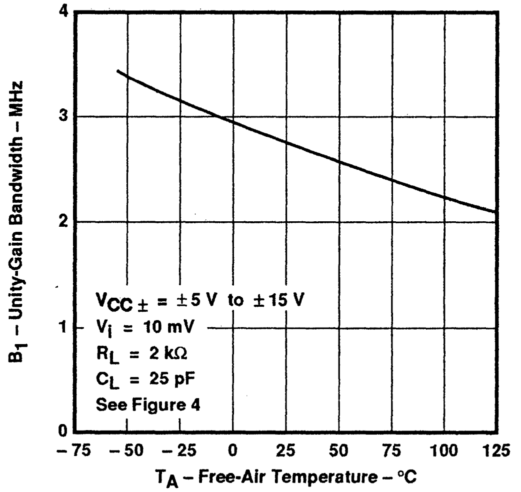


Figure 44

PHASE MARGIN
vs
SUPPLY VOLTAGE

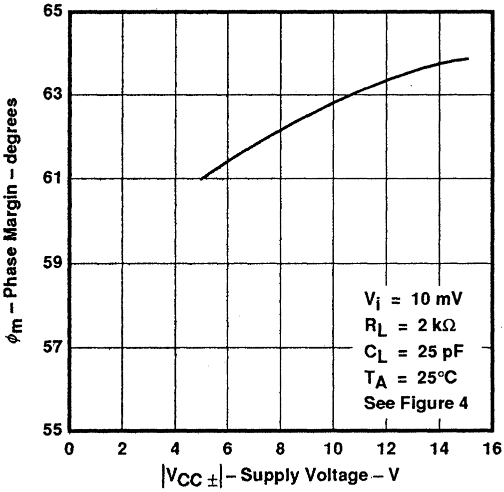


Figure 45

---

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS[†]

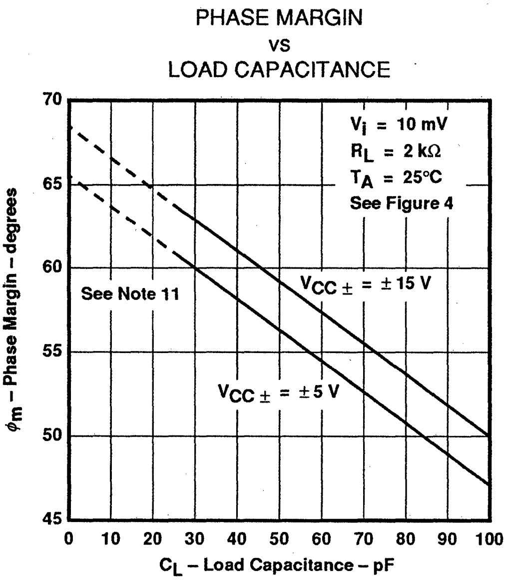


Figure 46

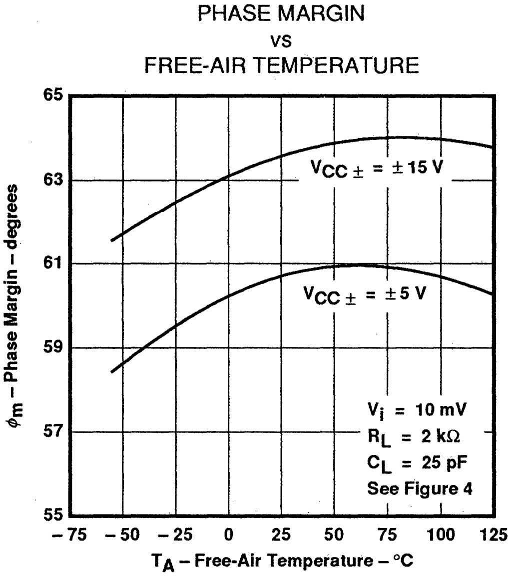


Figure 47

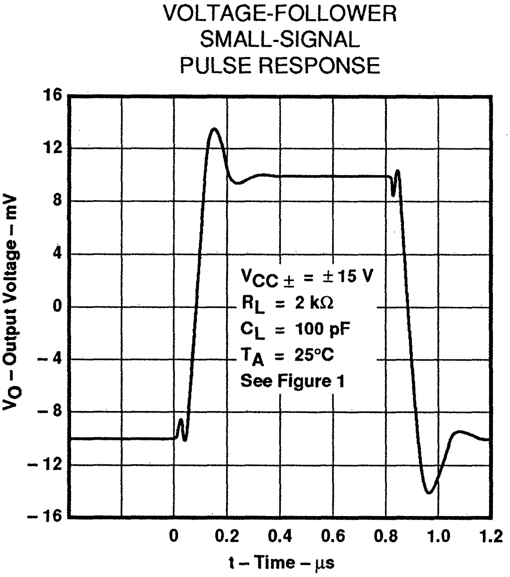


Figure 48

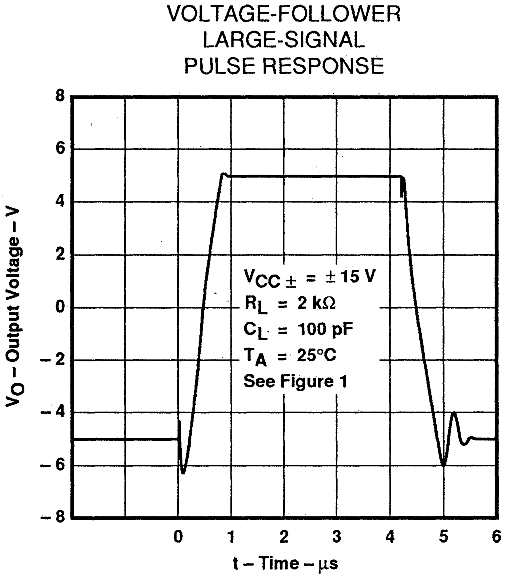


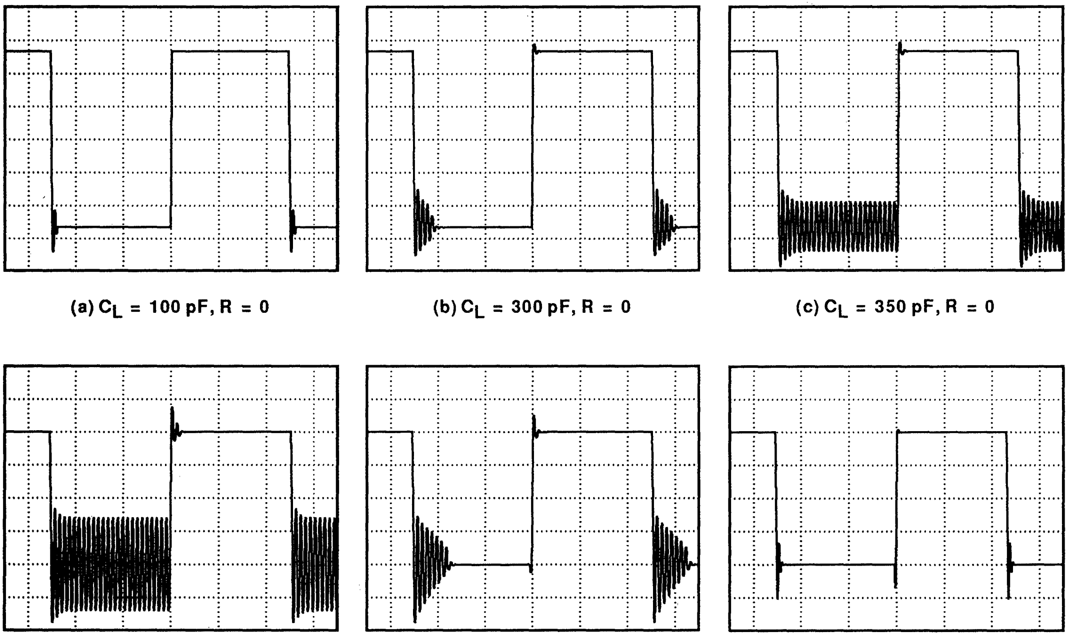
Figure 49

[†] Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.
NOTE 11: Values of phase margin below a load capacitance of 25 pF were estimated.

APPLICATION INFORMATION

output characteristics

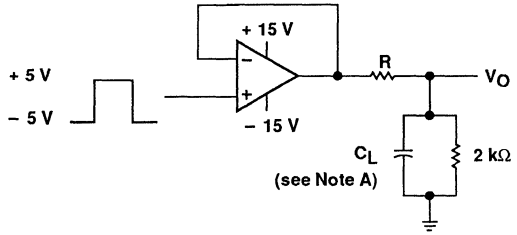
All operating characteristics (except bandwidth and phase margin) are specified with 100-pF load capacitance. The TL054 and TL054A will drive higher capacitive loads; however, as the load capacitance increases, the resulting response pole occurs at lower frequencies, thereby causing ringing, peaking, or even oscillation. The value of the load capacitance at which oscillation occurs varies with production lots. If an application appears to be sensitive to oscillation due to load capacitance, adding a small resistance in series with the load should alleviate the problem. Capacitive loads of 1000 pF and larger may be driven if enough resistance is added in series with the output (see Figure 50).



(a) C_L = 100 pF, R = 0 (b) C_L = 300 pF, R = 0 (c) C_L = 350 pF, R = 0

(d) C_L = 1000 pF, R = 0 (e) C_L 1000 pF, R = 50 Ω (f) C_L = 1000 pF, R = 2 kΩ

Figure 50. Effect of Capacitive Loads



NOTE A: C_L includes fixture capacitance.

Figure 51. Test Circuit for Output Characteristics

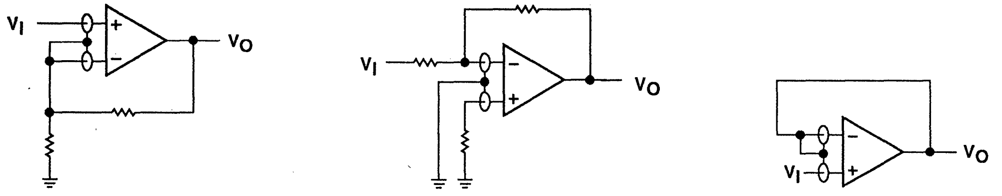
APPLICATION INFORMATION

input characteristics

The TL054 and TL054A are specified with a minimum and a maximum input voltage that, if exceeded at either input, could cause the device to malfunction.

Because of the extremely high input impedance and resulting low bias current requirements, the TL054 and TL054A are well suited for low-level signal processing; however, leakage currents on printed circuit boards and sockets can easily exceed bias current requirements and cause degradation in system performance. It is a good practice to include guard rings around inputs (see Figure 52). These guards should be driven from a low-impedance source at the same voltage level as the common-mode input.

The inputs of any unused amplifiers should be tied to ground to avoid possible oscillation.



(a) NONINVERTING AMPLIFIER (b) INVERTING AMPLIFIER (c) UNITY-GAIN AMPLIFIER

Figure 52. Use of Guard Rings

noise performance

The noise specifications in op amp circuits are greatly dependent on the current in the first-stage differential amplifier. The low input bias current requirements of the TL054 and TL054A result in very low current noise. This feature makes the devices especially favorable over bipolar devices when using values of circuit impedance greater than 50 kΩ.

APPLICATION INFORMATION

Instrumentation amplifier with adjustable gain/null

The instrumentation amplifier in Figure 53 benefits greatly from the high input impedance and stable input offset voltage of the TL054A. Amplifiers U1A, U1B, and U1C form the actual instrumentation amplifier, while U1D provides offset null. Potentiometer R1 provides gain adjust. With R1 = 2 kΩ, the circuit gain equals 100, while with R1 = 200 kΩ, the circuit gain equals two. The following equation shows the instrumentation amplifier gain as a function of R1:

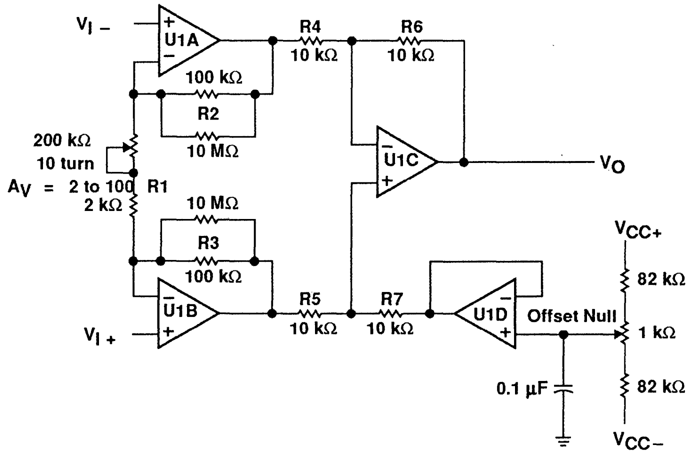
$$A_V = 1 + \left(\frac{R2 + R3}{R1}\right)$$

Readjusting the offset null is necessary whenever the circuit gain is changed. Note that if U1D is needed for another application, R7 can be terminated at ground. The low input offset voltage of the TL054A minimizes the dc error of the circuit. For best matching, all resistors should be one percent tolerance. The matching between R4, R5, R6, and R7 controls the CMRR of this application.

The following equation shows the output voltages when the input voltage equals zero. This dc error can be nulled by adjusting the offset null potentiometer; however, any change in offset voltage over time or temperature also creates an error. To calculate the error from changes in offset, consider the three offset components in the equation as delta offsets rather than initial offsets. The improved stability of Texas Instruments enhanced JFETs minimizes the error resulting from change in input offset voltage with time. Assuming V_{IN} equals zero, V_O can be shown as a function of the offset voltage:

$$V_O = V_{IO2}\left[\left(1 + \frac{R3}{R1}\right)\left(\frac{R7}{R5 + R7}\right)\left(1 + \frac{R6}{R4}\right) + \frac{R2}{R1}\left(\frac{R6}{R4}\right)\right]$$

$$- V_{IO1}\left[\frac{R3}{R1}\left(\frac{R7}{R5 + R7}\right)\left(1 + \frac{R6}{R4}\right) + \frac{R6}{R4}\left(1 + \frac{R2}{R1}\right)\right] + V_{IO3}\left(1 + \frac{R6}{R4}\right)$$



NOTE A: U1A through U1D = TL054A; $V_{CC\pm} = \pm 15$ V.

Figure 53. Instrumentation Amplifier

APPLICATION INFORMATION

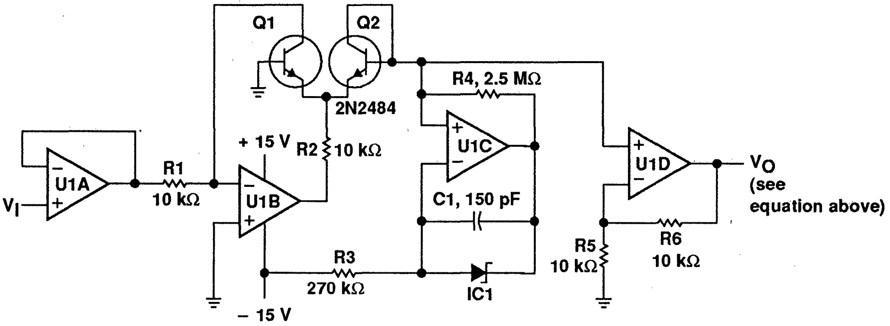
high input impedance log amplifier

The low input offset voltage and high input impedance of the TL054A create a precision log amplifier (see figure 54). IC1 is a 2.5-V, low-current precision, shunt regulator. Transistors Q1 and Q2 must be a closely matched NPN pair. For best performance over temperature, R4 should be a metal film resistor with a low temperature coefficient.

In this circuit, U1A serves as a high-impedance unity-gain buffer. Amplifier U1B converts the input voltage to a current through R1 and Q1. Amplifier U1C, IC1, and R4 form a 1 μA temperature-stable current source that sets the base-emitter voltage of Q2. Amplifier U1D then amplifies the difference between the base-emitter voltage of Q1 and Q2. The output voltage is given by the following equation:

$$V_O = -\left[1+\frac{R6}{R5}\right]\left[\frac{kT}{q}\right]\left[\ln\frac{V_I}{(R1\times1\times10^{-6})}\right]$$

where k = 1.38 × 10^{-23}, q = 1.602 × 10^{-19}, and T is in kelvins.



NOTES: U1A thru U1D = TL054A.
IC1 = LM385, LT1004, or LT1009 voltage reference.

Figure 54. Log Amplifier

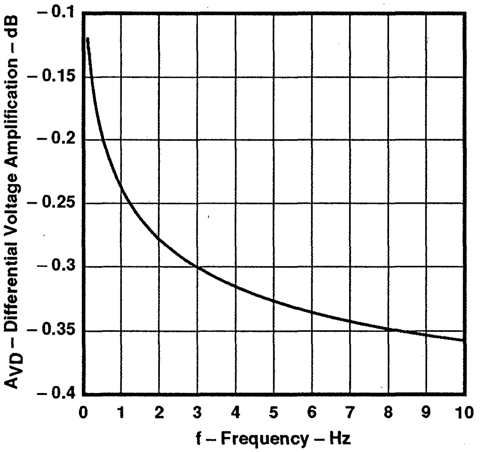


Figure 55. Output Voltage vs Input Voltage for Log Amplifier

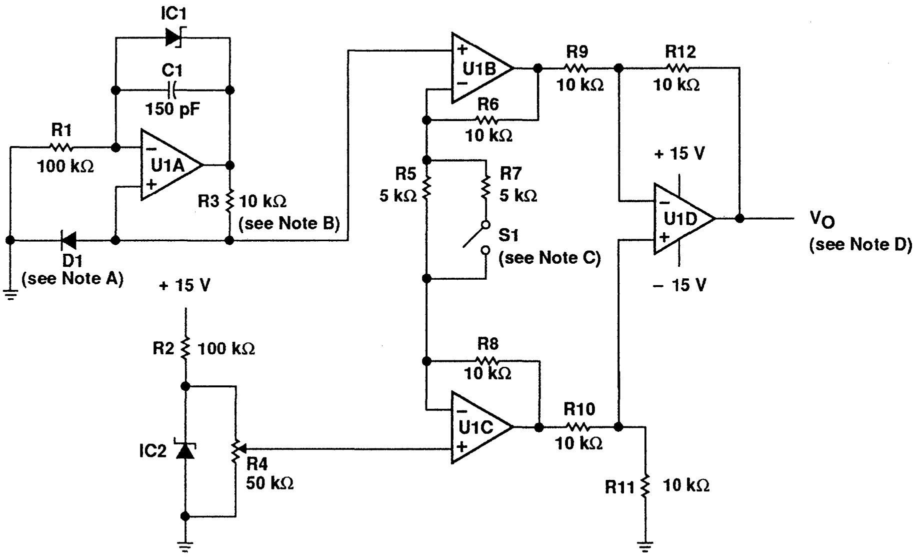
APPLICATION INFORMATION

analog thermometer

By combining a current source that does not vary over temperature with an instrumentation amplifier, a precise analog thermometer can be built (see Figure 56). Amplifier U1A and IC1 establish a constant current through the temperature sensing diode D1. For this section of the circuit to operate correctly, the TL054 must use split supplies and R3 must be a metal film resistor with a low temperature coefficient.

The temperature-sensitive voltage from the diode is compared to a temperature-stable voltage reference set by IC2. R4 should be adjusted to provide the correct output voltage when the diode is at a known temperature. Although this potentiometer resistance varies with temperature, the divider ratio of the potentiometer remains constant.

Amplifiers U1B, U1C, and U1D form the instrumentation amplifier that converts the difference between the diode and reference voltage to a voltage proportional to the temperature. With switch S1 closed, the amplifier gain equals 5, and the output voltage is proportional to temperature in degrees Celsius. With S1 open, the amplifier gain is 9, and the output is proportional to temperature in degrees Fahrenheit. Every time that S1 is changed, R4 must be recalibrated. By setting S1 correctly, the output voltage equals 10 mV per degree (C or F).



NOTES: A. Temperature sensing diode ≈ (− 2 mV/°C).
B. Metal film (low temperature coefficient).
C. Switch open for °F and closed for °C.
D. $V_O \propto$ Temperature; 10 mV/°C or 10 mV/°F.
E. U1A thru U1D = TL054. IC1, IC2 = LM385, LT1004, or LT1009 voltage reference.

Figure 56. Analog Thermometer

APPLICATION INFORMATION

voltage-ratio-to-dB converter

The application in Figure 57 measures the amplitude ratio of two signals and then converts the ratio to decibels. The output voltage provides a resolution of 100 mV/dB. The two inputs can be either dc or sinusoidal ac signals. When using ac signals, both signals should be the same frequency or output glitches will occur. For measuring two input signals of different frequencies, extra filtering should be added after the rectifiers.

The circuit contains three low-offset TL054A devices. Two of these devices provide the rectification and logarithmic conversion of the inputs. The third TL054A forms an instrumentation amplifier. The stage performing the logarithmic conversion also requires two well-matched NPN transistors.

The input signal first passes through a high impedance unity-gain buffer U1A (U2A). Then U1B (U2B) rectifies the input signal at a gain of 0.5, and U1C (U2C) provides a noninverting gain of 2 so that the system gain is still one. U1D (U2D), R6 (R13), and Q1 (Q2) perform the logarithmic conversion of the rectified input signal. The instrumentation amplifier formed by U3A, U3B, U3D scales the difference of the two logarithmic voltages by a gain of 33.6. As a result, the output voltage equals 100 mV/dB. The 1-kΩ potentiometer on the input of U3C calibrates the zero dB reference level. The following equations are used to derive the relationship between the input voltage ratio expressed in decibels and the output voltage.

$$X\,dB = 20\log\left[\frac{V_A}{V_B}\right] = 20\left[\frac{\ln(V_A) - \ln(V_B)}{\ln(10)}\right]$$

$$X\,dB = 8.686\left[\ln(V_A) - \ln(V_B)\right]$$

$$V_{BE(Q1)} = \frac{kT}{q}\ln\left[\frac{V_A}{R \times I_S}\right] \qquad V_{BE(Q2)} = \frac{kT}{q}\ln\left[\frac{V_B}{R \times I_S}\right]$$

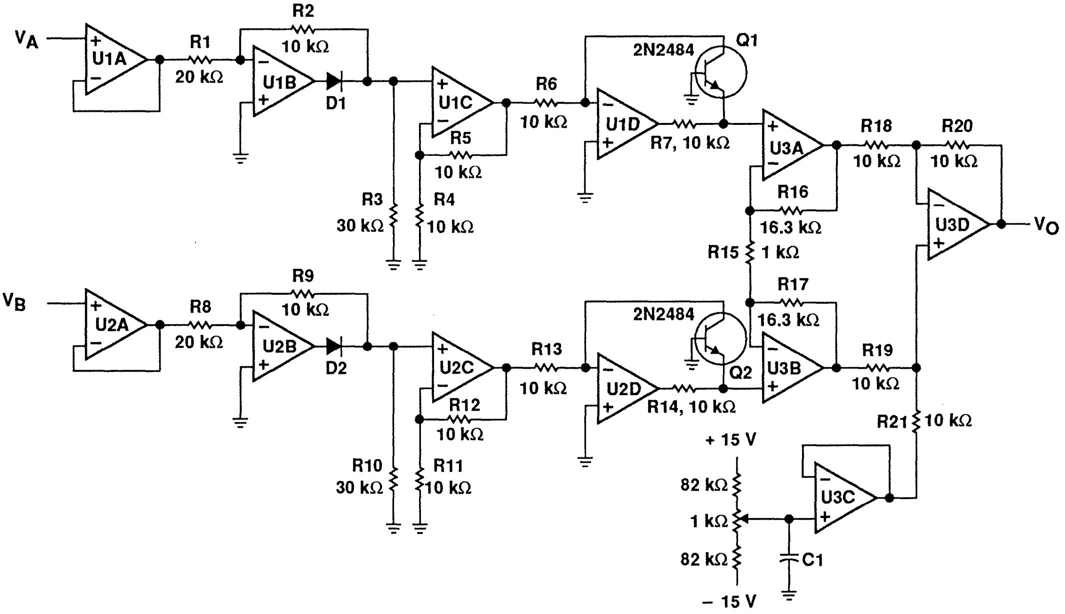
$$\Delta V_{BE} = V_{BE(Q1)} - V_{BE(Q2)} = \frac{kT}{q}\left[\ln(V_A) - \ln(V_B)\right]$$

$$X\,dB = \frac{8.686}{kT/q}\left[V_{BE(Q1)} - V_{BE(Q2)}\right] = 336\left[V_{BE(Q1)} - V_{BE(Q2)}\right] \text{ at } 25°\text{C}.$$

where $k = 1.38 \times 10^{-23}$, $q = 1.602 \times 10^{-19}$, and T is in kelvins.

This would give a resolution of 1 V/dB. Therefore, the gain of the instrumentation amplifier is set at 33.6 to obtain 100 mV/dB.

APPLICATION INFORMATION



NOTES: U1A through U3D = TL054A, $V_{CC\pm}$ = ± 15 V.
D1 and D2 = 1N914.

Figure 57. Voltage-Ratio-to-dB Converter

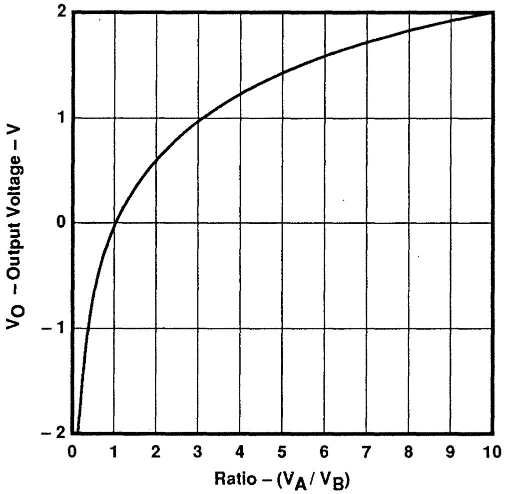


Figure 58. Output Voltage vs the Ratio of the Input Voltages for Voltage-to-dB Converter

TL061, TL061A, TL061B
TL062, TL062A, TL062B, TL064, TL064A, TL064B
LOW-POWER JFET-INPUT OPERATIONAL AMPLIFIERS

D2392, NOVEMBER 1978—REVISED SEPTEMBER 1990

15 DEVICES COVER MILITARY, INDUSTRIAL, AND COMMERCIAL TEMPERATURE RANGES

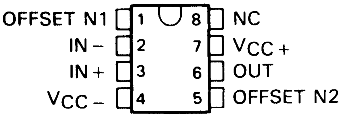
- **Very Low Power Consumption**
- **Typical Supply Current . . . 200 μA (per Amplifier)**
- **Wide Common-Mode and Differential Voltage Ranges**
- **Low Input Bias and Offset Currents**
- **Common-Mode Input Voltage Range Includes V_{CC+}**
- **Output Short-Circuit Protection**
- **High Input Impedance . . . JFET-Input Stage**
- **Internal Frequency Compensation**
- **Latch-Up-Free Operation**
- **High Slew Rate . . . 3.5 V/μs Typ**

description

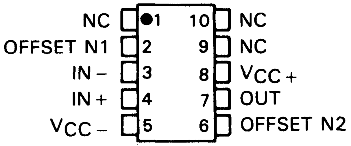
The JFET-input operational amplifiers of the TL061 series are designed as low-power versions of the TL081 series amplifiers. They feature high input impedance, wide bandwidth, high slew rate, and low input offset and bias currents. The TL061 series features the same terminal assignments as the TL071 and TL081 series. Each of these JFET-input operational amplifiers incorporates well-matched, high-voltage JFET and bipolar transistors in a monolithic integrated circuit.

C-suffix devices are characterized for operation from 0°C to 70°C. I-suffix devices are characterized for operation from −40°C to 85°C, and M-suffix devices are characterized for operation over the full military temperature range of −55°C to 125°C.

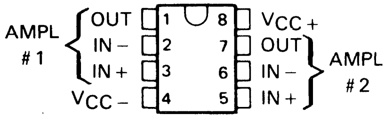
TL061, TL061A, TL061B
D, JG, OR P PACKAGE
(TOP VIEW)



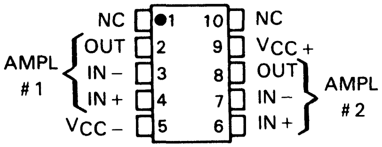
TL061 . . . U PACKAGE
(TOP VIEW)



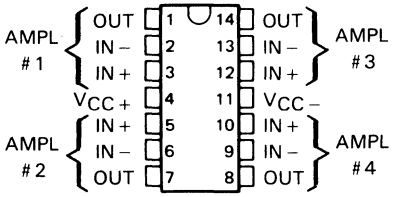
TL062, TL062A, TL062B
D, JG, OR P PACKAGE
(TOP VIEW)



TL062 . . . U PACKAGE
(TOP VIEW)

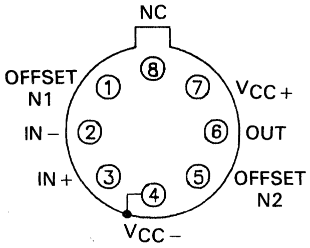


TL064 . . . D, J, N, OR W PACKAGE
TL064A, TL064B . . . D OR N PACKAGE
(TOP VIEW)



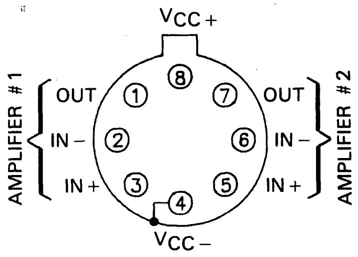
TEXAS INSTRUMENTS
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

TL061 . . . L PACKAGE
(TOP VIEW)



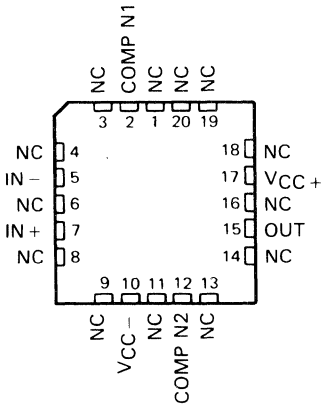
PIN 4 IS IN ELECTRICAL CONTACT
WITH THE CASE

TL062 . . . L PACKAGE
(TOP VIEW)

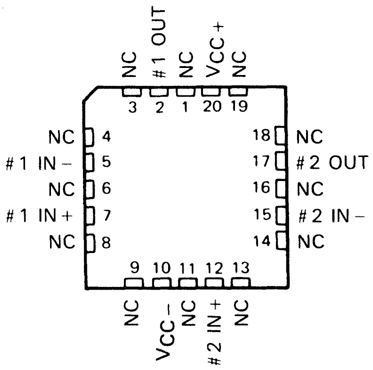


PIN 4 IS IN ELECTRICAL CONTACT
WITH THE CASE

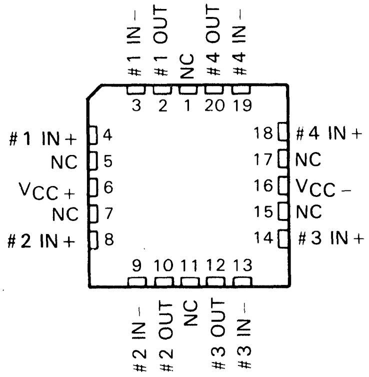
TL061 . . . FK PACKAGE
(TOP VIEW)



TL062 . . . FK PACKAGE
(TOP VIEW)



TL064 . . . FK PACKAGE
(TOP VIEW)



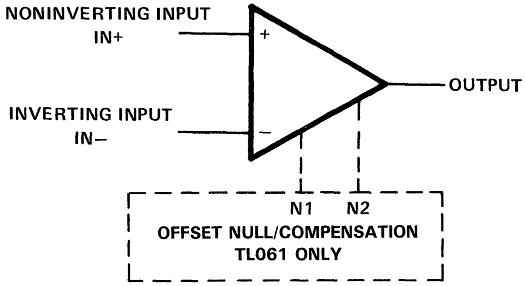
NC—No internal connection

AVAILABLE OPTIONS

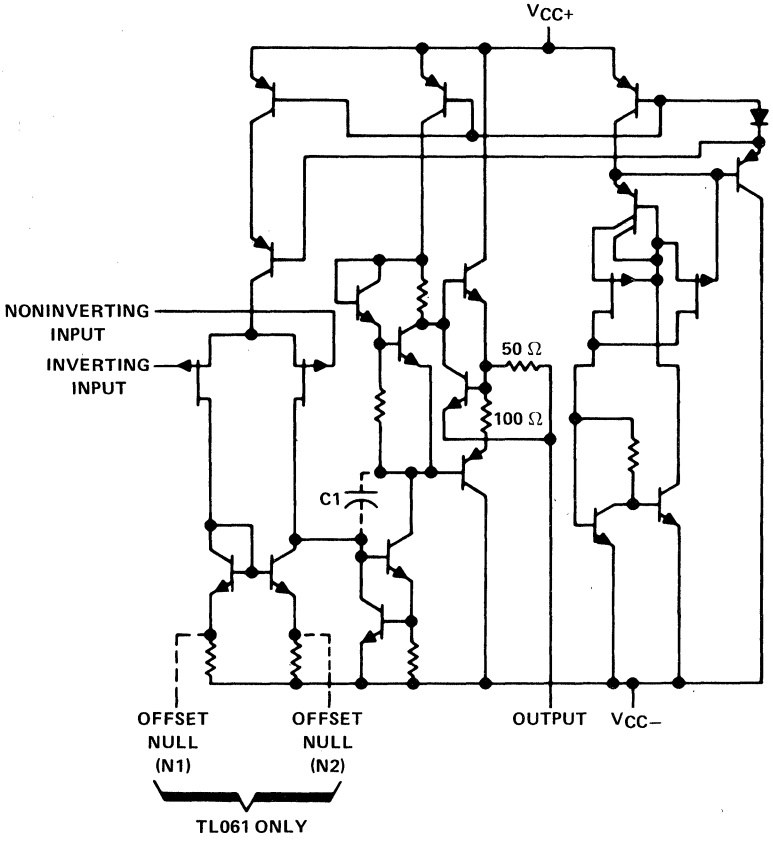
T_A	V_{IO} MAX at 25°C	PACKAGE									
		SMALL OUTLINE (D008)	SMALL OUTLINE (D014)	CHIP CARRIER (FK)	CERAMIC DIP (J)	CERAMIC DIP (JG)	PLUG-IN (L)	PLASTIC DIP (N)	PLASTIC DIP (P)	FLAT PACK (U)	FLAT PACK (W)
0°C to 70°C	15 mV	TL061CD							TL061CP		
	6 mV	TL061ACD							TL061ACP		
	3 mV	TL061BCD							TL061BCP		
	15 mV	TL062CD							TL062CP		
	6 mV	TL062ACD							TL062ACP		
	3 mV	TL062BCD							TL062BCP		
	15 mV		TL064CD					TL064CN			
	6 mV		TL064ACD					TL064ACN			
	3 mV		TL064BCD					TL064BCN			
−40°C to 85°C	6 mV	TL061ID							TL061IP		
	6 mV	TL062ID							TL062IP		
	6 mV		TL064ID					TL064IN			
−55°C to 125°C	6 mV			TL061MFK		TL061MJG	TL061ML			TL061MU	
	6 mV			TL062MFK		TL062MJG	TL062ML			TL062MU	
	9 mV			TL064MFK	TL064MJ						TL064MW

The D package is available taped and reeled. Add the suffix R to the device type, (e.g., TL061CDR).

symbol (each amplifier)



schematic (each amplifier)



C1 = 10 pF on TL061, TL062, and TL064
Component values shown are nominal.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

		TL06_C, TL06_AC, TL06_BC	TL06_I	TL06_M	UNIT
Supply voltage, V_{CC+} (see Note 1)		18	18	18	V
Supply voltage, V_{CC-} (see Note 1)		−18	−18	−18	V
Differential input voltage (see Note 2)		±30	±30	±30	V
Input voltage (see Notes 1 and 3)		±15	±15	±15	V
Duration of output short circuit (see Note 4)		unlimited	unlimited	unlimited	
Continuous total dissipation		See Dissipation Rating Table			
Operating free-air temperature range		0 to 70	−40 to 85	−55 to 125	°C
Storage temperature range		−65 to 150	−65 to 150	−65 to 150	°C
Case temperature for 60 seconds	FK package			260	°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds	J, JG, U or W package			300	°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	D, N or P package	260	260		°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	L package			300	°C

NOTES: 1. All voltage values, except differential voltages, are with respect to the midpoint between V_{CC+} and V_{CC-}.
2. Differential voltages are at the noninverting input terminal with respect to the inverting input terminal.
3. The magnitude of the input voltage must never exceed the magnitude of the supply voltage or 15 V, whichever is less.
4. The output may be shorted to ground or to either supply. Temperature and/or supply voltages must be limited to ensure that the dissipation rating is not exceeded.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR	DERATE ABOVE T_A	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING	$T_A = 125°C$ POWER RATING
D (8-pin)	680 mW	5.8 mW/°C	33°C	464 mW	377 mW	N/A
D (14-pin)	680 mW	7.6 mW/°C	60°C	608 mW	494 mW	N/A
FK	680 mW	11.0 mW/°C	88°C	680 mW	680 mW	275 mW
J	680 mW	11.0 mW/°C	88°C	680 mW	680 mW	275 mW
JG	680 mW	8.4 mW/°C	69°C	672 mW	546 mW	210 mW
L	680 mW	6.6 mW/°C	47°C	528 mW	429 mW	165 mW
N	680 mW	9.2 mW/°C	76°C	680 mW	598 mW	N/A
P	680 mW	8.0 mW/°C	65°C	640 mW	520 mW	N/A
U	675 mW	5.4 mW/°C	25°C	432 mW	351 mW	135 mW
W	680 mW	8.0 mW/°C	65°C	640 mW	520 mW	200 mW

electrical characteristics, $V_{CC\pm}$ = ± 15 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		TL061M TL062M			TL064M			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_O = 0,	T_A = 25°C		3	6		3	9	mV
		R_S = 50 Ω,	T_A = −55°C to 125°C			9			15	
α_{VIO}	Temperature coefficient of input offset voltage	V_O = 0, R_S = 50 Ω, T_A = −55°C to 125°C			10			10		μV/°C
I_{IO}	Input offset current‡	V_O = 0	T_A = 25°C		5	100		5	100	pA
			T_A = −55°C to 125°C			*20			*20	nA
I_{IB}	Input bias current	V_O = 0	T_A = 25°C		30	200		30	200	pA
			T_A = −55°C to 125°C			*50			*50	nA
V_{ICR}	Common-mode input voltage range	T_A = 25°C		±11.5	−12 to +15		±11.5	−12 to +15		V
V_{OM}	Maximum peak output voltage swing	R_L = 10 kΩ, T_A = 25°C		±10	±13.5		±10	±13.5		V
		R_L ≥ 10 lΩ, T_A = −55°C to 125°C		±10			±10			
A_{VD}	Large-signal differential voltage amplification	V_O = ± 10 V,	T_A = 25°C	4	6		4	6		V/mV
		R_L ≥ 10 kΩ	T_A = −55°C to 125°C	4			4			
B_1	Unity-gain bandwidth	R_L = 10 kΩ, T_A = 25°C								MHz
r_i	Input resistance	T_A = 25°C			10^{12}			10^{12}		Ω
CMRR	Common-mode rejection ratio	V_{IC} = V_{ICR} min, V_O = 0, R_S = 50 Ω, T_A = 25°C		80	86		80	86		dB
k_{SVR}	Supply voltage rejection ratio ($\Delta V_{CC\pm}/\Delta V_{IO}$)	V_{CC} = ±15 V to ±9 V, V_O = 0, R_S = 50 Ω, T_A = 25°C		80	95		80	95		dB
P_D	Total power dissipation (each amplifier)	No load, V_O = 0, T_A = 25°C			6	7.5		6	7.5	mW
I_{CC}	Supply current (each amplifier)	No load, V_O = 0 , T_A = 25°C			200	250		200	250	μA
V_{o1}/V_{o2}	Crosstalk attenuation	A_{VD} = 100, T_A = 25°C			120			120		dB

*This parameter is not production tested.

†All characteristics are measured under open-loop conditions with zero common-mode voltage unless otherwise specified.

‡Input bias currents of a FET-input operational amplifier are normal junction reverse currents, which are temperature sensitive as shown in Figure 17. Pulse techniques must be used that will maintain the junction temperature as close to the ambient temperature as possible.

electrical characteristics, $V_{CC\pm} = \pm 15$ V (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		TL061C TL062C TL064C			TL061AC TL062AC TL064AC			TL061BC TL062BC TL064BC			TL061I TL062I TL064I			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	$V_O = 0$, $R_S = 50\ \Omega$	$T_A = 25°C$		3	15		3	6		2	3		3	6	mV
			T_A = full range			20			7.5			5			9	
α_{VIO}	Temperature coefficient of input offset voltage	$V_O = 0$, $R_S = 50\ \Omega$, T_A = full range			10			10			10			10		µV/°C
I_{IO}	Input offset current‡	$V_O = 0$	$T_A = 25°C$		5	200		5	100		5	100		5	100	pA
			T_A = full range			5			3			3			10	nA
I_{IB}	Input bias current‡	$V_O = 0$	$T_A = 25°C$		30	400		30	200		30	200		30	200	pA
			T_A = full range			10			7			7			20	nA
V_{ICR}	Common-mode input voltage range	$T_A = 25°C$		±11	−12 to +15		±11.5	−12 to +15		±11.5	−12 to +15		±11.5	−12 to +15		V
V_{OM}	Maximum peak output voltage swing	$R_L = 10\ k\Omega$, $T_A = 25°C$		±10	±13.5		±10	±13.5		±10	±13.5		±10	±13.5		V
		$R_L \geq 10\ k\Omega$, T_A = full range		±10			±10			±10			±10			
A_{VD}	Large-signal differential voltage amplification	$V_O = \pm 10$ V, $R_L \geq 10\ k\Omega$	$T_A = 25°C$	3	6		4	6		4	6		4	6		V/mV
			T_A = full range	3			4			4			4			
B_1	Unity-gain bandwidth	$R_L = 10\ k\Omega$, $T_A = 25°C$			1			1			1			1		MHz
r_i	Input resistance	$T_A = 25°C$			10^{12}			10^{12}			10^{12}			10^{12}		Ω
CMRR	Common-mode rejection ratio	$V_{IC} = V_{ICR}$ min, $V_O = 0$, $R_S = 50\ \Omega$, $T_A = 25°C$		70	86		80	86		80	86		80	86		dB
k_{SVR}	Supply voltage rejection ratio ($\Delta V_{CC\pm}/\Delta V_{IO}$)	$V_{CC} = \pm 15$ V to ± 9 V, $V_O = 0$, $R_S = 50\ \Omega$, $T_A = 25°C$		70	95		80	95		80	95		80	95		dB
P_D	Total power dissipation (each amplifier)	No load, $V_O = 0$, $T_A = 25°C$			6	7.5		6	7.5		6	7.5		6	7.5	mW
I_{CC}	Supply current (each amplifier)	No load, $V_O = 0$, $T_A = 25°C$			200	250		200	250		200	250		200	250	µA
V_{O1}/V_{O2}	Crosstalk attenuation	$A_{VD} = 100$, $T_A = 25°C$			120			120			120			120		dB

---

† All characteristics are measured under open-loop conditions with zero common-mode voltage unless otherwise specified. Full range for T_A is 0°C to 70°C for TL06_C, TL06_AC, and TL06_BC and −40°C to 85°C for TL06_I.

‡ Input bias currents of a FET-input operational amplifier are normal junction reverse currents, which are temperature sensitive as shown in Figure 17. Pulse techniques must be used that will maintain the junction temperature as close to the ambient temperature as possible.

operating characteristics, $V_{CC\pm} = \pm15$ V, $T_A = 25°C$

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain (see Note 5)	V_I = 10 V, C_L = 100 pF,	R_L = 10 kΩ, See Figure 1	1.5	3.5		V/μs
t_r	Rise time	V_I = 20 mV,	R_L = 10 kΩ,		0.2		μs
	Overshoot factor	C_L = 100 pF,	See Figure 1		10%		
V_n	Equivalent input noise voltage	R_S = 100 Ω,	f = 1 kHz		42		nV/√Hz

NOTE 5: Slew rate at −55°C to 125°C is 0.7 V/μs min.

PARAMETER MEASUREMENT INFORMATION

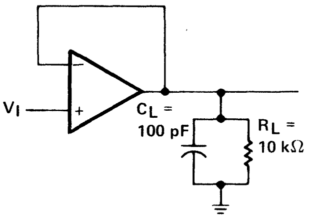


FIGURE 1. UNITY-GAIN AMPLIFIER

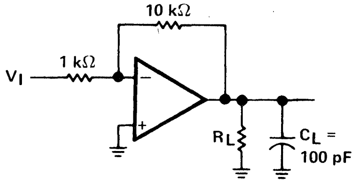


FIGURE 2. GAIN-OF-10 INVERTING AMPLIFIER

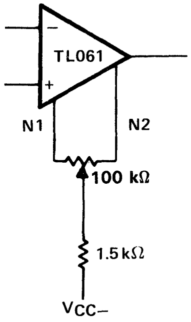


FIGURE 3. INPUT OFFSET VOLTAGE NULL CIRCUIT

TYPICAL CHARACTERISTICS†

MAXIMUM PEAK OUTPUT VOLTAGE
vs
SUPPLY VOLTAGE

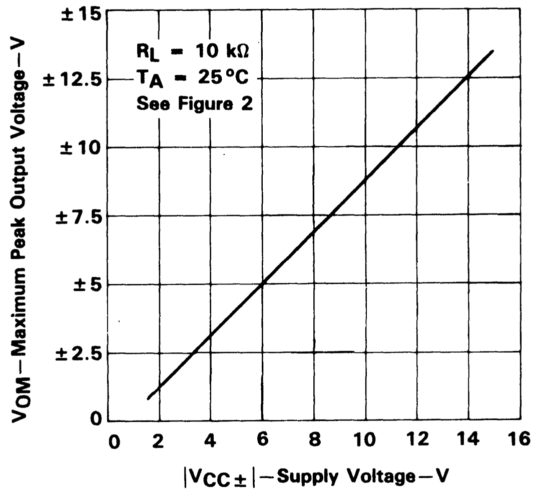


FIGURE 4

MAXIMUM PEAK OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

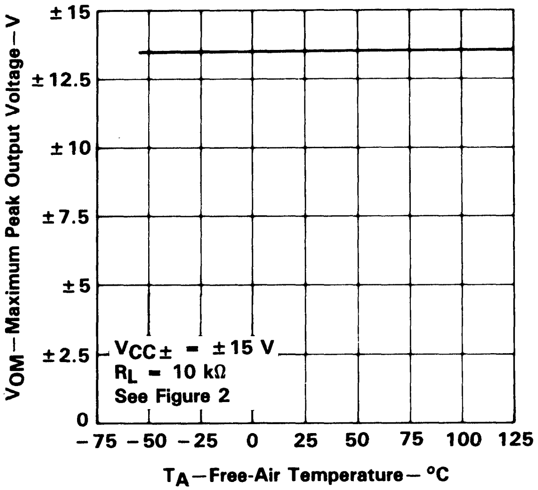


FIGURE 5

MAXIMUM PEAK OUTPUT VOLTAGE
vs
LOAD RESISTANCE

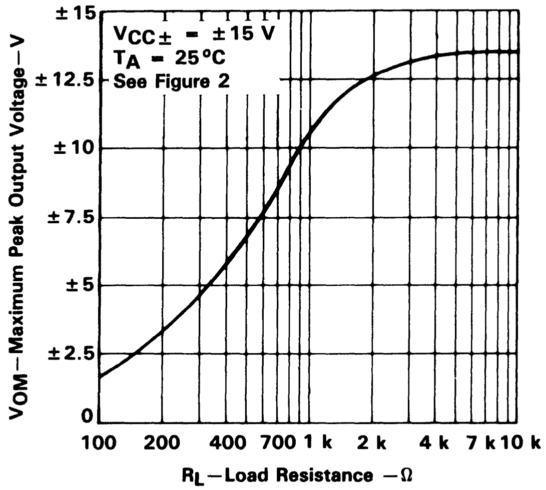


FIGURE 6

MAXIMUM PEAK OUTPUT VOLTAGE
vs
FREQUENCY

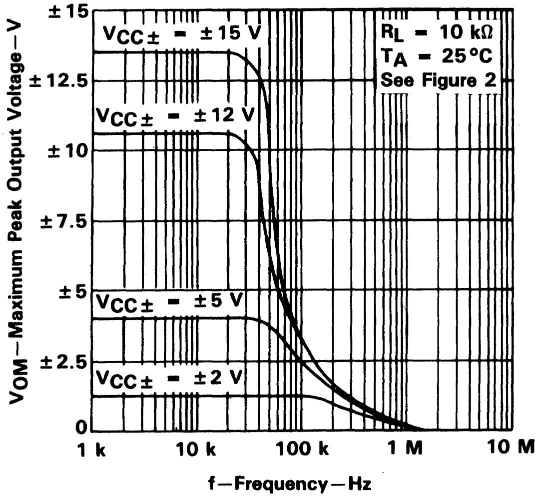


FIGURE 7

---

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

DIFFERENTIAL VOLTAGE AMPLIFICATION
vs
FREE-AIR TEMPERATURE

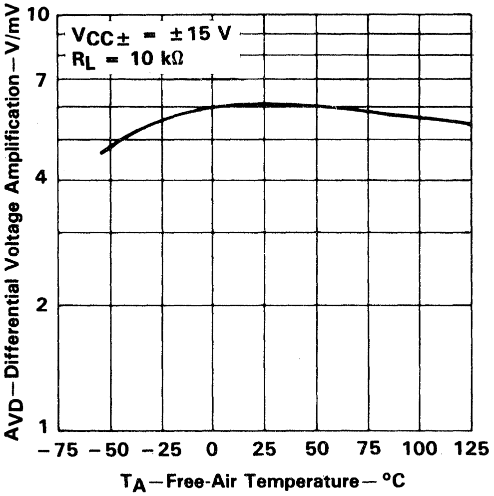


FIGURE 8

LARGE-SIGNAL
DIFFERENTIAL VOLTAGE AMPLIFICATION
AND PHASE SHIFT
vs
FREQUENCY

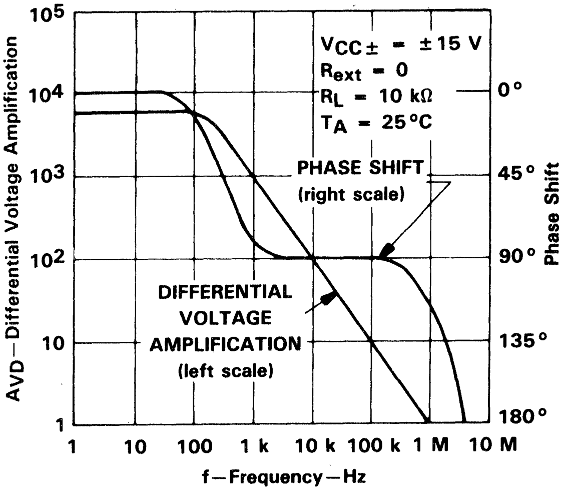


FIGURE 9

SUPPLY CURRENT
vs
SUPPLY VOLTAGE

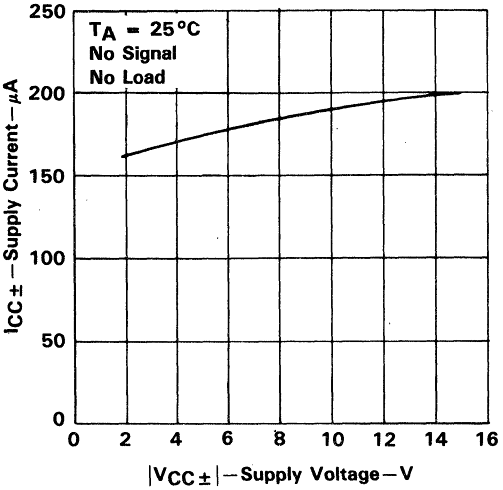


FIGURE 10

SUPPLY CURRENT
vs
FREE-AIR TEMPERATURE

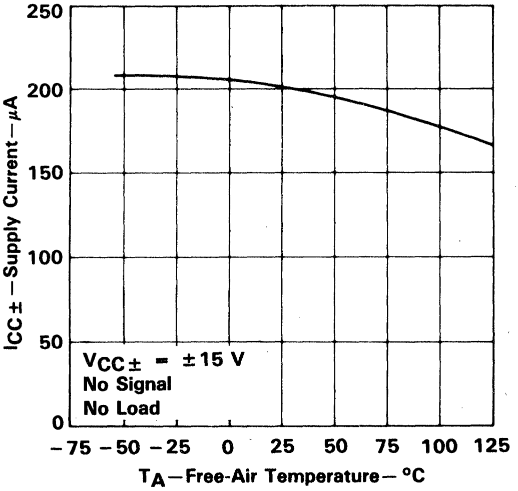


FIGURE 11

---

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

TOTAL POWER DISSIPATED
vs
FREE-AIR TEMPERATURE

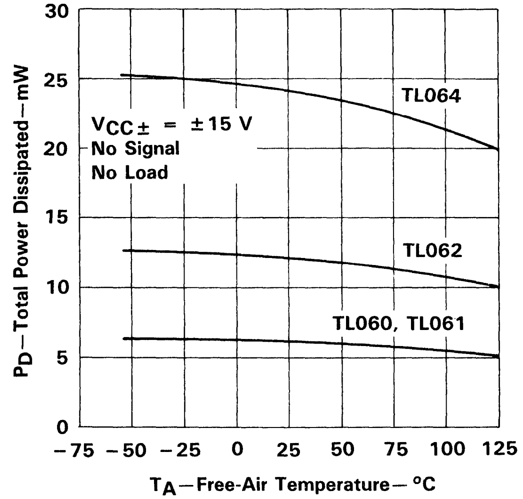


FIGURE 12

ALL EXCEPT TL06_C
COMMON-MODE REJECTION RATIO
vs
FREE-AIR TEMPERATURE

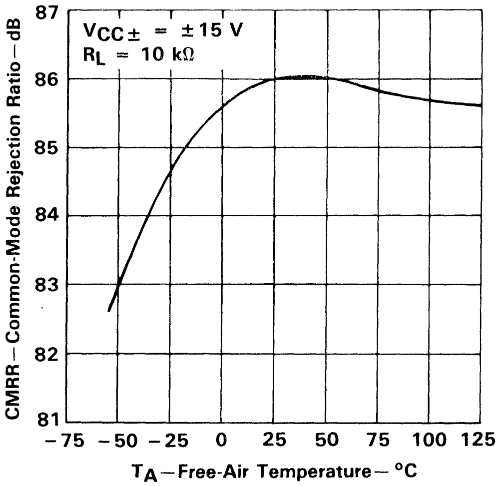


FIGURE 13

NORMALIZED UNITY GAIN BANDWIDTH
SLEW RATE, AND PHASE SHIFT
vs
FREE-AIR TEMPERATURE

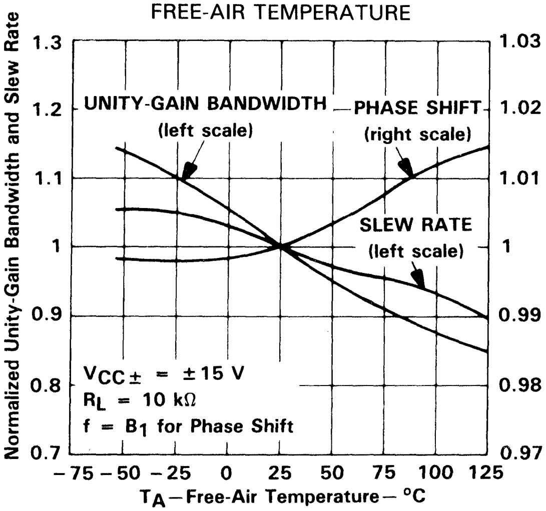


FIGURE 14

INPUT BIAS CURRENT
vs
FREE-AIR TEMPERATURE

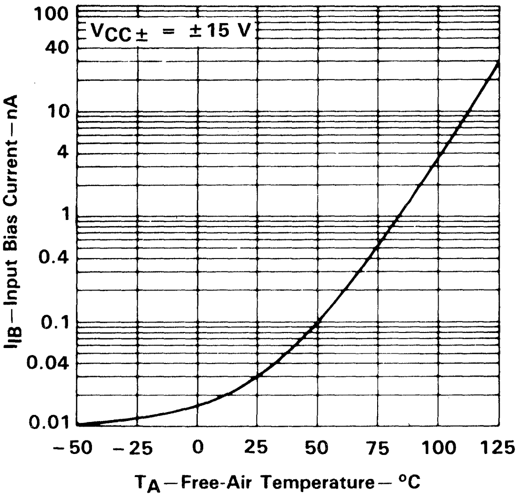


FIGURE 15

---

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

VOLTAGE FOLLOWER
LARGE SIGNAL PULSE RESPONSE

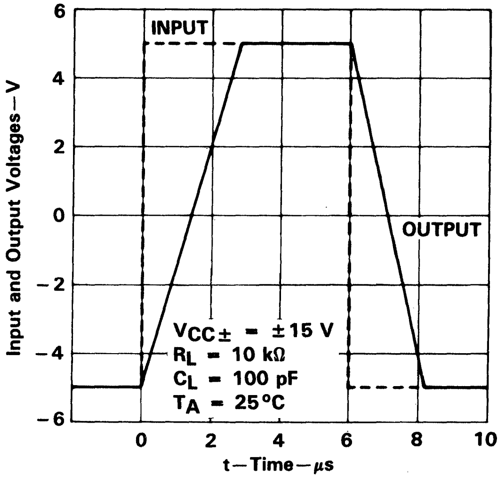


FIGURE 16

OUTPUT VOLTAGE
vs
ELAPSED TIME

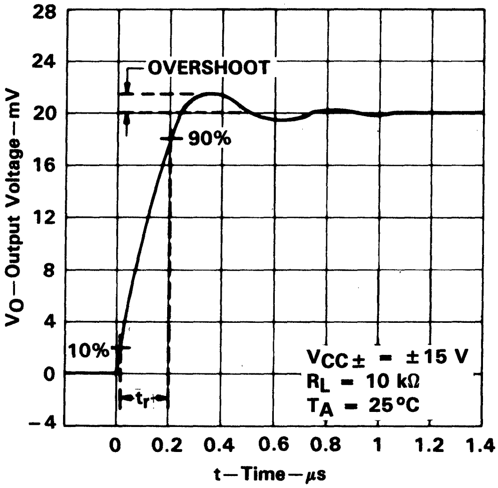


FIGURE 17

EQUIVALENT INPUT NOISE VOLTAGE
vs
FREQUENCY

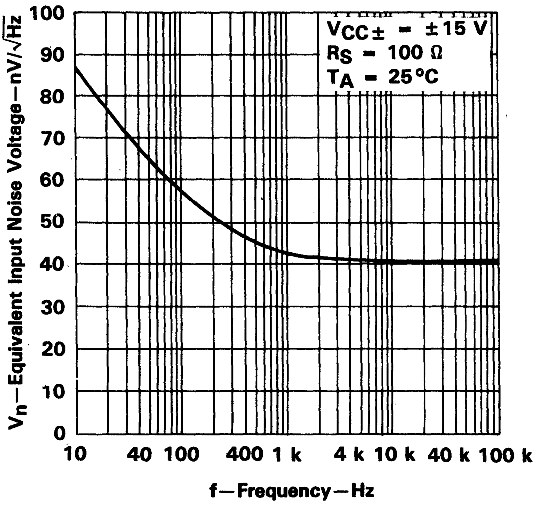


FIGURE 18

---

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL APPLICATION DATA

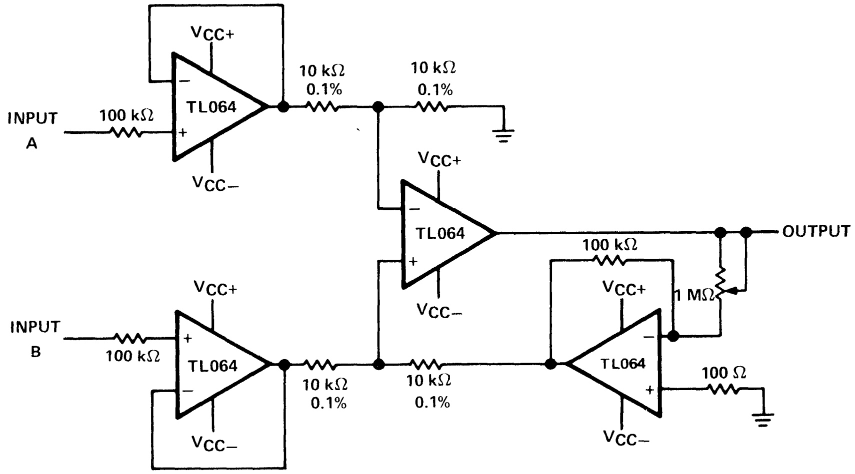
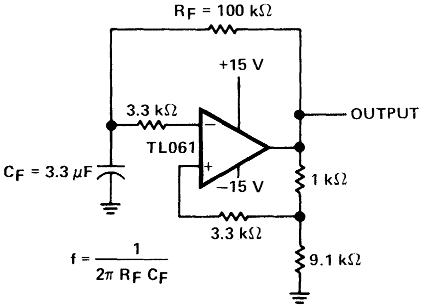
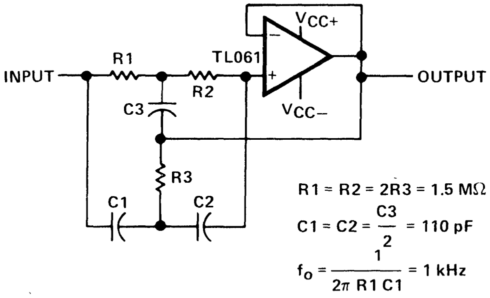


FIGURE 19. INSTRUMENTATION AMPLIFIER



$f = \frac{1}{2\pi R_F C_F}$

FIGURE 20. 0.5-Hz SQUARE-WAVE OSCILLATOR



$R1 = R2 = 2R3 = 1.5\ M\Omega$

$C1 = C2 = \frac{C3}{2} = 110\ pF$

$f_o = \frac{1}{2\pi\ R1\ C1} = 1\ kHz$

FIGURE 21. HIGH-Q NOTCH FILTER

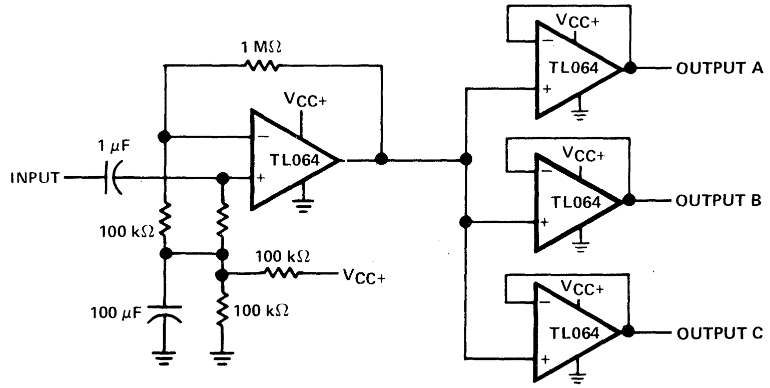


FIGURE 22. AUDIO DISTRIBUTION AMPLIFIER

TYPICAL APPLICATION DATA

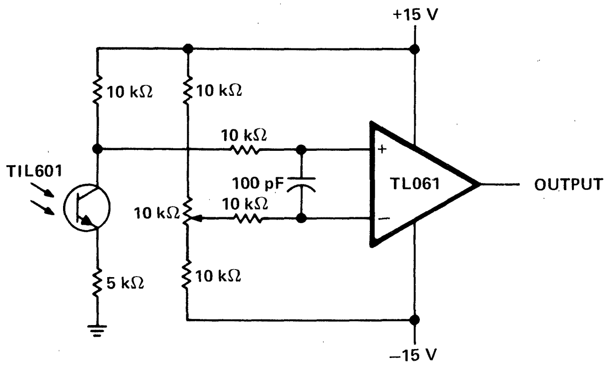


FIGURE 23. LOW-LEVEL LIGHT DETECTOR PREAMPLIFIER

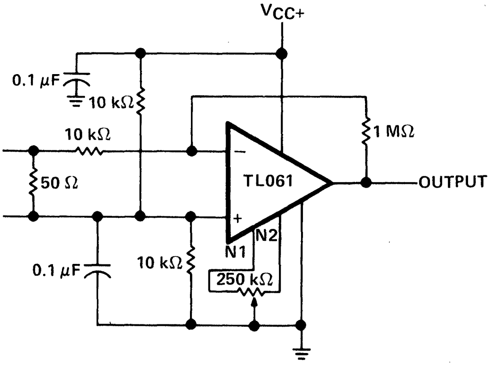


FIGURE 24. AC AMPLIFIER

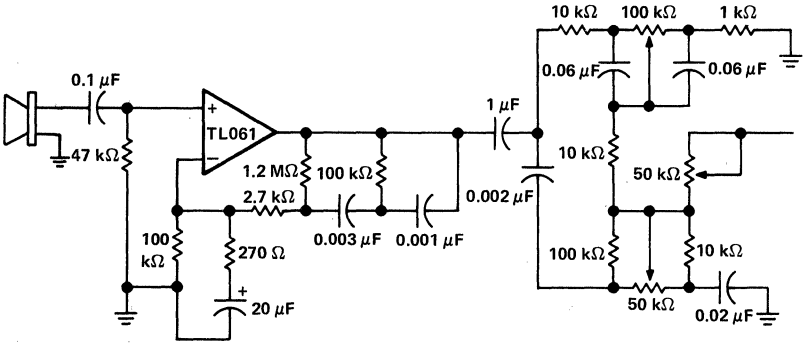


FIGURE 25. MICROPHONE PREAMPLIFIER WITH TONE CONTROL

TYPICAL APPLICATION DATA

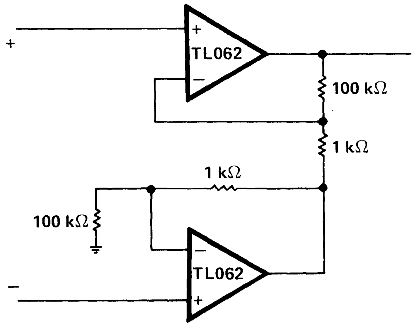


FIGURE 26. INSTRUMENTATION AMPLIFIER

IC PREAMPLIFIER RESPONSE CHARACTERISTICS

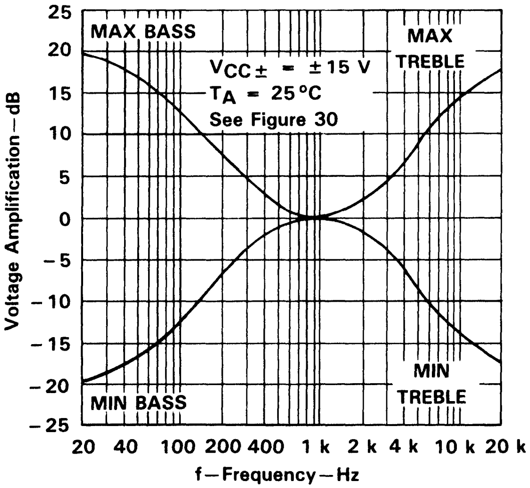


FIGURE 27

TYPICAL APPLICATION DATA

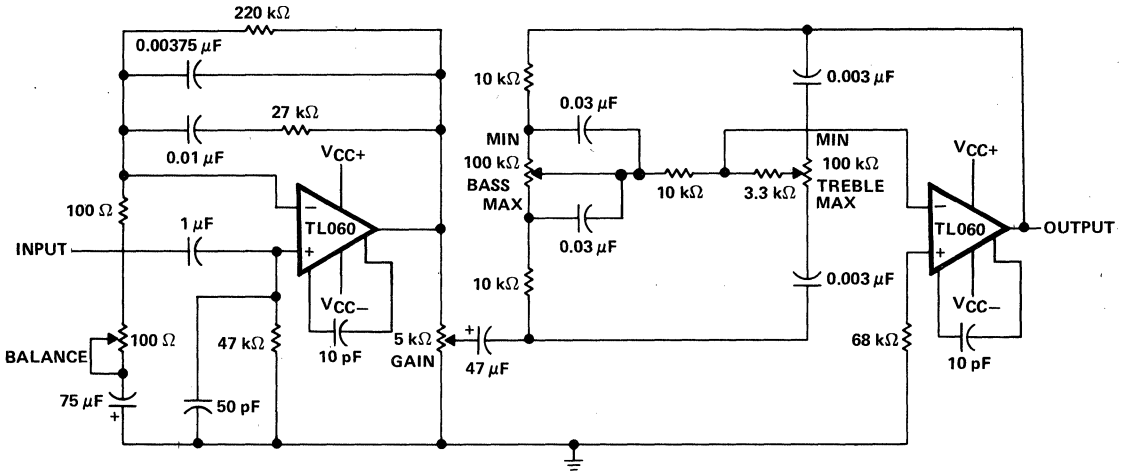


FIGURE 30. IC PREAMPLIFIER

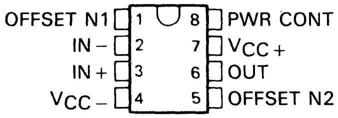
TL066AC, TL066C, TL066I, TL066M
ADJUSTABLE LOW-POWER JFET-INPUT OPERATIONAL AMPLIFIERS

D2494, FEBRUARY 1979—REVISED OCTOBER 1990

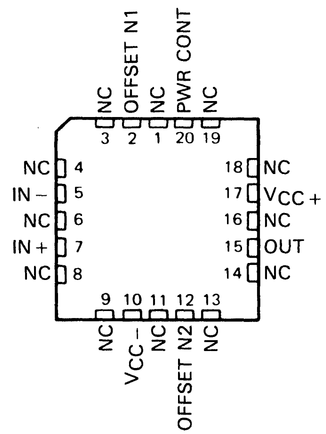
4 DEVICES COVER COMMERCIAL, INDUSTRIAL, AND MILITARY TEMPERATURE RANGES

- **Very Low, Adjustable ("Programmable") Power Consumption**
- **Adjustable Supply Current . . . 5 μA to 200 μA**
- **Very Low Input Bias and Offset Currents**
- **Wide Supply Range . . . ±1.2 V to ±18 V**
- **Wide Common-Mode and Differential Voltage Range**
- **Output Short-Circuit Protection**
- **High Input Impedance . . . JFET-Input Stage**
- **Unity-Gain Bandwidth . . . 1 MHz Typ (100 kHz at 25 μW)**
- **High Slew Rate . . . 3.5 V/μs Typ**
- **Internal Frequency Compensation**
- **Latch-Up-Free Operation**
- **Common-Mode Input Voltage Range Includes V_{CC+}**

TL066AC, TL066C, TL066I . . . D OR P PACKAGE
TL066M . . . JG PACKAGE
(TOP VIEW)



TL066M . . . FK PACKAGE
(TOP VIEW)



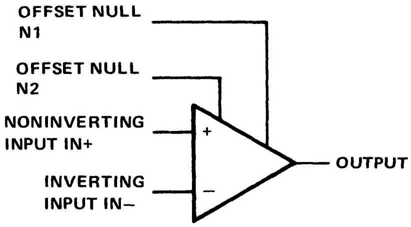
NC—No internal connection

TL066M IS NOT RECOMMENDED FOR NEW DESIGNS

description

The TL066 series are JFET-input operational amplifiers similar to the TL061 with the additional feature of being power-adjustable. They feature very low input offset and bias currents, high input impedance, wide bandwidth, and high slew rate. The power-control feature permits the amplifiers to be adjusted to require as little as 25 μW of power. This type of amplifier, which provides for changing several characteristics by varying one external element, is sometimes referred to as being "programmable." The JFET-input stage combined with the adjustable-low-power feature results in superior bandwidth and slew-rate performance compared to low-power bipolar-input devices.

symbol



The TL066AC and TL066C are characterized for operation from 0°C to 70°C. The TL066I is characterized for operation from −40°C to 85°C; the TL066M is characterized for operation over the full military temperature range of −55°C to 125°C.

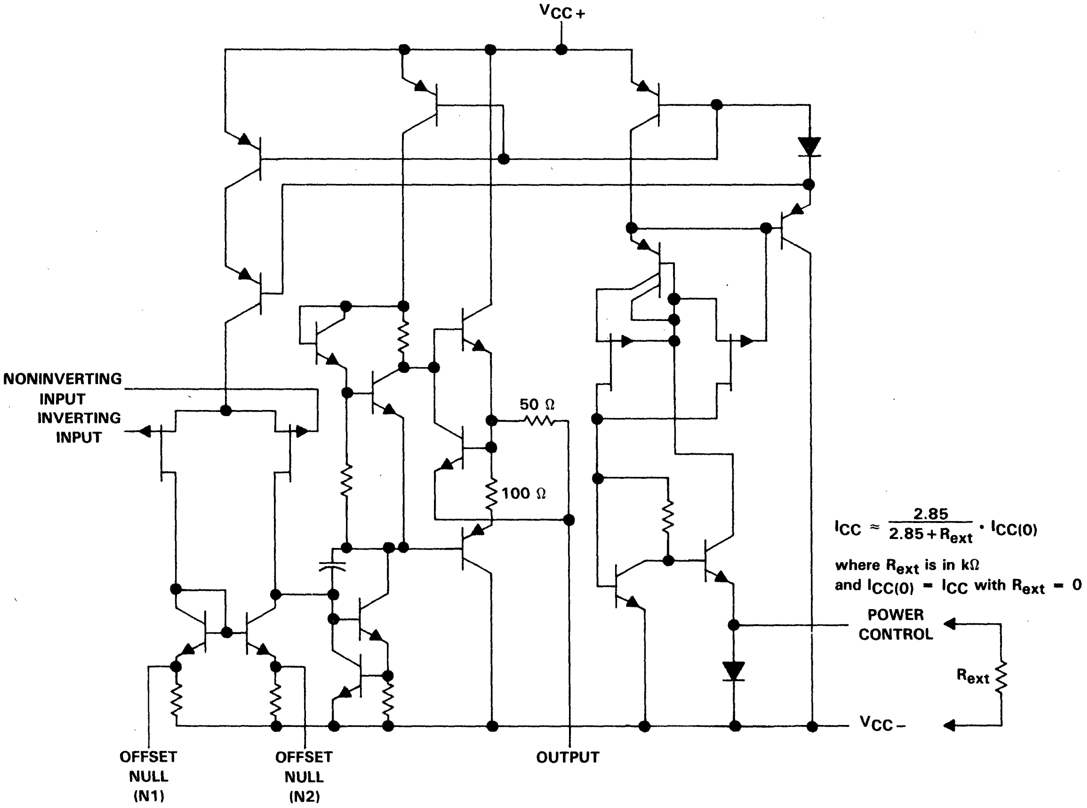
TEXAS INSTRUMENTS
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

AVAILABLE OPTIONS

T_A	V_{IO} MAX AT 25°C	PACKAGE			
		SMALL-OUTLINE (D)	CHIP-CARRIER (FK)	CERAMIC DIP (JG)	PLASTIC DIP (P)
0°C to 70°C	15 mV 6 mV	TL066CD TL066ACD			TL066CP TL066ACP
−40°C to 85°C	6 mV	TL066ID			TL066IP
−55°C to 125°C	6 mV		TL066MFK	TL066MJG	

The D package is available taped and reeled. Add the suffix "R" to the device type, (e.g., TL066CDR).

schematic



$$I_{CC} \approx \frac{2.85}{2.85 + R_{ext}} \cdot I_{CC(0)}$$

where R_{ext} is in kΩ
and $I_{CC(0)} = I_{CC}$ with $R_{ext} = 0$

Component values shown are nominal.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

		TL066AC, TL066C	TL066I	TL066M	UNIT
Supply voltage, V_{CC+} (see Note 1)		18	18	18	V
Supply voltage, V_{CC-} (see Note 1)		−18	−18	−18	V
Differential input voltage (see Note 2)		±30	±30	±30	V
Input voltage (see Notes 1 and 3)		±15	±15	±15	V
Voltage between power-control terminal and V_{CC-}		±0.5	±0.5	±0.5	V
Duration of output short circuit (see Note 4)		unlimited	unlimited	unlimited	
Continuous total dissipation		See Dissipation Rating Table			
Operating free-air temperature range		0 to 70	−40 to 85	−55 to 125	°C
Storage temperature range		−65 to 150	−65 to 150	−65 to 150	°C
Case temperature for 60 seconds	FK package			260	°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds	JG package			300	°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	D or P package	260	260		°C

NOTES: 1. All voltage values, except differential voltages, are with respect to the midpoint between V_{CC+} and V_{CC-}.
2. Differential voltages are at the noninverting input terminal with respect to the inverting input terminal.
3. The magnitude of the input voltage must never exceed the magnitude of the supply voltage or 15 V, whichever is less.
4. The output may be shorted to ground or to either supply. Temperature and/or supply voltages must be limited to ensure that the dissipation rating is not exceeded.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR	DERATE ABOVE T_A	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING	$T_A = 125°C$ POWER RATING
D	680 mW	5.8 mW/°C	33°C	464 mW	377 mW	N/A
FK	680 mW	11.0 mW/°C	88°C	680 mW	680 mW	275 mW
JG	680 mW	8.4 mW/°C	69°C	672 mW	546 mW	210 mW
P	680 mW	8.0 mW/°C	65°C	640 mW	520 mW	N/A

electrical characteristics, V_{CC} = ±15 V

PARAMETER		TEST CONDITIONS†	TL066C MIN	TL066C TYP	TL066C MAX	TL066I MIN	TL066I TYP	TL066I MAX	TL066M MIN	TL066M TYP	TL066M MAX	UNIT
V_{IO}	Input offset voltage	V_O = 0, R_S = 50 Ω, T_A = 25°C		3	15		3	6		3	6	mV
		V_O = 0, R_S = 50 Ω, T_A = full range			20			9			9	
α_{VIO}	Temperature coefficient of input offset voltage	V_O = 0, R_S = 50 Ω, T_A = full range		10			10			10		µV/°C
I_{IO}	Input offset current‡	V_O = 0, T_A = 25°C		5	200		5	100		5	100	pA
		V_O = 0, T_A = full range			5			10			20	nA
I_{IB}	Input bias current‡	V_O = 0, T_A = 25°C		30	400		30	200		30	200	pA
		V_O = 0, T_A = full range			10			20			50	nA
V_{ICR}	Common-mode input voltage range	T_A = 25°C	±11	−12 to +15		±11.5	−12 to +15		±11.5	−12 to +15		V
V_{OM}	Maximum peak output voltage swing	T_A = 25°C, R_L ≥ 10 kΩ	±10	±13.5		±10	±13.5		±10	±13.5		V
		T_A = full range, R_L ≥ 10 kΩ	±10	±13.5		±10	±13.5		±10	±13.5		
A_{VD}	Large-signal differential voltage amplification	R_L ≥ 10 kΩ, V_O = ±10 V, T_A = 25°C	3	6		4	6		4	6		V/mV
		R_L ≥ 10 kΩ, V_O = ±10 V, T_A = full range	3						4			
B_1	Unity-gain bandwidth	T_A = 25°C, R_L = 10 kΩ		1			1			1		MHz
r_i	Input resistance	T_A = 25°C		10^{12}			10^{12}			10^{12}		Ω
r_o	Output resistance	T_A = 25°C, f = 1 kHz		220			220			220		Ω
CMRR	Common-mode rejection ratio	V_{IC} = V_{ICR} min, V_O = 0, R_S = 50 Ω, T_A = 25°C	70	76		80	86		80	86		dB
k_{SVR}	Supply voltage rejection ratio ($\Delta V_{CC\pm}/\Delta V_{IO}$)	V_{CC} = ±9 V to ±15 V, V_O = 0, R_S = 50 Ω, T_A = 25°C	70	95		80	95		80	95		dB
P_D	Total power dissipation	V_O = 0, No load, T_A = 25°C		6	7.5		6	7.5		6	7.5	mW
I_{CC}	Supply current	V_O = 0, No load, T_A = 25°C		200	250		200	250		200	250	µA

† All characteristics are measured under open-loop conditions with zero common-mode input voltage unless otherwise specified. Full range of T_A is 0°C to 70°C for TL066C; −40°C to 85°C for TL066I; and −55°C to 125°C for TL066M. The electrical parameters are measured with the power-control terminal (pin 8) connected to V_{CC-}.

‡ Input bias currents of a FET-input operational amplifier are normal junction reverse currents, which are temperature-sensitive. Pulse techniques must be used that will maintain the junction temperature as close to the ambient temperature as possible.

electrical characteristics, V_{CC} = ±15 V

PARAMETER		TEST CONDITIONS†	TL066AC			UNIT
			MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_O = 0, R_S = 50 Ω, T_A = 25°C		3	6	mV
		V_O = 0, R_S = 50 Ω, $_A$ = full range			7.5	
α_{VIO}	Temperature coefficient of input offset voltage	V_O = 0, R_S = 50 Ω, T_A = full range		10		μV/°C
I_{IO}	Input offset current‡	V_O = 0, T_A = 25°C		5	100	pA
		V_O = 0, T_A = full range			3	nA
I_{IB}	Input bias current‡	V_O = 0, T_A = 25°C		30	200	pA
		V_O = 0, T_A = full range			7	nA
V_{ICR}	Common-mode input voltage range	T_A = 25°C	±11.5	−12 to ±15		V
V_{OM}	Maximum peak output voltage swing	T_A = 25°C, R_L ≥ 10 kΩ,	±10	±13.5		V
		T_A = full range, R_L ≥ 10 kΩ	±10	±13.5		
A_{VD}	Large-signal differential voltage amplification	R_L ≥ 10 kΩ, V_O = ±10 V, T_A = 25°C	4	6		V/mV
		R_L ≥ 10 kΩ, V_O = ±10 V, T_A = full range	4			
B_1	Unity-gain bandwidth	T_A = 25°C, R_L = 10 kΩ		1		MHz
r_i	Input resistance	T_A = 25°C		10^{12}		Ω
r_o	Output resistance	T_A = 25°C, f = 1 kHz		220		Ω
CMRR	Common-mode rejection ratio	V_{IC} = V_{ICR} min, V_O = 0, R_S = 50 Ω, T_A = 25°C	80	86		dB
k_{SVR}	Supply voltage rejection ratio ($\Delta V_{CC\pm}/\Delta V_{IO}$)	V_{CC} = ±9 V to ±15 V, V_O = 0, R_S = 50 Ω, T_A = 25°C	80	95		dB
P_D	Total power dissipation	No load, V_O = 0, T_A = 25°C		6	7.5	mW
I_{CC}	Supply current	No load, V_O = 0, T_A = 25°C		200	250	μA

† All characteristics are measured under open-loop conditions with zero common-mode input voltage unless otherwise specified. Full range of T_A is 0°C to 70°C. The electrical parameters are measured with the power-control terminal connected to V_{CC-}.

‡ Input bias currents of a FET-input operational amplifier are normal junction reverse currents, which are temperature-sensitive. Pulse techniques must be used that will maintain the junction temperature as close to the ambient temperature as possible.

operating characteristics, $V_{CC\pm}$ = ±15 V, T_A = 25°C, R_{ext} = 0

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain	V_I = 10 V, C_L = 100 pF,	R_L = 10 kΩ, See Figure 1	1.5	3.5		V/μs
t_r	Rise time	V_I = 20 mV,	R_L = 10 kΩ		0.2		μs
	Overshoot factor	C_L = 100 pF,	See Figure 1		10%		
V_n	Equivalent input noise voltage	R_S = 100 Ω,	f = 1 kHz		42		nV/√Hz

PARAMETER MEASUREMENT INFORMATION

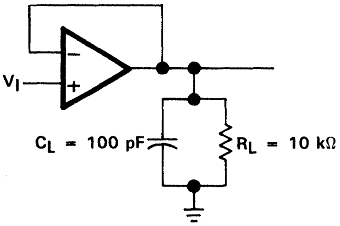


FIGURE 1. UNITY-GAIN AMPLIFIER

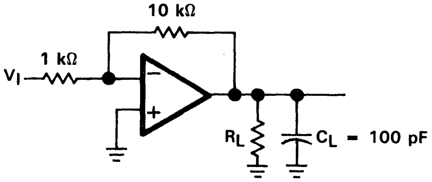


FIGURE 2. GAIN-OF-10 INVERTING AMPLIFIER

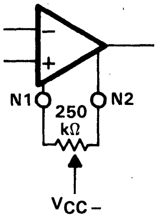
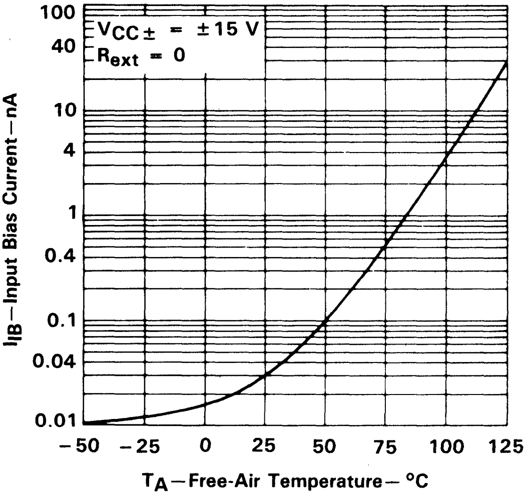


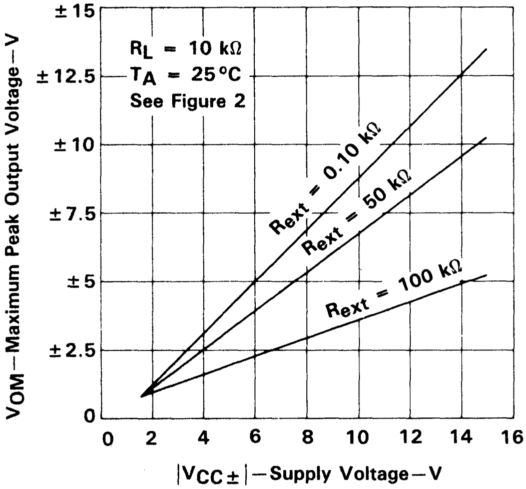
FIGURE 3. INPUT OFFSET VOLTAGE NULL CIRCUIT

TYPICAL CHARACTERISTICS†



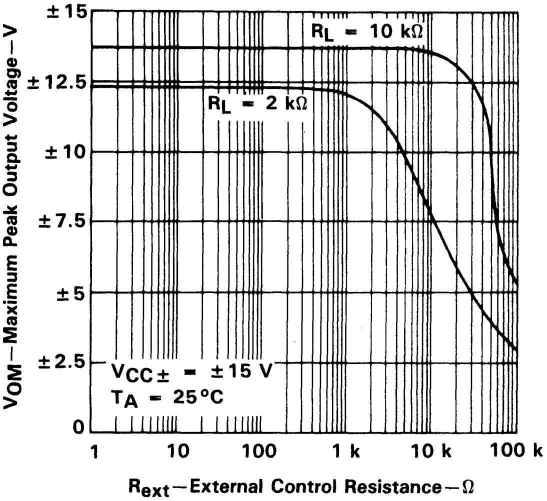
INPUT BIAS CURRENT
vs
FREE-AIR TEMPERATURE

FIGURE 4



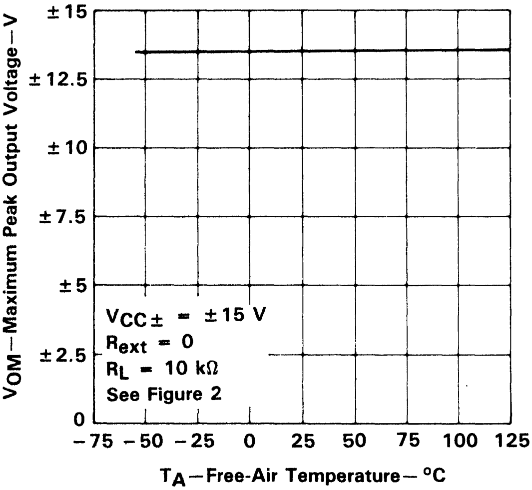
MAXIMUM PEAK OUTPUT VOLTAGE
vs
SUPPLY VOLTAGE

FIGURE 5



MAXIMUM PEAK OUTPUT VOLTAGE
vs
EXTERNAL CONTROL RESISTANCE

FIGURE 6



MAXIMUM PEAK OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

FIGURE 7

---

† Data at high and low temperatures are applicable only within the rated free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS[†]

MAXIMUM PEAK OUTPUT VOLTAGE
vs
LOAD RESISTANCE

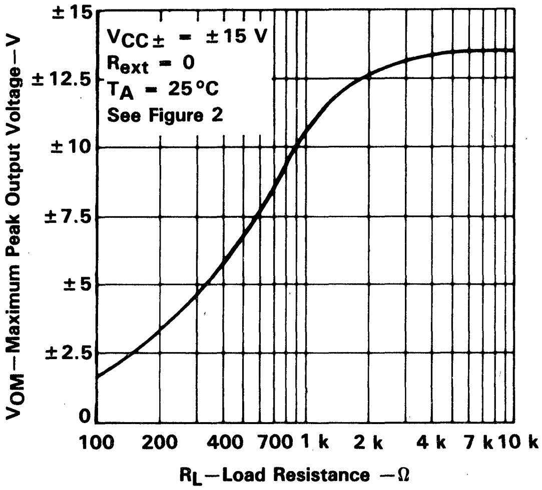


FIGURE 8

MAXIMUM PEAK OUTPUT VOLTAGE
vs
FREQUENCY

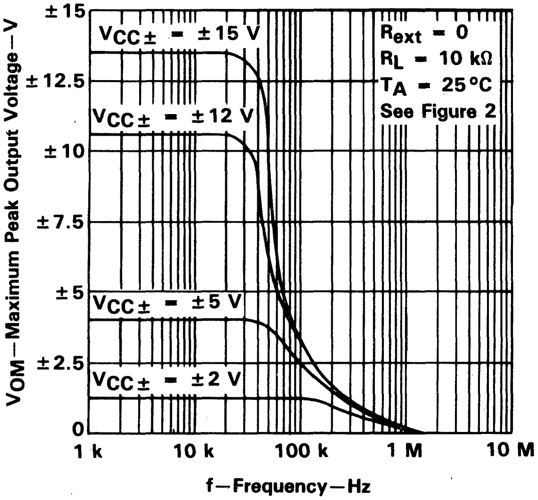


FIGURE 9

DIFFERENTIAL VOLTAGE AMPLIFICATION
vs
EXTERNAL CONTROL RESISTANCE

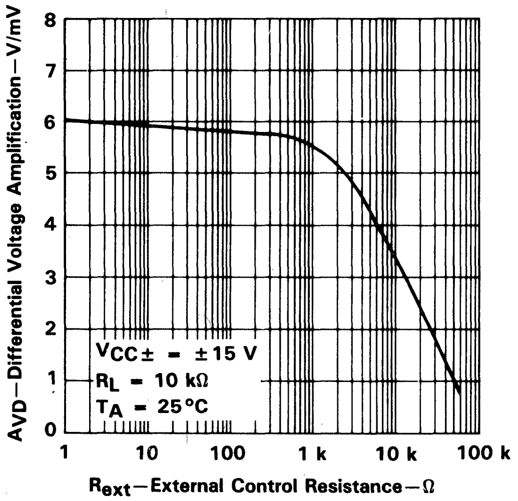


FIGURE 10

DIFFERENTIAL VOLTAGE AMPLIFICATION
vs
FREE-AIR TEMPERATURE

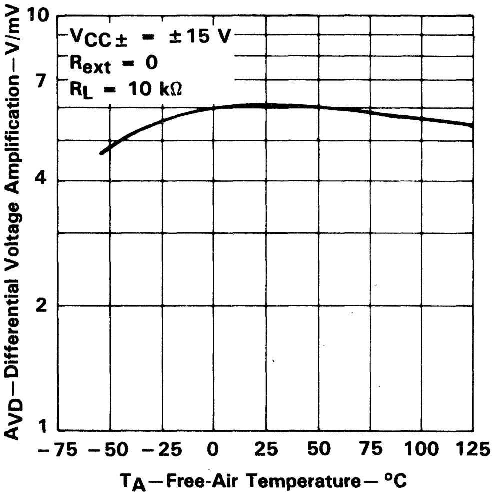


FIGURE 11

[†] Data at high and low temperatures are applicable only within the rated free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

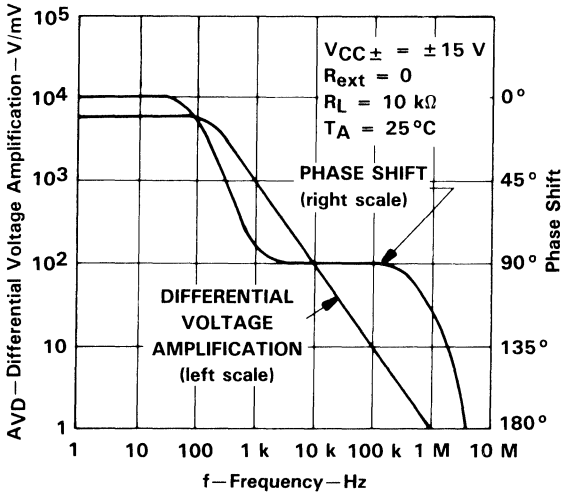

LARGE SIGNAL
DIFFERENTIAL VOLTAGE AMPLIFICATION
AND PHASE SHIFT
vs
FREQUENCY

FIGURE 12

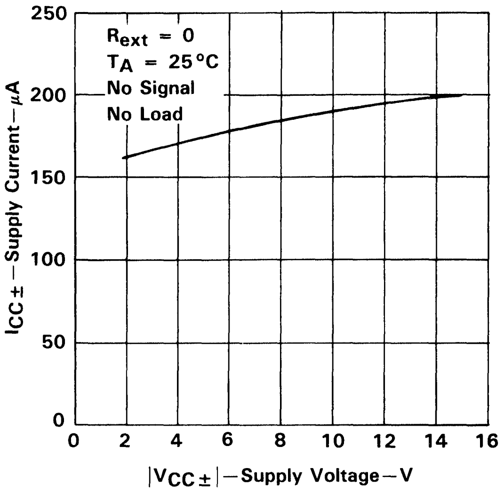

SUPPLY CURRENT
vs
SUPPLY VOLTAGE

FIGURE 13

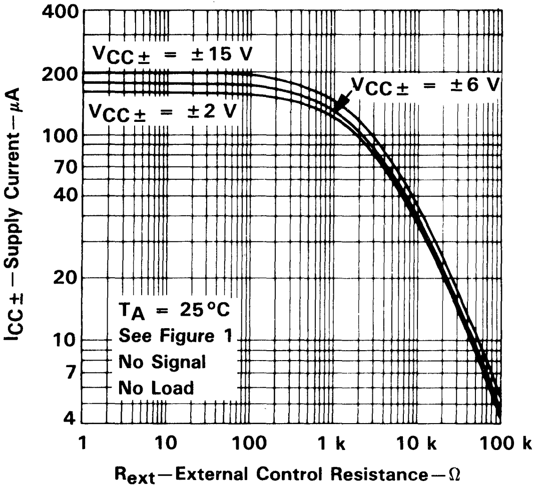

SUPPLY CURRENT
vs
EXTERNAL CONTROL RESISTANCE

FIGURE 14

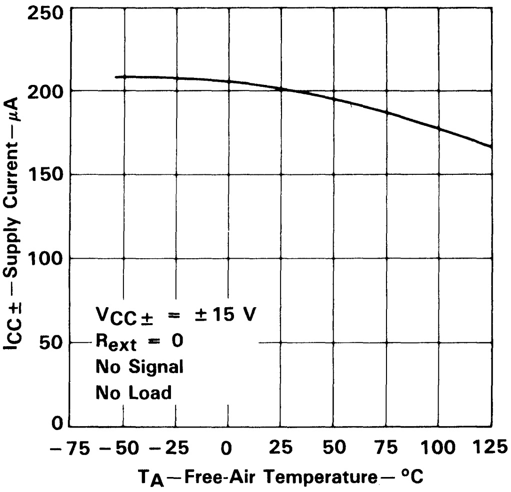

SUPPLY CURRENT
vs
FREE-AIR TEMPERATURE

FIGURE 15

---

†Data at high and low temperatures are applicable only within the rated free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

TOTAL POWER DISSIPATION
vs
EXTERNAL CONTROL RESISTANCE

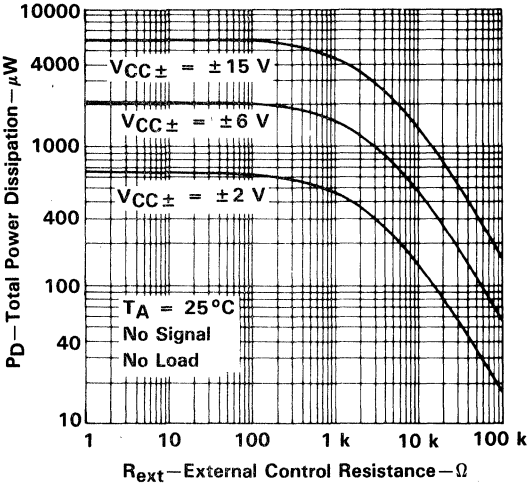


FIGURE 16

ALL EXCEPT TL066C
COMMON-MODE REJECTION RATIO
vs
EXTERNAL CONTROL RESISTANCE

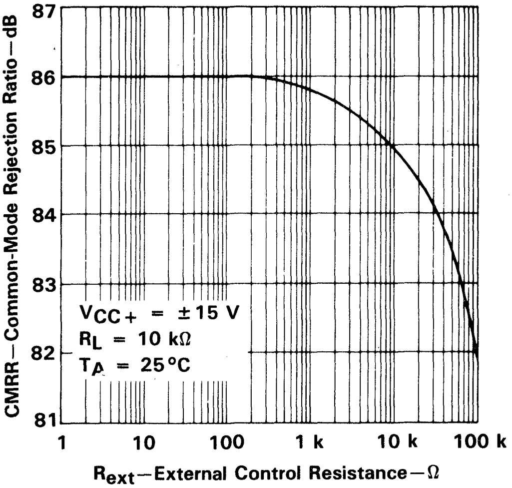


FIGURE 17

ALL EXCEPT TL066C
COMMON-MODE REJECTION RATIO
vs
FREE-AIR TEMPERATURE

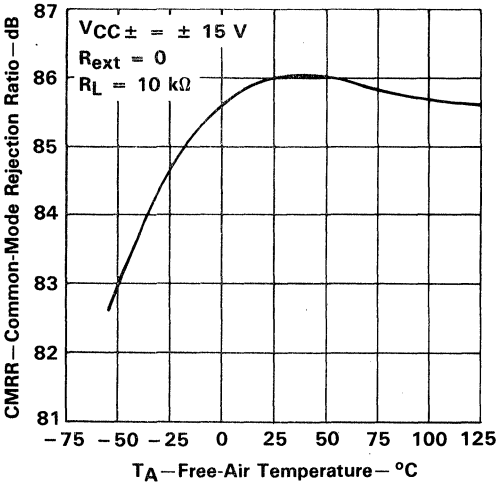


FIGURE 18

EQUIVALENT INPUT NOISE VOLTAGE
vs
FREQUENCY

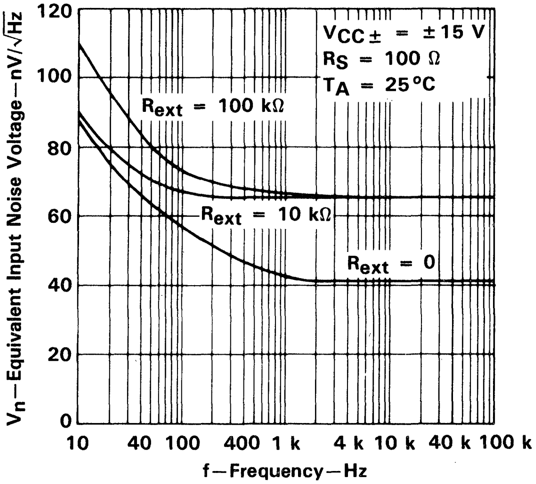


FIGURE 19

---

†Data at high and low temperatures are applicable only within the rated free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

EQUIVALENT INPUT NOISE VOLTAGE
vs
SOURCE RESISTANCE

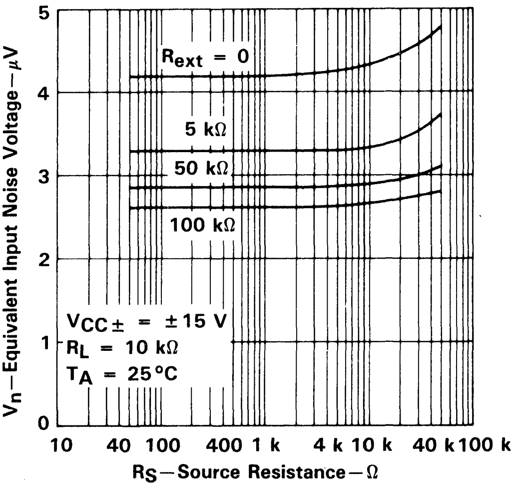


FIGURE 20

UNITY GAIN BANDWIDTH
vs
EXTERNAL CONTROL RESISTANCE

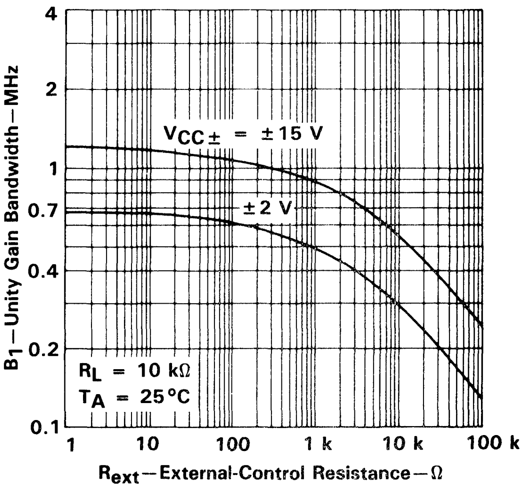


FIGURE 21

SLEW RATE
vs
EXTERNAL CONTROL RESISTANCE

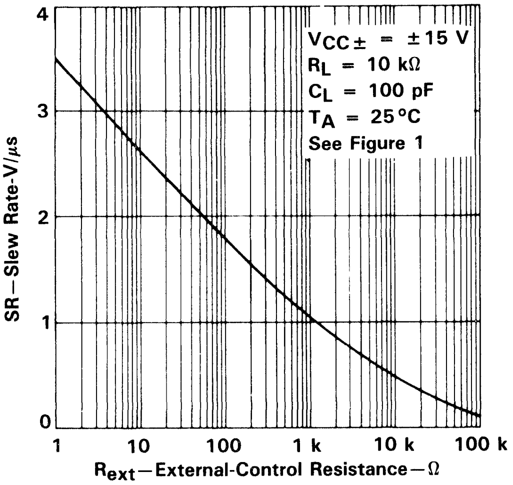


FIGURE 22

NORMALIZED UNITY GAIN BANDWIDTH
SLEW RATE, AND PHASE SHIFT
vs
FREE-AIR TEMPERATURE

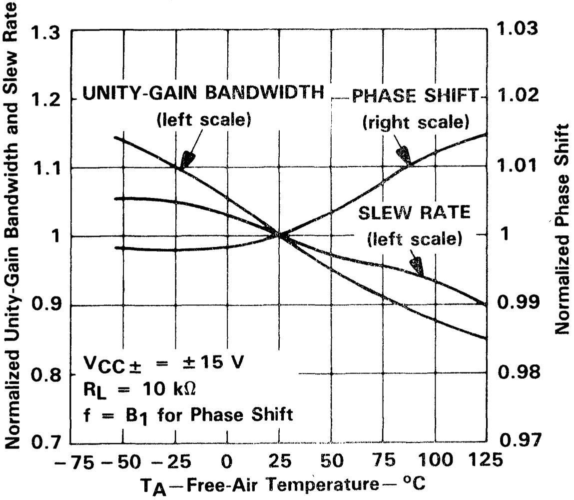


FIGURE 23

---

†Data at high and low temperatures are applicable only within the rated free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

VOLTAGE FOLLOWER
LARGE SIGNAL PULSE RESPONSE

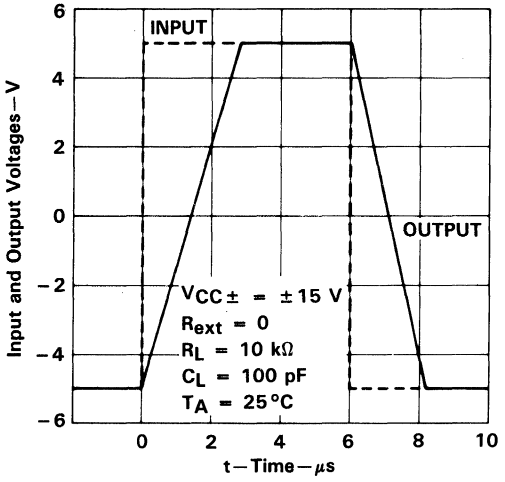


FIGURE 24

OUTPUT VOLTAGE
vs
ELAPSED TIME

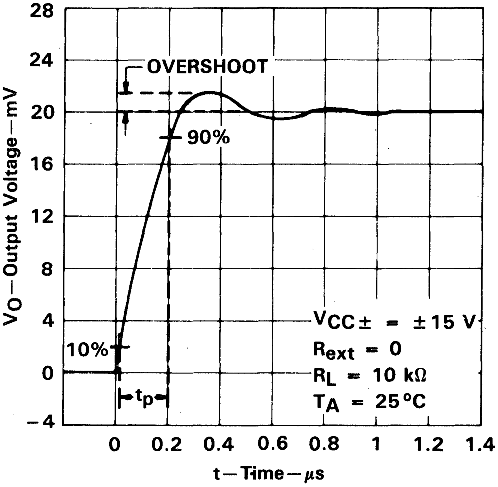


FIGURE 25

†Data at high and low temperatures are applicable only within the rated free-air temperature ranges of the various devices.

TYPICAL APPLICATION DATA

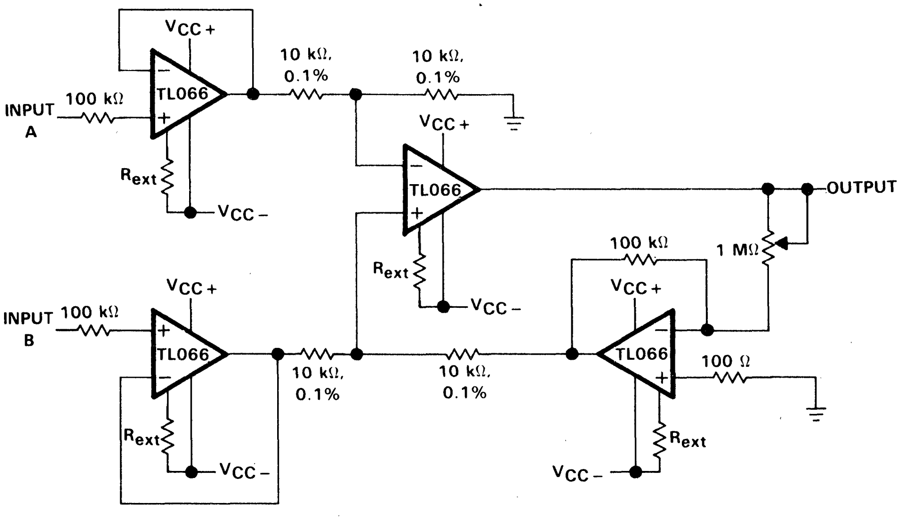


FIGURE 26. INSTRUMENTATION AMPLIFIER

TYPICAL APPLICATION DATA

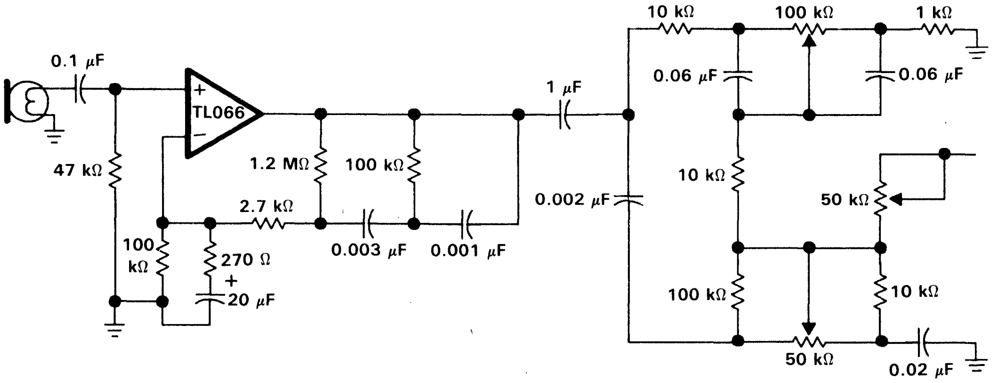


FIGURE 27. MICROPHONE PREAMPLIFIER WITH TONE CONTROL

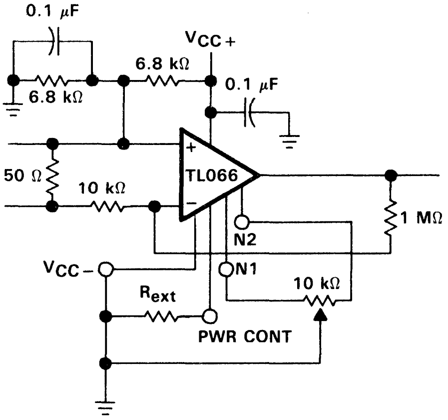


FIGURE 28. AC AMPLIFIER

TYPICAL APPLICATION DATA

IC PREAMPLIFIER RESPONSE CHARACTERISTICS

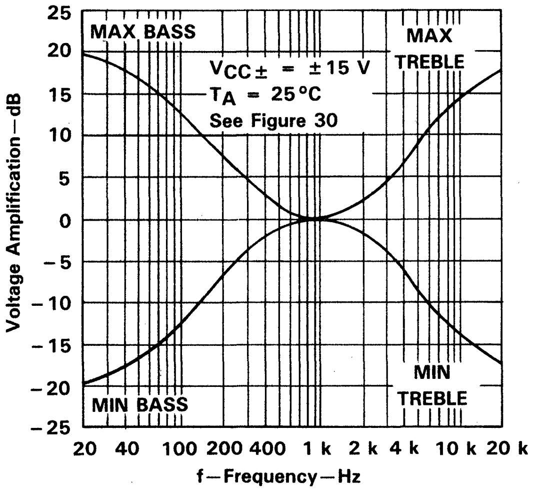


FIGURE 29

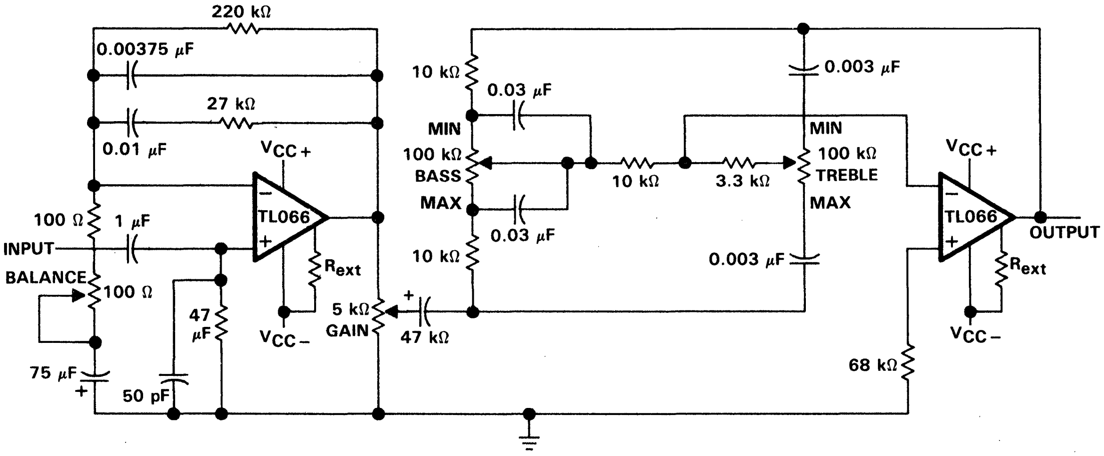


FIGURE 30. IC PREAMPLIFIER

TL070, TL071, TL071A, TL071B
TL072, TL072A, TL072B, TL074, TL074A, TL074B
LOW-NOISE JFET-INPUT OPERATIONAL AMPLIFIERS

D2393, SEPTEMBER 1978—REVISED SEPTEMBER 1990

19 DEVICES COVER COMMERCIAL, INDUSTRIAL, AND MILITARY TEMPERATURE RANGES

- Low Power Consumption
- Wide Common-Mode and Differential Voltage Ranges
- Low Input Bias and Offset Currents
- Output Short-Circuit Protection
- Low Total Harmonic Distortion . . . 0.003% Typ
- Common-Mode Input Voltage Range Includes V_{CC+}
- Low Noise . . . V_n = 18 nV/$\sqrt{Hz}$ Typ
- High Input Impedance . . . JFET-Input Stage
- Internal Frequency Compensation (Except TL070)
- Latch-Up-Free Operation
- High Slew Rate . . . 13 V/μs Typ

description

The JFET-input operational amplifiers in the TL07__ series are designed as low-noise versions of the TL08__ series amplifiers with low input bias and offset currents and fast slew rate. The low harmonic distortion and low noise make the TL07__ series ideally suited as amplifiers for high-fidelity and audio preamplifier applications. Each amplifier features JFET-inputs (for high input impedance) coupled with bipolar output stages all integrated on a single monolithic chip.

The C suffix devices are characterized for operation from 0°C to 70°C. The I suffix devices are characterized for operation from −40°C to 85°C. The M suffix devices are characterized for operation over the full military temperature range of −55°C to 125°C.

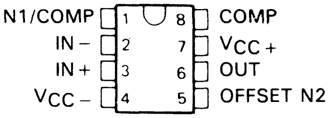
AVAILABLE OPTIONS

T_A	V_{IO} MAX AT 25°C	PACKAGE							
		SMALL OUTLINE (D)	CHIP CARRIER (FK)	CERAMIC DIP (J)	CERAMIC DIP (JG)	METAL CAN (L)	PLASTIC DIP (N)	PLASTIC DIP (P)	FLAT PACK (W)
0°C to 70°C	10 mV	TL070CD						TL070CP	
	10 mV	TL071CD						TL071CP	
	6 mV	TL071ACD						TL071ACP	
	3 mV	TL071BCD						TL071BCP	
	10 mV	TL072CD						TL072CP	
	6 mV	TL072ACD						TL072ACP	
	3 mV	TL072BCD						TL072BCP	
	10 mV	TL074CD					TL074CN		
	6 mV	TL074ACD					TL074ACN		
	3 mV	TL074BCD					TL074BCN		
−40°C to 85°C	6 mV	TL071ID						TL071IP	
	6 mV	TL072ID						TL072P	
	6 mV	TL074ID					TL074IN		
−55°C to 125°C	6 mV		TL071MFK		TL071MJG	TL071ML			
	6 mV		TL072MFK		TL072MJG	TL072ML			
	9 mV		TL074MFK	TL074MJ					TL074MW

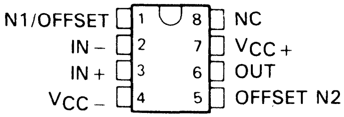
The D package is available taped and reeled. Add the suffix R to the device type (e.g., TL071CDR).

TEXAS INSTRUMENTS
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

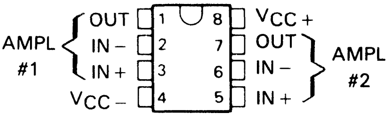
TL070
D OR P PACKAGE
(TOP VIEW)



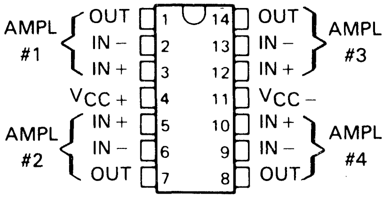
TL071, TL071A, TL071B
D, JG, OR P PACKAGE
(TOP VIEW)



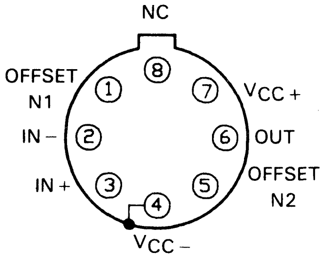
TL072, TL072A, TL072B
D, JG, OR P PACKAGE
(TOP VIEW)



TL074, TL074A, TL074B
D, J, OR N PACKAGE
TL074 . . . W PACKAGE
(TOP VIEW)

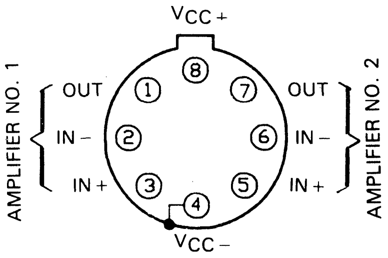


TL071 . . . L PACKAGE
(TOP VIEW)



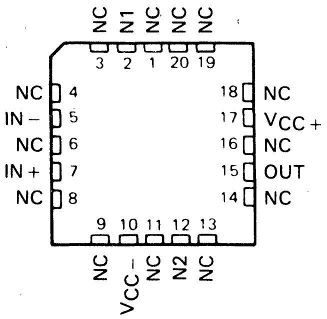
PIN 4 IS IN ELECTRICAL CONTACT
WITH THE CASE

TL072 . . . L PACKAGE
(TOP VIEW)

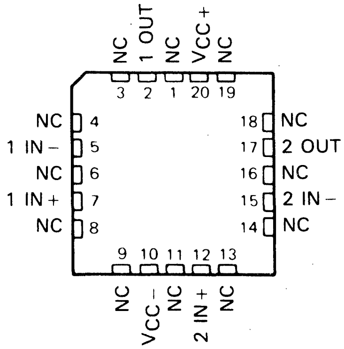


PIN 4 IS IN ELECTRICAL CONTACT
WITH THE CASE

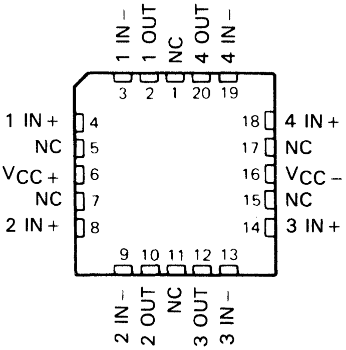
TL071
FK PACKAGE
(TOP VIEW)



TL072
FK PACKAGE
(TOP VIEW)

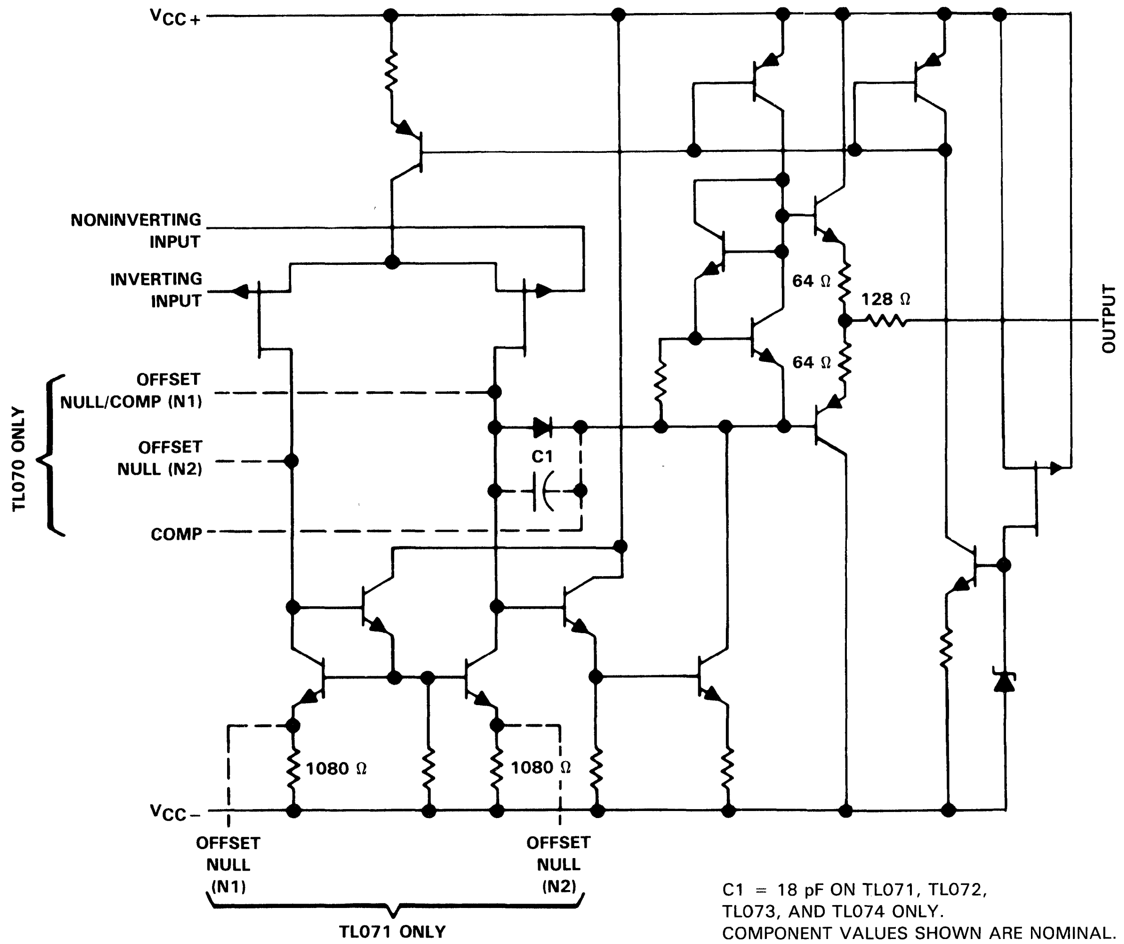


TL074
FK PACKAGE
(TOP VIEW)



NC—No internal connection

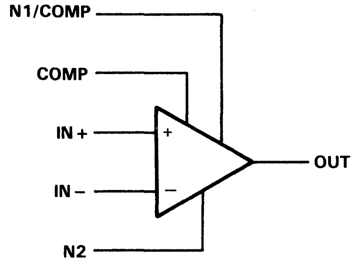
schematic (each amplifier)



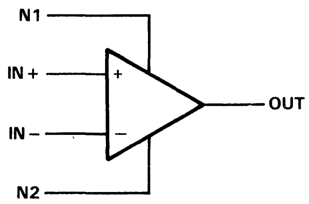
C1 = 18 pF ON TL071, TL072,
TL073, AND TL074 ONLY.
COMPONENT VALUES SHOWN ARE NOMINAL.

symbols

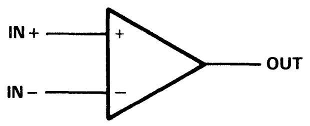
TL070



TL071



TL072 (EACH AMPLIFIER)
TL074 (EACH AMPLIFIER)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

		TL07__C TL07__AC TL07__BC	TL07__I	TL07__M	UNIT
Supply voltage, V_{CC+} (see Note 1)		18	18	18	V
Supply voltage, V_{CC-} (see Note 1)		−18	−18	−18	V
Differential input voltage (see Note 2)		±30	±30	±30	V
Input voltage (see Notes 1 and 3)		±15	±15	±15	V
Duration of output short circuit (see Note 4)		unlimited	unlimited	unlimited	
Continuous total dissipation		See Dissipation Rating Table			
Operating free-air temperature range		0 to 70	−40 to 85	−55 to 125	°C
Storage temperature range		−65 to 150	−65 to 150	−65 to 150	°C
Case temperature for 60 seconds	FK package			260	°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds	J, JG, or W package			300	°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	D, N, or P package	260	260		°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	L package			300	°C

NOTES: 1. All voltage values, except differential voltages, are with respect to the midpoint between V_{CC+} and V_{CC-}.
2. Differential voltages are at the noninverting input terminal with respect to the inverting input terminal.
3. The magnitude of the input voltage must never exceed the magnitude of the supply voltage or 15 V, whichever is less.
4. The output may be shorted to ground or to either supply. Temperature and/or supply voltages must be limited to ensure that the dissipation rating is not exceeded.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR	DERATE ABOVE T_A	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING	$T_A = 125°C$ POWER RATING
D (8-pin)	680 mW	5.8 mW/°C	33°C	464 mW	377 mW	N/A
D (14-pin)	680 mW	7.6 mW/°C	60°C	608 mW	494 mW	N/A
FK	680 mW	11.0 mW/°C	88°C	680 mW	680 mW	275 mW
J	680 mW	11.0 mW/°C	88°C	680 mW	680 mW	275 mW
JG	680 mW	8.4 mW/°C	69°C	672 mW	546 mW	210 mW
L	680 mW	6.6 mW/°C	25°C	528 mW	429 mW	165 mW
N	680 mW	9.2 mW/°C	76°C	680 mW	598 mW	N/A
P	680 mW	8.0 mW/°C	65°C	640 mW	520 mW	N/A
W	680 mW	8.0 mW/°C	65°C	640 mW	520 mW	200 mW

electrical characteristics, $V_{CC\pm}$ = ±15 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		TL071M TL072M			TL074M			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_O = 0,	T_A = 25°C		3	6		3	9	mV
		R_S = 50 Ω,	T_A = −55°C to 125°C			9			15	
αV_{IO}	Temperature coefficient of input offset voltage	V_O = 0, R_S = 50 Ω, T_A = −55°C to 125°C			18			18		µV/°C
I_{IO}	Input offset current‡	V_O = 0	T_A = 25°C		5	100		5	100	pA
			T_A = −55°C to 125°C			20			20	nA
I_{IB}	Input bias current	V_O = 0	T_A = 25°C		65	200		65	200	pA
			T_A = −55°C to 125°C			50			50	nA
V_{ICR}	Common-mode input voltage range	T_A = 25°C		±11	−12 to +15		±11	−12 to +15		V
V_{OM}	Maximum peak output voltage swing	R_L = 10 kΩ	T_A = 25°C	±12	±13.5		±12	±13.5		V
		R_L ≥ 10 kΩ	T_A = −55°C to 125°C	±12			±12			
		R_L ≥ 2 kΩ		±10			±10			
A_{VD}	Large-signal differential voltage amplification	V_O = ±10 V,	T_A = 25°C	35	200		35	200		V/mV
		R_L ≥ 2 kΩ	T_A = −55°C to 125°C	15			15			
B_1	Unity-gain bandwidth	T_A = 25°C			3			3		MHz
r_i	Input resistance	T_A = 25°C			10^{12}			10^{12}		Ω
CMRR	Common-mode rejection ratio	V_{IC} = V_{ICR} min, V_O = 0, R_S = 50 Ω, T_A = 25°C		80	86		80	86		dB
k_{SVR}	Supply voltage rejection ratio ($\Delta V_{CC\pm}/\Delta V_{IO}$)	V_{CC} = ±15 V to ±9 V, V_O = 0, R_S = 50 Ω, T_A = 25°C		80	86		80	86		dB
I_{CC}	Supply current (each amplifier)	No load, V_O = 0, T_A = 25°C			1.4	2.5		1.4	2.5	mA
V_{O1}/V_{O2}	Crosstalk attenuation	A_{VD} = 100, T_A = 25°C			120			120		dB

---

† All characteristics are measured under open-loop conditions with zero common-mode voltage unless otherwise specified.

‡ Input bias currents of a FET-input operational amplifier are normal junction reverse currents, which are temperature sensitive as shown in Figure 6. Pulse techniques must be used that will maintain the junction temperature as close to the ambient temperature as possible.

electrical characteristics, $V_{CC\pm} = \pm15$ V (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		TL070C TL071C TL072C TL074C			TL071AC TL072AC TL074AC			TL071BC TL072BC TL074BC			TL071I TL072I TL074I			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	$V_O = \Omega$, $R_S = 50\ \Omega$	$T_A = 25°C$		3	10		3	6		2	3		3	6	mV
			T_A = full range			13			7.5			5			8	
$\alpha_{V_{IO}}$	Temperature coefficient of input offset voltage	$V_O = 0$, $R_S = 50\ \Omega$, T_A = full range			18			18			18			18		µV/°C
I_{IO}	Input offset current‡	$V_O = 0$	$T_A = 25°C$		5	100		5	100		5	100		5	100	pA
			T_A = full range			10			2			2			2	nA
I_{IB}	Input bias current‡	$V_O = 0$	$T_A = 25°C$		65	200		65	200		65	200		65	200	pA
			T_A = full range			7			7			7			20	nA
V_{ICR}	Common-mode input voltage range	$T_A = 25°C$		±11	−12 to +15		±11	−12 to +15		±11	−12 to +15		±11	−12 to +15		V
V_{OM}	Maximum peak output voltage swing	$R_L = 10\ k\Omega$	$T_A = 25°C$	±12	±13.5		±12	±13.5		±12	±13.5		±12	±13.5		V
		$R_L \geq 10\ k\Omega$	T_A = full range	±12			±12			±12			±12			
		$R_L \geq 2\ k\Omega$		±10			±10			±10			±10			
A_{VD}	Large-signal differential voltage amplification	$V_O = \pm10$ V, $R_L \geq 2\ k\Omega$	$T_A = 25°C$	25	200		50	200		50	200		50	200		V/mV
			T_A = full range	15			25			25			25			
B_1	Unity-gain bandwidth	$T_A = 25°C$			3			3			3			3		MHz
r_i	Input resistance	$T_A = 25°C$			10^{12}			10^{12}			10^{12}			10^{12}		Ω
CMRR	Common-mode rejection ratio	$V_{IC} = V_{ICR}$ min, $V_O = 0$, $R_S = 50\ \Omega$, $T_A = 25°C$		70	100		80	100		80	100		80	100		dB
k_{SVR}	Supply voltage rejection ratio ($\Delta V_{CC\pm}/\Delta V_{IO}$)	$V_{CC} = \pm15$ V to ±9 V, $V_O = 0$, $R_S = 50\ \Omega$, $T_A = 25°C$		70	100		80	100		80	100		80	100		dB
I_{CC}	Supply current (each amplifier)	No load, $V_O = 0$, $T_A = 25°C$			1.4	2.5		1.4	2.5		1.4	2.5		1.4	2.5	mA
V_{o1}/V_{o2}	Crosstalk attenuation	$A_{VD} = 100$, $T_A = 25°C$			120			120			120			120		dB

[†] All characteristics are measured under open-loop conditions with zero common-mode voltage unless otherwise specified. Full range for T_A is 0°C to 70°C for TL07__C, TL07__AC, TL07__BC and −40°C to 85°C for TL07__I.

[‡] Input bias currents of a FET-input operational amplifier are normal junction reverse currents, which are temperature sensitive as shown in Figure 6. Pulse techniques must be used that will maintain the junction temperature as close to the ambient temperature as possible.

operating characteristics, $V_{CC\pm} = \pm 15$ V, $T_A = 25°C$

PARAMETER		TEST CONDITIONS		TL07_M			ALL OTHERS			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
SR	Slew rate at unity gain	$V_I = 10$ V, $C_L = 100$ pF,	$R_L = 2$ kΩ, See Figure 1	5	13		8	13		V/μs
t_r	Rise time	$V_I = 20$ mV, $C_L = 100$ pF,	$R_L = 2$ kΩ, See Figure 1		0.1			0.1		μs
	overshoot factor				20			20		%
V_n	Equivalent input noise voltage	$R_S = 100$ Ω	f = 1 kHz		18			18		nV/√Hz
			f = 10 Hz to 10 kHz		4			4		μV
I_n	Equivalent input noise current	$R_S = 100$ Ω,	f = 1 kHz		0.01			0.01		pA/√Hz
THD	Total harmonic distortion	$V_{O(rms)} = 10$ V, $R_L \geq 2$ kΩ,	$R_S \leq 1$ kΩ, f = 1 kHz		0.003			0.003		%

PARAMETER MEASUREMENT INFORMATION

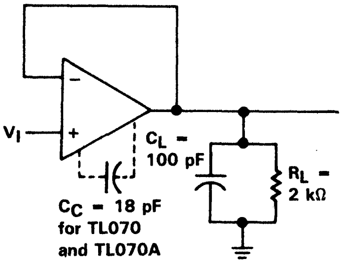


FIGURE 1. UNITY-GAIN AMPLIFIER

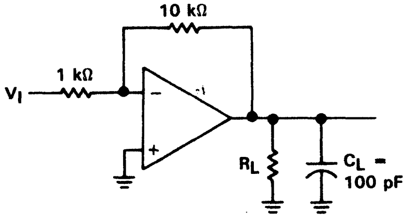


FIGURE 2. GAIN-OF-10 INVERTING AMPLIFIER

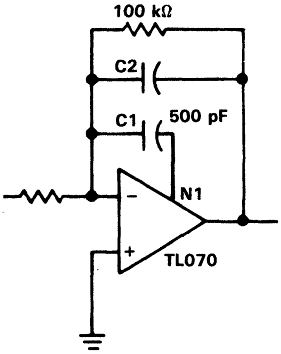


FIGURE 3. FEED-FORWARD COMPENSATION

INPUT OFFSET VOLTAGE NULL CIRCUITS

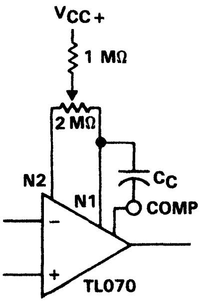


FIGURE 4

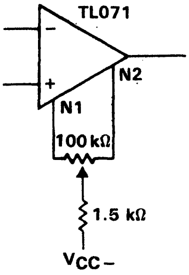


FIGURE 5

TYPICAL CHARACTERISTICS†

INPUT BIAS CURRENT
vs
FREE-AIR TEMPERATURE

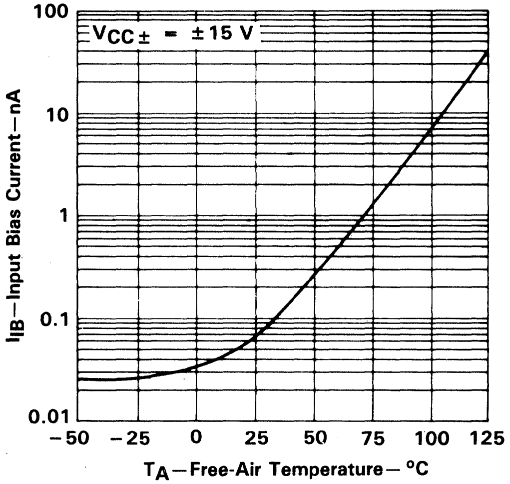


FIGURE 6

MAXIMUM PEAK OUTPUT VOLTAGE
vs
FREQUENCY

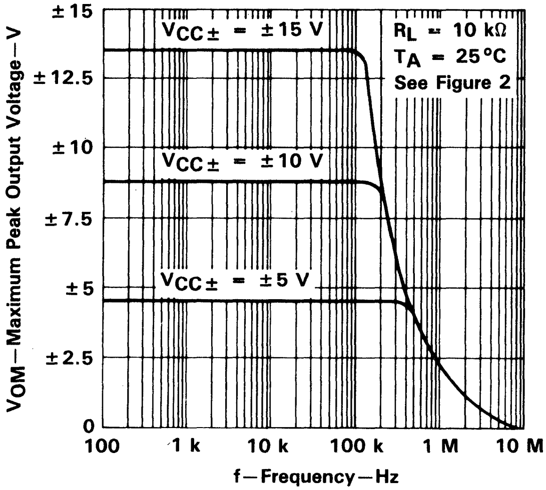


FIGURE 7

MAXIMUM PEAK OUTPUT VOLTAGE
vs
FREQUENCY

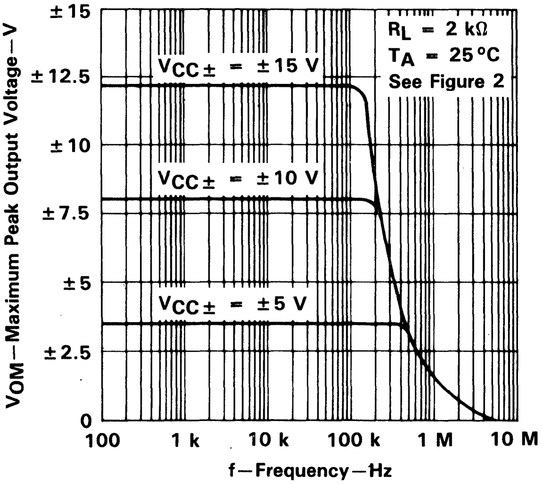


FIGURE 8

MAXIMUM PEAK OUTPUT VOLTAGE
vs
FREQUENCY

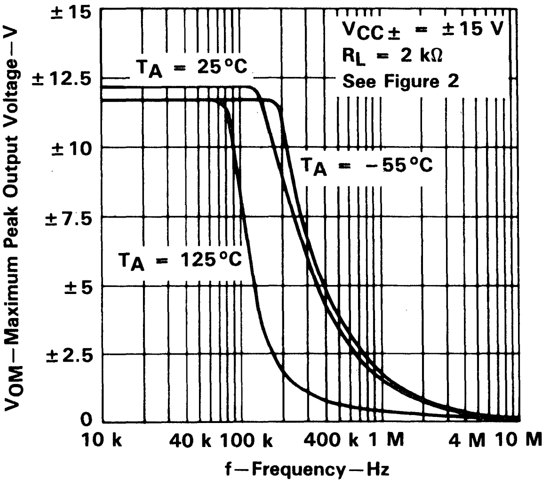


FIGURE 9

---

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices. An 18-pF compensation capacitor is used with TL070.

TYPICAL CHARACTERISTICS†

MAXIMUM PEAK OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

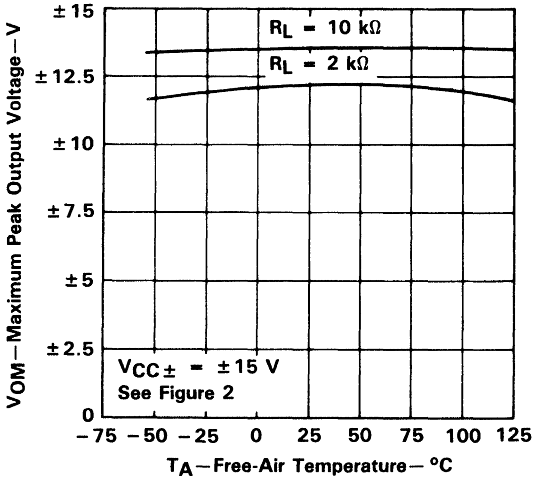


FIGURE 10

MAXIMUM PEAK OUTPUT VOLTAGE
vs
LOAD RESISTANCE

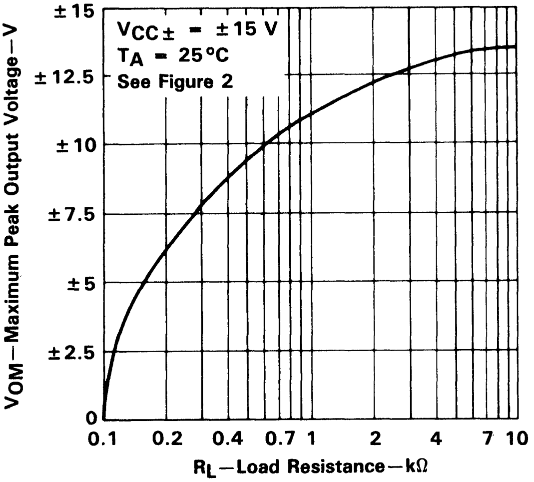


FIGURE 11

MAXIMUM PEAK OUTPUT VOLTAGE
vs
SUPPLY VOLTAGE

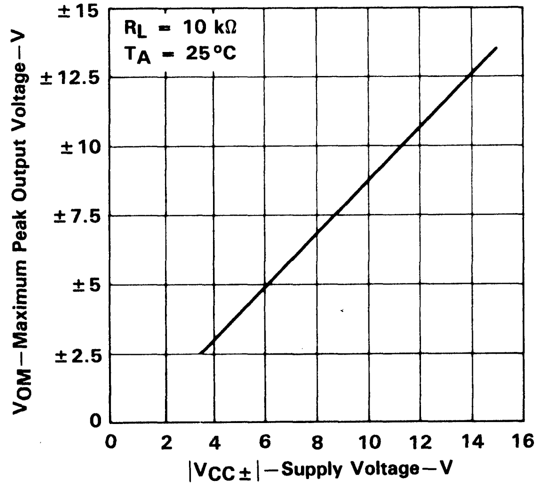


FIGURE 12

LARGE-SIGNAL
DIFFERENTIAL VOLTAGE AMPLIFICATION
vs
FREE-AIR TEMPERATURE

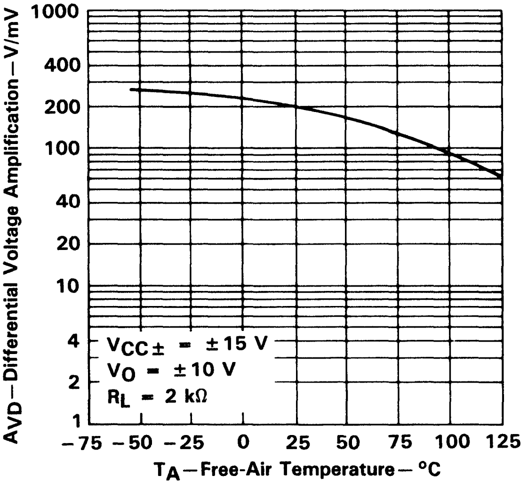


FIGURE 13

---

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices. An 18-pF compensation capacitor is used with TL070.

TYPICAL CHARACTERISTICS†

TL070
DIFFERENTIAL VOLTAGE AMPLIFICATION vs FREQUENCY WITH FEED-FORWARD COMPENSATION

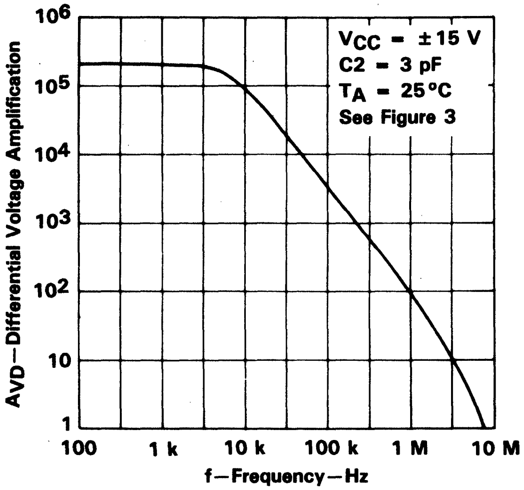


FIGURE 14

LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION and PHASE SHIFT vs FREQUENCY

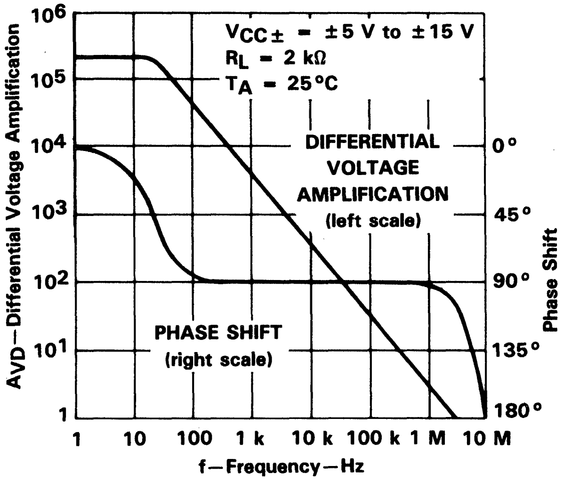


FIGURE 15

NORMALIZED UNITY-GAIN BANDWIDTH and PHASE SHIFT vs FREE-AIR TEMPERATURE

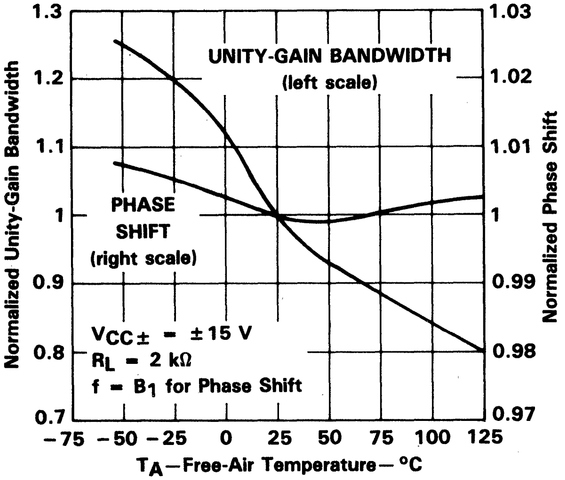


FIGURE 16

COMMON-MODE REJECTION RATIO vs FREE-AIR TEMPERATURE

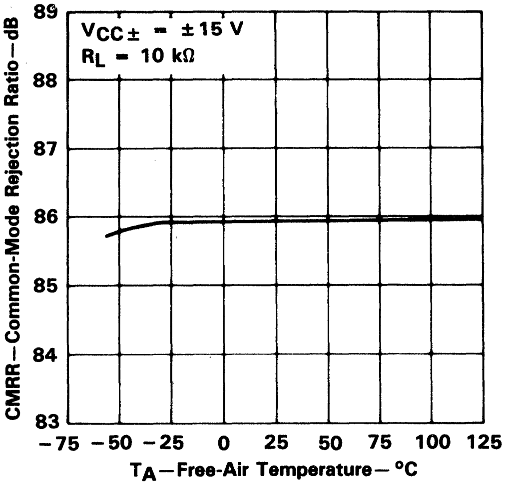


FIGURE 17

---

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices. An 18-pF compensation capacitor is used with TL070.

TYPICAL CHARACTERISTICS†

SUPPLY CURRENT PER AMPLIFIER
vs
SUPPLY VOLTAGE

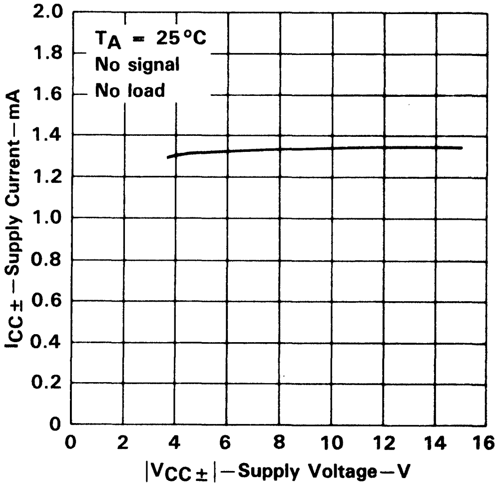


FIGURE 18

SUPPLY CURRENT PER AMPLIFIER
vs
FREE-AIR TEMPERATURE

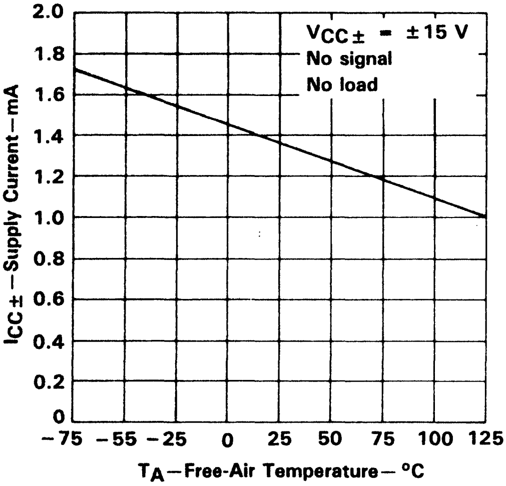


FIGURE 19

TOTAL POWER DISSIPATED
vs
FREE-AIR TEMPERATURE

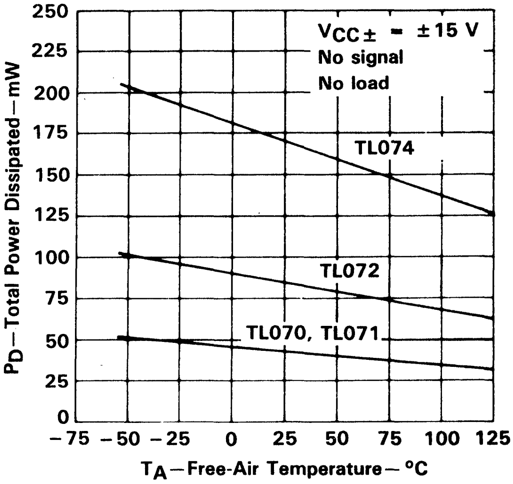


FIGURE 20

NORMALIZED SLEW RATE
vs
FREE-AIR TEMPERATURE

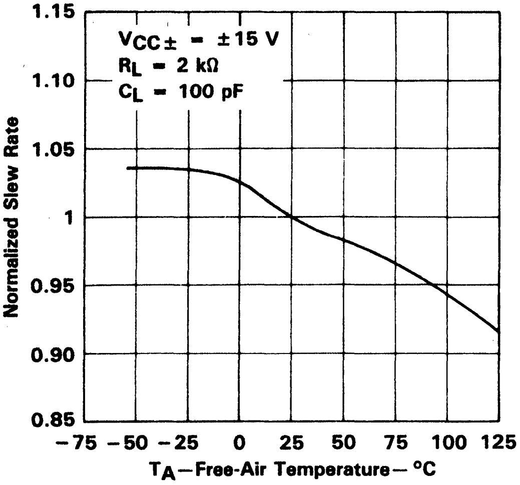


FIGURE 21

---

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices. An 18-pF compensation capacitor is used with TL070.

TYPICAL CHARACTERISTICS

EQUIVALENT INPUT NOISE VOLTAGE
vs
FREQUENCY

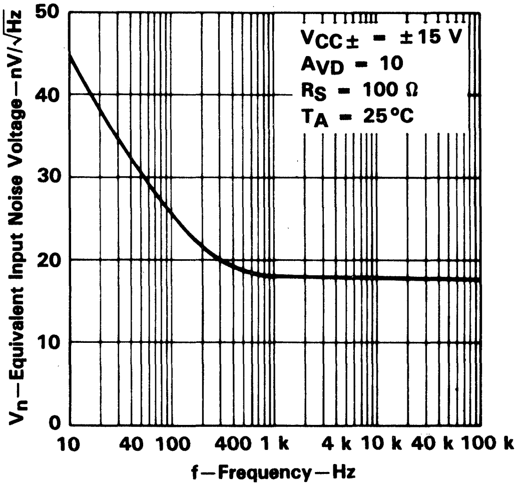


FIGURE 22

TOTAL HARMONIC DISTORTION
vs
FREQUENCY

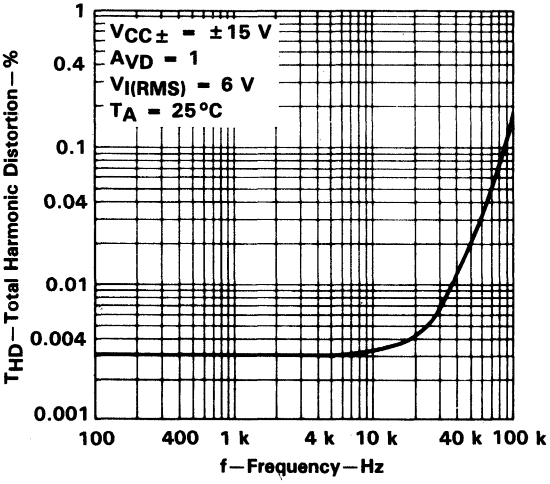


FIGURE 23

VOLTAGE-FOLLOWER
LARGE-SIGNAL PULSE RESPONSE

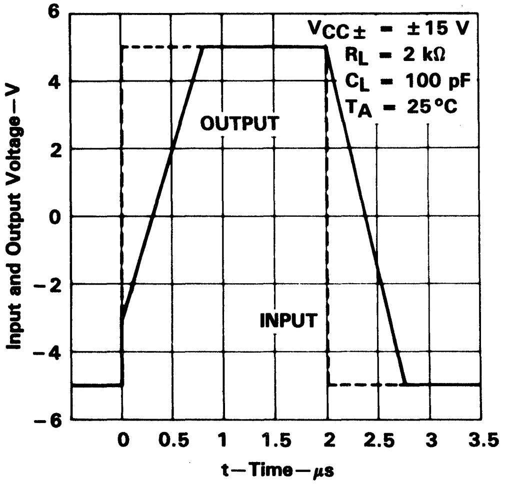


FIGURE 24

OUTPUT VOLTAGE
vs
ELAPSED TIME

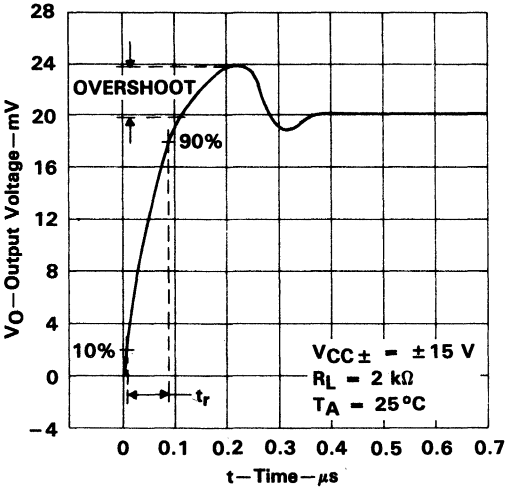
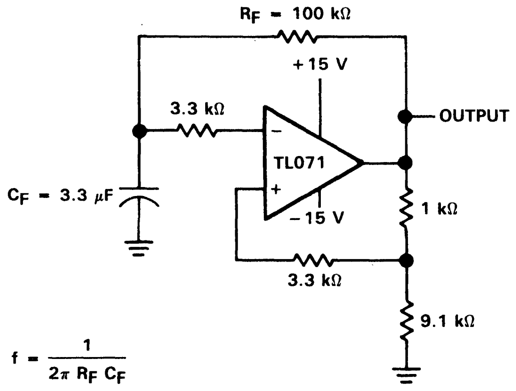


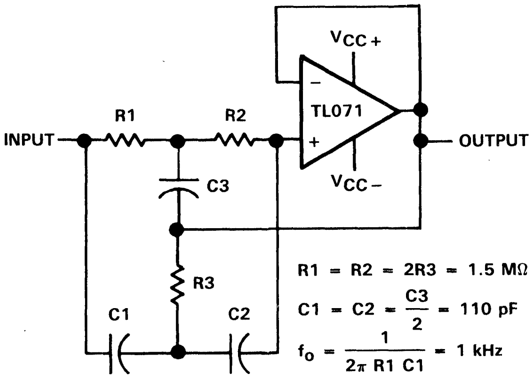
FIGURE 25

TYPICAL APPLICATION DATA



$$f = \frac{1}{2\pi R_F C_F}$$

FIGURE 26. 0.5-Hz SQUARE-WAVE OSCILLATOR



$R1 = R2 = 2R3 = 1.5\ M\Omega$

$C1 = C2 = \frac{C3}{2} = 110\ pF$

$f_o = \frac{1}{2\pi\ R1\ C1} = 1\ kHz$

FIGURE 27. HIGH-Q NOTCH FILTER

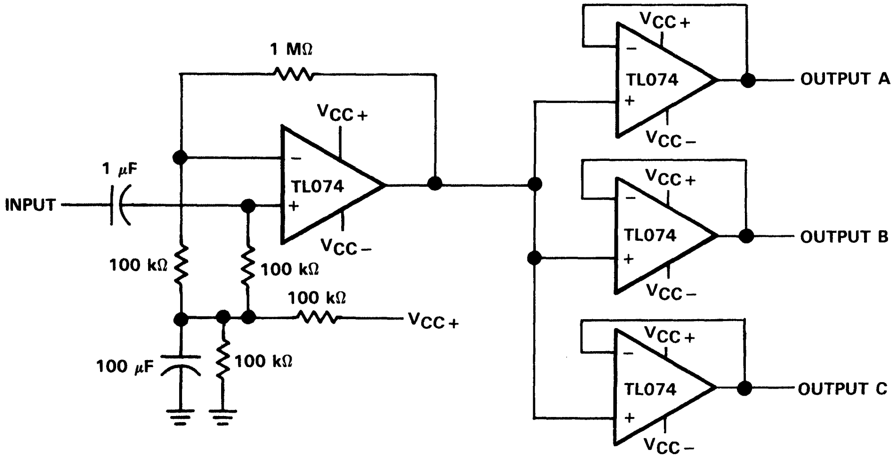
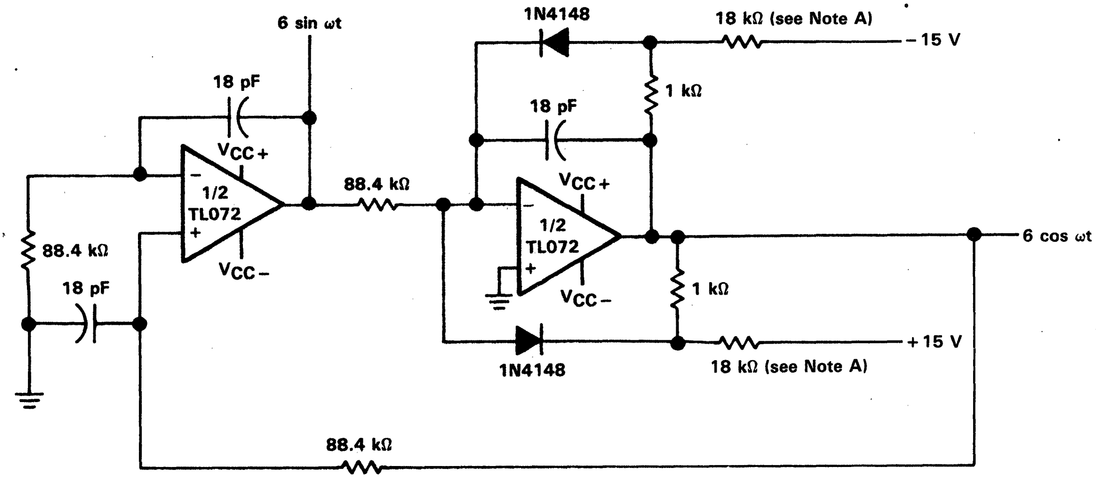


FIGURE 28. AUDIO DISTRIBUTION AMPLIFIER

TYPICAL APPLICATION DATA



Note A: These resistor values may be adjusted for a symmetrical output.

FIGURE 29. 100-kHz QUADRATURE OSCILLATOR

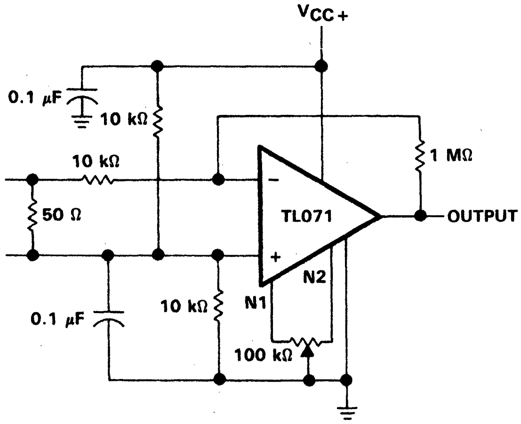


FIGURE 30. AC AMPLIFIER

TYPICAL APPLICATION DATA

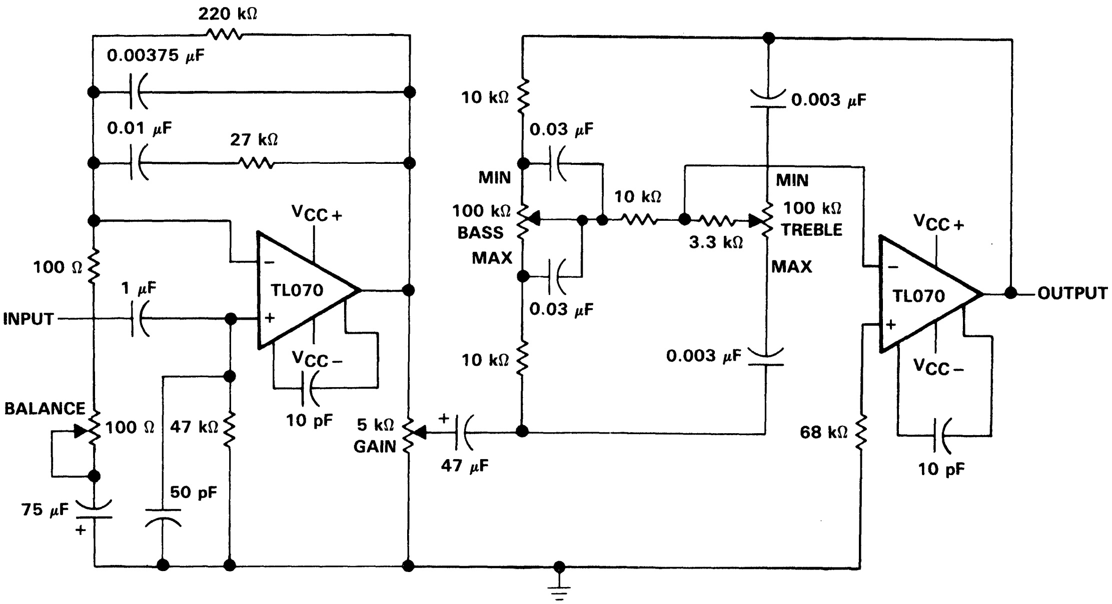


FIGURE 31. IC PREAMPLIFIER

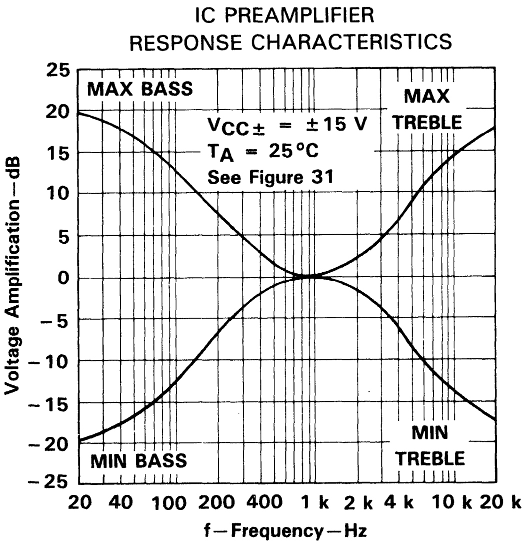


FIGURE 32

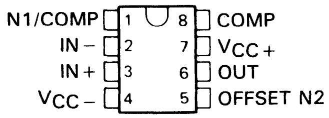
TL080, TL081, TL082, TL084, TL081A, TL082A, TL084A
TL081B, TL082B, TL084B
JFET-INPUT OPERATIONAL AMPLIFIERS

D2297, FEBRUARY 1977—REVISED OCTOBER 1990

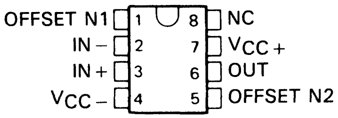
24 DEVICES COVER MILITARY, INDUSTRIAL AND COMMERCIAL TEMPERATURE RANGES

- **Low-Power Consumption**
- **Wide Common-Mode and Differential Voltage Ranges**
- **Low Input Bias and Offset Currents**
- **Output Short-Circuit Protection**
- **Low Total Harmonic Distortion . . . 0.003% Typ**
- **High Input Impedance . . . JFET-Input Stage**
- **Internal Frequency Compensation (Except TL080, TL080A)**
- **Latch-Up-Free Operation**
- **High Slew Rate . . . 13 V/μs Typ**
- **Common-Mode Input Voltage Range Includes V_{CC+}**

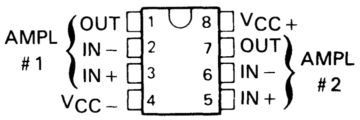
TL080
D, JG, OR P PACKAGE
(TOP VIEW)



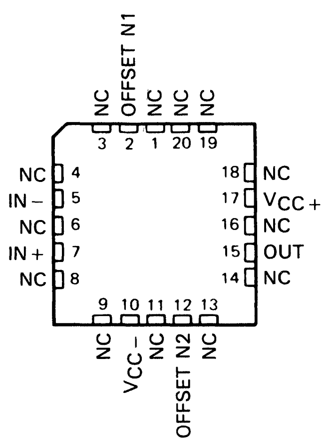
TL081, TL081A, TL081B
D, JG, OR P PACKAGE
(TOP VIEW)



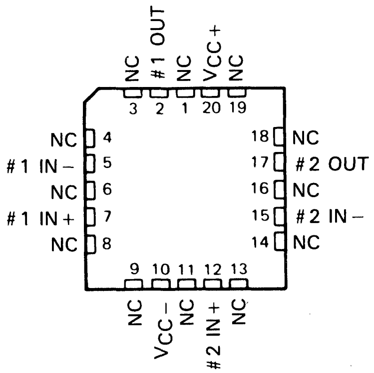
TL082, TL082A, TL082B
D, JG, OR P PACKAGE
(TOP VIEW)



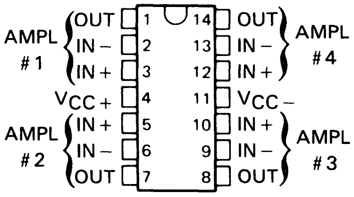
TL081M . . . FK CHIP CARRIER PACKAGE
(TOP VIEW)



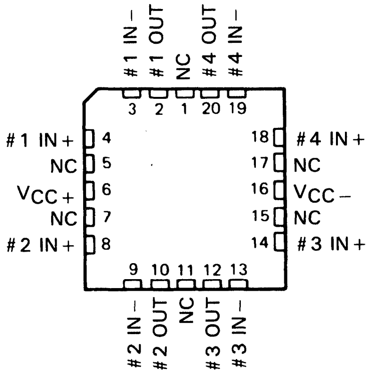
TL082M . . . FK CHIP CARRIER PACKAGE
(TOP VIEW)



TL084, TL084A, TL084B
D, J, OR N PACKAGE
(TOP VIEW)



TL084M . . . FK CHIP CARRIER PACKAGE
(TOP VIEW)



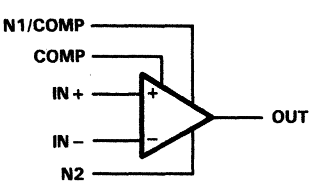
NC—No internal connection

TEXAS INSTRUMENTS

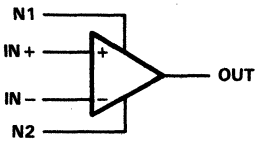
On products compliant to MIL-STD-883, Class B, all parameters are tested unless otherwise noted. On all other products, production processing does not necessarily include testing of all parameters.

symbols

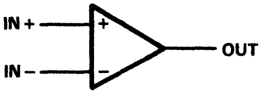
TL080



TL081



TL082 (each amplifier)
TL084 (each amplifier)



description

The TL08_ JFET-input operational amplifier family is designed to offer a wider selection than any previously developed operational amplifier family. Each of these JFET-input operational amplifiers incorporates well-matched, high-voltage JFET and bipolar transistors in a monolithic integrated circuit. The devices feature high slew rates, low input bias and offset currents, and low offset voltage temperature coefficient. Offset adjustment and external compensation options are available within the TL08_ family.

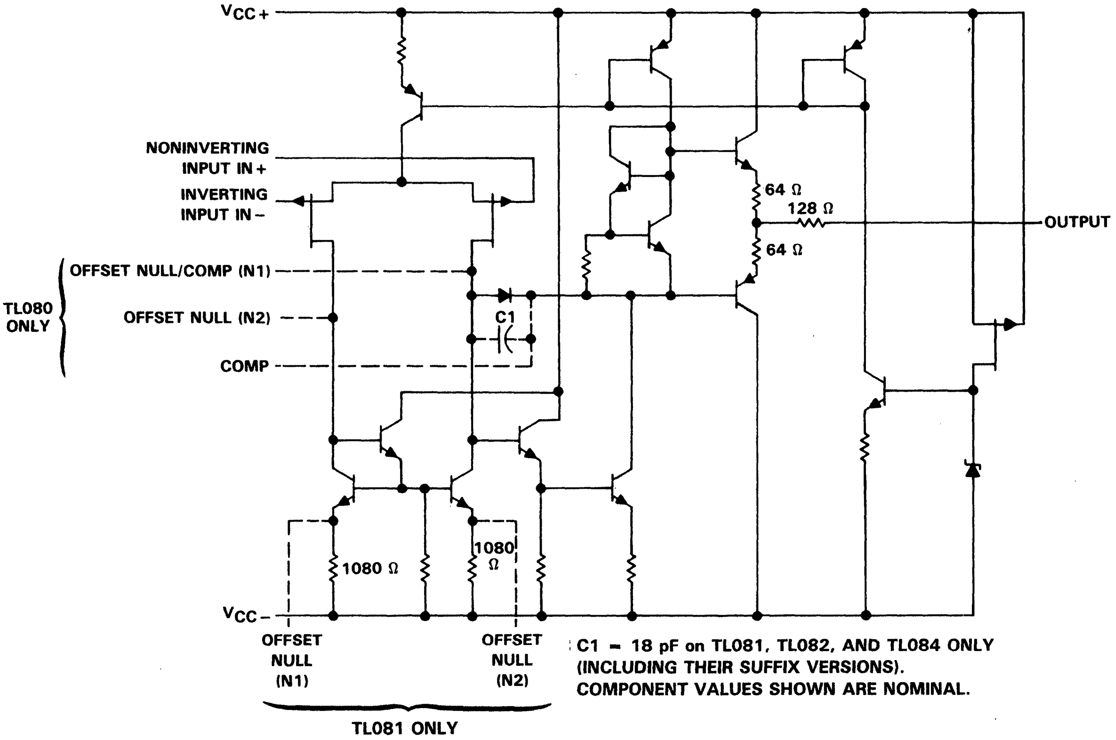
Device types with a "C" suffix are characterized for operation from 0°C to 70°C, those with an "I" suffix are characterized for operation from −40°C to 85°C, and those with an "M" suffix are characterized for operation over the full military temperature range of −55°C to 125°C.

AVAILABLE OPTIONS

T_A	V_{IO} MAX AT 25°C	PACKAGE						
		SMALL OUTLINE (D008)	SMALL OUTLINE (D014)	CHIP CARRIER (FK)	CERAMIC DIP (J)	CERAMIC DIP (JG)	PLASTIC DIP (N)	PLASTIC DIP (P)
0°C to 70°C	15 mV	TL080CD	—	—	—	—	—	TL080CP
	15 mV	TL081CD						TL081CP
	6 mV	TL081ACD						TL081ACP
	3 mV	TL081BCD						TL081BCP
	15 mV	TL082CD	—	—	—	—	—	TL082CP
	6 mV	TL082ACD						TL082ACP
	3 mV	TL082BCD						TL082BCP
	15 mV	—	TL084CD	—	—	—	TL084CN	—
	6 mV		TL084ACD				TL084ACN	
	3 mV		TL084BCD				TL084BCN	
−40°C to 85°C	6 mV	TL081ID		—	—	—		TL081IP
	6 mV	TL082ID						TL082IP
	6 mV	TL083ID						
	6 mV	TL084ID	TL084ID				TL084IN	
−55°C to 125°C	6 mV	—	—	TL081MFK		TL081MJG	—	—
	6 mV			TL082MFK		TL082MJG		
	9 mV			TL084MFK	TL084MJ			

The D package is available taped and reeled. Add "R" suffix to device type, (e.g., TL080CDR).

schematic (each amplifier)



C1 = 18 pF on TL081, TL082, AND TL084 ONLY (INCLUDING THEIR SUFFIX VERSIONS).
COMPONENT VALUES SHOWN ARE NOMINAL.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

		TL08_C TL08_AC TL08_BC	TL08_I	TL08_M	UNIT
Supply voltage, V_{CC+} (see Note 1)		18	18	18	V
Supply voltage, V_{CC-} (see Note 1)		−18	−18	−18	V
Differential input voltage (see Note 2)		±30	±30	±30	V
Input voltage (see Notes 1 and 3)		±15	±15	±15	V
Duration of output short circuit (see Note 4)		unlimited	unlimited	unlimited	
Continuous total dissipation		See Dissipation Rating Table			
Operating free-air temperature range		0 to 70	−40 to 85	−55 to 125	°C
Storage temperature range		−65 to 150	−65 to 150	−65 to 150	°C
Case temperature for 60 seconds	FK package			260	°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds	J or JG package			300	°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	D, N, or P package	260	260		°C

NOTES: 1. All voltage values, except differential voltages, are with respect to the midpoint between V_{CC+} and V_{CC-}.
2. Differential voltages are at the noninverting input terminal with respect to the inverting input terminal.
3. The magnitude of the input voltage must never exceed the magnitude of the supply voltage or 15 V, whichever is less.
4. The output may be shorted to ground or to either supply. Temperature and/or supply voltages must be limited to ensure that the dissipation rating is not exceeded.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR	DERATE ABOVE T_A	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING	$T_A = 125°C$ POWER RATING
D (8 Pin)	680 mW	5.8 mW/°C	32°C	464 mW	377 mW	N/A
D (14 Pin)	680 mW	7.6 mW/°C	60°C	608 mW	494 mW	N/A
FK	680 mW	11.0 mW/°C	88°C	680 mW	680 mW	275 mW
J	680 mW	11.0 mW/°C	88°C	680 mW	680 mW	275 mW
JG	680 mW	8.4 mW/°C	69°C	672 mW	546 mW	210 mW
N	680 mW	9.2 mW/°C	76°C	680 mW	598 mW	N/A
P	680 mW	8.0 mW/°C	65°C	640 mW	520 mW	N/A

electrical characteristics, $V_{CC\pm} = \pm 15$ V (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		TL080C TL081C TL082C TL084C			TL081AC TL082AC TL084AC			TL081BC TL082BC TL084BC			TL081I TL082I TL083I TL084I			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	$V_O = 0$, $R_S = 50\ \Omega$	$T_A = 25°C$		3	15		3	6		2	3		3	6	mV
			T_A = full range			20			7.5			5			9	
α_{VIO}	Temperature coefficient of input offset voltage	$V_O = 0$, $R_S = 50\ \Omega$, T_A = full range			18			18			18			18		µV/°C
I_{IO}	Input offset current‡	$V_O = 0$	$T_A = 25°C$		5	200		5	100		5	100		5	100	pA
			T_A = full range			2			2			2			10	nA
I_{IB}	Input bias current‡	$V_O = 0$	$T_A = 25°C$		30	400		30	200		30	200		30	200	pA
			T_A = full range			10			7			7			20	nA
V_{ICR}	Common-mode input voltage range	$T_A = 25°C$		±11	−12 to 15		±11	−12 to 15		±11	−12 to 15		±11	−12 to 15		V
V_{OM}	Maximum peak output voltage swing	$T_A = 25°C$, $R_L = 10\ k\Omega$		±12	±13.5		±12	±13.5		±12	±13.5		±12	±13.5		V
		T_A = full range	$R_L = \geq 10\ k\Omega$	±12			±12			±12			±12			
			$R_L \geq 2\ k\Omega$	±10	±12		±10	±12		±10	±12		±10	±12		
A_{VD}	Large-signal differential voltage amplification	$V_O = \pm 10$ V, $R_L \geq 2\ k\Omega$, $T_A = 25°C$		25	200		50	200		50	200		50	200		V/mV
		$V_O = \pm 10$ V, $R_L \geq 2\ k\Omega$, T_A = full range		15			25			25			25			
B_1	Unity-gain bandwidth	$T_A = 25°C$			3			3			3			3		MHz
r_i	Input resistance	$T_A = 25°C$			10^{12}			10^{12}			10^{12}			10^{12}		Ω
CMRR	Common-mode rejection ratio	$V_{IC} = V_{ICR}$ min, $V_O = 0$, $R_S = 50\ \Omega$, $T_A = 25°C$		70	86		80	86		80	86		80	86		dB
k_{SVR}	Supply voltage rejection ratio ($\Delta V_{CC\pm}/\Delta V_{IO}$)	$V_{CC} = \pm 15$ V to ± 9 V, $V_O = 0$, $R_S = 50\ \Omega$, $T_A = 25°C$		70	86		80	86		80	86		80	86		dB
I_{CC}	Supply current (per amplifier)	No load, $T_A = 25°C$	$V_O = 0$,		1.4	2.8		1.4	2.8		1.4	2.8		1.4	2.8	mA
V_{o1}/V_{o2}	Crosstalk attenuation	$A_{VD} = 100$, $T_A = 25°C$			120			120			120			120		dB

† All characteristics are measured under open-loop conditions with zero common-mode input voltage unless otherwise specified. Full range for T_A is 0°C to 70°C for TL08__C, TL08__AC, and TL08__BC, and −40°C to 85°C for TL08__I.

‡ Input bias currents of a FET-input operational amplifier are normal junction reverse currents, which are temperature sensitive as shown in Figure 18. Pulse techniques must be used that will maintain the junction temperatures as close to the ambient temperature as is possible.

electrical characteristics, $V_{CC\pm}$ = ±15 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		MIN	TYP	MAX	MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	$V_O = 0$, $R_S = 50\ \Omega$	$T_A = 25°C$		3	6		3	9	mV
			$T_A = -55°C$ to $125°C$			9			15	
α_{VIO}	Temperature coefficient of input offset voltage	$V_O = 0$, $R_S = 50\ \Omega$, $T_A = -55°C$ to $125°C$			18			18		μV/°C
I_{IO}	Input offset current‡	$V_O = 0$	$T_A = 25°C$		5	100		5	100	pA
			$T_A = 125°C$			20			20	nA
I_{IB}	Input bias current‡	$V_O = 0$	$T_A = 25°C$		30	200		30	200	pA
			$T_A = 125°C$			50			50	nA
V_{ICR}	Common-mode input voltage range	$T_A = 25°C$		±11	−12 to 15		±11	−12 to 15		V
V_{OM}	Maximum peak output voltage swing	$T_A = 25°C$,	$R_L = 10\ k\Omega$	±12	±13.5		±12	±13.5		V
		$T_A = -55°C$ to $125°C$	$R_L \geq 10\ k\Omega$	±12			±12			
			$R_L \geq 2\ k\Omega$	±10	±12		±10	±12		
A_{VD}	Large-signal differential voltage amplification	$V_O = \pm 10$ V, $T_A = 25°C$	$R_L \geq 2\ k\Omega$,	25	200		25	200		V/mV
		$V_O = \pm 10$ V, $T_A = -55°C$ to $125°C$	$R_L \geq 2\ k\Omega$,	15			15			
B_1	Unity-gain bandwidth	$T_A = 25°C$			3			3		MHz
r_i	Input resistance	$T_A = 25°C$			10^{12}			10^{12}		Ω
CMRR	Common-mode rejection ratio	$V_{IC} = V_{ICR}$ min, $R_S = 50\ \Omega$,	$V_O = 0$, $T_A = 25°C$	80	86		80	86		dB
k_{SVR}	Supply voltage rejection ratio ($\Delta V_{CC\pm}/\Delta V_{IO}$)	$V_{CC} = \pm 15$ V to ± 9 V, $R_S = 50\ \Omega$,	$V_O = 0$, $T_A = 25°C$	80	86		80	86		dB
I_{CC}	Supply current (per amplifier)	No load, $T_A = 25°C$	$V_O = 0$,		1.4	2.8		1.4	2.8	mA
V_{o1}/V_{o2}	Crosstalk attenuation	$A_{VD} = 100$,	$T_A = 25°C$		120			120		dB

† All characteristics are measured under open-loop conditions with zero common-mode input voltage unless otherwise specified.

‡ Input bias currents of a FET-input operational amplifier are normal junction reverse currents, which are temperature sensitive as shown in Figure 18. Pulse techniques must be used that will maintain the junction temperatures as close to the ambient temperature as is possible.

operating characteristics, $V_{CC\pm} = \pm 15$ V, $T_A = 25°C$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS				MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain	$V_I = 10$ V, $C_L = 100$ pF,	$R_L = 2$ kΩ, See Figure 1			8*	13		V/µs
		$V_I = 10$ V, $C_L = 100$ pF, See Figure 1	$R_L = 2$ kΩ $T_A = -55°C$ to 125°C		TL081M TL082M TL084M	5*			
t_r	Rise time	$V_I = 20$ mV,	$R_L = 2$ kΩ,				0.05		µs
	Overshoot factor	$C_L = 100$ pF,	See Figure 1				20%		
V_n	Equivalent input noise voltage	$R_S = 100$ Ω		f = 1 kHz			18		nV/√Hz
				f = 10 Hz to 10 kHz			4		µV
I_n	Equivalent input noise current	$R_S = 100$ Ω,	f = 1 kHz				0.01		pA/√Hz
THD	Total harmonic distortion	$V_{O(rms)} = 10$ V, $R_L \geq 2$ kΩ,	$R_S \leq 1$ kΩ, f = 1 kHz				0.003%		

*On products compliant to MIL-STD-883, Class B, this parameter is not production tested.

PARAMETER MEASUREMENT INFORMATION

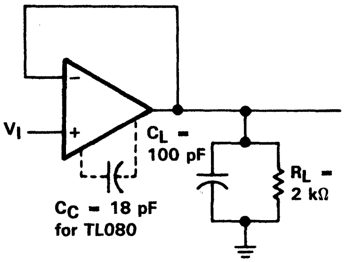


FIGURE 1. UNITY-GAIN AMPLIFIER

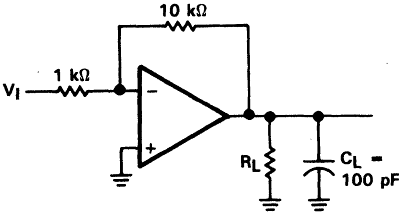


FIGURE 2. GAIN-OF-10 INVERTING AMPLIFIER

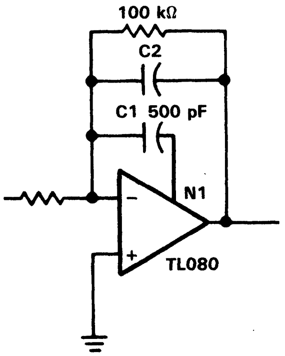


FIGURE 3. FEED-FORWARD COMPENSATION

INPUT OFFSET VOLTAGE NULL CIRCUITS

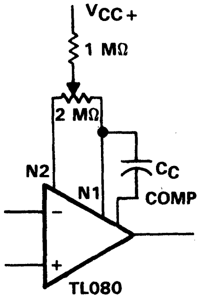


FIGURE 4

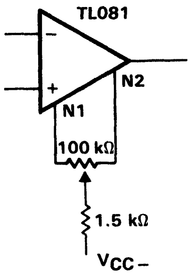


FIGURE 5

TYPICAL CHARACTERISTICS†

MAXIMUM PEAK OUTPUT VOLTAGE
vs
FREQUENCY

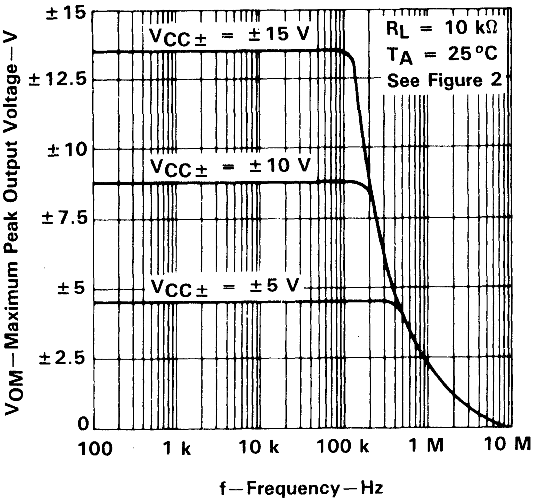


FIGURE 6

MAXIMUM PEAK OUTPUT VOLTAGE
vs
FREQUENCY

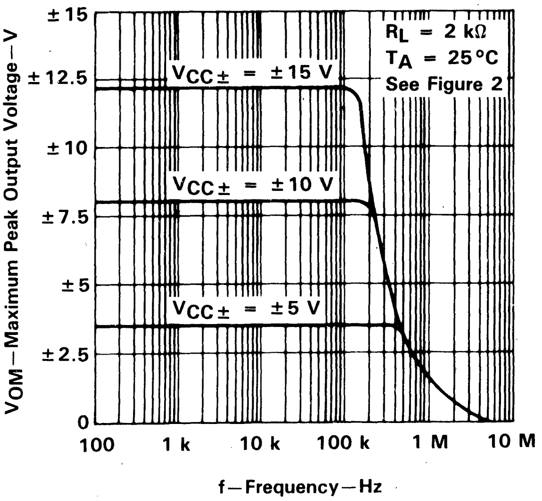


FIGURE 7

MAXIMUM PEAK OUTPUT VOLTAGE
vs
FREQUENCY

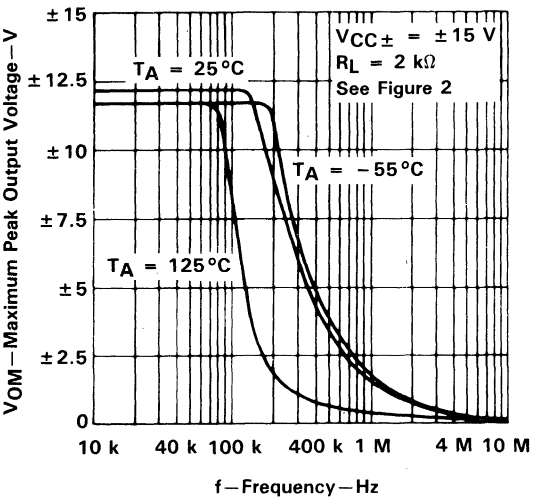


FIGURE 8

MAXIMUM PEAK OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

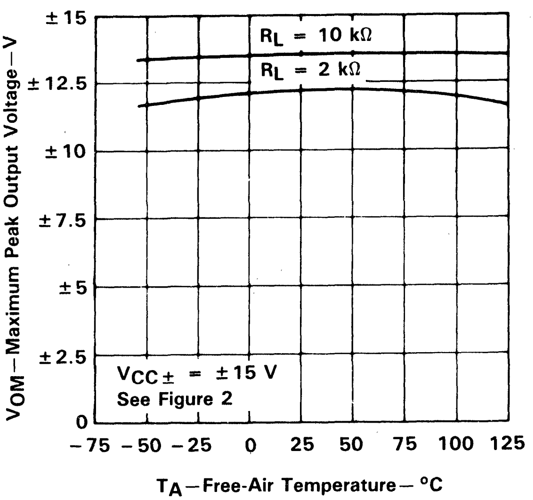
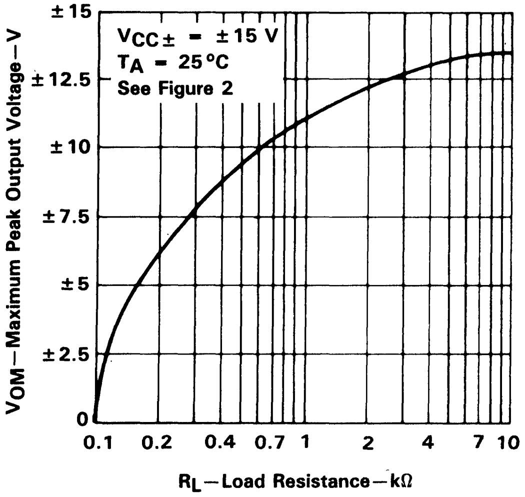


FIGURE 9

---

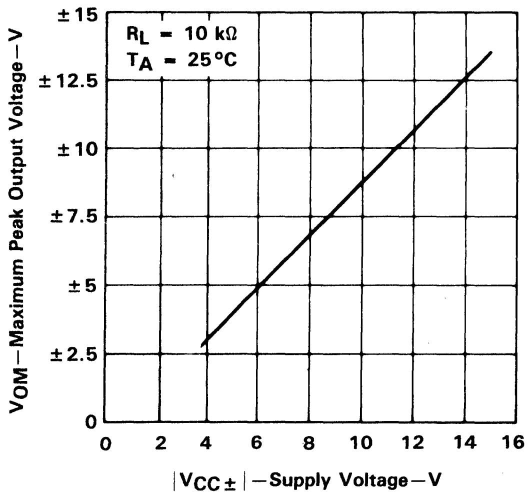
† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices. A 12-pF compensation capacitor is used with TL080.

TYPICAL CHARACTERISTICS†



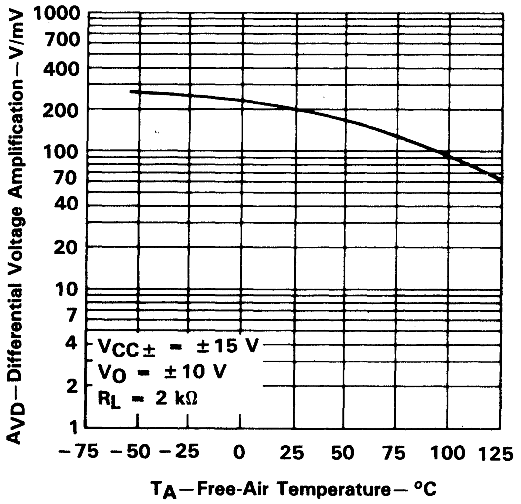
MAXIMUM PEAK OUTPUT VOLTAGE
vs
LOAD RESISTANCE

FIGURE 10



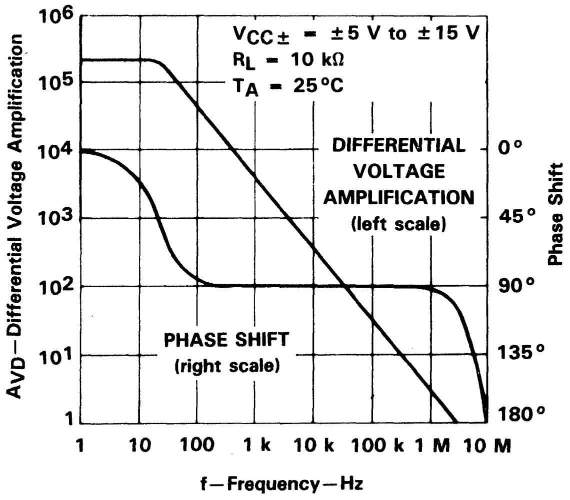
MAXIMUM PEAK OUTPUT VOLTAGE
vs
SUPPLY VOLTAGE

FIGURE 11



LARGE-SIGNAL
DIFFERENTIAL VOLTAGE AMPLIFICATION
vs
FREE-AIR TEMPERATURE

FIGURE 12



LARGE-SIGNAL
DIFFERENTIAL VOLTAGE AMPLIFICATION
and PHASE SHIFT
vs
FREQUENCY

FIGURE 13

---

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices. A 12-pF compensation capacitor is used with TL080.

TYPICAL CHARACTERISTICS†

TL080
DIFFERENTIAL VOLTAGE AMPLIFICATION
vs
FREQUENCY WITH FEED-FORWARD COMPENSATION

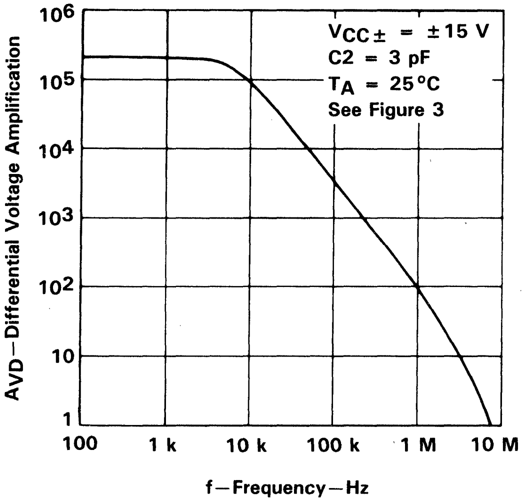


FIGURE 14

TOTAL POWER DISSIPATED
vs
FREE-AIR TEMPERATURE

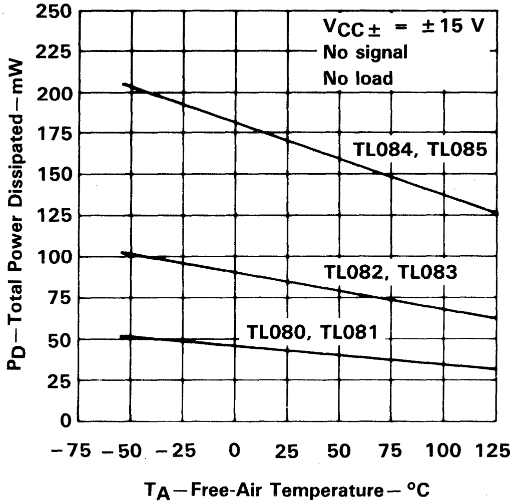


FIGURE 15

SUPPLY CURRENT PER AMPLIFIER
vs
FREE-AIR TEMPERATURE

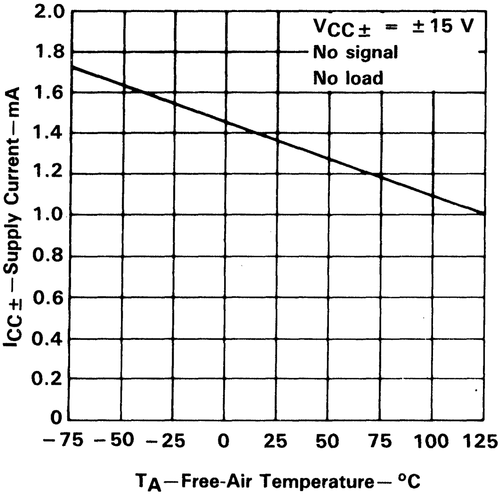


FIGURE 16

SUPPLY CURRENT
vs
SUPPLY VOLTAGE

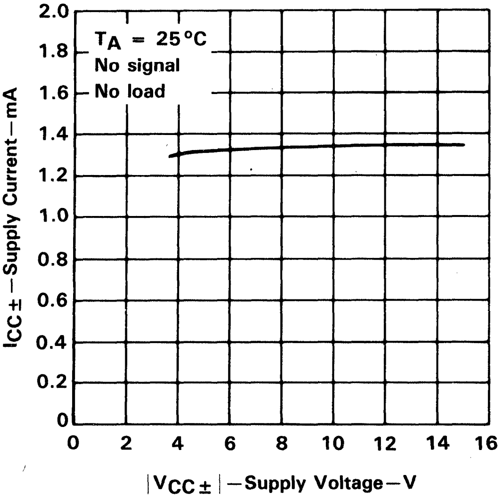


FIGURE 17

---

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices. A 12-pF compensation capacitor is used with TL080.

TYPICAL CHARACTERISTICS†

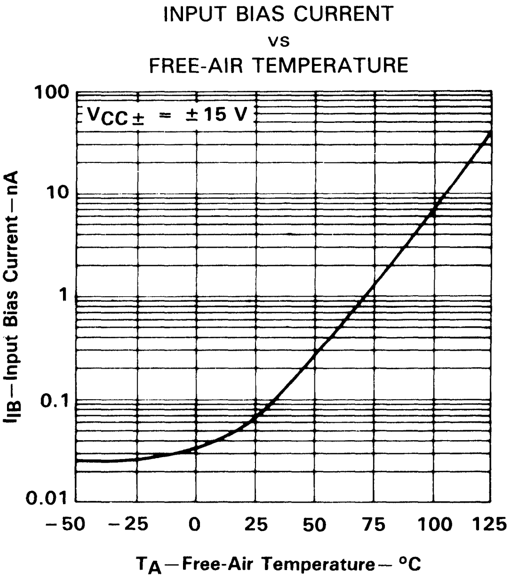


FIGURE 18

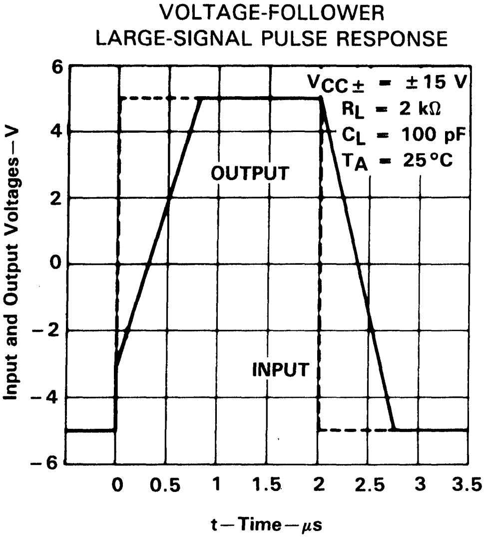


FIGURE 19

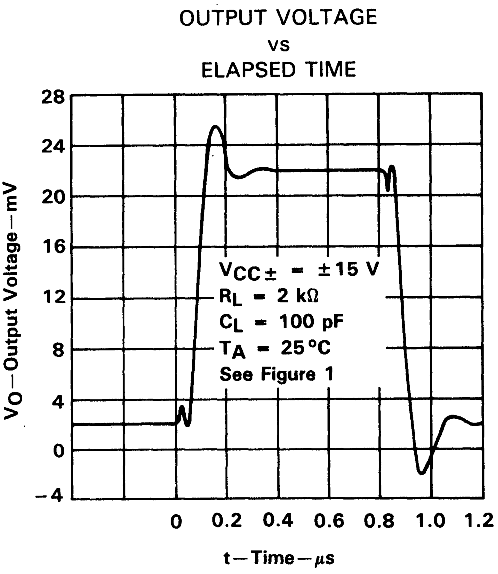


FIGURE 20

---

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices. A 12-pF compensation capacitor is used with TL080.

TYPICAL CHARACTERISTICS†

COMMON-MODE REJECTION RATIO
vs
FREE-AIR TEMPERATURE

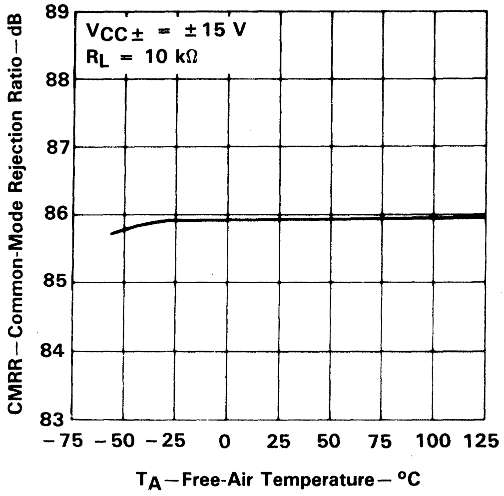


FIGURE 21

EQUIVALENT INPUT NOISE VOLTAGE
vs
FREQUENCY

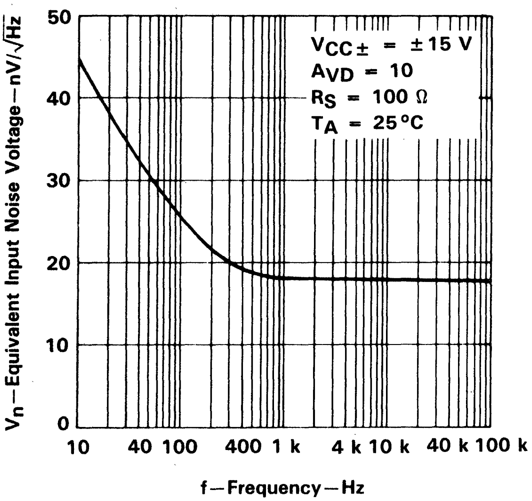


FIGURE 22

TOTAL HARMONIC DISTORTION
vs
FREQUENCY

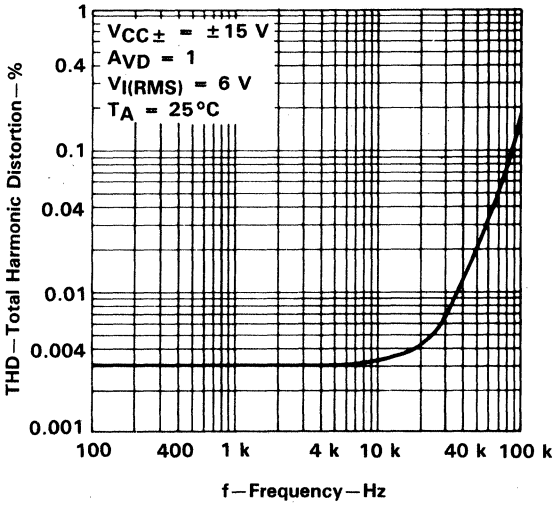


FIGURE 23

---

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices. A 12-pF compensation capacitor is used with TL080.

TYPICAL APPLICATION DATA

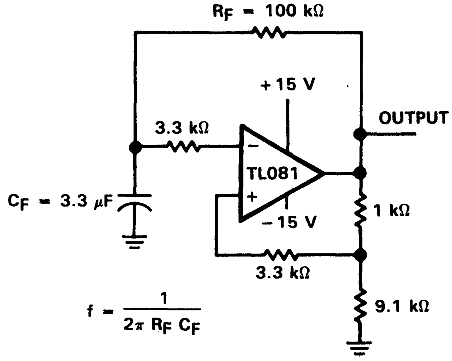


FIGURE 24. 0.5-Hz SQUARE-WAVE OSCILLATOR

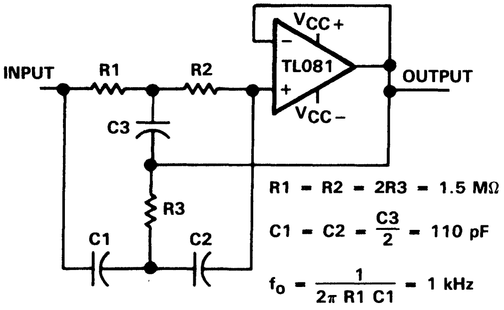


FIGURE 25. HIGH-Q NOTCH FILTER

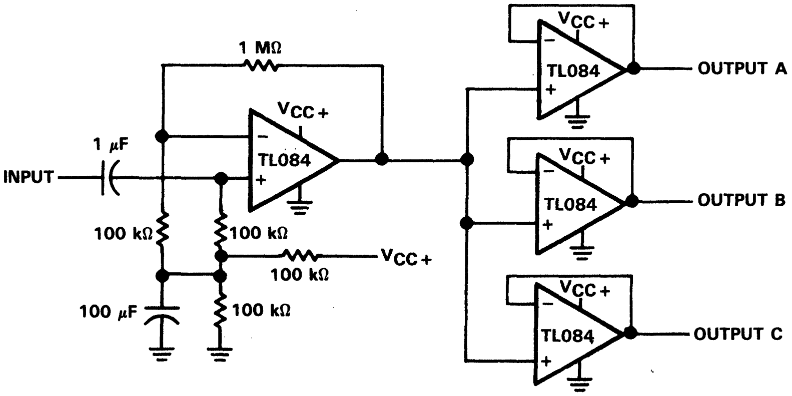
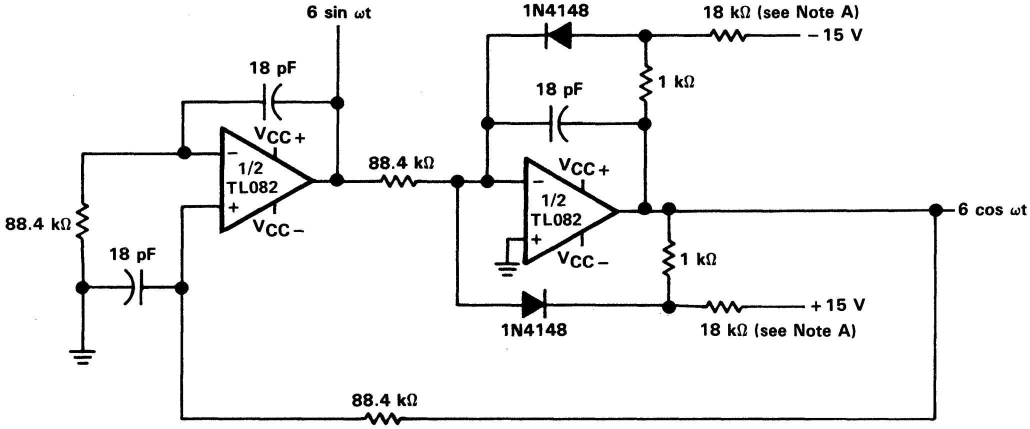


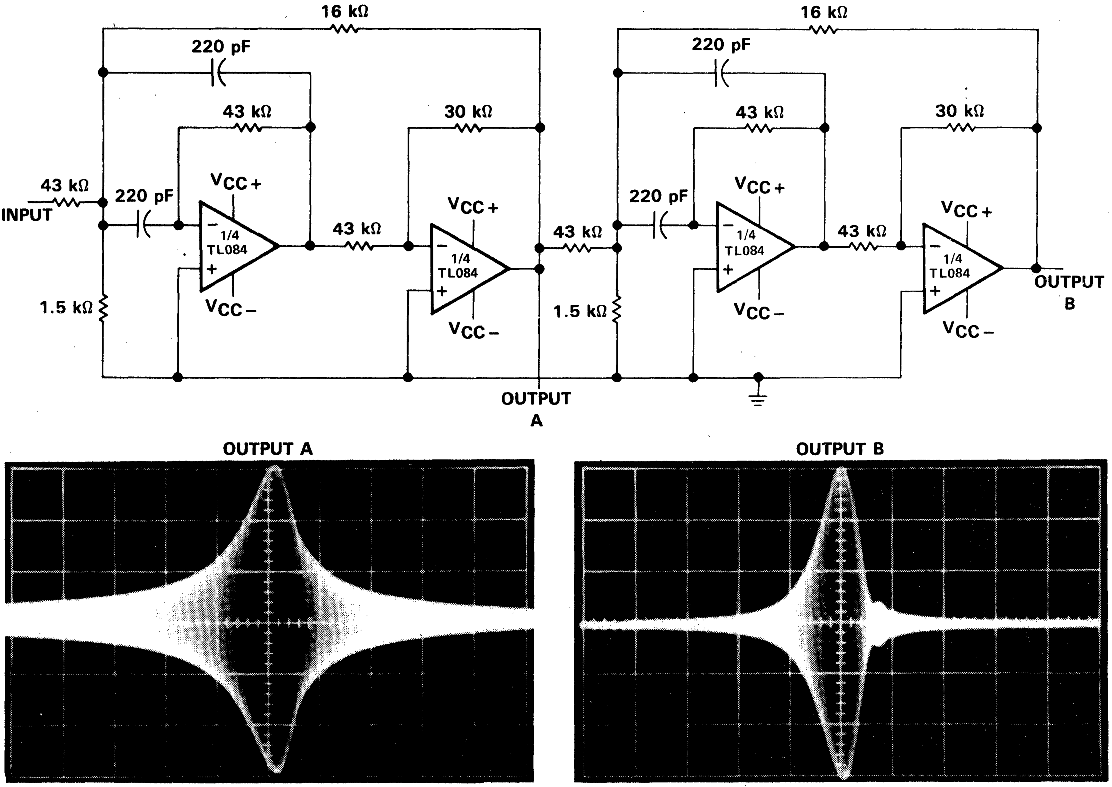
FIGURE 26. AUDIO DISTRIBUTION AMPLIFIER



NOTE A: These resistor values may be adjusted for a symmetrical output.

FIGURE 27. 100-kHZ QUADRATURE OSCILLATOR

TYPICAL APPLICATION DATA



2 kHz/div
SECOND-ORDER BANDPASS FILTER
f_o = 100 kHz, Q = 30, GAIN = 4

2 kHz/div
CASCADED BANDPASS FILTER
f_o = 100 kHz, Q = 69, GAIN = 16

FIGURE 28. POSITIVE-FEEDBACK BANDPASS FILTER

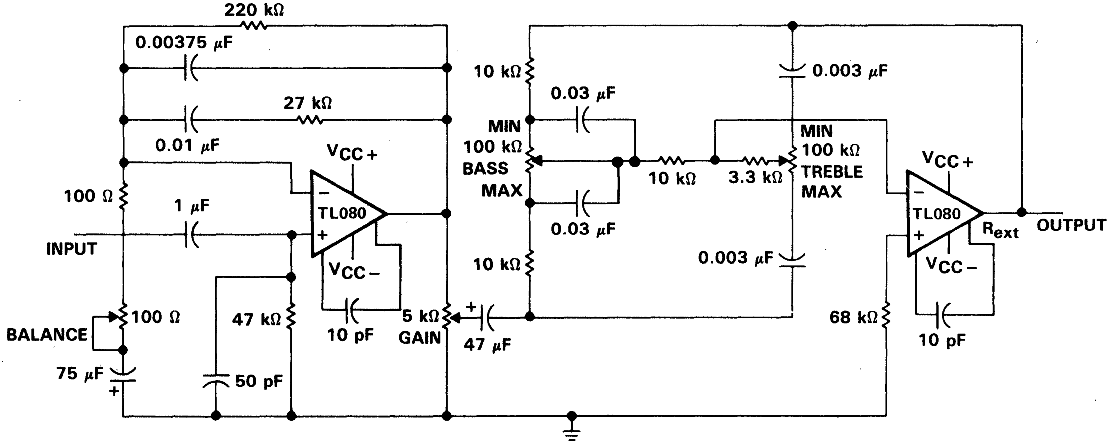


FIGURE 29. IC PREAMPLIFIER

TL087, TL088, TL287, TL288
JFET-INPUT OPERATIONAL AMPLIFIERS

D2484, MARCH 1979—REVISED MARCH 1989

- **Low Input Offset Voltage . . . 0.5 mV Max**
- **Low Power Consumption**
- **Wide Common-Mode and Differential Voltage Ranges**
- **Low Input Bias and Offset Currents**
- **High Input Impedance . . . JFET-Input Stage**
- **Internal Frequency Compensation**
- **Latch-Up-Free Operation**
- **High Slew Rate . . . 18 V/μs Typ**
- **Low Total Harmonic Distortion . . . 0.003% Typ**

description

These JFET-input operational amplifiers incorporate well-matched high-voltage JFET and bipolar transistors in a monolithic integrated circuit. They feature low input offset voltage, high slew rate, low input bias and offset currents, and low temperature coefficient of input offset voltage. Offset-voltage adjustment is provided for the TL087 and TL088.

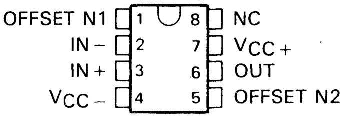
The M-suffix devices are characterized for operation over the full military temperature range of −55°C to 125°C. The I-suffix devices are characterized for operation from −40°C to 85°C, and the C-suffix devices are characterized for operation from 0°C to 70°C.

AVAILABLE OPTIONS

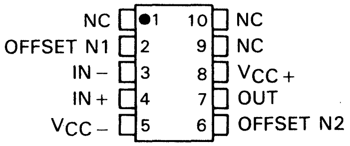
T_A	TYPE	V_{IO} MAX AT 25°C	PACKAGE				
			SMALL OUTLINE (D)	CERAMIC DIP (JG)	METAL CAN (L)	PLASTIC DIP (P)	FLAT (U)
0°C to 70°C	Single	0.5 mV	TL087CD	TL087CJG	TL087CL	TL087CP	
		1 mV	TL088CD	TL088CJG	TL088CL	TL088CP	
	Dual	0.5 mV	TL287CD	TL287CJG	TL287CL	TL287CP	
		1 mV	TL288CD	TL288CJG	TL288CL	TL288CP	
−40°C to 85°C	Single	0.5 mV	TL087ID	TL087IJG	TL087IL	TL087IP	
		1 mV	TL088ID	TL088IJG	TL088IL	TL088IP	
	Dual	0.5 mV	TL287ID	TL287IJG	TL287IL	TL287IP	
		1 mV	TL288ID	TL288IJG	TL288IL	TL288IP	
−55°C to 125°C	Single	1 mV		TL088MJG	TL088ML		TL088MU
	Dual	1 mV		TL288MJG	TL288ML		TL288MU

The D package is available taped and reeled. Add the suffix R to the device type (e.g., TL087CDR).

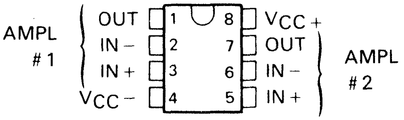
TL087, TL088
D, JG, OR P PACKAGE
(TOP VIEW)



TL088M
U PACKAGE
(TOP VIEW)

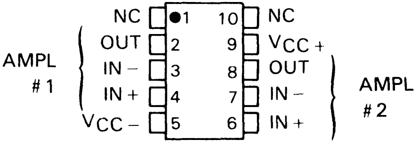


TL287, TL288
D, JG, OR P PACKAGE
(TOP VIEW)

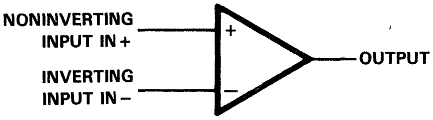


NC—No internal connection

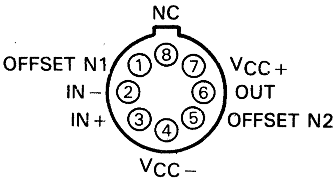
TL288M
U PACKAGE
(TOP VIEW)



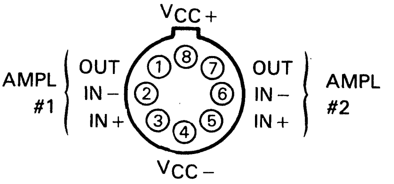
symbol (each amplifier)



TL087, TL088
L PACKAGE
(TOP VIEW)



TL287, TL288
L PACKAGE
(TOP VIEW)



Pin 4 (L Package) is in electrical contact with the case
NC—No internal connection

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

		TL088M TL288M	TL087I TL088I TL287I TL288I	TL087C TL088C TL287C TL288C	UNIT
Supply voltage, V_{CC+} (see Note 1)		18	18	18	V
Supply voltage, V_{CC-} (see Note 1)		−18	−18	−18	V
Differential input voltage (see Note 2)		±30	±30	±30	V
Input voltage (see Notes 1 and 3)		±15	±15	±15	V
Input current, I_I (each input)		±1	±1	±1	mA
Output current, I_O (each output)		±80	±80	±80	mA
Total V_{CC+} terminal current		160	160	160	mA
Total V_{CC-} terminal current		−160	−160	−160	mA
Duration of output short circuit (see Note 4)		unlimited	unlimited	unlimited	
Continuous total dissipation		See Dissipation Rating Table			
Operating free-air temperature range		−55 to 125	−25 to 85	0 to 70	°C
Storage temperature range		−65 to 150	−65 to 150	−65 to 150	°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds	JG, L, or U package	300	300	300	°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	D or P package		260	260	°C

NOTES: 1. All voltage values, except differential voltages, are with respect to the midpoint between V_{CC+} and V_{CC-}.
2. Differential voltages are at the noninverting input terminal with respect to the inverting input terminal.
3. The magnitude of the input voltage must never exceed the magnitude of the supply voltage or 15 V, whichever is less.
4. The output may be shorted to ground or to either supply. Temperature and/or supply voltages must be limited to ensure that the dissipation rating is not exceeded.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le$ 25°C POWER RATING	DERATING FACTOR ABOVE T_A = 25°C	T_A = 70°C POWER RATING	T_A = 85°C POWER RATING	T_A = 125°C POWER RATING
D	725 mW	5.8 mW/°C	464 mW	377 mW	N/A
JG	1050 mW	8.4 mW/°C	672 mW	546 mW	210 mW
L	650 mW	5.2 mW/°C	416 mW	338 mW	130 mW
P	1000 mW	8.0 mW/°C	640 mW	520 mW	N/A
U	675 mW	5.4 mW/°C	432 mW	351 mW	135 mW

recommended operating conditions

		M-SUFFIX			I-SUFFIX			C-SUFFIX			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		±5		±15	±5		±15	±5		±15	V
Common-mode input voltage, V_{IC}	$V_{CC\pm}$ = ±5 V	−1		4	−1		4	−1		4	V
	$V_{CC\pm}$ = ±15 V	−11		11	−11		11	−11		11	V
Input voltage, V_I	$V_{CC\pm}$ = ±5 V	−1		4	−1		4	−1		4	V
	$V_{CC\pm}$ = ±15 V	−11		11	−11		11	−11		11	V
Operating free-air temperature, T_A		−55		125	−40		85	0		70	°C

electrical characteristics, $V_{CC\pm} = \pm 15$ V

PARAMETER		TEST CONDITIONS†		TL088M TL288M			TL087I TL088I TL287I TL288I			TL087C TL088C TL287C TL288C			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	R_S = 50 Ω, V_O = 0, T_A = 25°C	TL087, TL287					0.1	0.5		0.1	0.5	mV
			TL088, TL288		0.1	3		0.1	1		0.1	1	
		R_S = 50 Ω, V_O = 0, T_A = full range	TL087, TL287						2			1.5	
			TL088, TL288			6			3			2.5	
α_{VIO}	Temperature coefficient of input offset voltage	R_S = 50 Ω,	T_A = 25°C to MAX		10			8			8		μV/°C
I_{IO}	Input offset current	T_A = 25°C			5			5	100		5	100	pA
		T_A = full range				25			3			2	nA
I_{IB}	Input bias current‡	T_A = 25°C			30			30	200		30	200	pA
		T_A = full range				100			20			7	nA
V_{ICR}	Common-mode input voltage range	T_A = 25°C		$V_{CC-}+4$ to $V_{CC+}-4$			$V_{CC-}+4$ to $V_{CC+}-4$			$V_{CC-}+4$ to $V_{CC+}-4$			V
V_{OPP}	Maximum-peak-to-peak output voltage swing	T_A = 25°C,	R_L = 10 kΩ	24	27		24	27		24	27		V
		T_A = full range	$R_L \geq$ 10 kΩ	24			24			24			
			$R_L \geq$ 2 kΩ	20			20			20			
A_{VD}	Large-signal differential voltage amplification	$R_L \geq$ 2 kΩ, T_A = 25°C	V_O = ±10 V,	50	105		50	105		50	105		V/mV
		$R_L \geq$ 2 kΩ, T_A = full range	V_O = ±10 V,	25			25			25			
B_1	Unity-gain bandwidth	T_A = 25°C			3			3			3		MHz
r_i	Input resistance	T_A = 25°C			10^{12}			10^{12}			10^{12}		Ω
CMRR	Common-mode rejection ratio	R_S = 50 Ω, V_{IC} = V_{ICR} min,	V_O = 0 V, T_A = 25°C	80	93		80	93		80	93		dB
k_{SVR}	Supply voltage rejection ratio ($\Delta V_{CC\pm}/\Delta V_{IO}$)	R_S = 50 Ω, $V_{CC\pm}$ = ±9 V to ±15 V, T_A = 25°C	V_O = 0 V,	80	99		80	99		80	99		dB
I_{CC}	Supply current (per amplifier)	No load, T_A = 25°C	V_O = 0,		2.6	2.8		2.6	2.8		2.6	2.8	mA

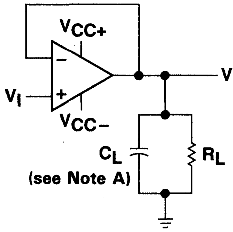
† All characteristics are measured under open-loop conditions with zero common-mode input voltage unless otherwise specified. Full range for T_A is −55°C to 125°C for TL__88M; −40°C to 85°C for TL__8__I; and 0°C to 70°C for TL__8__C.

‡ Input bias currents of a FET-input operational amplifier are normal junction reverse currents, which are temperature sensitive. Pulse techniques must be used that will maintain the junction temperature as close to the ambient temperature as possible.

operating characteristics $V_{CC} = \pm 15$ V, $T_A = 25°C$

PARAMETER		TEST CONDITIONS		TL088M, TL288M			TL087I, TL087C TL088I, TL088C			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
SR	Slew rate at unity gain	$V_I = 10$ V, $C_L = 100$ pF,	$R_L = 2$ kΩ, $A_{VD} = 1$		18		8	18		V/μs
t_r	Rise time	$V_I = 20$ mV,	$R_L = 2$ kΩ,		55			55		ns
	Overshoot factor	$C_L = 100$ pF,	$A_{VD} = 1$		25%			25%		
V_n	Equivalent input noise voltage	$R_S = 100$ Ω,	f = 1 kHz		19			19		nV/$\sqrt{Hz}$

PARAMETER MEASUREMENT INFORMATION



NOTE A: C_L includes fixture capacitance.

FIGURE 1. SLEW RATE, RISE/FALL TIME, AND OVERSHOOT TEST CIRCUIT

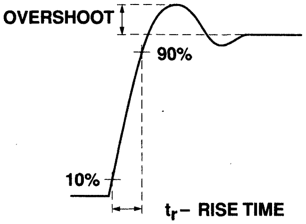


FIGURE 2. RISE TIME AND OVERSHOOT WAVEFORM

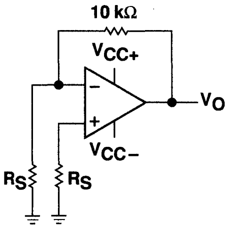
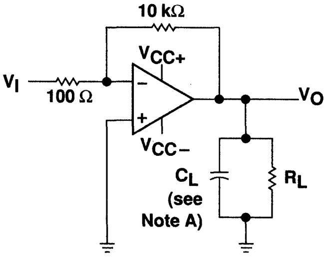


FIGURE 3. NOISE VOLTAGE TEST CIRCUIT



NOTE A: C_L includes fixture capacitance.

FIGURE 4. UNITY-GAIN BANDWIDTH AND PHASE MARGIN TEST CIRCUIT

typical values

Typical values as presented in this data sheet represent the median (50% point) of device parametric performance.

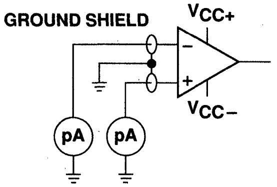


FIGURE 5. INPUT BIAS AND OFFSET CURRENT TEST CIRCUIT

input bias and offset current

At the picoamp bias current level typical of these JFET operational amplifiers, accurate measurement of the bias current becomes difficult. Not only does this measurement require a picoammeter, but test socket leakages can easily exceed the actual device bias currents. To accurately measure these small currents, Texas Instruments uses a two-step process. The socket leakage is measured using picoammeters with bias voltages applied, but with no device in the socket. The device is then inserted in the socket and a second test that measures both the socket leakage and the device input bias current is performed. The two measurements are then subtracted algebraically to determine the bias current of the device.

TYPICAL CHARACTERISTICS

table of graphs

			FIGURE
αV_{IO}	Temperature coefficient of input offset voltage	Distribution	6, 7
I_{IO}	Input offset current	vs Temperature	8
I_{IB}	Input bias current	vs V_{IC}	9
		vs Temperature	8
V_I	Common-mode input voltage range limits	vs V_{CC}	10
		vs Temperature	11
V_{ID}	Differential input voltage	vs Output voltage	12
V_{OM}	Maximum peak output voltage swing	vs V_{CC}	13
		vs Output current	17
		vs Frequency	14, 15, 16
		vs Temperature	18
A_{VD}	Differential voltage amplification	vs R_L	19
		vs Frequency	20
		vs Temperature	21
z_o	Output impedance	vs Frequency	24
CMRR	Common-mode rejection ratio	vs Frequency	22
		vs Temperature	23
k_{SVR}	Supply-voltage rejection ratio	vs Temperature	25
I_{OS}	Short-circuit output current	vs V_{CC}	26
		vs Time	27
		vs Temperature	28
I_{CC}	Supply current	vs V_{CC}	29
		vs Temperature	30
SR	Slew Rate	vs R_L	31
		vs Temperature	32
	Overshoot factor	vs C_L	33
V_n	Equivalent input noise voltage	vs Frequency	34
THD	Total harmonic distortion	vs Frequency	35
B_1	Unity-gain bandwidth	vs V_{CC}	36
		vs Temperature	37
ϕ_m	Phase margin	vs V_{CC}	38
		vs C_L	39
		vs Temperature	40
	Phase shift	vs Frequency	20
	Pulse response	Small-signal	41
		Large-signal	42

TYPICAL CHARACTERISTICS[†]

DISTRIBUTION OF TL088 INPUT OFFSET VOLTAGE TEMPERATURE COEFFICIENT

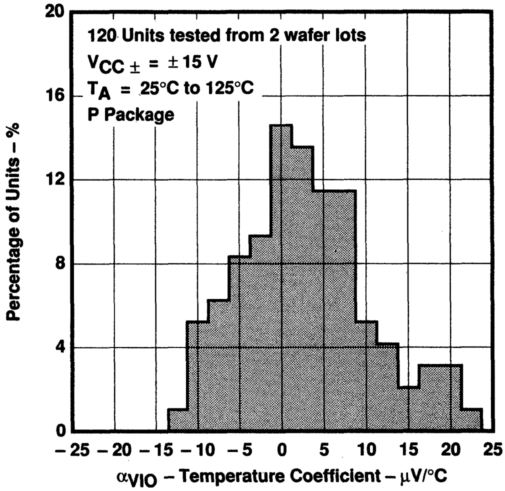


FIGURE 6

DISTRIBUTION OF TL288 INPUT OFFSET VOLTAGE TEMPERATURE COEFFICIENT

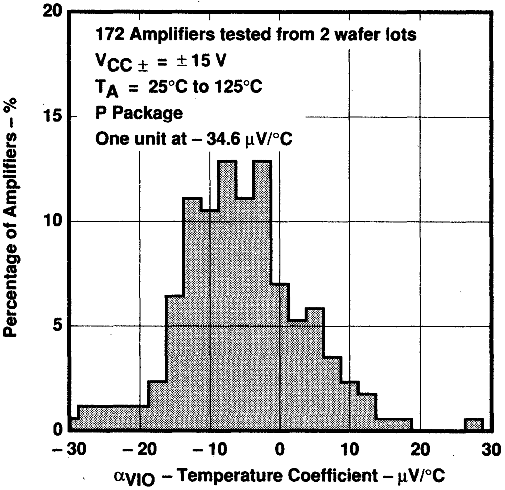


FIGURE 7

INPUT BIAS CURRENT AND INPUT OFFSET CURRENT vs FREE-AIR TEMPERATURE

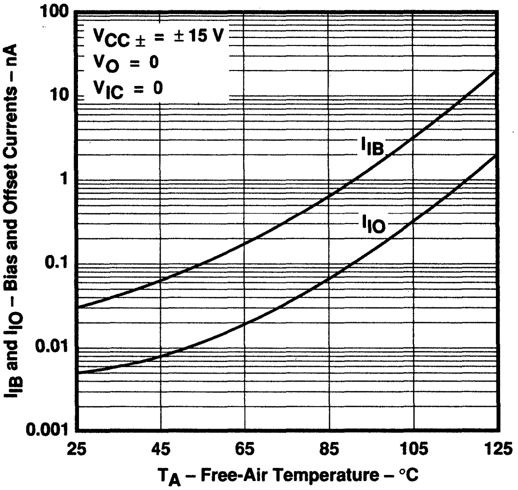


FIGURE 8

INPUT BIAS CURRENT vs COMMON-MODE INPUT VOLTAGE

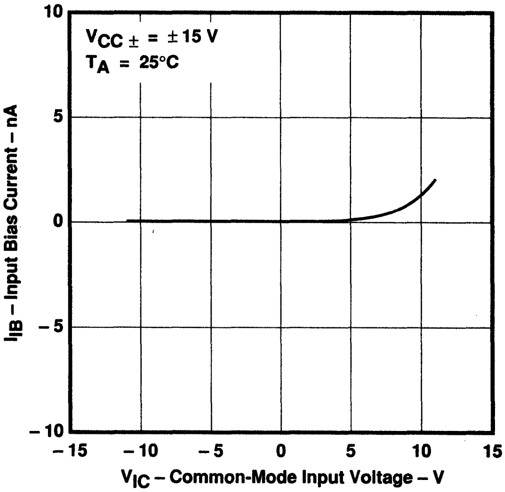


FIGURE 9

[†] Data at high and low temperatures are applicable within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

COMMON-MODE INPUT VOLTAGE RANGE LIMITS vs SUPPLY VOLTAGE

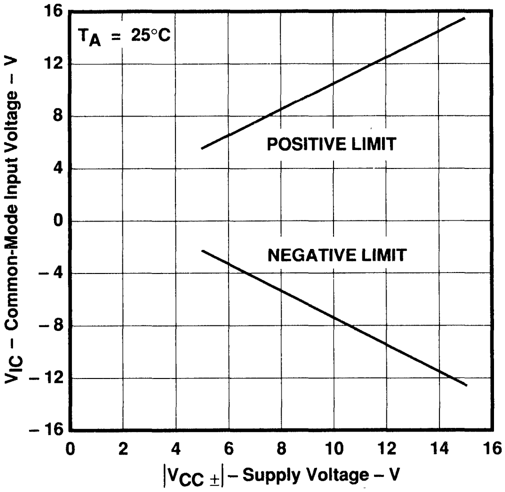


FIGURE 10

COMMON-MODE INPUT VOLTAGE RANGE LIMITS vs FREE-AIR TEMPERATURE

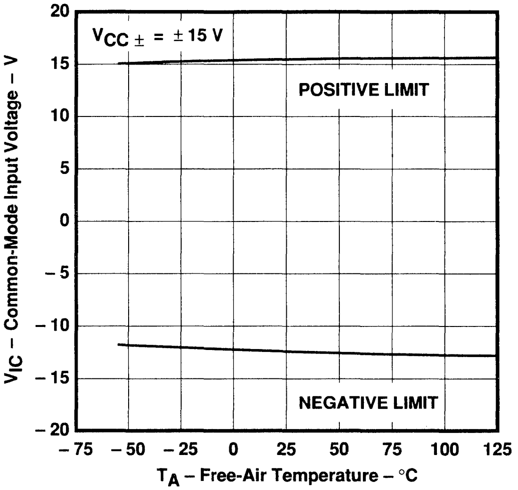


FIGURE 11

OUTPUT VOLTAGE vs DIFFERENTIAL INPUT VOLTAGE

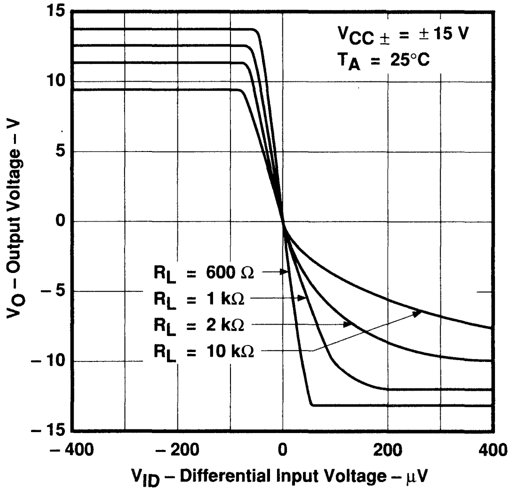


FIGURE 12

MAXIMUM PEAK OUTPUT VOLTAGE vs SUPPLY VOLTAGE

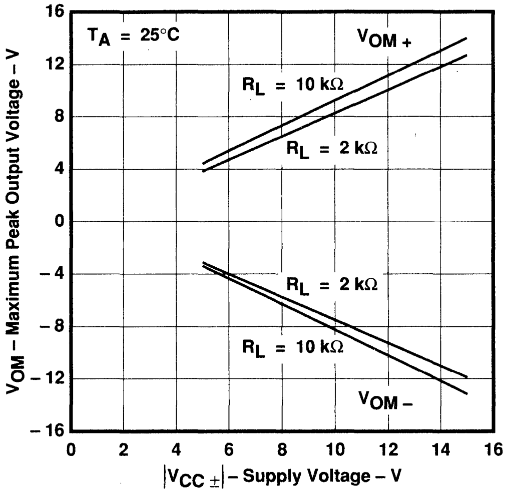


FIGURE 13

---

†Data at high and low temperatures are applicable within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE
vs
FREQUENCY

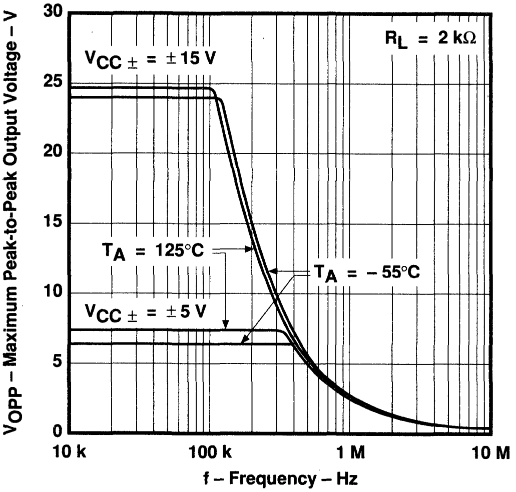


FIGURE 14

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE
vs
FREQUENCY

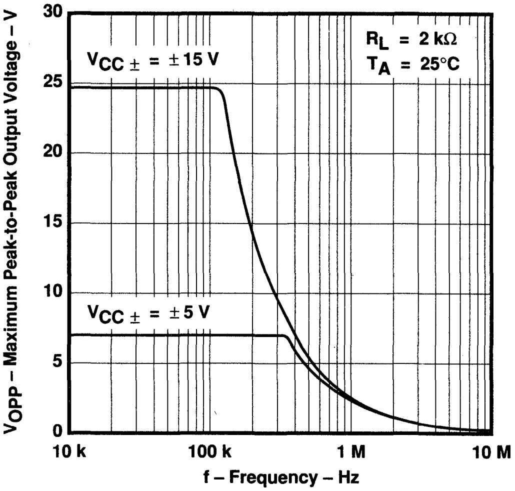


FIGURE 15

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE
vs
FREQUENCY

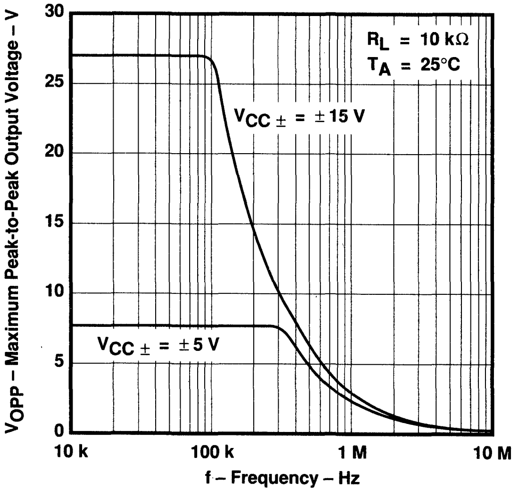


FIGURE 16

MAXIMUM PEAK OUTPUT VOLTAGE
vs
OUTPUT CURRENT

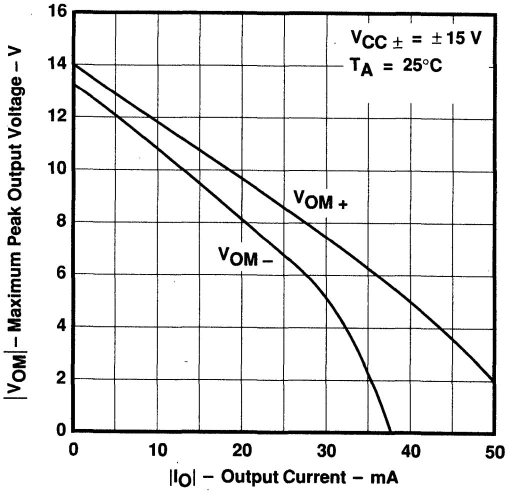


FIGURE 17

---

†Data at high and low temperatures are applicable within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

MAXIMUM PEAK OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

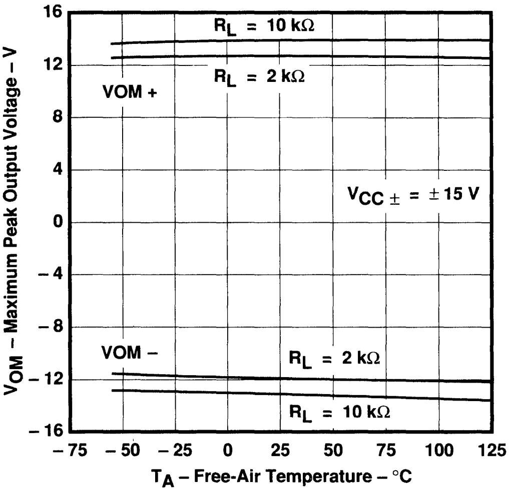


FIGURE 18

LARGE-SIGNAL VOLTAGE AMPLIFICATION
vs
LOAD RESISTANCE

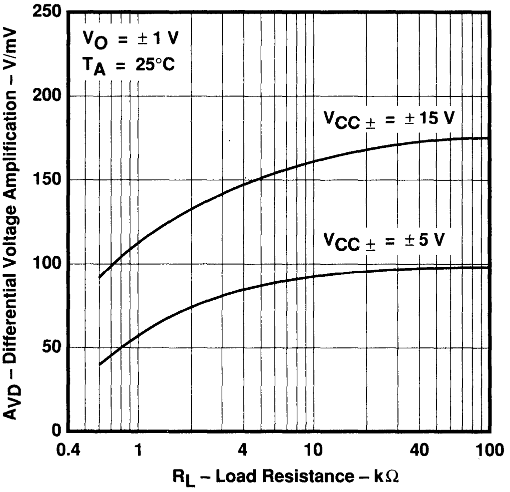


FIGURE 19

LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION AND PHASE SHIFT
vs
FREQUENCY

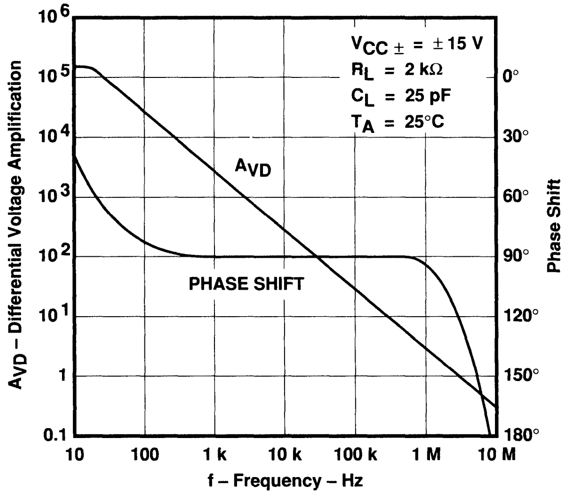


FIGURE 20

LARGE-SIGNAL VOLTAGE AMPLIFICATION
vs
FREE-AIR TEMPERATURE

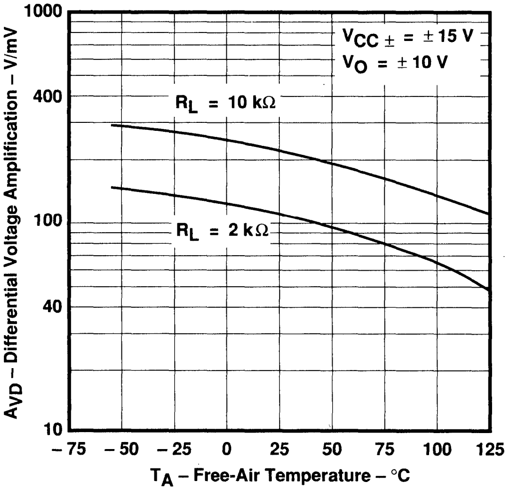


FIGURE 21

---

† Data at high and low temperatures are applicable within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS[†]

COMMON-MODE REJECTION RATIO
vs
FREQUENCY

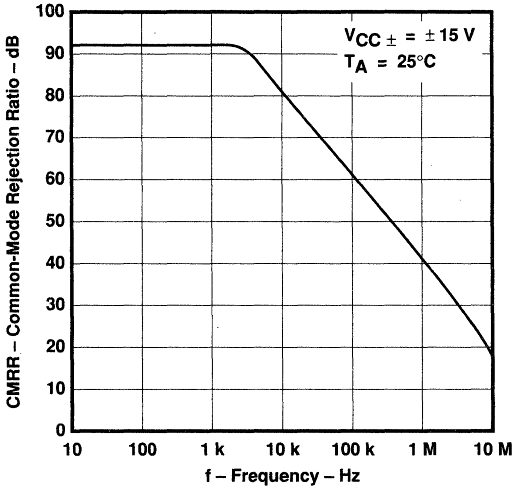


FIGURE 22

COMMON-MODE REJECTION RATIO
vs
FREE-AIR TEMPERATURE

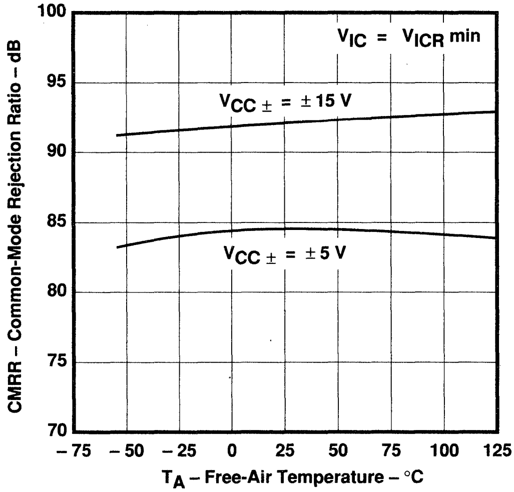


FIGURE 23

OUTPUT IMPEDANCE
vs
FREQUENCY

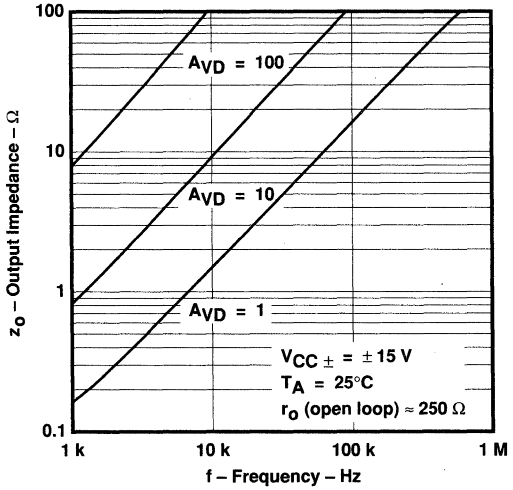


FIGURE 24

SUPPLY-VOLTAGE REJECTION RATIO
vs
FREE-AIR TEMPERATURE

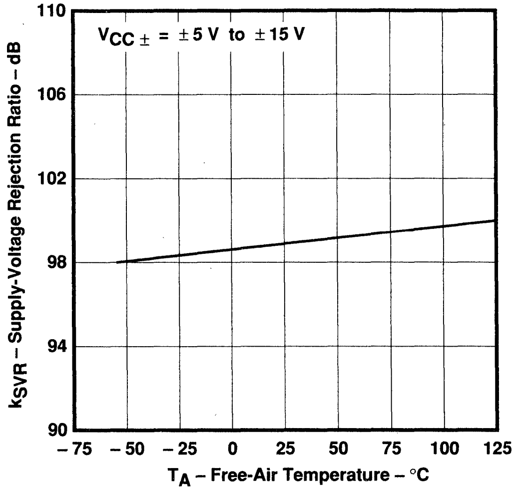


FIGURE 25

[†] Data at high and low temperatures are applicable within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

SHORT-CIRCUIT OUTPUT CURRENT
vs
SUPPLY VOLTAGE

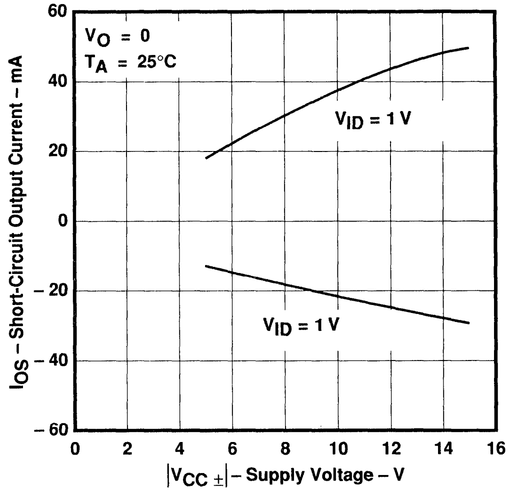


FIGURE 26

SHORT-CIRCUIT OUTPUT CURRENT
vs
TIME

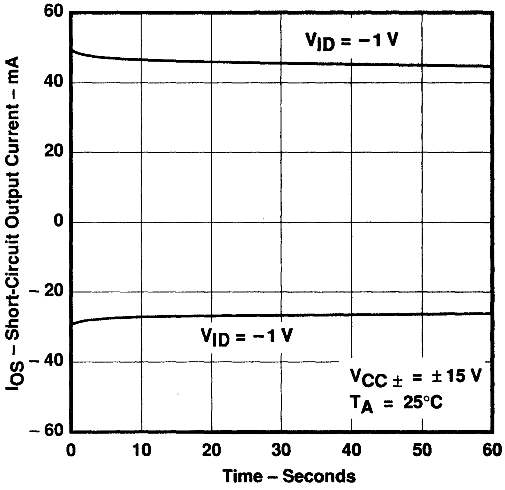


FIGURE 27

SHORT-CIRCUIT OUTPUT CURRENT
vs
FREE-AIR TEMPERATURE

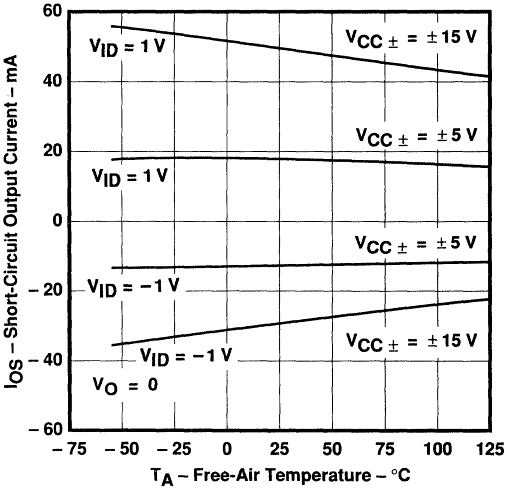


FIGURE 28

---

† Data at high and low temperatures are applicable within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

SUPPLY CURRENT
vs
SUPPLY VOLTAGE

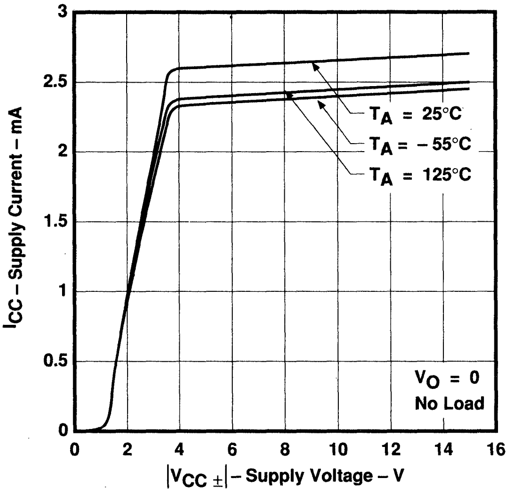


FIGURE 29

SUPPLY CURRENT
vs
FREE-AIR TEMPERATURE

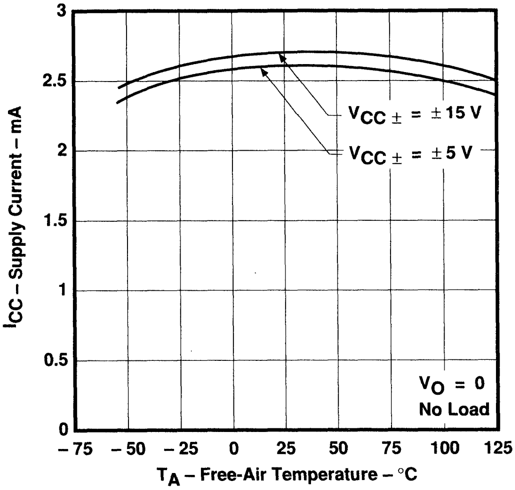


FIGURE 30

SLEW RATE
vs
LOAD RESISTANCE

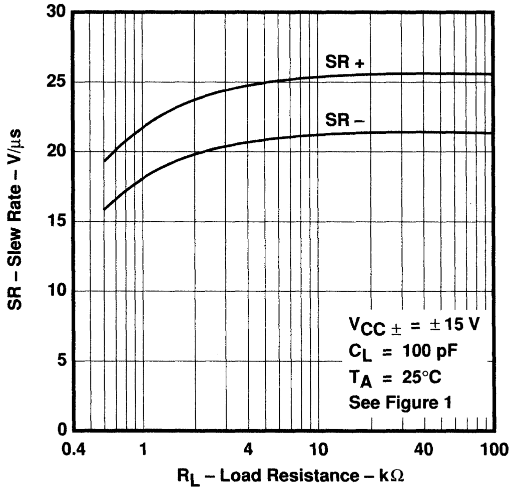


FIGURE 31

SLEW RATE
vs
FREE-AIR TEMPERATURE

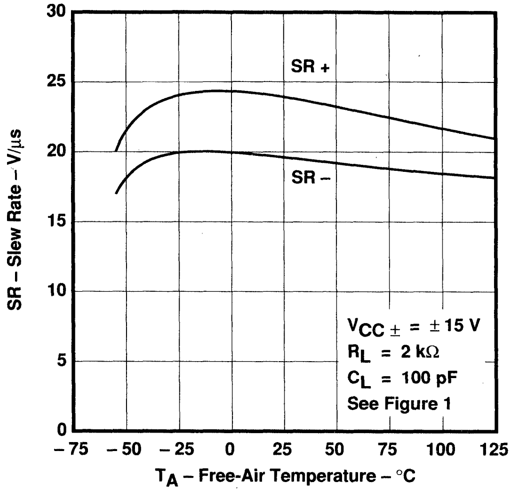


FIGURE 32

---

†Data at high and low temperatures are applicable within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

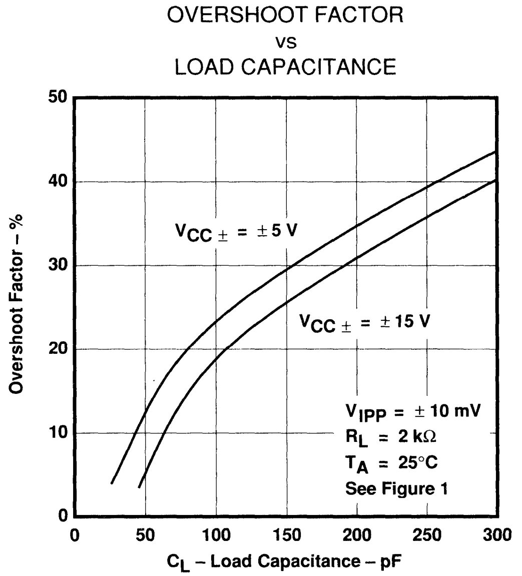


FIGURE 33

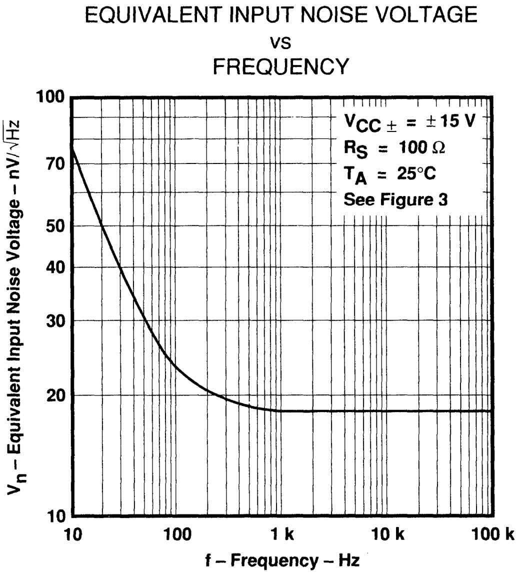


FIGURE 34

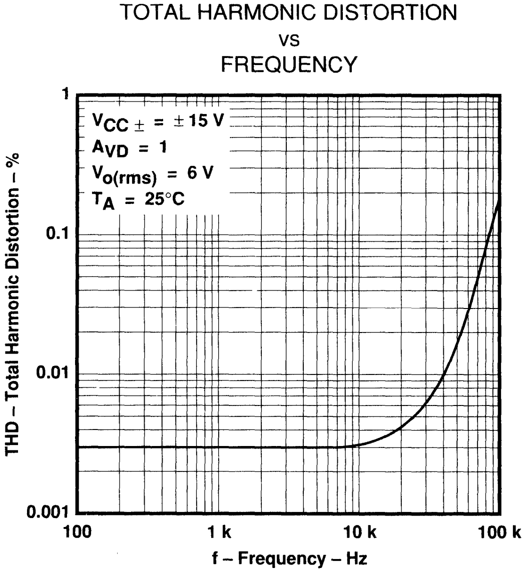


FIGURE 35

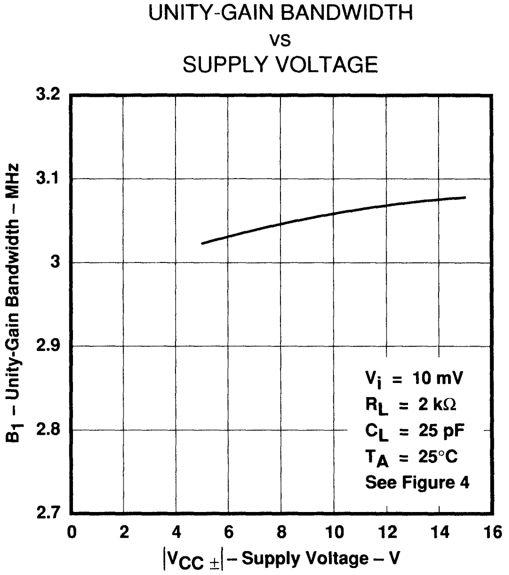


FIGURE 36

---

†Data at high and low temperatures are applicable within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

UNITY-GAIN BANDWIDTH
vs
FREE-AIR TEMPERATURE

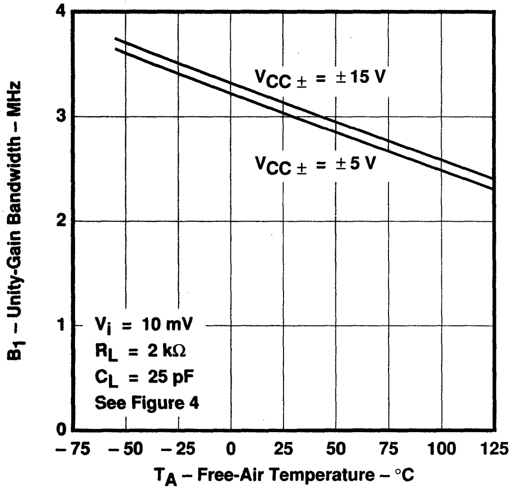


FIGURE 37

PHASE MARGIN
vs
SUPPLY VOLTAGE

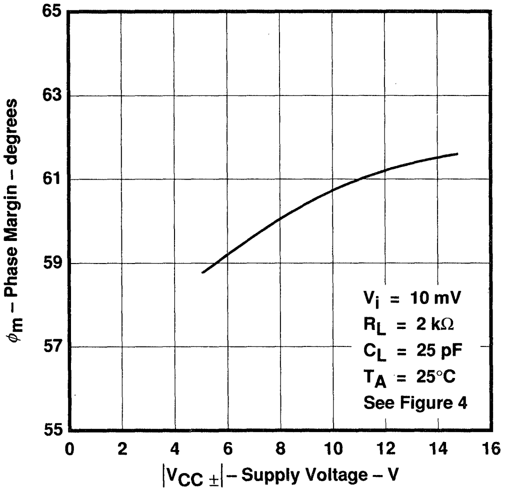


FIGURE 38

PHASE MARGIN
vs
LOAD CAPACITANCE

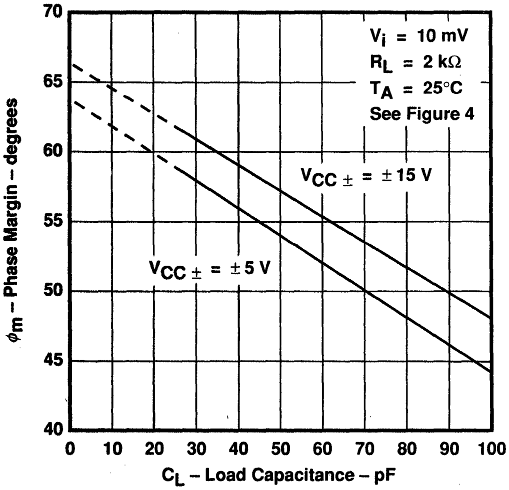


FIGURE 39

PHASE MARGIN
vs
FREE-AIR TEMPERATURE

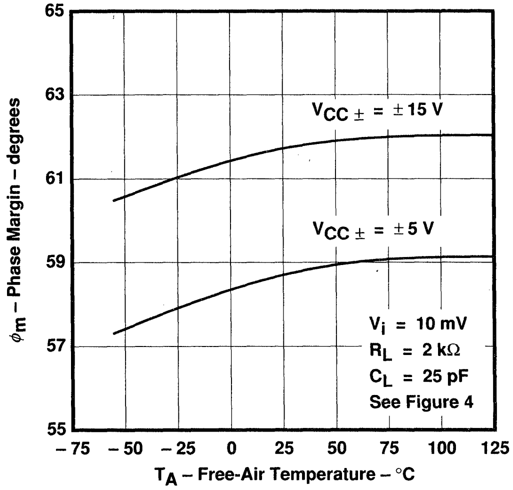


FIGURE 40

---

†Data at high and low temperatures are applicable within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS

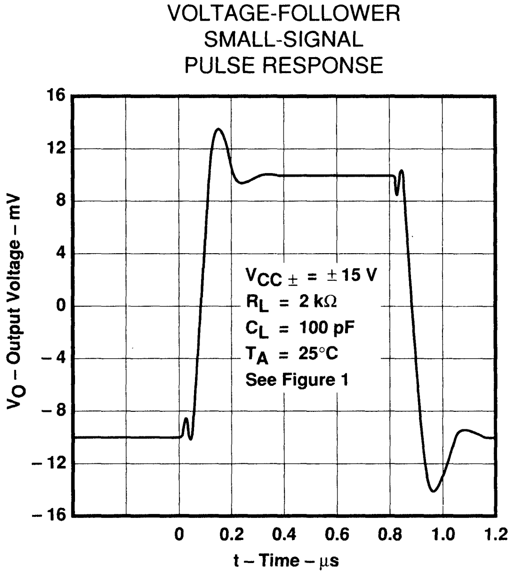


FIGURE 41

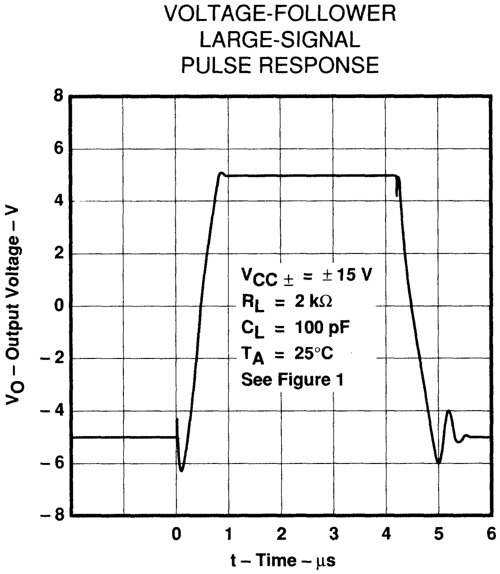
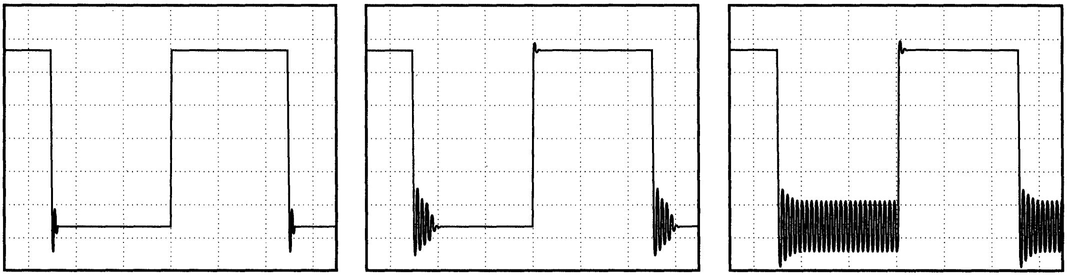


FIGURE 42

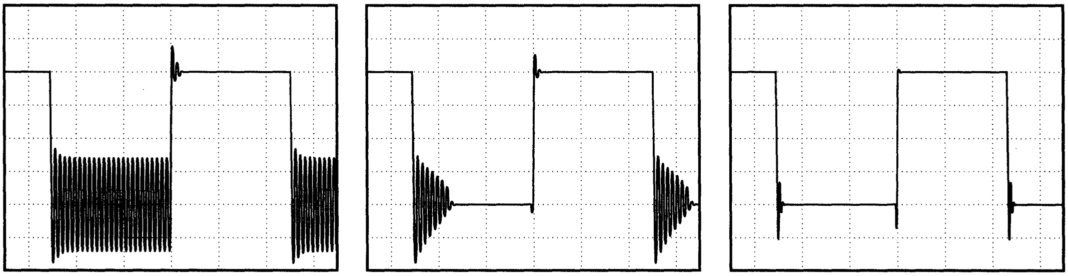
TYPICAL APPLICATION DATA

output characteristics

All operating characteristics are specified with 100-pF load capacitance. These amplifiers will drive higher capacitive loads; however, as the load capacitance increases, the resulting response pole occurs at lower frequencies, thereby causing ringing, peaking, or even oscillation. The value of the load capacitance at which oscillation occurs varies with production lots. If an application appears to be sensitive to oscillation due to load capacitance, adding a small resistance in series with the load should alleviate the problem. Capacitive loads of 1000 pF and larger may be driven if enough resistance is added in series with the output (see Figure 43).

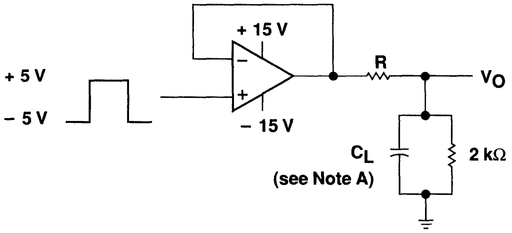


(a) C_L = 100 pF, R = 0 (b) C_L = 300 pF, R = 0 (c) C_L = 350 pF, R = 0



(d) C_L = 1000 pF, R = 0 (e) C_L 1000 pF, R = 50 Ω (f) C_L = 1000 pF, R = 2 kΩ

FIGURE 43. EFFECT OF CAPACITIVE LOADS



NOTE A: C_L includes fixture capacitance.

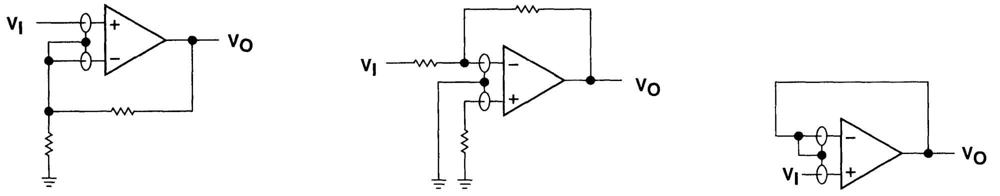
FIGURE 44. TEST CIRCUIT FOR OUTPUT CHARACTERISTICS

TYPICAL APPLICATION DATA

input characteristics

These amplifiers are specified with a minimum and a maximum input voltage that, if exceeded at either input, could cause the device to malfunction.

Because of the extremely high input impedance and resulting low bias current requirements, these amplifiers are well suited for low-level signal processing; however, leakage currents on printed circuit boards and sockets can easily exceed bias current requirements and cause degradation in system performance. It is good practice to include guard rings around inputs (see Figure 45). These guards should be driven from a low-impedance source at the same voltage level as the common-mode input.



(a) NONINVERTING AMPLIFIER (b) INVERTING AMPLIFIER (c) UNITY-GAIN AMPLIFIER

FIGURE 45. USE OF GUARD RINGS

noise performance

The noise specifications in op amp circuits are greatly dependent on the current in the first-stage differential amplifier. The low input bias current requirements of these amplifiers result in a very low current noise. This feature makes the devices especially favorable over bipolar devices when using values of circuit impedance greater than 50 kΩ.

TL2828Z, TL2828Y
HIGH-TEMPERATURE DUAL OPERATIONAL AMPLIFIERS

D3971, DECEMBER 1991

- **Operating Free-Air Temperature Range – 40°C to 150°C**
- **Wide Range of Supply Voltages:**
  Single Supply
  Or Dual Supplies . . . 4 V to 30 V
- **Low Supply Current Drain Indepedent of Supply Voltage . . . 0.7 mA Typ**
- **Internal Frequency Compensation**
- **Low Input Bias and Offset Parameters**
  Input Offset Voltage . . . 3 mV Typ
  Input Offset Current . . . 2 nA Typ
  Input Bias Current . . . 15 nA Typ
- **Differential Input Voltage Range Equal to Maximum-Rated Supply Voltage . . . 30 V**
- **Open-Loop Differential Voltage Amplification 100 V/mV Typ**

description

These devices consist of two independent high-gain frequency-compensated operational amplifiers that are designed specifically to operate over a wide range of voltages from a single supply. Operation from split supplies is also possible as long as the difference between the two supplies is 4 V to 30 V, and V_{CC} is at least 1.5 V more positive than the common-mode input voltage. The low supply current drain is independent of the magnitude of the supply voltage.

Applications include transducer amplifiers, dc amplification blocks, and all the conventional operational amplifier circuits that now can be implemented more easily in single-supply voltage systems. For example, the TL2828Z can be operated on automotive engine blocks directly off the standard 12-V supply with minimal electrical protection.

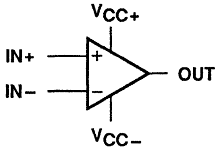
The TL2828Z is characterized for operation over the extended temperature range of – 40°C to 150°C.

AVAILABLE OPTIONS

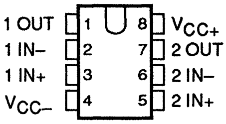
T_A	V_{IO} max AT 25°C	PACKAGE		
		SMALL-OUTLINE (D)	PLASTIC DIP (P)	CHIP FORM (Y)
– 40°C to 150°C	7 mV	TL2828ZD	TL2828ZP	TL2828Y

D packages are available taped and reeled. Add "R" suffix to device type (i.e., TL2828ZDR). The chip form is tested at T_A = 25°C.

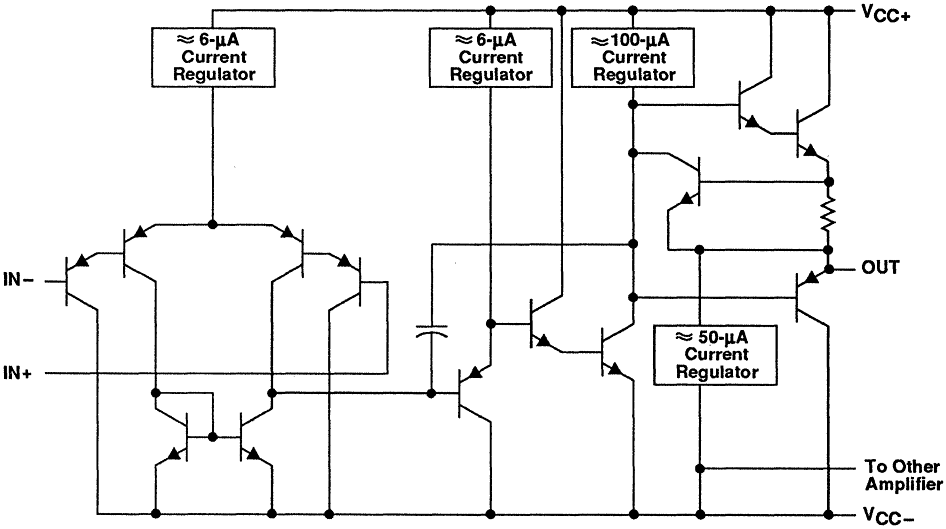
symbol (each amplifier)



TL2828Z . . . D OR P PACKAGE
(TOP VIEW)



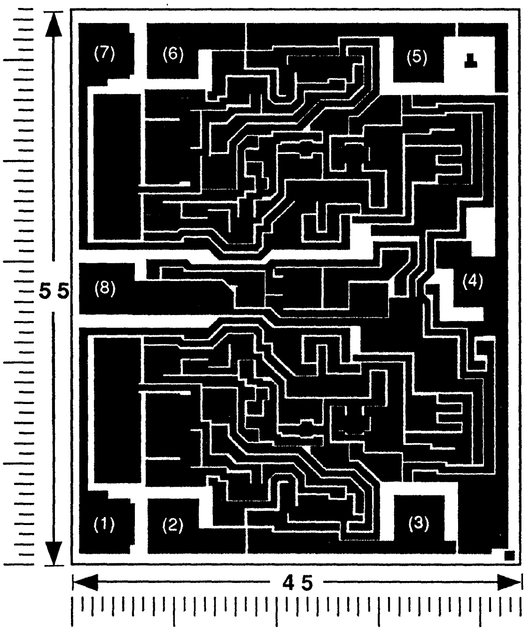
equivalent schematic (each amplifier)

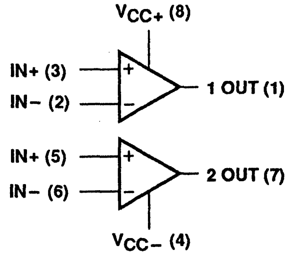


chip information

These chips, properly assembled, display characteristics similar to the TL2828Z. Thermal compression bonding may be used on the gold bonding pads. Chips may be mounted with conductive epoxy or a gold-silicon preform.

BONDING PAD ASSIGNMENTS





CHIP THICKNESS:
15 TYPICAL

BONDING PADS:
4 X 4 MINIMUM

$T_J$max = 165°C

TOLERANCES
ARE ± 10%

ALL DIMENSIONS ARE IN MILS

PIN (4) INTERNALLY CONNECTED
TO BACKSIDE OF THE CHIP

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC+} (see Note 1)	16 V
Supply voltage, V_{CC-}	−16 V
Differential input voltage (see Note 2)	± 32 V
Input voltage range, V_I (any input)	−16 to 16 V
Input current, I_I (each input)	± 1 mA
Output current, I_O	± 40 mA
Total current into V_{CC+} terminal	60 mA
Total current out of V_{CC-} terminal	60 mA
Duration of short-circuit current at (or below) 25°C (see Note 3)	unlimited
Continuous total dissipation	See Dissipation Rating Table
Operating free-air temperature range, T_A	– 40°C to 150°C
Storage temperature range	−65°C to 165°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C

NOTES: 1. All voltage values, except differential voltages, are with respect to the midpoint between V_{CC+} and V_{CC-} when dual supplies are specified (e.g., $V_{CC\pm} = \pm 15$ V) and with respect to V_{CC-} when a single supply is specified (e.g., $V_{CC} = 5$ V).

2. Differential voltages are at the noninverting input with respect to the inverting input. Excessive current will flow if the input is below V_{CC-}.

3. The output may be shorted to either supply. Temperature and/or supply voltages must be limited to ensure that the maximum dissipation rating is not exceeded.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 105°C$ POWER RATING	$T_A = 125°C$ POWER RATING	$T_A = 150°C$ POWER RATING
D	812 mW	5.8 mW/°C	551 mW	348 mW	232 mW	87 mW
P	1120 mW	8.0 mW/°C	760 mW	480 mW	320 mW	120 mW

recommended operating conditions

		MIN	MAX	UNIT
Supply voltage, $V_{CC\pm}$		± 2	± 15	V
Common-mode input voltage, V_{IC}	$V_{CC\pm} = \pm 2.5$ V	−2.5	0.5	V
	$V_{CC\pm} = \pm 15$ V	−15	13	
Input voltage range	$V_{CC\pm} = \pm 2.5$ V	−2.5	0.5	V
	$V_{CC\pm} = \pm 15$ V	−15	13	
Operating free-air temperature, T_A		– 40	150	°C

electrical characteristics at specified free-air temperature, V_{CC} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A†	MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	V_{IC} = 0, V_O = 1.4 V, R_S = 50 Ω	25°C		3	7	mV
			Full range			10	
α_{VIO}	Temperature coefficient of input offset voltage		Full range		15		µV/°C
I_{IO}	Input offset current		25°C		2	30	nA
			Full range			200	
I_{IB}	Input bias current		25°C		−15	−100	nA
			Full range			– 500	
V_{ICR}	Common-mode input voltage range	R_S = 50 Ω	25°C	0 to 3.5	0 to 3.5		V
			Full range	0 to 3			
V_{OH}	High-level output voltage	I_{OH} = 0.1 mA	25°C	3.3	3.7		V
			Full range	3.2			
		I_{OH} = 1 mA	25°C	3.3	3.6		
			Full range	3.2			
V_{OL}	Low-level output voltage	I_{OL} = 0.1 mA	25°C	0.8	0.6		V
			Full range	1			
		I_{OL} = 1 mA	25°C	0.9	0.7		
			Full range	1.1			
A_{VD}	Large-signal differential voltage amplification	V_O = 1 V to 3.5 V, R_L = 2 kΩ	25°C	25	100		V/mV
			Full range	0.7			
CMRR	Common-mode rejection ratio	V_{IC} = V_{ICR}min, V_O = 1.4 V, R_S = 50 Ω	25°C	65	80		dB
			Full range	45			
k_{SVR}	Supply-voltage rejection ratio	V_{CC} = 5 V to 30 V, V_O = 1.4 V, R_L = 10 kΩ	25°C	65	100		dB
			Full range	65			
I_{CC}	Supply current (total package)	V_{IC} = 0, V_O = 2.5 V, No load	25°C		0.7	1.2	mA
			Full range			1.2	
ΔI_{CC}	Supply current change over operating temperature range		Full range		140		µA

†Full range is – 40°C to 150°C.

electrical characteristics at specified free-air temperature, $V_{CC\pm}$ = ±15 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A†	MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	V_{IC} = 0, V_O = 0, R_S = 50 Ω	25°C		3	7	mV
			Full range			10	
α_{VIO}	Temperature coefficient of input offset voltage		Full range		15		µV/°C
I_{IO}	Input offset current		25°C		2	30	nA
			Full range			200	
I_{IB}	Input bias current		25°C		−15	−100	nA
			Full range			−500	
V_{ICR}	Common-mode input voltage range	R_S = 50 Ω	25°C	−15 to 13.5			V
			Full range	−15 to 13			
V_{OM+}	Maximum positive peak output voltage swing	I_O = − 0.1 mA	25°C	13.2	14.1		V
			Full range	13.1			
		I_O = −1 mA	25°C	13.1	14		
			Full range	13			
		I_O = −10 mA	25°C	12.8	13.6		
			Full range	12.7			
V_{OM-}	Maximum negative peak output voltage swing	I_O = 0.1 mA	25°C	−13.7	−14.4		V
			Full range	−13.1			
		I_O = 1 mA	25°C	−13.6	−14.3		
			Full range	−13			
		I_O = 7 mA	25°C	−12.9	−13.8		
			Full range	−12.5			
A_{VD}	Large-signal differential voltage amplification	R_L = 2 kΩ, V_O = −5 V to 5 V	25°C	25	100		V/mV
			Full range	0.8			
CMRR	Common-mode rejection ratio	V_{IC} = V_{ICR}min, V_O = 1.4 V, R_S = 50 Ω	25°C	65	75		dB
			Full range	50			
k_{SVR}	Supply-voltage rejection ratio	V_{CC} = 5 V to 30 V, R_L = 10 kΩ, V_O = 1.4 V	25°C	65	100		dB
			Full range	65			
I_{CC}	Supply current (total package)	V_{IC} = 0, V_O = 0, No load	25°C		0.7	2	mA
			Full range			2	
ΔI_{CC}	Supply current change over operating temperature range		Full range		140		µA

†Full range is – 40°C to 150°C.

operating characteristics at specified free-air temperature, $V_{CC\pm} = \pm 15$ V

PARAMETER		TEST CONDITIONS	T_A†	MIN	TYP	MAX	UNIT
SR+	Positive slew rate	$V_O = 1$ V to 4.5 V, $A_{VD} = 1$, $R_L = 2$ kΩ‡, $C_L = 100$ pF	25°C	0.15			V/µs
			Full range	0.1			
SR–	Negative slew rate		25°C	0.15			
			Full range	0.1			
V_n	Equivalent input noise voltage	f = 10 Hz	25°C		39		nV/√Hz
		f = 10 kHz			23		
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 10 Hz	25°C		0.9		µV
B_1	Unity-gain bandwidth	$R_L = 10$ kΩ‡, $C_L = 100$ pF	25°C		400		kHz
ϕ_m	Phase margin	$R_L = 10$ kΩ‡, $C_L = 100$ pF	25°C		60°		

† Full range is – 40°C to 150°C.
‡ R_L terminates at 0 V.

electrical characteristics at $V_{CC\pm}$ = ± 15 V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	V_{IC} = 0, V_O = 0, R_S = 50 Ω		3	7	mV
I_{IO}	Input offset current			2	30	nA
I_{IB}	Input bias current			−15	−100	
V_{ICR}	Common-mode input voltage range	R_S = 50 Ω	−15 to 13.5			V
V_{OM+}	Maximum positive peak output voltage swing	I_O = − 0.1 mA	13.2	14.1		V
		I_O = −1 mA	13.1	14		
		I_O = −10 mA	12.8	13.6		
V_{OM-}	Maximum negative peak output voltage swing	I_O = 0.1 mA	−13.7	−14.4		V
		I_O = 1 mA	−13.6	−14.3		
		I_O = 10 mA	−12.9	−13.8		
A_{VD}	Large-signal differential voltage amplification	V_O = 1 V to −1.5 V, R_L = 2 kΩ	25	100		V/mV
CMRR	Common-mode rejection ratio	V_{IC} = 0 to 28 V, V_O = 1.4 V, R_S = 50 Ω	65	75		dB
k_{SVR}	Supply-voltage rejection ratio	V_{CC} = 5 V to 30 V, V_O = 1.4 V, R_L = 10 kΩ	65	100		dB
I_{CC}	Supply current (total package)	V_{IC} = 0, V_O = 0, No load		0.7	2	mA

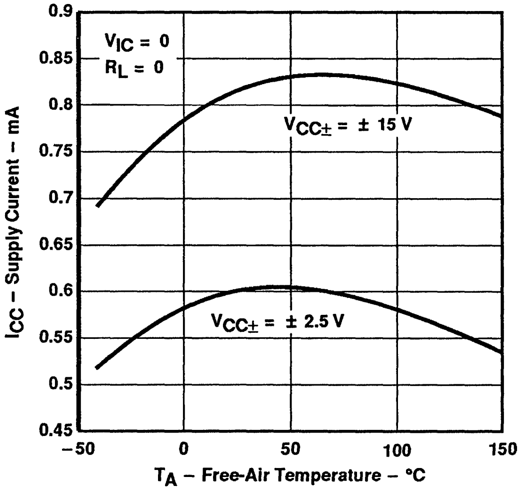
TL2829Z, TL2829Y
HIGH-TEMPERATURE QUADRUPLE OPERATIONAL AMPLIFIERS

D3827, APRIL 1991

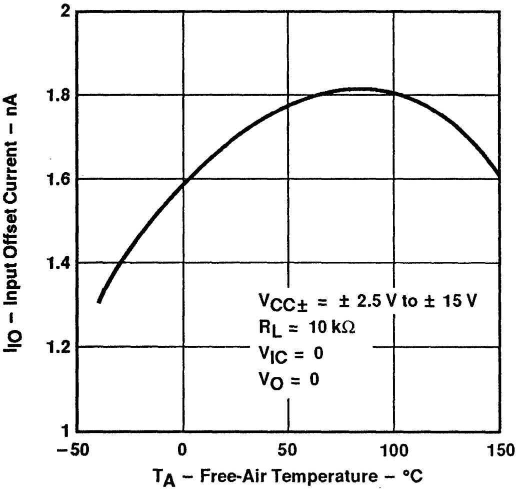
available features

- **Free-Air Operating Temperature Range – 40°C to 150°C**
- **Wide Range of Supply Voltages: Single Supply . . . 4 V to 30 V Or Dual Supplies**
- **Low Supply Current Drain Independent of Supply Voltage . . . 0.8 mA**
- **Internal Frequency Compensation**
- **Low Input Bias and Offset Parameters at 25°C**
  - **Input Offset Voltage . . . 3 mV Typ**
  - **Input Offset Current . . . 2 nA Typ**
  - **Input Bias Current . . . 15 nA Typ**
- **Differential Input Voltage Range Equal to Maximum-Rated Supply Voltage . . . 30 V**
- **Open-Loop Differential Voltage Amplification 100 V/mV Typ at 25°C**

SUPPLY CURRENT vs FREE-AIR TEMPERATURE



INPUT OFFSET CURRENT vs FREE-AIR TEMPERATURE



description

These devices consist of four independent, high-gain frequency-compensated operational amplifiers that are designed specifically to operate from a single supply over a wide range of voltages. Operation from split supplies is also possible as long as the difference between the two supplies is 4 V to 30 V, and V_{CC} is at least 1.5 V more positive than the input common-mode voltage. The low supply current drain is independent of the magnitude of the supply voltage.

AVAILABLE OPTIONS

T_A	V_{IO} max AT 25°C	PACKAGE		
		SMALL-OUTLINE (D)	PLASTIC DIP (N)	CHIP FORM (Y)
– 40°C to 150°C	7 mV	TL2829ZD	TL2829ZN	TL2829Y

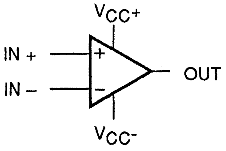
†D packages are available taped and reeled. Add “R” suffix to device type, (i.e., TL2829ZDR).

TEXAS INSTRUMENTS
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

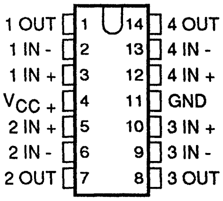
Applications include transducer amplifiers, d-c amplification blocks, and all the conventional operational amplifier circuits that now can be implemented more easily in single-supply-voltage systems. For example, the TL2829 can be operated on automotive engine blocks directly off the standard 12-V supply with minimal electrical protection.

The TL2829 is characterized for operation over the extended (Z) temperature range of – 40°C to 150°C.

symbol (each amplifier)



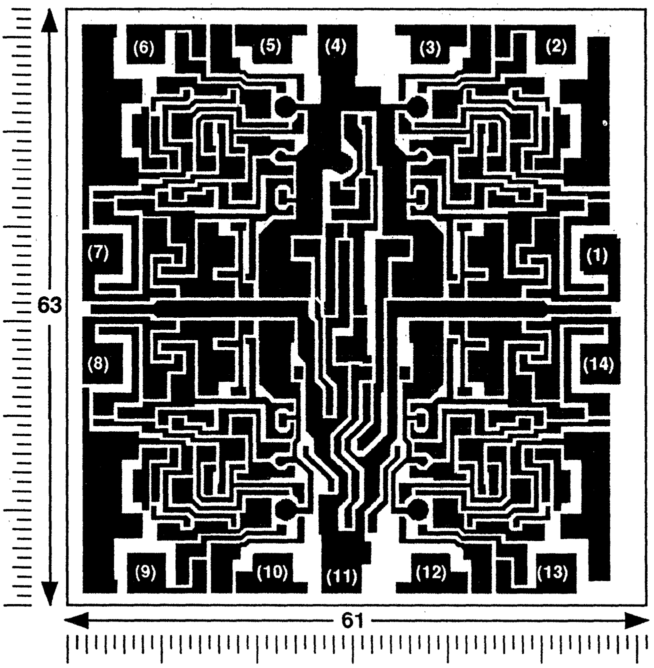
TL2829Z . . . D OR N PACKAGE
(TOP VIEW)

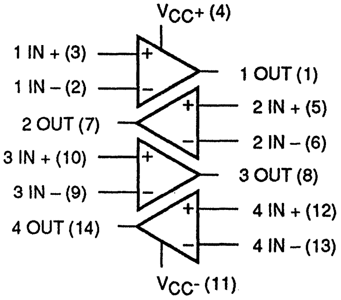


chip information

These chips, properly assembled, display characteristics similar to the TL2829. Thermal compression bonding may be used on the gold bonding pads. Chips may be mounted with conductive epoxy or a gold-silicon preform.

BONDING PAD ASSIGNMENTS





CHIP THICKNESS:
15 TYPICAL

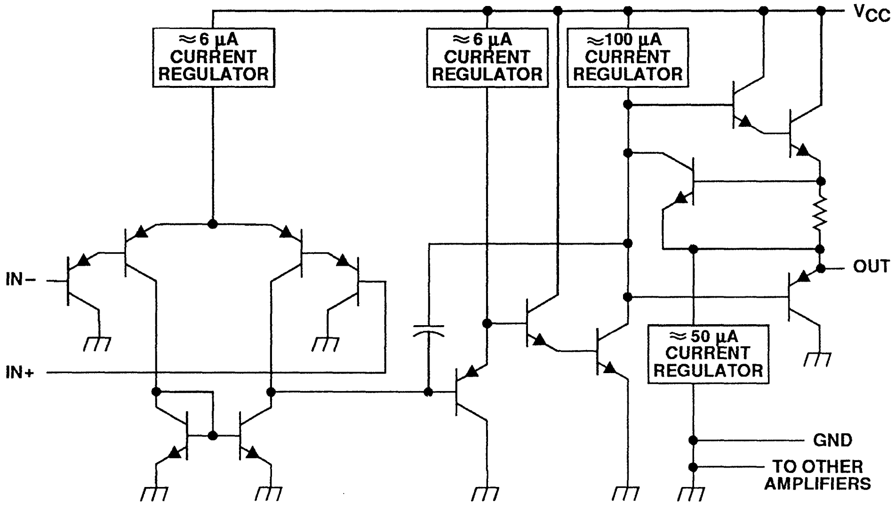
BONDING PADS:
4 X 4 MINIMUM

$T_J$max = 165°C

TOLERANCES
ARE ± 10%

ALL DIMENSIONS
ARE IN MILS

equivalent schematic (each amplifier)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC+} (see Note 1)	16 V
Supply voltage, V_{CC-}	– 16 V
Differential input voltage (see Note 2)	± 32 V
Input voltage range, V_I (any input)	– 16 to 16 V
Input current, I_I (each input)	± 1 mA
Output current, I_O	± 40 mA
Total current into V_{CC+} terminal	60 mA
Total current out of V_{CC-} terminal	60 mA
Duration of short-circuit current at (or below) 25°C (see Note 3)	unlimited
Continuous total dissipation	See Dissipation Rating Table
Operating free-air temperature range, T_A: Z-suffix	– 40°C to 150°C
Storage temperature range	– 65°C to 165°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D or N package	300°C

NOTES: 1. All voltage values, except differential voltages, are with respect to the midpoint between V_{CC+} and V_{CC-} when dual supplies are specified (e.g., $V_{CC\pm} = \pm 15$ V) and with respect to V_{CC-} when a single supply is specified (e.g., $V_{CC} = 5$ V).

2. Differential voltages are at the noninverting input with respect to the inverting input. Excessive current will flow if input is brought below V_{CC-}.

3. The output may be shorted to either supply. Temperature and/or supply voltages must be limited to ensure that the maximum dissipation rating is not exceeded.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 100°C$ POWER RATING	$T_A = 125°C$ POWER RATING	$T_A = 150°C$ POWER RATING
D	1064 mW	7.6 mW/°C	722 mW	494 mW	304mW	114 mW
N	1764 mW	12.6 mW/°C	1197 mW	819 mW	504 mW	189 mW

recommended operating conditions

		MIN	MAX	UNIT
Supply voltage, $V_{CC\pm}$		± 2	± 15	V
Common-mode input voltage, V_{IC}	$V_{CC\pm} = \pm 2.5$ V	– 2.5	0.5	V
	$V_{CC\pm} = \pm 15$ V	– 15	13	
Input voltage range	$V_{CC\pm} = \pm 2.5$ V	– 2.5	0.5	V
	$V_{CC\pm} = \pm 15$ V	– 15	13	
Operating free-air temperature, T_A: Z-suffix		– 40	150	°C

electrical characteristics at specified free-air temperature, V_{CC} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A†	MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	V_O = 1.4 V, V_{IC} = 0, R_S = 50 Ω	25°C		3	7	mV
			Full range			10	
α_{VIO}	Temperature coefficient of input offset voltage		Full range		15		µV/°C
I_{IO}	Input offset current		25°C		2.0	30	nA
			Full range			200	
I_{IB}	Input bias current		25°C		– 12	– 100	nA
			Full range			– 500	
V_{ICR}	Common-mode input voltage range	R_S = 50 Ω	25°C	0 to 3.5	0 to 3.5		V
			Full range	0 to 3			
V_{OH}	High-level output voltage	I_{OH} = 0.1 mA	25°C	3.3	3.7		V
			Full range	3.2			
		I_{OH} = 1 mA	25°C	3.3	3.6		
			Full range	3.2			
V_{OL}	Low-level output voltage	I_{OL} = 0.1 mA	25°C	0.8	0.6		V
			Full range	1			
		I_{OL} = 1 mA	25°C	0.9	0.7		
			Full range	1.1			
A_{VD}	Large-signal differential voltage amplification	V_O = 1 V to 3.5 V, R_L = 2 kΩ	25°C	25	60		V/mV
			Full range	0.7			
CMRR	Common-mode rejection ratio	V_O = 1.4 V, V_{IC} = V_{ICR}min, R_S = 50 Ω	25°C	65	81		dB
			Full range	50			
k_{SVR}	Supply-voltage rejection ratio	V_{CC} = 5 V to 30 V, V_O = 1.4 V, R_L = 10 kΩ	25°C	65	103		dB
			Full range	65			
I_{CC}	Supply current (total package)	V_O = 2.5 V, V_{IC} = 0, No load	25°C		0.6	1.2	mA
			Full range			1.2	
ΔI_{CC}	Supply current change over operating temperature range		Full range		140		µA

† Full range is – 40°C to 150°C.

electrical characteristics at specified free-air temperature, $V_{CC\pm}$ = ± 15 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A†	MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	$V_O = 0$, $R_S = 50\ \Omega$, $V_{IC} = 0$	25°C		3	7	mV
			Full range			10	
α_{VIO}	Temperature coefficient of input offset voltage		Full range		15		µV/°C
I_{IO}	Input offset current		25°C		2	30	nA
			Full range			200	
I_{IB}	Input bias current		25°C		– 15	– 100	nA
			Full range			– 500	
V_{ICR}	Common-mode input voltage range	$R_S = 50\ \Omega$	25°C	– 15 to 13.5			V
			Full range	– 15 to 13			
V_{OM+}	Maximum positive peak output voltage swing	$I_O = -0.1$ mA	25°C	13.2	14.1		V
			Full range	13.1			
		$I_O = -1$ mA	25°C	13.1	14		
			Full range	13			
		$I_O = -10$ mA	25°C	12.8	13.6		
			Full range	12.7			
V_{OM-}	Maximum negative peak output voltage swing	$I_O = 0.1$ mA	25°C	– 13.7	– 14.4		V
			Full range	– 13.1			
		$I_O = 1$ mA	25°C	– 13.6	– 14.3		
			Full range	– 13			
		$I_O = 10$ mA	25°C	– 12.9	– 13.8		
			Full range	– 12.9			
A_{VD}	Large-signal differential voltage amplification	$R_L = 2\ k\Omega$, $V_O = -5$ V to 5 V	25°C	25	210		V/mV
			Full range	0.8			
CMRR	Common-mode rejection ratio	$V_O = 1.4$ V, $R_S = 50\ \Omega$ $V_{IC} = V_{ICR}\text{min}$	25°C	65	75		dB
			Full range	50			
k_{SVR}	Supply-voltage rejection ratio	$V_{CC} = 5$ V to 30 V, $R_L = 10\ k\Omega$, $V_O = 1.4$ V	25°C	65	103		dB
			Full range	65			
I_{CC}	Supply current (total package)	$V_O = 0$, $V_{IC} = 0$, No load	25°C		0.8	3	mA
			Full range			3	
ΔI_{CC}	Supply current change over operating temperature range		Full range		140		µA

† Full range is – 40°C to 150°C.

operating characteristics at specified free-air temperature, $V_{CC\pm}$ = ± 15 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A†	MIN	TYP	MAX	UNIT
SR +	Positive slew rate	V_{CC} = 15 V, V_O = 1 V to 4.5 V, A_{VD} = 1, R_L = 2 kΩ‡, C_L = 100 pF	25°C	0.2			V/µs
			Full range	0.1			
SR –	Negative slew rate		25°C	0.25			
			Full range	0.2			
V_n	Equivalent input noise voltage	f = 10 Hz	25°C		39		nV/√Hz
		f = 10 kHz			23		
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 10 Hz	25°C		0.9		µV
B_n	Unity-gain bandwidth	R_L = 10 kΩ‡, C_L = 100 pF	25°C		400		kHz
ϕ_m	Phase margin at unity-gain	R_L = 10 kΩ‡, C_L = 100 pF	25°C		60°		

† Full range is – 40°C to 150°C.

‡ R_L terminates at 0 V.

electrical characteristics at $V_{CC\pm}$ = ± 15 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	V_O = 0, V_{IC} = 0, R_S = 50 Ω		3	7	mV
I_{IO}	Input offset current			2	30	nA
I_{IB}	Input bias current			− 15	− 100	
V_{ICR}	Common-mode input voltage range	R_S = 50 Ω	− 15 to 13.5			V
V_{OM+}	Maximum positive peak output voltage swing	I_O = − 0.1 mA	13.2	14.1		V
		I_O = − 1 mA	13.1	14		
		I_O = − 10 mA	12.8	13.6		
V_{OM-}	Maximum negative peak output voltage swing	I_O = 0.1 mA	− 13.7	− 14.4		V
		I_O = 1 mA	− 13.6	− 14.3		
		I_O = 10 mA	− 12.9	− 13.8		
A_{VD}	Large-signal differential voltage amplification	V_O = 1 V to − 1.5 V, R_L = 2 kΩ	25	210		V/mV
CMRR	Common-mode rejection ratio	V_O = 1.4 V, V_{IC} = 0 to 28 V, R_S = 50 Ω	65	75		dB
k_{SVR}	Supply-voltage rejection ratio	V_{CC} = 5 V to 30 V, V_O = 1.4 V, R_L = 10 kΩ	65	103		dB
I_{CC}	Supply current (total package)	V_O = 0, V_{IC} = 0, No load		0.8	3	mA

TYPICAL CHARACTERISTICS

TABLE OF GRAPHS			FIGURE
I_{IO}	Input offset current	vs Temperature	1
I_{IB}	Input bias current	vs Temperature (V_{CC} = ± 2.5 V)	2
		vs Temperature (V_{CC} = ± 15 V)	3
V_{OM+}	High-level output voltage	vs Temperature (V_{CC} = ± 2.5 V)	4
		vs Temperature (V_{CC} = ± 15 V)	5
V_{OM-}	Low-level output voltage	vs Temperature (V_{CC} = ± 2.5 V)	6
		vs Temperature (V_{CC} = ± 15 V)	7
I_{OS}	Short-circuit output current	vs Temperature (V_{ID} = 1 V)	8
		vs Temperature (V_{ID} = − 1 V)	9
A_{VD}	Differential voltage amplification	vs Temperature	10
CMRR	Common-mode rejection ratio	vs Temperature	11
k_{SVR}	Supply-voltage rejection ratio	vs Temperature	12
I_{CC}	Supply current	vs Temperature	13
SR+	Positive slew rate	vs Temperature	14
SR-	Negative slew rate	vs Temperature	15
	Equivalent input noise voltage	Over a 10-second period	16

TYPICAL CHARACTERISTICS

INPUT OFFSET CURRENT vs FREE-AIR TEMPERATURE

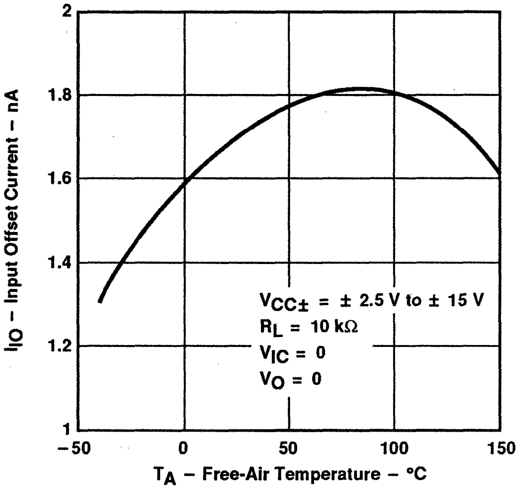


Figure 1

INPUT BIAS CURRENT vs FREE-AIR TEMPERATURE

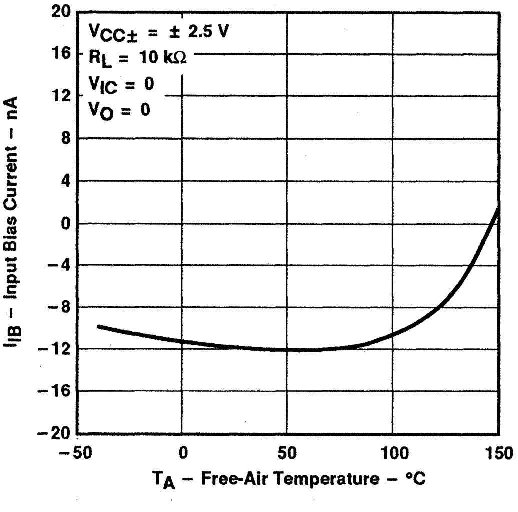


Figure 2

INPUT BIAS CURRENT vs FREE-AIR TEMPERATURE

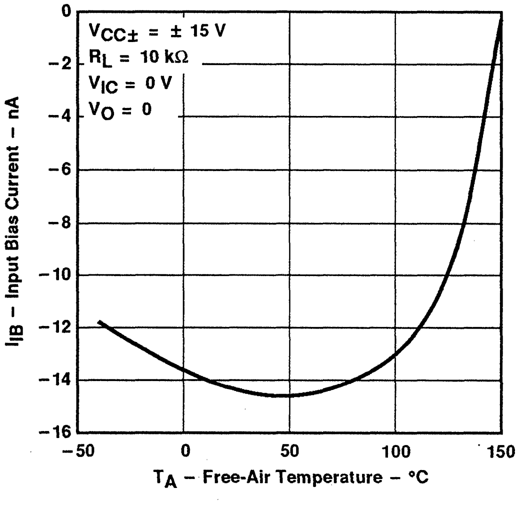


Figure 3

TYPICAL CHARACTERISTICS

MAXIMUM POSITIVE PEAK OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

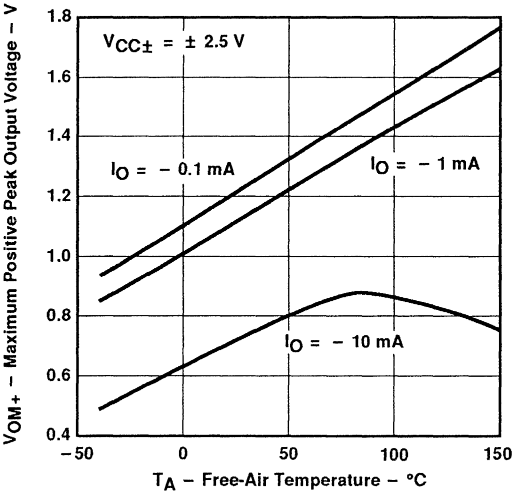


Figure 4

MAXIMUM POSITIVE PEAK OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

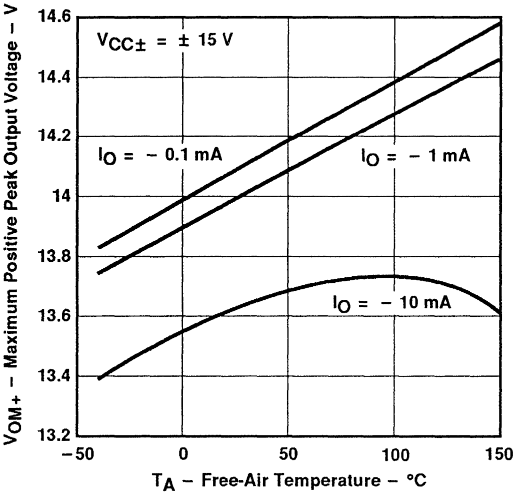


Figure 5

MAXIMUM NEGATIVE PEAK OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

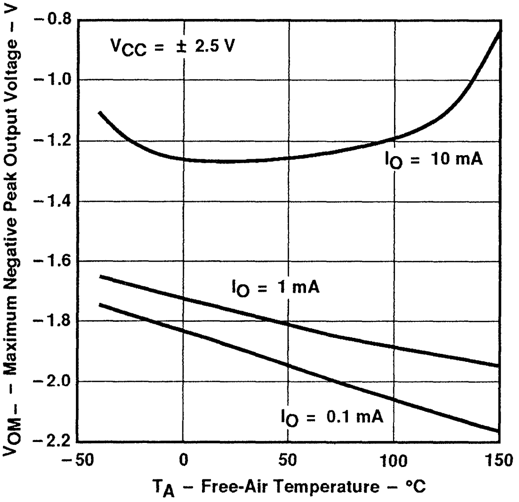


Figure 6

MAXIMUM NEGATIVE PEAK OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

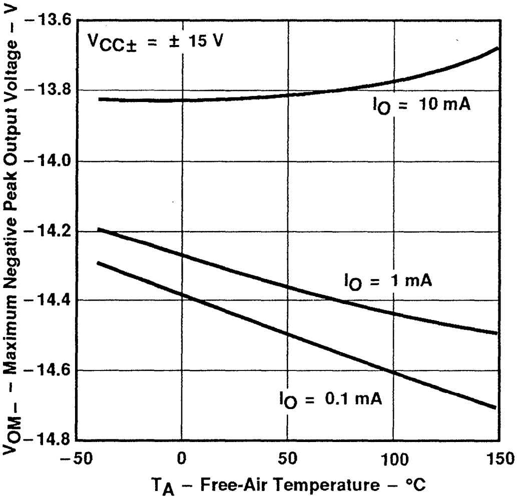


Figure 7

TYPICAL CHARACTERISTICS

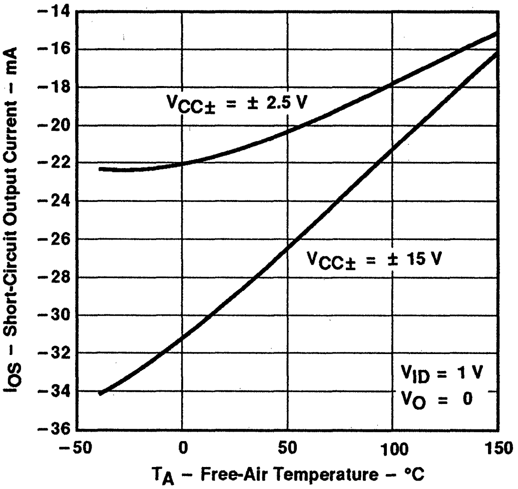

SHORT-CIRCUIT OUTPUT CURRENT
vs
FREE-AIR TEMPERATURE

Figure 8

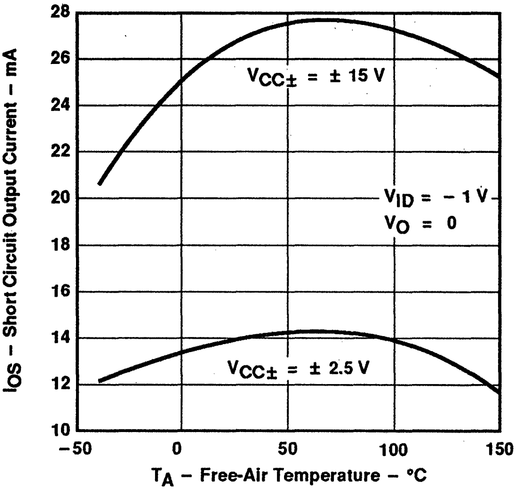

SHORT-CIRCUIT OUTPUT CURRENT
vs
FREE-AIR TEMPERATURE

Figure 9

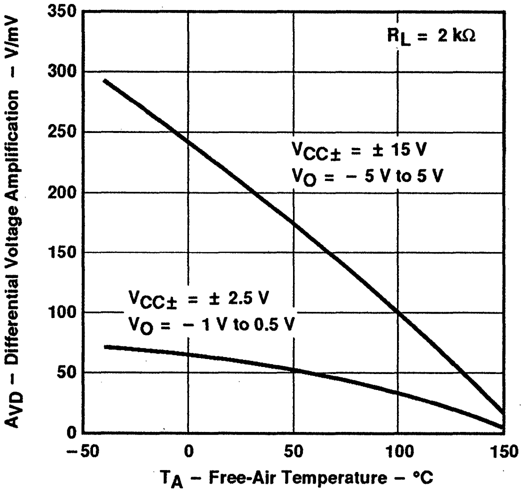

LARGE-SIGNAL VOLTAGE AMPLIFICATION
vs
FREE-AIR TEMPERATURE

Figure 10

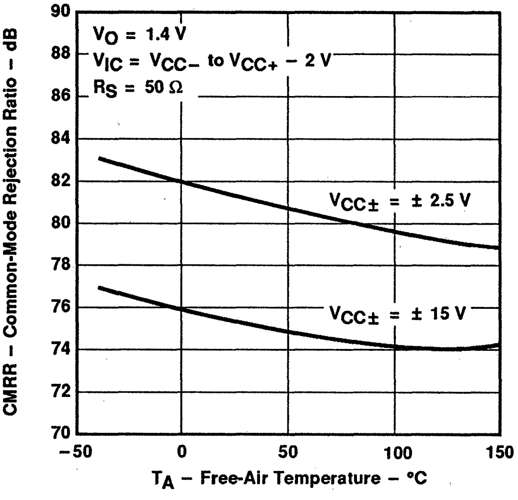

COMMON-MODE REJECTION RATIO
vs
FREE-AIR TEMPERATURE

Figure 11

TYPICAL CHARACTERISTICS

SUPPLY-VOLTAGE REJECTION RATIO vs FREE-AIR TEMPERATURE

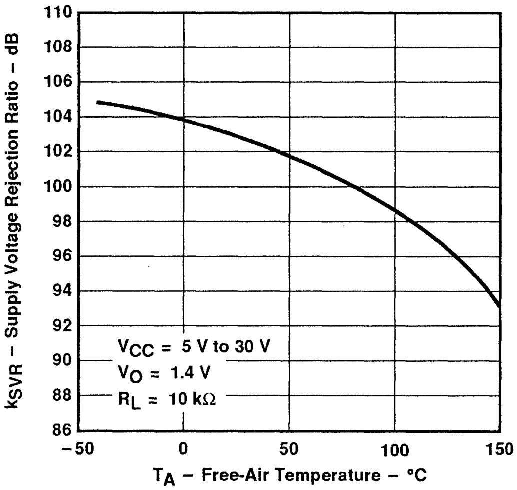


Figure 12

SUPPLY CURRENT vs FREE-AIR TEMPERATURE

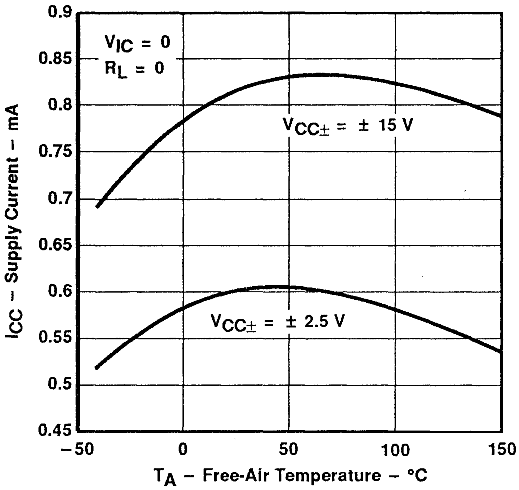


Figure 13

POSITIVE SLEW RATE vs FREE-AIR TEMPERATURE

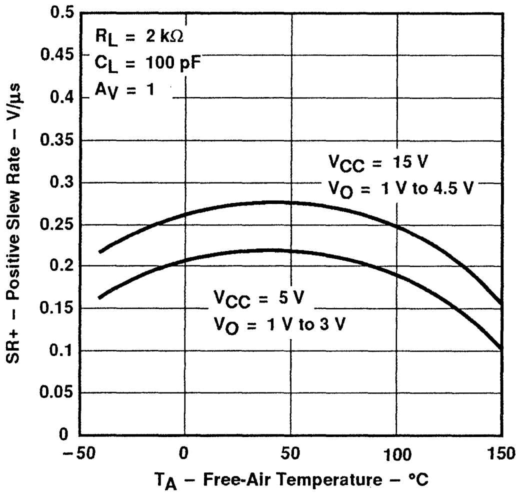


Figure 14

NEGATIVE SLEW RATE vs FREE-AIR TEMPERATURE

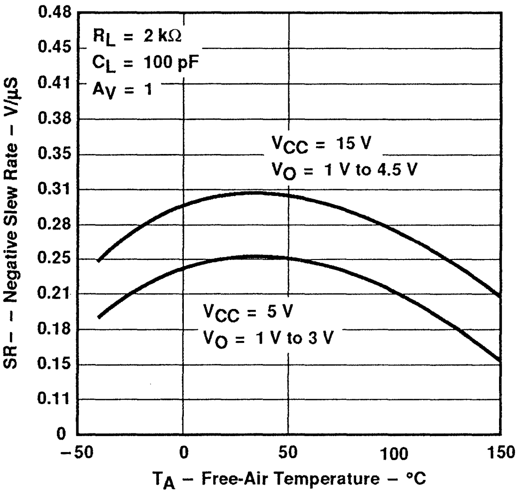


Figure 15

TYPICAL CHARACTERISTICS

EQUIVALENT INPUT NOISE VOLTAGE OVER A 10-SECOND PERIOD

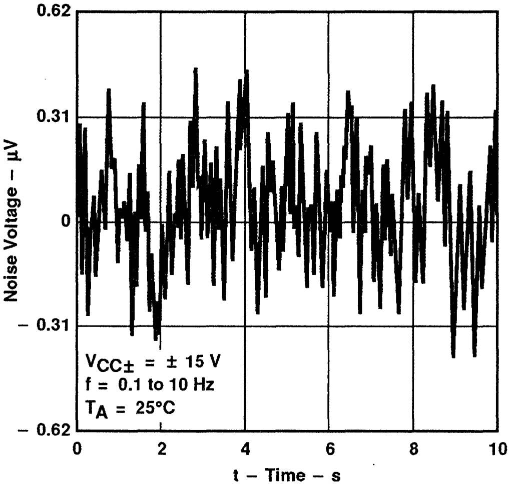


Figure 16

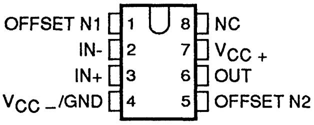
TL33071, TL33072, TL33074, TL34071,TL34072,TL34074
TL35071, TL35072, TL35074
HIGH-SLEW-RATE, SINGLE-SUPPLY OPERATIONAL AMPLIFIERS

D3825, MARCH 1991 – REVISED JULY 1991

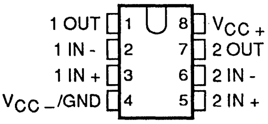
available features

- Wide Gain-Bandwidth Product . . . 4.5 MHz
- High Slew Rate . . . 13 V/μs
- Fast Settling Time . . . 1.1 μs to 0.1 %
- Wide-Range Single-Supply Operation
  4 V to 44 V
- Wide Input Common-Mode Range Includes Ground (V_{CC-})
- Low Total Harmonic Distortion . . . 0.02 %
- Low Input Offset Voltage . . . 3 mV Max (A Suffix)
- Large Output Voltage Swing
  – 14.7 V to 14 V (With ± 15-V Supplies)
- Large Capacitance Drive Capability
  0 to 10,000 pF
- Excellent Phase Margin . . . 60°
- Excellent Gain Margin . . . 12 dB
- Output Short-Circuit Protection

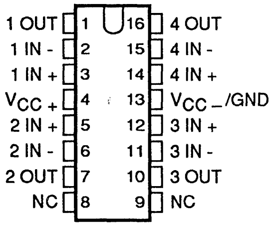
D-8 OR P PACKAGE
(SINGLE, TOP VIEW)



D-8 OR P PACKAGE
(DUAL, TOP VIEW)

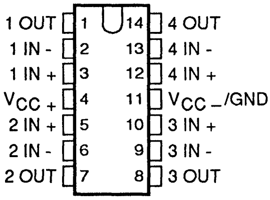


DW PACKAGE
(QUAD, TOP VIEW)



NC – No internal connection

N PACKAGE
(QUAD, TOP VIEW)



AVAILABLE OPTIONS

T_A	COMPLEXITY	PACKAGE			
		PLASTIC DIP		SMALL OUTLINE	
		STANDARD GRADE	PRIME GRADE	STANDARD GRADE	PRIME GRADE
0°C	Single	TL34071P	TL34071AP	TL34071D	TL34071AD
to	Dual	TL34072P	TL34072AP	TL34072D	TL34072AD
70°C	Quad	TL34074N	TL34074AN	TL34074DW	TL34074ADW
– 40°C	Single	TL33071P	TL33071AP	TL33071D	TL33071AD
to	Dual	TL33072P	TL33072AP	TL33072D	TL33072AD
105°C	Quad	TL33074N	TL33074AN	TL33074DW	TL33074ADW
– 55°C	Single	TL35071P	TL35071AP	TL35071D	TL35071AD
to	Dual	TL35072P	TL35072AP	TL35072D	TL35072AD
125°C	Quad	TL35074N	TL35074AN	TL35074DW	TL35074ADW

D packages are available taped and reeled. Add "R" suffix to device type (e.g.,TL34071ADR).

TEXAS INSTRUMENTS
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

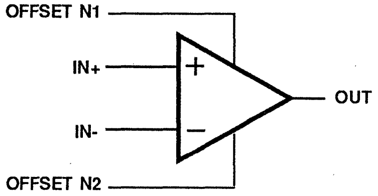
description

Quality, low cost, bipolar fabrication with innovative design concepts are employed for the TL33071/2/4, TL34071/2/4, and TL35071/2/4 series of monolithic operational amplifiers. This series of operational amplifiers offer 4.5 MHz of gain bandwidth product, 13 V/µs slew rate and fast settling time without the use of JFET device technology. Although this series can be operated from split supplies, it is particularly suited for single-supply operation, since the common-mode input voltage range includes ground potential (V_{CC-}). With a Darlington input stage, this series exhibits high input resistance, low input offset voltage, and high gain. The all-NPN output stage, characterized by no dead-band crossover distortion and large output voltage swing, provides high-capacitance drive capability, excellent phase and gain margins, low open-loop high-frequency output impedance, and symmetrical source/sink ac frequency response.

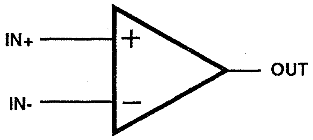
The TL33071/2/4, TL34071/1/4, and TL35071/2/4 series of devices are available in standard or prime performance (A-Suffix) grades and are specified over the commercial (0°C to 70°C), industrial/vehicular (– 40°C to 105°C) or military (– 55°C to 125°C) temperature ranges. These low-cost amplifiers are available in single, dual and quad configurations and are pin-compatible with the (low-cost) MC33071/2/4, MC34071/2/4, and MC35071/2/4 series of amplifiers. Packaging options include standard plastic DIP and SO packages.

symbol

SINGLE



DUAL AND QUAD
(PER AMPLIFIER)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC+} (see Note 1)	22 V
Supply voltage, V_{CC-}	−22 V
Differential input voltage (see Note 2)	±44 V
Input voltage range, V_I (any input)	$V_{CC\pm}$
Input current, I_I (each input)	±1 mA
Output current, I_O	±80 mA
Total current into V_{CC+} terminal	80 mA
Total current out of V_{CC-} terminal	80 mA
Duration of short-circuit current at (or below) 25°C (see Note 3)	unlimited
Continuous total dissipation	See Dissipation Rating Table
Operating free-air temperature range, TA: TL3307_	− 40°C to 105°C
TL3407_	0°C to 70°C
TL3507_	− 55°C to125°C
Storage temperature range	− 65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D, DW, N, or P package	260°C

NOTES: 1. All voltage values, except differential voltages, are with respect to the midpoint between V_{CC+} and V_{CC-}.
2. Differential voltages are at the noninverting input with respect to the inverting input. Excessive current will flow if input is brought below $V_{CC-} - 0.3$ V.
3. The output may be shorted to either supply. Temperature and/or supply voltages must be limited to ensure that the maximum dissipation rating is not exceeded.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 105°C$ POWER RATING	$T_A = 125°C$ POWER RATING
D-8	725 mW	5.8 mW/°C	464 mW	261 mW	145 mW
DW	1025 mW	8.2 mW/°C	656 mW	369 mW	205 mW
N	1150 mW	9.2 mW/°C	736 mW	414 mW	230 mW
P	1000 mW	8.0 mW/°C	640 mW	360 mW	200 mW

recommended operating conditions

		TL3307_		TL3407_		TL3507_		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
Supply voltage, $V_{CC\pm}$		± 2	± 22	± 2	± 22	± 2	± 22	V
Common-mode input voltage, V_{IC}	$V_{CC} = 5$ V	0	2.7	0	2.9	0	2.7	V
	$V_{CC\pm} = \pm15$ V	− 15	12.7	− 15	12.9	− 15	12.7	
Operating free-air temperature, T_A		− 40	105	0	70	− 55	125	°C

electrical characteristics at specified free-air temperature, $V_{CC\pm}$ = ±15 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A†	A SUFFIX			NON-A SUFFIX			UNIT
					MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IO}	Input offset voltage	V_{IC} = 0, V_O = 0, R_S = 50 Ω	V_{CC} = 5 V	25°C		0.5	3		1.5	5	mV
			V_{CC} = ±15 V	25°C		0.5	3		1.0	5	
				Full range			5			7	
α_{VIO}	Temperature coefficient of input offset voltage		V_{CC} = ±15 V	Full range		10			10		µV/°C
I_{IO}	Input offset current		V_{CC} = ±15 V	25°C		6	50		6	50	nA
				Full range			300			300	
I_{IB}	Input bias current		V_{CC} = 5 V	25°C		− 0.8	− 2		− 0.8	− 2	µA
				Full range			− 2.3			− 2.3	
			V_{CC} = ±15 V	25°C		− 0.7	− 1.5		− 0.7	− 1.5	
				Full range			− 1.6			− 1.6	
V_{ICR}	Common-mode input voltage range	R_S = 50 Ω		25°C	− 15 V to 13.2 V			− 15 V to 13.2 V			V
				Full range	− 15 V to 12.8 V			− 15 V to 12.8 V			
V_{OH}	High-level output voltage	V_{CC+} = 5 V, V_{CC-} = 0, R_L = 2 kΩ		25°C	3.7	4		3.7	4		V
		R_L = 10 kΩ		25°C	13.6	14		13.6	14		
		R_L = 2 kΩ		Full range	13.4			13.4			
V_{OL}	Low-level output voltage	V_{CC+} = 5 V, V_{CC-} = 0, R_L = 2 kΩ		25°C		0.1	0.3		0.1	0.3	V
		R_L = 10 kΩ		25°C		− 14.7	− 14.3		− 14.7	− 14.3	
		R_L = 2 kΩ		Full range			− 13.5			− 13.5	
A_{VD}	Large-signal differential voltage amplification	V_O = ± 10 V, R_L = 2 kΩ		25°C	50	100		25	100		V/mV
				Full range	25			20			
I_{OS}	Short-circuit output current	Source: V_{ID} = 1 V, V_O = 0		25°C	−10	−30		−10	−30		mA
		Sink: V_{ID} = −1 V, V_O = 0			20	30		20	30		
CMRR	Common-mode rejection ratio	V_{IC} = V_{ICR} min, R_S = 50 Ω		25°C	80	97		70	97		dB
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm} / \Delta V_{IO}$)	$V_{CC\pm}$ = ± 13.5 V to ± 16.5 V, R_S = 100 Ω		25°C	80	97		70	97		dB
I_{CC}	Supply current (per channel)	V_O = 0, No Load		25°C		3.5	4.5		3.5	4.5	mA
				Full range			4.7			4.7	
		V_{CC+} = 5 V, V_{CC-} = 0, V_O = 0, No Load		25°C		3.4	4.4		3.4	4.4	
				Full range			4.6			4.6	

†Full range is 0°C to 70°C for the TL3407_ devices, – 40°C to 105°C for the TL3307_ devices, and – 55°C to 125°C for the TL3507_ devices.
‡All typical values are at T_A = 25°C.

operating characteristics at $V_{CC\pm}$ = ±15 V, T_A = 25°C

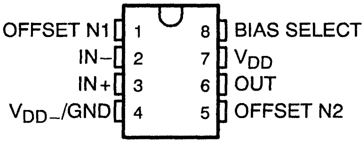
PARAMETER		TEST CONDITIONS		A SUFFIX			NON-A SUFFIX			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
SR +	Positive slew rate	V_I = – 10 V to 10 V, R_L = 2 kΩ	A_V = 1	8	10		8	10		V/μs
SR –	Negative slew rate		A_V = – 1		13			13		
	Settling time	A_{VD} = – 1, 10-V Step	To 0.1%		1.1			1.1		μs
			To 0.01%		2.2			2.2		
V_n	Equivalent input noise voltage	f = 1 kHz, R_S = 100 Ω			32			32		nV/√Hz
I_n	Equivalent input noise current	f = 1 kHz			0.22			0.22		pA/√Hz
THD	Total harmonic distortion	V_O = 2 V to 20 V, R_L = 2 kΩ, A_{VD} = 10, f = 10 kHz			0.02			0.02		%
GBW	Gain-bandwidth product	f = 100 kHz		3.5	4.5		3.5	4.5		MHz
BW	Power bandwidth	R_L = 2 kΩ, $V_{O(PP)}$ = 20 V, A_{VD} = 1, THD = 5.0%			200			200		kHz
ϕ_m	Phase margin	R_L = 2 kΩ, C_L = 0			60°			60°		
		R_L = 2 kΩ, C_L = 300 pF			40°			40°		
	Gain margin	R_L = 2 kΩ, C_L = 0			12			12		dB
		R_L = 2 kΩ, C_L = 300 pF			4			4		
r_i	Differential input resistance	V_{IC} = 0			150			150		MΩ
C_i	Input capacitance	V_{IC} = 0			2.5			2.5		pF
	Channel separation	f = 10 kHz			120			120		dB
z_o	Open-loop output impedance	f = 1 MHz			30			30		Ω

TLC251C, TLC251AC, TLC251BC, TLC251Y
PROGRAMMABLE LOW-POWER LinCMOS™ OPERATIONAL AMPLIFIERS

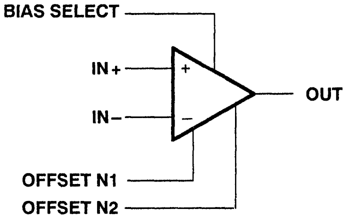
D2751, JULY 1983–REVISED NOVEMBER 1991

- **Wide Range of Supply Voltages 1.4 V to 16 V**
- **True Single-Supply Operation**
- **Common-Mode Input Voltage Range Includes the Negative Rail**
- **Low Noise . . . 30 nV/√Hz Typ at 1 kHz (High Bias)**
- **ESD Protection Exceeds 2000 V Per MIL-STD-833C, Method 3015.1**

D OR P PACKAGE
(TOP VIEW)



symbol



description

The TLC251C, TLC251AC, and TLC251BC are low-cost, low-power programmable operational amplifiers designed to operate with single or dual supplies. Unlike traditional metal-gate CMOS op amps, these devices utilize Texas Instruments silicon-gate LinCMOS™ process, giving them stable input offset voltages without sacrificing the advantages of metal-gate CMOS. This series of parts is available in selected grades of input offset voltage and can be nulled with one external potentiometer. Because the input common-mode range extends to the negative rail and the power consumption is extremely low, this family is ideally suited for battery-powered or energy-conserving applications. A bias-select pin can be used to program one of three ac performance and power-dissipation levels to suit the application. The series features operation down to a 1.4-V supply and is stable at unity gain.

These devices have internal electrostatic-discharge (ESD) protection circuits that will prevent catastrophic failures at voltages up to 2000 V as tested under MIL-STD-883C, Method 3015.1. However, care should be exercised in handling these devices as exposure to ESD may result in a degradation of the device parametric performance.

Because of the extremely high input impedance and low input bias and offset currents, applications for the TLC251C series include many areas that have previously been limited to BIFET and NFET product types. Any circuit using high-impedance elements and requiring small offset errors is a good candidate for cost-effective use of these devices. Many features associated with bipolar technology are available with LinCMOS™ operational amplifiers without the power penalties of traditional bipolar devices. Remote and inaccessible equipment applications are possible using the low-voltage and low-power capabilities of the TLC251C series.

AVAILABLE OPTIONS

T_A	V_{IO} max AT 25°C	PACKAGE		CHIP FORM (Y)
		SMALL OUTLINE (D)	PLASTIC DIP (P)	
0°C to 70°C	10 mV	TLC251CD	TLC251CP	TLC251Y
	5 mV	TLC251ACD	TLC251ACP	–
	2 mV	TLC251BCD	TLC251BCP	–

The D package is available taped and reeled. Add the suffix "R" to the device type (e.g., TLC251CDR). Chips are tested at 25°C.

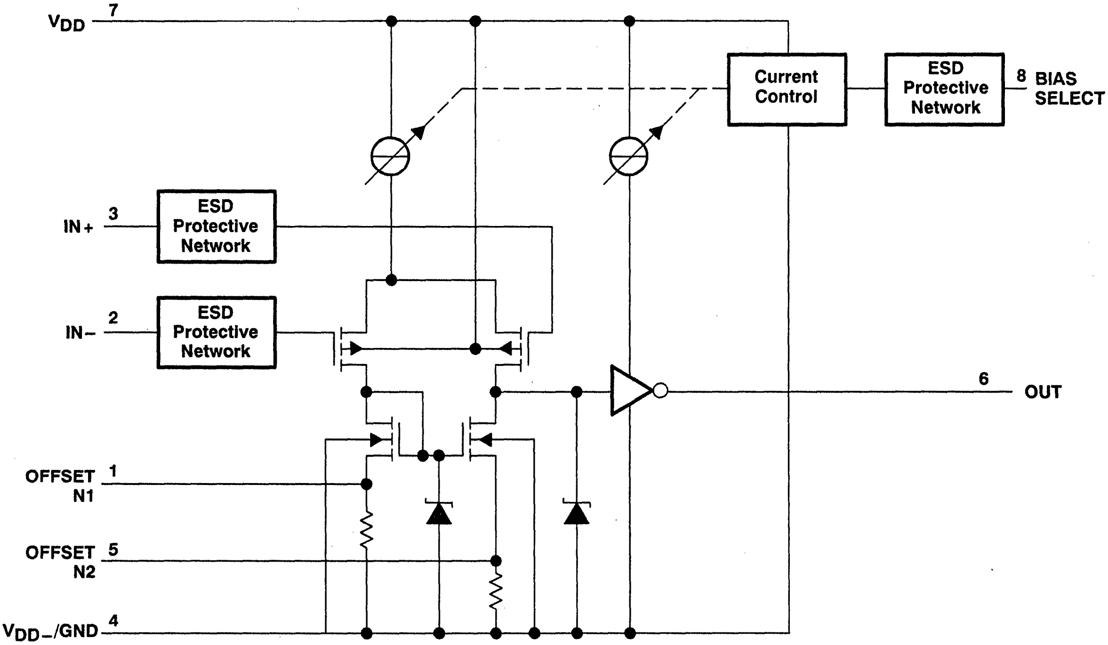
LinCMOS is a trademark of Texas Instruments Incorporated.

description (continued)

In addition, by driving the bias-select input with a logic signal from a microprocessor, these operational amplifiers can have software-controlled performance and power consumption. The TLC251C series is well suited to solve the difficult problems associated with single battery and solar cell-powered applications.

The TLC251C series is characterized for operation from 0°C to 70°C.

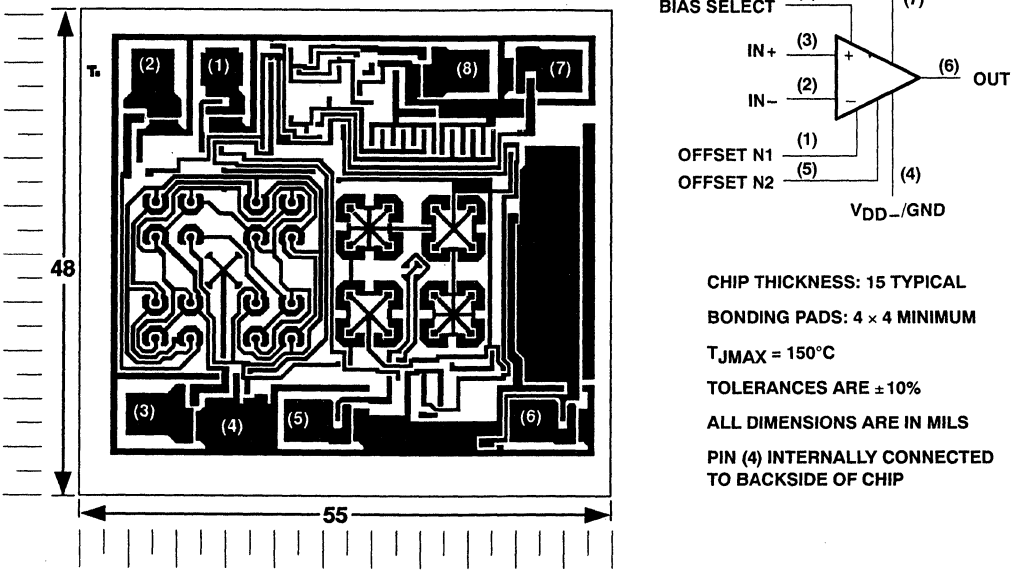
schematic



chip information

These chips, properly assembled, display characteristics similar to the TLC251C. Thermal compression or ultrasonic bonding may be used on the doped aluminum bonding pads. Chips may be mounted with conductive epoxy or a gold-silicon preform.

BONDING PAD ASSIGNMENTS



CHIP THICKNESS: 15 TYPICAL

BONDING PADS: 4 × 4 MINIMUM

T_{JMAX} = 150°C

TOLERANCES ARE ±10%

ALL DIMENSIONS ARE IN MILS

PIN (4) INTERNALLY CONNECTED TO BACKSIDE OF CHIP

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{DD} (see Note 1)	18 V
Differential input voltage (see Note 2)	±18 V
Input voltage range (any input)	−0.3 V to 18 V
Duration of short circuit at (or below) 25°C free-air temperature (see Note 3)	unlimited
Continuous total dissipation	See Dissipation Rating Table
Operating free-air temperature range	0°C to 70°C
Storage temperature range	−65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C

NOTES: 1. All voltage values, except differential voltages, are with respect to V_{DD-}/GND terminal.
2. Differential voltages are at the noninverting input terminal, with respect to the inverting input terminal.
3. The output may be shorted to either supply. Temperature and/or supply voltages must be limited to ensure the maximum dissipation rating is not exceeded.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING
D	725 mW	5.8 mW/°C	464 mW
P	1000 mW	8.0 mW/°C	640 mW

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{DD}		1.4		16	V
Common-mode input voltage, V_{IC}	V_{DD} = 1.4 V	0		0.2	V
	V_{DD} = 5 V	−0.2		4	
	V_{DD} = 10 V	−0.2		9	
	V_{DD} = 16 V	−0.2		14	
Operating free-air temperature, T_A		0		70	°C
Bias select pin voltage		See Application Information			

HIGH-BIAS MODE

electrical characteristics at specified free-air temperature

PARAMETER			TEST CONDITIONS	T_A†	V_{DD} = 5 V			V_{DD} = 10 V			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	TLC251C	V_O = 1.4 V, V_{IC} = 0 V, R_S = 50 Ω, R_L = 10 kΩ	25°C		1.1	10		1.1	10	mV
				Full range			12			12	
		TLC251AC		25°C		0.9	5		0.9	5	
				Full range			6.5			6.5	
		TLC251BC		25°C		0.34	2		0.39	2	
				Full range			3			3	
α_{VIO}	Average temperature coefficient of input offset voltage			25°C to 70°C		1.8			2		μV/°C
I_{IO}	Input offset current (see Note 4)		V_O = V_{DD}/2, V_{IC} = V_{DD}/2	25°C		0.1			0.1		pA
				70°C		7	300		7	300	
I_{IB}	Input bias current (see Note 4)		V_O = V_{DD}/2, V_{IC} = V_{DD}/2	25°C		0.6			0.7		pA
				70°C		40	600		50	600	
V_{ICR}	Common-mode input voltage range (see Note 5)			25°C	−0.2 to 4	−0.3 to 4.2		−0.2 to 9	−0.3 to 9.2		V
				Full range	−0.2 to 3.5			−0.2 to 8.5			V
V_{OH}	High-level output voltage		V_{ID} = 100 mV, R_L = 10 kΩ	25°C	3.2	3.8		8	8.5		V
				0°C	3	3.8		7.8	8.5		
				70°C	3	3.8		7.8	8.4		
V_{OL}	Low-level output voltage		V_{ID} = −100 mV, I_{OL} = 0	25°C		0	50		0	50	mV
				0°C		0	50		0	50	
				70°C		0	50		0	50	
A_{VD}	Large-signal differential voltage amplification		R_L = 10 kΩ, See Note 6	25°C	5	23		10	36		V/mV
				0°C	4	27		7.5	42		
				70°C	4	20		7.5	32		
CMRR	Common-mode rejection ratio		V_{IC} = V_{ICR}min	25°C	65	80		65	85		dB
				0°C	60	84		60	88		
				70°C	60	85		60	88		
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)		V_{DD} = 5 V to 10 V, V_O = 1.4 V	25°C	65	95		65	95		dB
				0°C	60	94		60	94		
				70°C	60	96		60	96		
$I_{I(SEL)}$	Input current to bias select pin		$V_{I(SEL)}$ = 0	25°C		−1.4			−1.9		μA
I_{DD}	Supply current		V_O = V_{DD}/2, V_{IC} = V_{DD}/2, No load	25°C		675	1600		950	2000	μA
				0°C		775	1800		1125	2200	
				70°C		575	1300		750	1700	

† Full range is 0°C to 70°C.

NOTES: 4. The typical values of input bias current and input offset current below 5 pA were determined mathematically.

5. This range also applies to each input individually.

6. At V_{DD} = 5 V, V_O = 0.25 V to 2 V; at V_{DD} = 10 V, V_O = 1 V to 6 V.

HIGH-BIAS MODE

operating characteristics, V_{DD} = 5 V

PARAMETER		TEST CONDITIONS		T_A	MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain	R_L = 10 kΩ, C_L = 20 pF	$V_{I(PP)}$ = 1 V	25°C		3.6		V/μs
				0°C		4		
				70°C		3		
			$V_{I(PP)}$ = 2.5 V	25°C		2.9		
				0°C		3.1		
				70°C		2.5		
V_n	Equivalent input noise voltage	f = 1 kHz, R_S = 100 Ω		25°C		25		nV/√Hz
B_{OM}	Maximum output swing bandwidth	V_O = V_{OH}, C_L = 20 pF, R_L = 10 kΩ		25°C		320		kHz
				0°C		340		
				70°C		260		
B_1	Unity-gain bandwidth	V_I = 10 mV, C_L = 20 pF		25°C		1.7		MHz
				0°C		2		
				70°C		1.3		
ϕ_m	Phase margin	V_I = 10 mV, f = B_1, C_L = 20 pF		25°C		46°		
				0°C		47°		
				70°C		44°		

operating characteristics, V_{DD} = 10 V

PARAMETER		TEST CONDITIONS		T_A	MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain	R_L = 10 kΩ, C_L = 20 pF	$V_{I(PP)}$ = 1 V	25°C		5.3		V/μs
				0°C		5.9		
				70°C		4.3		
			$V_{I(PP)}$ = 5.5 V	25°C		4.6		
				0°C		5.1		
				70°C		3.8		
V_n	Equivalent input noise voltage	f = 1 kHz, R_S = 100 Ω		25°C		25		nV/√Hz
B_{OM}	Maximum output swing bandwidth	V_O = V_{OH}, C_L = 20 pF, R_L = 10 kΩ		25°C		200		kHz
				0°C		220		
				70°C		140		
B_1	Unity-gain bandwidth	V_I = 10 mV, C_L = 20 pF		25°C		2.2		MHz
				0°C		2.5		
				70°C		1.8		
ϕ_m	Phase margin	V_I = 10 mV, f = B_1, C_L = 20 pF		25°C		49°		
				0°C		50°		
				70°C		46°		

MEDIUM-BIAS MODE

electrical characteristics at specified free-air temperature

PARAMETER			TEST CONDITIONS	T_A†	V_{DD} = 5 V			V_{DD} = 10 V			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	TLC251C	V_O = 1.4 V, V_{IC} = 0 V, R_S = 50 Ω, R_L = 100 kΩ	25°C		1.1	10		1.1	10	mV
				Full range			12			12	
		TLC251AC		25°C		0.9	5		0.9	5	
				Full range			6.5			6.5	
		TLC251BC		25°C		0.25	2		0.26	2	
				Full range			3			3	
α_{VIO}	Average temperature coefficient of input offset voltage			25°C to 70°C		1.7			2.1		µV/°C
I_{IO}	Input offset current (see Note 4)		V_O = V_{DD}/2, V_{IC} = V_{DD}/2	25°C		0.1			0.1		pA
				70°C		7	300		7	300	
I_{IB}	Input bias current (see Note 4)		V_O = V_{DD}/2, V_{IC} = V_{DD}/2	25°C		0.6			0.7		pA
				70°C		40	600		50	600	
V_{ICR}	Common-mode input voltage range (see Note 5)			25°C	−0.2 to 4	−0.3 to 4.2		−0.2 to 9	−0.3 to 9.2		V
				Full range	−0.2 to 3.5			−0.2 to 8.5			V
V_{OH}	High-level output voltage		V_{ID} = 100 mV, R_L = 100 kΩ	25°C	3.2	3.9		8	8.7		V
				0°C	3	3.9		7.8	8.7		
				70°C	3	4		7.8	8.7		
V_{OL}	Low-level output voltage		V_{ID} = −100 mV, I_{OL} = 0	25°C		0	50		0	50	mV
				0°C		0	50		0	50	
				70°C		0	50		0	50	
A_{VD}	Large-signal differential voltage amplification		R_L = 100 kΩ, See Note 6	25°C	25	170		25	275		V/mV
				0°C	15	200		15	320		
				70°C	15	140		15	230		
CMRR	Common-mode rejection ratio		V_{IC} = V_{ICR}min	25°C	65	91		65	94		dB
				0°C	60	91		60	94		
				70°C	60	92		60	94		
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)		V_{DD} = 5 V to 10 V, V_O = 1.4 V	25°C	70	93		70	93		dB
				0°C	60	92		60	92		
				70°C	60	94		60	94		
$I_{I(SEL)}$	Input current to bias select pin		$V_{I(SEL)}$ = V_{DD}/2	25°C		−130			−160		nA
I_{DD}	Supply current		V_O = V_{DD}/2, V_{IC} = V_{DD}/2, No load	25°C		105	280		143	300	µA
				0°C		125	320		173	400	
				70°C		85	220		110	280	

† Full range is 0°C to 70°C.

NOTES: 4. The typical values of input bias current and input offset current below 5 pA were determined mathematically.
5. This range also applies to each input individually.
6. At V_{DD} = 5 V, V_O = 0.25 V to 2 V; at V_{DD} = 10 V, V_O = 1 V to 6 V.

MEDIUM-BIAS MODE

operating characteristics, V_{DD} = 5 V

PARAMETER		TEST CONDITIONS		T_A	MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain	R_L = 100 kΩ, C_L = 20 pF	$V_{I(PP)}$ = 1 V	25°C		0.43		V/μs
				0°C		0.46		
				70°C		0.36		
			$V_{I(PP)}$ = 2.5 V	25°C		0.40		
				0°C		0.43		
				70°C		0.34		
V_n	Equivalent input noise voltage	f = 1 kHz, R_S = 100 Ω		25°C		32		nV/√Hz
B_{OM}	Maximum output swing bandwidth	V_O = V_{OH}, C_L = 20 pF, R_L = 100 kΩ		25°C		55		kHz
				0°C		60		
				70°C		50		
B_1	Unity-gain bandwidth	V_I = 10 mV, C_L = 20 pF		25°C		525		kHz
				0°C		600		
				70°C		400		
ϕ_m	Phase margin	V_I = 10 mV, f = B_1, C_L = 20 pF		25°C		40°		
				0°C		41°		
				70°C		39°		

operating characteristics, V_{DD} = 10 V

PARAMETER		TEST CONDITIONS		T_A	MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain	R_L = 100 kΩ, C_L = 20 pF	$V_{I(PP)}$ = 1 V	25°C		0.62		V/μs
				0°C		0.67		
				70°C		0.51		
			$V_{I(PP)}$ = 5.5 V	25°C		0.56		
				0°C		0.61		
				70°C		0.46		
V_n	Equivalent input noise voltage	f = 1 kHz, R_S = 100 Ω		25°C		32		nV/√Hz
B_{OM}	Maximum output swing bandwidth	V_O = V_{OH}, C_L = 20 pF, R_L = 100 kΩ		25°C		35		kHz
				0°C		40		
				70°C		30		
B_1	Unity-gain bandwidth	V_I = 10 mV, C_L = 20 pF		25°C		635		kHz
				0°C		710		
				70°C		510		
ϕ_m	Phase margin	V_I = 10 mV, f = B_1, C_L = 20 pF		25°C		43°		
				0°C		44°		
				70°C		42°		

LOW-BIAS MODE

electrical characteristics at specified free-air temperature

PARAMETER			TEST CONDITIONS	T_A†	V_{DD} = 5 V			V_{DD} = 10 V			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	TLC251C	V_O = 1.4 V, V_{IC} = 0 V, R_S = 50 Ω, R_L = 1 MΩ	25°C		1.1	10		1.1	10	mV
				Full range			12			12	
		TLC251AC		25°C		0.9	5		0.9	5	
				Full range			6.5			6.5	
		TLC251BC		25°C		0.24	2		0.26	2	
				Full range			3			3	
α_{VIO}	Average temperature coefficient of input offset voltage			25°C to 70°C		1.1			1		µV/°C
I_{IO}	Input offset current (see Note 4)		$V_O = V_{DD}/2$, $V_{IC} = V_{DD}/2$	25°C		0.1			0.1		pA
				70°C		7	300		7	300	
I_{IB}	Input bias current (see Note 4)		$V_O = V_{DD}/2$, $V_{IC} = V_{DD}/2$	25°C		0.6			0.7		pA
				70°C		40	600		50	600	
V_{ICR}	Common-mode input voltage range (see Note 5)			25°C	−0.2 to 4	−0.3 to 4.2		−0.2 to 9	−0.3 to 9.2		V
				Full range	−0.2 to 3.5			−0.2 to 8.5			V
V_{OH}	High-level output voltage		V_{ID} = 100 mV, R_L = 1 MΩ	25°C	3.2	4.1		8	8.9		V
				0°C	3	4.1		7.8	8.9		
				70°C	3	4.2		7.8	8.9		
V_{OL}	Low-level output voltage		V_{ID} = −100 mV, I_{OL} = 0	25°C		0	50		0	50	mV
				0°C		0	50		0	50	
				70°C		0	50		0	50	
A_{VD}	Large-signal differential voltage amplification		R_L = 1 MΩ, See Note 6	25°C	50	520		50	870		V/mV
				0°C	50	700		50	1030		
				70°C	50	380		50	660		
CMRR	Common-mode rejection ratio		$V_{IC} = V_{ICR}$min	25°C	65	94		65	97		dB
				0°C	60	95		60	97		
				70°C	60	95		60	97		
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)		V_{DD} = 5 V to 10 V, V_O = 1.4 V	25°C	70	97		70	97		dB
				0°C	60	97		60	97		
				70°C	60	98		60	98		
$I_{I(SEL)}$	Input current to bias select pin		$V_{I(SEL)} = V_{DD}$	25°C		65			95		nA
I_{DD}	Supply current		$V_O = V_{DD}/2$, $V_{IC} = V_{DD}/2$, No load	25°C		10	17		14	23	µA
				0°C		12	21		18	33	
				70°C		8	14		11	20	

† Full range is 0°C to 70°C.

NOTES: 4. The typical values of input bias current and input offset current below 5 pA were determined mathematically.

5. This range also applies to each input individually.

6. At V_{DD} = 5 V, V_O = 0.25 V to 2 V; at V_{DD} = 10 V, V_O = 1 V to 6 V.

LOW-BIAS MODE

operating characteristics, V_{DD} = 5 V

PARAMETER		TEST CONDITIONS		T_A	MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain	R_L = 1 MΩ, C_L = 20 pF	$V_{I(PP)}$ = 1 V	25°C		0.03		V/μs
				0°C		0.04		
				70°C		0.03		
			$V_{I(PP)}$ = 2.5 V	25°C		0.03		
				0°C		0.03		
				70°C		0.02		
V_n	Equivalent input noise voltage	f = 1 kHz, R_S = 100 Ω		25°C		68		nV/√Hz
B_{OM}	Maximum output swing bandwidth	V_O = V_{OH}, C_L = 20 pF, R_L = 1 MΩ		25°C		5		kHz
				0°C		6		
				70°C		4.5		
B_1	Unity-gain bandwidth	V_I = 10 mV, C_L = 20 pF		25°C		85		kHz
				0°C		100		
				70°C		65		
ϕ_m	Phase margin	V_I = 10 mV, f = B_1, C_L = 20 pF		25°C		34°		
				0°C		36°		
				70°C		30°		

operating characteristics, V_{DD} = 10 V

PARAMETER		TEST CONDITIONS		T_A	MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain	R_L = 1 MΩ, C_L = 20 pF	$V_{I(PP)}$ = 1 V	25°C		0.05		V/μs
				0°C		0.05		
				70°C		0.04		
			$V_{I(PP)}$ = 5.5 V	25°C		0.04		
				0°C		0.05		
				70°C		0.04		
V_n	Equivalent input noise voltage	f = 1 kHz, R_S = 100 Ω		25°C		68		nV/√Hz
B_{OM}	Maximum output swing bandwidth	V_O = V_{OH}, C_L = 20 pF, R_L = 1 MΩ		25°C		1		kHz
				0°C		1.3		
				70°C		0.9		
B_1	Unity-gain bandwidth	V_I = 10 mV, C_L = 20 pF		25°C		110		kHz
				0°C		125		
				70°C		90		
ϕ_m	Phase margin	V_I = 10 mV, f = B_1, C_L = 20 pF		25°C		38°		
				0°C		40°		
				70°C		34°		

electrical characteristics at specified free-air temperature, V_{DD} = 1.4 V

PARAMETER			TEST CONDITIONS†	T_A‡	BIAS	MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	TLC251C	V_O = 0.2 V, R_S = 50 Ω	25°C	Any			10	mV
				Full range				12	
		TLC251AC		25°C	Any			5	
				Full range				6.5	
		TLC251BC		25°C	Any			2	
				Full range				3	
α_{VIO}	Average temperature coefficient of input offset voltage			25°C to 70°C	Any		1		μV/°C
I_{IO}	Input offset current		V_O = 0.2 V	25°C	Any		1		pA
				Full range				300	
I_{IB}	Input bias current		V_O = 0.2 V	25°C	Any		1		pA
				Full range				600	
V_{ICR}	Common-mode input voltage range			25°C	Any	0 to 0.2			V
V_{OM}	Peak output voltage swing§		V_{ID} = 100 mV	25°C	Any	450	700		mV
A_{VD}	Large-signal differential voltage amplification		V_O = 100 to 300 mV, R_S = 50 Ω	25°C	Low		20		V/mV
					High		10		
CMRR	Common-mode rejection ratio		R_S = 50 Ω, V_O = 0.2 V, $V_{IC} = V_{ICR}min$	25°C	Any	60	77		dB
I_{DD}	Supply current		V_O = 0.2 V, No load	25°C	Low		5	17	μA
					High		150	190	

† All characteristics are measured under open-loop conditions with zero common-mode input voltage unless otherwise specified. Unless otherwise noted, an output load resistor is connected from the output to ground and has the following values: for low bias, R_L = 1 MΩ, for medium bias, R_L = 100 kΩ, and for high bias, R_L = 10 kΩ.

‡ Full range is 0°C to 70°C.

§ The output will swing to the potential of the V_{DD-}/GND pin.

operating characteristics, V_{DD} = 1.4 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	BIAS	MIN	TYP	MAX	UNIT
B_1	Unity-gain-bandwidth	C_L = 100 pF	Low		12		kHz
			High		12		
SR	Slew rate at unity gain	See Figure 1	Low		0.001		V/μs
			High		0.1		
	Overshoot factor	See Figure 1	Low		35%		
			High		30%		

electrical characteristics, V_{DD} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	HIGH-BIAS MODE			MEDIUM-BIAS MODE			LOW-BIAS MODE			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_O = 1.4 V, V_{IC} = 0 V, R_S = 50 Ω, R_L†		1.1	10		1.1	10		1.1	10	mV
α_{VIO}	Average temperature coefficient of input offset voltage			1.8			1.7			1.1		μV/°C
I_{IO}	Input offset current (see Note 4)	V_O = $V_{DD}/2$, V_{IC} = $V_{DD}/2$		0.1			0.1			0.1		pA
I_{IB}	Input bias current (see Note 4)	V_O = $V_{DD}/2$, V_{IC} = $V_{DD}/2$		0.6			0.6			0.6		pA
V_{ICR}	Common-mode input voltage range (see Note 5)		−0.2 to 4	−0.3 to 4.2		−0.2 to 4	−0.3 to 4.2		−0.2 to 4	−0.3 to 4.2		V
V_{OH}	High-level output voltage	V_{ID} = 100 mV, R_L†	3.2	3.8		3.2	3.9		3.2	4.1		V
V_{OL}	Low-level output voltage	V_{ID} = −100 mV, I_{OL} = 0		0	50		0	50		0	50	mV
A_{VD}	Large-signal differential voltage amplification	V_O = 0.25 V, R_L†	5	23		25	170		50	480		V/mV
CMRR	Common-mode rejection ratio	V_{IC} = V_{ICR}min	65	80		65	91		65	94		dB
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)	V_{DD} = 5 V to 10 V, V_O = 1.4 V	65	95		70	93		70	97		dB
$I_{I(SEL)}$	Input current to bias select pin	$V_{I(SEL)}$ = $V_{DD}/2$		−1.4			−0.13			0.065		μA
I_{DD}	Supply current	No load, V_O = $V_{DD}/2$, V_{IC} = $V_{DD}/2$		675	1600		105	280		10	17	μA

† For high-bias mode, R_L = 10 kΩ, for medium-bias mode, R_L = 100 kΩ; and for low-bias mode, R_L = 1 MΩ.

NOTES: 4. The typical values of input bias current and input offset current below 5 pA were determined mathematically.

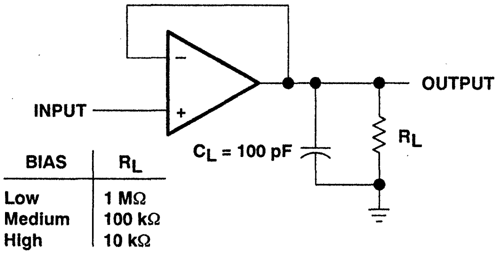
5. This range also applies to each input individually.

operating characteristics, V_{DD} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS		HIGH-BIAS MODE			MEDIUM-BIAS MODE			LOW-BIAS MODE			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
SR	Slew rate at unity gain	R_L†, C_L = 20 pF	$V_{I(PP)}$ = 1 V		3.6			0.43			0.03		V/µs
			$V_{I(PP)}$ = 2.5 V		2.9			0.40			0.03		
V_n	Equivalent input noise voltage	f = 1 kHz,	R_S = 100 Ω		25			32			68		nV/√Hz
B_{OM}	Maximum output swing bandwidth	V_O = V_{OH}, R_L = 10 kΩ	C_L = 20 pF,		320			55			4.5		kHz
B_1	Unity-gain bandwidth	V_I = 10 mV,	C_L = 20 pF		1700			525			65		kHz
ϕm	Phase margin	f = B_1, C_L = 20 pF	V_I = 10 mV,		46°			40°			34°		

† For high-bias mode, R_L = 10 kΩ; for medium-bias mode, R_L = 100 kΩ; and for low-bias mode, R_L = 1 MΩ.

PARAMETER MEASUREMENT INFORMATION



BIAS	R_L
Low	1 MΩ
Medium	100 kΩ
High	10 kΩ

Figure 1. Unity-Gain Amplifier

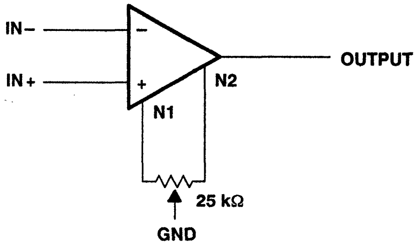


Figure 2. Input Offset Voltage Null Circuit

TYPICAL CHARACTERISTICS

SUPPLY CURRENT
vs
BIAS SELECT PIN VOLTAGE

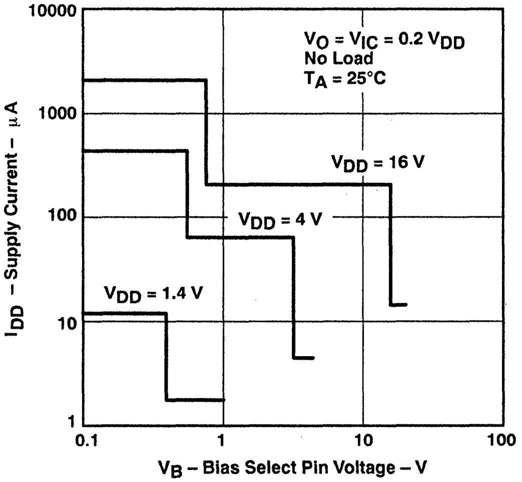


Figure 3

SUPPLY CURRENT
vs
SUPPLY VOLTAGE

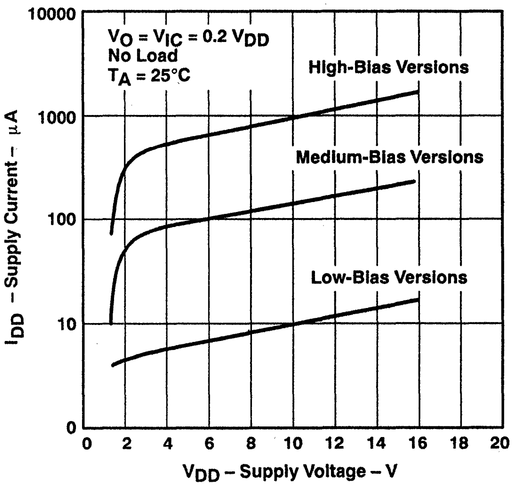


Figure 4

TYPICAL CHARACTERISTICS

SUPPLY CURRENT
vs
FREE-AIR TEMPERATURE

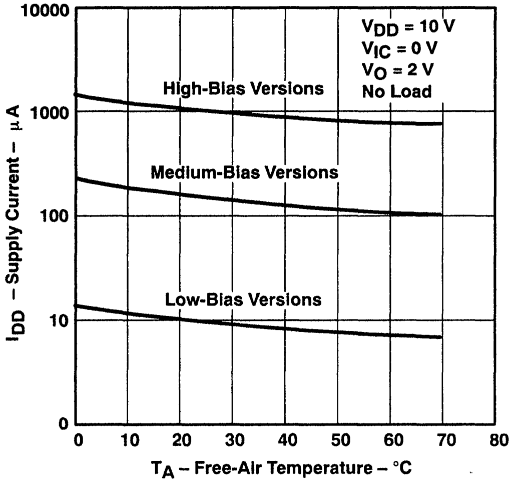


Figure 5

LOW BIAS
LARGE-SIGNAL
DIFFERENTIAL VOLTAGE AMPLIFICATION
and PHASE SHIFT
vs
FREQUENCY

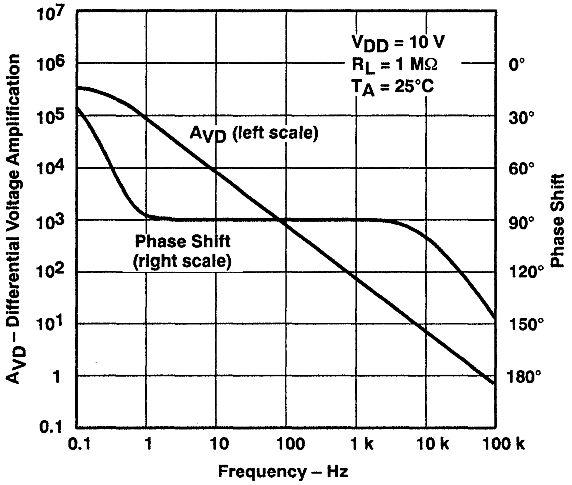


Figure 6

TYPICAL CHARACTERISTICS

MEDIUM BIAS
LARGE-SIGNAL
DIFFERENTIAL VOLTAGE AMPLIFICATION
and PHASE SHIFT
vs
FREQUENCY

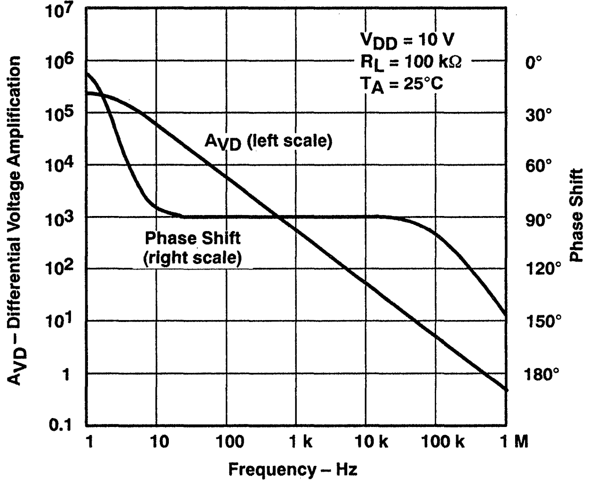


Figure 7

HIGH BIAS
LARGE-SIGNAL
DIFFERENTIAL VOLTAGE AMPLIFICATION
and PHASE SHIFT
vs
FREQUENCY

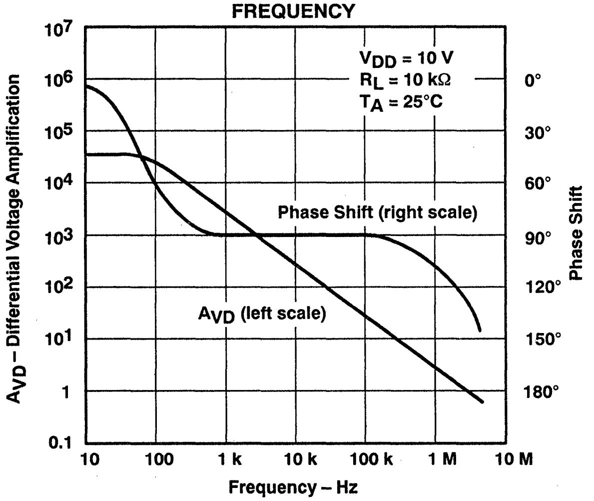


Figure 8

APPLICATION INFORMATION

latch-up avoidance

Junction-isolated CMOS circuits have an inherent parasitic PNPN structure that can function as an SCR. Under certain conditions, this SCR may be triggered into a low-impedance state, resulting in excessive supply current. To avoid such conditions, no voltage greater than 0.3 V beyond the supply rails should be applied to any pin. In general, the op amp supplies should be applied simultaneously with, or before, application of any input signals.

using the bias select pin

The TLC251C series has a bias select pin that allows the selection of one of three I_{DD} conditions (10, 150, and 1000 μA typical). This allows the user to trade-off power and ac performance. As shown in the typical supply current (I_{DD}) versus supply voltage (V_{DD}) curves (Figure 4), the I_{DD} varies only slightly from 4 V to 16 V. Below 4 V, the I_{DD} varies more significantly. Note that the I_{DD} values in the medium- and low-bias modes at V_{DD} = 1.4 V are typically 2 μA, and in the high mode are typically 12 μA. The following table shows the recommended bias select pin connections at V_{DD} = 10 V.

BIAS MODE	AC PERFORMANCE	BIAS SELECT CONNECTION†	TYPICAL I_{DD}‡
Low	Low	V_{DD}	10 μA
Medium	Medium	0.8 V to 9.2 V	150 μA
High	High	Ground pin	1000 μA

† The bias select pin may also be controlled by external circuitry to conserve power, etc. For information regarding the bias select pin, see Figure 3 in the typical characteristics curves.

‡ For I_{DD} characteristics at voltages other than 10 V, see Figure 4 in the typical characteristics curves.

output stage considerations

The amplifier's output stage consists of a source-follower-connected pullup transistor and an open-drain pulldown transistor. The high-level output voltage (V_{OH}) is virtually independent of the I_{DD} selection and increases with higher values of V_{DD} and reduced output loading. The low-level output voltage (V_{OL}) decreases with reduced output current and higher input common-mode voltage. With no load, V_{OL} is essentially equal to the V_{DD-}/GND pin potential.

input offset nulling

The TLC251C series offers external offset null control. Nulling may be achieved by adjusting a 25-kΩ potentiometer connected between the offset null terminals with the wiper connected to the device V_{DD-}/GND pin as shown in Figure 2. The amount of nulling range varies with the bias selection. At an I_{DD} setting of 1000 μA (high bias), the nulling range will allow the maximum offset specified to be trimmed to zero. In low or medium bias or when the amplifier is used below 4 V, total nulling may not be possible for all units.

supply configurations

Even though the TLC251C series is characterized for single-supply operation, it can be used effectively in a split-supply configuration when the input common-mode voltage (V_{ICR}), output swing (V_{OL} and V_{OH}), and supply voltage limits are not exceeded.

circuit layout precautions

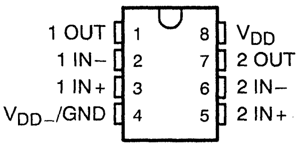
The user is cautioned that whenever extremely high circuit impedances are used, care must be exercised in layout, construction, board cleanliness, and supply filtering to avoid hum and noise pickup, as well as excessive dc leakages.

TLC252C, TLC25L2C, TLC25M2C, TLC252Y, TLC25L2Y, TLC25M2Y
LinCMOS™ DUAL OPERATIONAL AMPLIFIERS

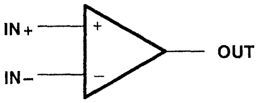
D2752, JUNE 1983–REVISED SEPTEMBER 1991

- **A-Suffix Versions Offer 5-mV V_{IO}**
- **B-Suffix Versions Offer 2-mV V_{IO}**
- **Wide Range of Supply Voltages 1.4 V to 16 V**
- **True Single-Supply Operation**
- **Common-Mode Input Voltage Includes the Negative Rail**
- **Low Noise . . . 30 nV/√Hz Typ at f = 1 kHz (High-Bias Versions)**

D OR P PACKAGE
(TOP VIEW)



symbol (each amplifier)



description

The TLC252C, TLC25L2C, and TLC25M2C are low-cost, low-power dual operational amplifiers designed to operate with single or dual supplies. These devices utilize the Texas Instruments silicon gate LinCMOS™ process, giving them stable input offset voltages that are available in selected grades of 2, 5, or 10 mV maximum, very high input impedances, and extremely low input offset and bias currents. Because the input common-mode range extends to the negative rail and the power consumption is extremely low, this series is ideally suited for battery-powered or energy-conserving applications. The series offers operation down to a 1.4-V supply, is stable at unity gain, and has excellent noise characteristics.

These devices have internal electrostatic-discharge (ESD) protection circuits that will prevent catastrophic failures at voltages up to 2000 V as tested under MIL-STD-883C, Method 3015.1. However, care should be exercised in handling these devices as exposure to ESD may result in a degradation of the device parametric performance.

Because of the extremely high input impedance and low input bias and offset currents, applications for the TLC252C series include many areas that have previously been limited to BIFET and NFET product types. Any circuit using high-impedance elements and requiring small offset errors is a good candidate for cost-effective use of these devices. Many features associated with bipolar technology are available with LinCMOS™ operational amplifiers without the power penalties of traditional bipolar devices. General applications such as

AVAILABLE OPTIONS

T_A	V_{IO} max AT 25°C	PACKAGE		CHIP FORM (Y)
		SMALL OUTLINE (D)	PLASTIC DIP (P)	
0°C to 70°C	10 mV	TLC252CD	TLC252CP	TLC252Y TLC25L2Y TLC25M2Y
	5 mV	TLC252ACD	TLC252ACP	
	2 mV	TLC252BCD	TLC252BCP	
	10 mV	TLC25L2CD	TLC25L2CP	
	5 mV	TLC25L2ACD	TLC25L2ACP	
	2 mV	TLC25L2BCD	TLC25L2BCP	
	10 mV	TLC25M2CD	TLC25M2CP	
	5 mV	TLC25M2ACD	TLC25M2ACP	
	2 mV	TLC25M2BCD	TLC25M2BCP	

The D package is available taped and reeled. Add the suffix "R" to the device type (e.g., TLC252CDR). Chips are tested at 25°C.

LinCMOS is a trademark of Texas Instruments Incorporated.

TEXAS INSTRUMENTS

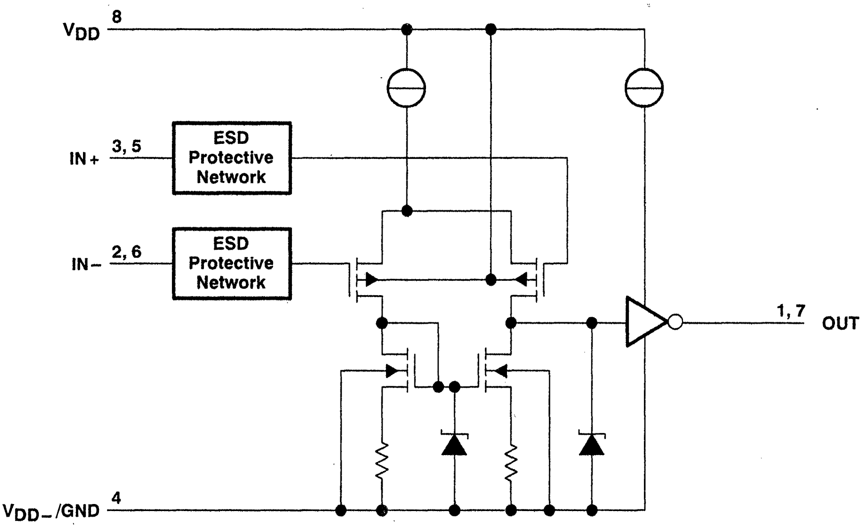
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

description (continued)

transducer interfacing, analog calculations, amplifier blocks, active filters, and signal buffering are all easily designed with the TLC252C series devices. Remote and inaccessible equipment applications are possible using their low-voltage and low-power capabilities. The TLC252C series is well suited to solve the difficult problems associated with single-battery and solar-cell-powered applications. This series includes devices that are characterized for the commercial temperature range and are available in 8-pin plastic dip (P) and the small outline (D) package. The device is also available in chip form (Y).

The TLC252C series is characterized for operation from 0°C to 70°C.

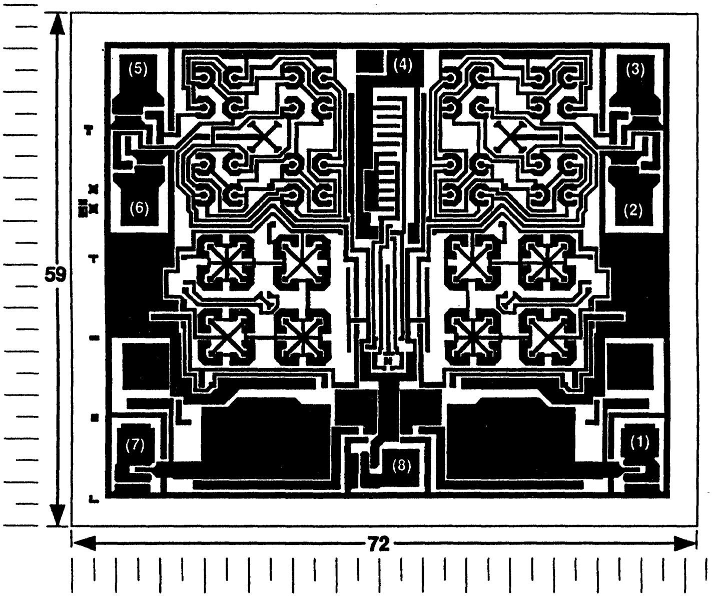
equivalent schematic (each amplifier)

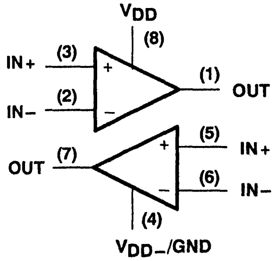


chip information

These chips, properly assembled, display characteristics similar to the TLC25_2C. Thermal compression or ultrasonic bonding may be used on the doped aluminum bonding pads. Chips may be mounted with conductive epoxy or a gold-silicon preform.

BONDING PAD ASSIGNMENTS





CHIP THICKNESS: 15 TYPICAL

BONDING PADS: 4 × 4 MINIMUM

T_{JMAX} = 150°C

TOLERANCES ARE ±10%

ALL DIMENSIONS ARE IN MILS

PIN (4) INTERNALLY CONNECTED TO BACKSIDE OF CHIP

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{DD} (see Note 1)	18 V
Differential input voltage (see Note 2)	±18 V
Input voltage range (any input)	−0.3 V to 18 V
Duration of short circuit at (or below) 25°C free-air temperature (see Note 3)	unlimited
Continuous total dissipation	See Dissipation Rating Table
Operating free-air temperature range	0°C to 70°C
Storage temperature range	−65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C

NOTES: 1. All voltage values, except differential voltages, are with respect to V_{DD-}/GND terminal.
2. Differential voltages are at the noninverting input terminal, with respect to the inverting input terminal.
3. The output may be shorted to either supply. Temperature and/or supply voltages must be limited to ensure the maximum dissipation rating is not exceeded.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING
D	725 mW	5.8 mW/°C	464 mW
P	1000 mW	8.0 mW/°C	640 mW

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{DD}		1.4		16	V
Common-mode input voltage, V_{IC}	$V_{DD} = 1.4$ V	0		0.2	V
	$V_{DD} = 5$ V	−0.2		4	
	$V_{DD} = 10$ V	−0.2		9	
	$V_{DD} = 16$ V	−0.2		14	
Operating free-air temperature, T_A		0		70	°C

electrical characteristics at specified free-air temperature, V_{DD} = 1.4 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS†		TLC252_C			TLC25L2_C			TLC25M2_C			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	TLC25_2C	V_O = 0.2 V, R_S = 50 Ω	25°C			10			10			10	mV
				0°C to 70°C			12			12			12	
		TLC25_2AC		25°C			5			5			5	
				0°C to 70°C			6.5			6.5			6.5	
		TLC25_2BC		25°C			2			2			2	
				0°C to 70°C			3			3			3	
α_{VIO}	Average temperature coefficient of input offset voltage			25°C to 70°C		1			1			1		µV/°C
I_{IO}	Input offset current		V_O = 0.2 V	25°C		1			1			1		pA
				0°C to 70°C			300			300			300	
I_{IB}	Input bias current		V_O = 0.2 V	25°C		1			1			1		pA
				0°C to 70°C			600			600			600	
V_{ICR}	Common-mode input voltage range			25°C	0 to 0.2			0 to 0.2			0 to 0.2			V
V_{OM}	Peak output voltage swing‡		V_{ID} = 100 mV	25°C	450	700		450	700		450	700		mV
A_{VD}	Large-signal differential voltage amplification		V_O = 100 to 300 mV, R_S = 50 Ω	25°C		10			20			20		V/mV
CMRR	Common-mode rejection ratio		V_O = 0.2 V, V_{IC} = V_{ICR}min	25°C	60	77		60	77		60	77		dB
I_{DD}	Supply current		V_O = 0.2 V, No load	25°C		300	375		25	34		200	250	µA

† All characteristics are measured under open-loop conditions with zero common-mode input voltage unless otherwise specified. Unless otherwise noted, an output load resistor is connected from the output to ground and has the following value: for low bias R_L = 1 MΩ, for medium bias R_L = 100 kΩ, and for high bias R_L = 10 kΩ.

‡ The output will swing to the potential of the V_{DD-}/GND pin.

operating characteristics, V_{DD} = 1.4 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	TLC252_C			TLC25L2_C			TLC25M2_C			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
B_1	Unity-gain bandwidth	A_V = 40 dB, C_L = 10 pF, R_S = 50 Ω		12			12			12		kHz
SR	Slew rate at unity gain	See Figure 1		0.1			0.001			0.01		V/µs
	Overshoot factor	See Figure 1		30%			35%			35%		

electrical characteristics at specified free-air temperature, V_{DD} = 5 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS		T_A†	MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	TLC252C	V_O = 1.4 V, R_S = 50 Ω,	V_{IC} = 0, R_L = 10 kΩ	25°C		1.1	10	mV
					Full range			12	
		TLC252AC	V_O = 1.4 V, R_S = 50 Ω,	V_{IC} = 0, R_L = 10 kΩ	25°C		0.9	5	
					Full range			6.5	
		TLC252BC	V_O = 1.4 V, R_S = 50 Ω,	V_{IC} = 0, R_L = 10 kΩ	25°C		0.23	2	
					Full range			3	
α_{VIO}	Average temperature coefficient of input offset voltage				25°C to 70°C		1.8		μV/°C
I_{IO}	Input offset current (see Note 4)		V_O = 2.5 V,	V_{IC} = 2.5 V	25°C		0.1		pA
					70°C		7	300	
I_{IB}	Input bias current (see Note 4)		V_O = 2.5 V,	V_{IC} = 2.5 V	25°C		0.6		pA
					70°C		40	600	
V_{ICR}	Common-mode input voltage range (see Note 5)				25°C	−0.2 to 4	−0.3 to 4.2		V
					Full range	−0.2 to 3.5			V
V_{OH}	High-level output voltage		V_{ID} = 100 mV,	R_L = 10 kΩ	25°C	3.2	3.8		V
					0°C	3	3.8		
					70°C	3	3.8		
V_{OL}	Low-level output voltage		V_{ID} = −100 mV,	I_{OL} = 0	25°C		0	50	mV
					0°C		0	50	
					70°C		0	50	
A_{VD}	Large-signal differential voltage amplification		V_O = 0.25 V to 2 V,	R_L = 10 kΩ	25°C	5	23		V/mV
					0°C	4	27		
					70°C	4	20		
CMRR	Common-mode rejection ratio		$V_{IC} = V_{ICR}min$		25°C	65	80		dB
					0°C	60	84		
					70°C	60	85		
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)		V_{DD} = 5 V to 10 V,	V_O = 1.4 V	25°C	65	95		dB
					0°C	60	94		
					70°C	60	96		
I_{DD}	Supply current (two amplifiers)		V_O = 2.5 V, No load	V_{IC} = 2.5 V,	25°C		1.4	3.2	mA
					0°C		1.6	3.6	
					70°C		1.2	2.6	

† Full range is 0°C to 70°C.

NOTES: 4. The typical values of input bias current and input offset current below 5 pA were determined mathematically.
5. This range also applies to each input individually.

electrical characteristics at specified free-air temperature, V_{DD} = 10 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS	T_A†	MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	TLC252C	$V_O = 1.4$ V, $V_{IC} = 0$, $R_S = 50\ \Omega$, $R_L = 10\ \mathrm{k}\Omega$	25°C		1.1	10	mV
				Full range			12	
		TLC252AC	$V_O = 1.4$ V, $V_{IC} = 0$, $R_S = 50\ \Omega$, $R_L = 10\ \mathrm{k}\Omega$	25°C		0.9	5	
				Full range			6.5	
		TLC252BC	$V_O = 1.4$ V, $V_{IC} = 0$, $R_S = 50\ \Omega$, $R_L = 10\ \mathrm{k}\Omega$	25°C		0.29	2	
				Full range			3	
α_{VIO}	Average temperature coefficient of input offset voltage			25°C to 70°C		2		μV/°C
I_{IO}	Input offset current (see Note 4)		$V_O = 5$ V, $V_{IC} = 5$ V	25°C		0.1		pA
				70°C		7	300	
I_{IB}	Input bias current (see Note 4)		$V_O = 5$ V, $V_{IC} = 5$ V	25°C		0.7		pA
				70°C		50	600	
V_{ICR}	Common-mode input voltage range (see Note 5)			25°C	−0.2 to 9	−0.3 to 9.2		V
				Full range	−0.2 to 8.5			V
V_{OH}	High-level output voltage		$V_{ID} = 100$ mV, $R_L = 10\ \mathrm{k}\Omega$	25°C	8	8.5		V
				0°C	7.8	8.5		
				70°C	7.8	8.4		
V_{OL}	Low-level output voltage		$V_{ID} = -100$ mV, $I_{OL} = 0$	25°C		0	50	mV
				0°C		0	50	
				70°C		0	50	
A_{VD}	Large-signal differential voltage amplification		$V_O = 1$ V to 6 V, $R_L = 10\ \mathrm{k}\Omega$	25°C	10	36		V/mV
				0°C	7.5	42		
				70°C	7.5	32		
CMRR	Common-mode rejection ratio		$V_{IC} = V_{ICR}\mathrm{min}$	25°C	65	85		dB
				0°C	60	88		
				70°C	60	88		
K_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)		$V_{DD} = 5$ V to 10 V, $V_O = 1.4$ V	25°C	65	95		dB
				0°C	60	94		
				70°C	60	96		
I_{DD}	Supply current (two amplifiers)		$V_O = 5$ V, $V_{IC} = 5$ V, No load	25°C		1.9	4	mA
				0°C		2.3	4.4	
				70°C		1.6	3.4	

† Full range is 0°C to 70°C.

NOTES: 4. The typical values of input bias current and input offset current below 5 pA were determined mathematically.
5. This range also applies to each input individually.

operating characteristics, V_{DD} = 5 V

PARAMETER		TEST CONDITIONS		T_A	MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain	R_L = 10 kΩ, C_L = 20 pF, See Figure 1	$V_{I(PP)}$ = 1 V	25°C		3.6		V/μs
				0°C		4		
				70°C		3		
			$V_{I(PP)}$ = 2.5 V	25°C		2.9		
				0°C		3.1		
				70°C		2.5		
V_n	Equivalent input noise voltage	f = 1 kHz, R_S = 100 Ω, See Figure 2		25°C		25		nV/√Hz
B_{OM}	Maximum output swing bandwidth	V_O = V_{OH}, C_L = 20 pF, R_L = 10 kΩ, See Figure 1		25°C		320		kHz
				0°C		340		
				70°C		260		
B_1	Unity-gain bandwidth	V_I = 10 mV, C_L = 20 pF, See Figure 3		25°C		1.7		MHz
				0°C		2		
				70°C		1.3		
ϕ_m	Phase margin	V_I = 10 mV, f = B_1, C_L = 20 pF, See Figure 3		25°C		46°		
				0°C		47°		
				70°C		43°		

operating characteristics, V_{DD} = 10 V

PARAMETER		TEST CONDITIONS		T_A	MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain	R_L = 10 kΩ, C_L = 20 pF, See Figure 1	$V_{I(PP)}$ = 1 V	25°C		5.3		V/μs
				0°C		5.9		
				70°C		4.3		
			$V_{I(PP)}$ = 5.5 V	25°C		4.6		
				0°C		5.1		
				70°C		3.8		
V_n	Equivalent input noise voltage	f = 1 kHz, R_S = 100 Ω, See Figure 2		25°C		25		nV/√Hz
B_{OM}	Maximum output swing bandwidth	V_O = V_{OH}, C_L = 20 pF, R_L = 10 kΩ, See Figure 1		25°C		200		kHz
				0°C		220		
				70°C		140		
B_1	Unity-gain bandwidth	V_I = 10 mV, C_L = 20 pF, See Figure 3		25°C		2.2		MHz
				0°C		2.5		
				70°C		1.8		
ϕ_m	Phase margin	V_I = 10 mV, f = B_1, C_L = 20 pF, See Figure 3		25°C		49°		
				0°C		50°		
				70°C		46°		

electrical characteristics at specified free-air temperature, V_{DD} = 5 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS	T_A†	MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	TLC25L2C	V_O = 1.4 V, V_{IC} = 0, R_S = 50 Ω, R_L = 1 MΩ	25°C		1.1	10	mV
				Full range			12	
		TLC25L2AC	V_O = 1.4 V, V_{IC} = 0, R_S = 50 Ω, R_L = 1 MΩ	25°C		0.9	5	
				Full range			6.5	
		TLC25L2BC	V_O = 1.4 V, V_{IC} = 0, R_S = 50 Ω, R_L = 1 MΩ	25°C		0.204	2	
				Full range			3	
α_{VIO}	Average temperature coefficient of input offset voltage			25°C to 70°C		1.1		μV/°C
I_{IO}	Input offset current (see Note 4)		V_O = 2.5 V, V_{IC} = 2.5 V	25°C		0.1		pA
				70°C		7	300	
I_{IB}	Input bias current (see Note 4)		V_O = 2.5 V, V_{IC} = 2.5 V	25°C		0.6		pA
				70°C		50	600	
V_{ICR}	Common-mode input voltage range (see Note 5)			25°C	−0.2 to 4	−0.3 to 4.2		V
				Full range	−0.2 to 3.5			V
V_{OH}	High-level output voltage		V_{ID} = 100 mV, R_L = 1 MΩ	25°C	3.2	4.1		V
				0°C	3	4.1		
				70°C	3	4.2		
V_{OL}	Low-level output voltage		V_{ID} = −100 mV, I_{OL} = 0	25°C		0	50	mV
				0°C		0	50	
				70°C		0	50	
A_{VD}	Large-signal differential voltage amplification		V_O = 0.25 V to 2 V, R_L = 1 MΩ	25°C	50	700		V/mV
				0°C	50	700		
				70°C	50	380		
CMRR	Common-mode rejection ratio		$V_{IC} = V_{ICR}\text{min}$	25°C	65	94		dB
				0°C	60	95		
				70°C	60	95		
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)		V_{DD} = 5 V to 10 V, V_O = 1.4 V	25°C	70	97		dB
				0°C	60	97		
				70°C	60	98		
I_{DD}	Supply current (two amplifiers)		V_O = 2.5 V, V_{IC} = 2.5 V, No load	25°C		20	34	μA
				0°C		24	42	
				70°C		16	28	

† Full range is 0°C to 70°C.

NOTES: 4. The typical values of input bias current and input offset current below 5 pA were determined mathematically.

5. This range also applies to each input individually.

electrical characteristics at specified free-air temperature, V_{DD} = 10 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS		T_A†	MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	TLC25L2C	V_O = 1.4 V, R_S = 50 Ω,	V_{IC} = 0, R_L = 1 MΩ	25°C		1.1	10	mV
					Full range			12	
		TLC25L2AC	V_O = 1.4 V, R_S = 50 Ω,	V_{IC} = 0, R_L = 1 MΩ	25°C		0.9	5	
					Full range			6.5	
		TLC25L2BC	V_O = 1.4 V, R_S = 50 Ω,	V_{IC} = 0, R_L = 1 MΩ	25°C		0.235	2	
					Full range			3	
α_{VIO}	Average temperature coefficient of input offset voltage				25°C to 70°C		1		μV/°C
I_{IO}	Input offset current (see Note 4)		V_O = 5 V,	V_{IC} = 5 V	25°C		0.1		pA
					70°C		8	300	
I_{IB}	Input bias current (see Note 4)		V_O = 5 V,	V_{IC} = 5 V	25°C		0.7		pA
					70°C		50	600	
V_{ICR}	Common-mode input voltage range (see Note 5)				25°C	−0.2 to 9	−0.3 to 9.2		V
					Full range	−0.2 to 8.5			V
V_{OH}	High-level output voltage		V_{ID} = 100 mV,	R_L = 1 MΩ	25°C	8	8.9		V
					0°C	7.8	8.9		
					70°C	7.8	8.9		
V_{OL}	Low-level output voltage		V_{ID} = −100 mV,	I_{OL} = 0	25°C		0	50	mV
					0°C		0	50	
					70°C		0	50	
A_{VD}	Large-signal differential voltage amplification		V_O = 1 V to 6 V,	R_L = 1 MΩ	25°C	50	860		V/mV
					0°C	50	1025		
					70°C	50	660		
CMRR	Common-mode rejection ratio		$V_{IC} = V_{ICR}$min		25°C	65	97		dB
					0°C	60	97		
					70°C	60	97		
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)		V_{DD} = 5 V to 10 V,	V_O = 1.4 V	25°C	70	97		dB
					0°C	60	97		
					70°C	60	98		
I_{DD}	Supply current (two amplifiers)		V_O = 5 V, No load	V_{IC} = 5 V,	25°C		29	46	μA
					0°C		36	66	
					70°C		22	40	

† Full range is 0°C to 70°C.

NOTES: 4. The typical values of input bias current and input offset current below 5 pA were determined mathematically.

5. This range also applies to each input individually.

operating characteristics, V_{DD} = 5 V

PARAMETER		TEST CONDITIONS		T_A	MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain	R_L = 1 MΩ, C_L = 20 pF, See Figure 1	$V_{I(PP)}$ = 1 V	25°C		0.03		V/μs
				0°C		0.04		
				70°C		0.03		
			$V_{I(PP)}$ = 2.5 V	25°C		0.03		
				0°C		0.03		
				70°C		0.02		
V_n	Equivalent input noise voltage	f = 1 kHz, R_S = 100 Ω, See Figure 2		25°C		68		nV/√Hz
B_{OM}	Maximum output swing bandwidth	V_O = V_{OH}, C_L = 20 pF, R_L = 1 MΩ, See Figure 1		25°C		5		kHz
				0°C		6		
				70°C		4.5		
B_1	Unity-gain bandwidth	V_I = 10 mV, C_L = 20 pF, See Figure 3		25°C		85		kHz
				0°C		100		
				70°C		65		
ϕ_m	Phase margin	V_I = 10 mV, f = B_1, C_L = 20 pF, See Figure 3		25°C		34°		
				0°C		36°		
				70°C		30°		

operating characteristics, V_{DD} = 10 V

PARAMETER		TEST CONDITIONS		T_A	MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain	R_L = 1 MΩ, C_L = 20 pF See Figure 1	$V_{I(PP)}$ = 1 V	25°C		0.05		V/μs
				0°C		0.05		
				70°C		0.04		
			$V_{I(PP)}$ = 5.5 V	25°C		0.04		
				0°C		0.05		
				70°C		0.04		
V_n	Equivalent input noise voltage	f = 1 kHz, R_S = 100 Ω, See Figure 2		25°C		68		nV/√Hz
B_{OM}	Maximum output swing bandwidth	V_O = V_{OH}, C_L = 20 pF, R_L = 1 MΩ, See Figure 1		25°C		1		kHz
				0°C		1.3		
				70°C		0.9		
B_1	Unity-gain bandwidth	V_I = 10 mV, C_L = 20 pF, See Figure 3		25°C		110		kHz
				0°C		125		
				70°C		90		
ϕ_m	Phase margin	V_I = 10 mV, f = B_1, C_L = 20 pF, See Figure 3		25°C		38°		
				0°C		40°		
				70°C		34°		

electrical characteristics at specified free-air temperature, V_{DD} = 5 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS		T_A†	MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	TLC25M2C	V_O = 1.4 V, R_S = 50 Ω,	V_{IC} = 0, R_L = 100 kΩ	25°C		1.1	10	mV
					Full range			12	
		TLC25M2AC	V_O = 1.4 V, R_S = 50 Ω,	V_{IC} = 0, R_L = 100 kΩ	25°C		0.9	5	
					Full range			6.5	
		TLC25M2BC	V_O = 1.4 V, R_S = 50 Ω,	V_{IC} = 0, R_L = 100 kΩ	25°C		0.22	2	
					Full range			3	
α_{VIO}	Average temperature coefficient of input offset voltage				25°C to 70°C		1.7		μV/°C
I_{IO}	Input offset current (see Note 4)		V_O = 2.5 V,	V_{IC} = 2.5 V	25°C		0.1		pA
					70°C		7	300	
I_{IB}	Input bias current (see Note 4)		V_O = 2.5 V,	V_{IC} = 2.5 V	25°C		0.6		pA
					70°C		40	600	
V_{ICR}	Common-mode input voltage range (see Note 5)				25°C	−0.2 to 4	−0.3 to 4.2		V
					Full range	−0.2 to 3.5			V
V_{OH}	High-level output voltage		V_{ID} = 100 mV,	R_L = 100 kΩ	25°C	3.2	3.9		V
					0°C	3	3.9		
					70°C	3	4		
V_{OL}	Low-level output voltage		V_{ID} = −100 mV,	I_{OL} = 0	25°C		0	50	mV
					0°C		0	50	
					70°C		0	50	
A_{VD}	Large-signal differential voltage amplification		V_O = 0.25 V to 2 V,	R_L = 100 kΩ	25°C	25	170		V/mV
					0°C	15	200		
					70°C	15	140		
CMRR	Common-mode rejection ratio		$V_{IC} = V_{ICR}$min		25°C	65	91		dB
					0°C	60	91		
					70°C	60	92		
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)		V_{DD} = 5 V to 10 V,	V_O = 1.4 V	25°C	70	93		dB
					0°C	60	92		
					70°C	60	94		
I_{DD}	Supply current (two amplifiers)		V_O = 2.5 V, No load	V_{IC} = 2.5 V,	25°C		210	560	μA
					0°C		250	640	
					70°C		170	440	

† Full range is 0°C to 70°C.

NOTES: 4. The typical values of input bias current and input offset current below 5 pA were determined mathematically.

5. This range also applies to each input individually.

electrical characteristics at specified free-air temperature, V_{DD} = 10 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS	T_A†	MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	TLC25M2C	V_O = 1.4 V, V_{IC} = 0, R_S = 50 Ω, R_L = 100 kΩ	25°C		1.1	10	mV
				Full range			12	
		TLC25M2AC	V_O = 1.4 V, V_{IC} = 0, R_S = 50 Ω, R_L = 100 kΩ	25°C		0.9	5	
				Full range			6.5	
		TLC25M2BC	V_O = 1.4 V, V_{IC} = 0, R_S = 50 Ω, R_L = 100 kΩ	25°C		0.224	2	
				Full range			3	
α_{VIO}	Average temperature coefficient of input offset voltage			25°C to 70°C		2.1		μV/°C
I_{IO}	Input offset current (see Note 4)		V_O = 5 V, V_{IC} = 5 V	25°C		0.1		pA
				70°C		7	300	
I_{IB}	Input bias current (see Note 4)		V_O = 5 V, V_{IC} = 5 V	25°C		0.7		pA
				70°C		50	600	
V_{ICR}	Common-mode input voltage range (see Note 5)			25°C	−0.2 to 9	−0.3 to 9.2		V
				Full range	−0.2 to 8.5			V
V_{OH}	High-level output voltage		V_{ID} = 100 mV, R_L = 100 kΩ	25°C	8	8.7		V
				0°C	7.8	8.7		
				70°C	7.8	8.7		
V_{OL}	Low-level output voltage		V_{ID} = −100 mV, I_{OL} = 0	25°C		0	50	mV
				0°C		0	50	
				70°C		0	50	
A_{VD}	Large-signal differential voltage amplification		V_O = 1 V to 6 V, R_L = 100 kΩ	25°C	25	275		V/mV
				0°C	15	320		
				70°C	15	230		
CMRR	Common-mode rejection ratio		$V_{IC} = V_{ICR}\text{min}$	25°C	65	94		dB
				0°C	60	94		
				70°C	60	94		
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)		V_{DD} = 5 V to 10 V, V_O = 1.4 V	25°C	70	93		dB
				0°C	60	92		
				70°C	60	94		
I_{DD}	Supply current (two amplifiers)		V_O = 5 V, V_{IC} = 5 V, No load	25°C		285	600	μA
				0°C		345	800	
				70°C		220	560	

† Full range is 0°C to 70°C.

NOTES: 4. The typical values of input bias current and input offset current below 5 pA were determined mathematically.

5. This range also applies to each input individually.

operating characteristics, V_{DD} = 5 V

PARAMETER		TEST CONDITIONS		T_A	MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain	R_L = 100 kΩ, C_L = 20 pF, See Figure 1	$V_{I(PP)}$ = 1 V	25°C		0.43		V/μs
				0°C		0.46		
				70°C		0.36		
			$V_{I(PP)}$ = 2.5 V	25°C		0.40		
				0°C		0.43		
				70°C		0.34		
V_n	Equivalent input noise voltage	f = 1 kHz, R_S = 100 Ω,	See Figure 2	25°C		32		nV/√Hz
B_{OM}	Maximum output swing bandwidth	V_O = V_{OH}, C_L = 20 pF, R_L = 100 kΩ, See Figure 1		25°C		55		kHz
				0°C		60		
				70°C		50		
B_1	Unity-gain bandwidth	V_I = 10 mV, C_L = 20 pF,	See Figure 3	25°C		525		kHz
				0°C		600		
				70°C		400		
ϕ_m	Phase margin	V_I = 10 mV, f = B_1, C_L = 20 pF, See Figure 3		25°C		40°		
				0°C		41°		
				70°C		39°		

operating characteristics, V_{DD} = 10 V

PARAMETER		TEST CONDITIONS		T_A	MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain	R_L = 100 kΩ, C_L = 20 pF, See Figure 1	$V_{I(PP)}$ = 1 V	25°C		0.62		V/μs
				0°C		0.67		
				70°C		0.51		
			$V_{I(PP)}$ = 5.5 V	25°C		0.56		
				0°C		0.61		
				70°C		0.46		
V_n	Equivalent input noise voltage	f = 1 kHz, R_S = 100 Ω,	See Figure 2	25°C		32		nV/√Hz
B_{OM}	Maximum output swing bandwidth	V_O = V_{OH}, C_L = 20 pF, R_L = 100 kΩ, See Figure 1		25°C		35		kHz
				0°C		40		
				70°C		30		
B_1	Unity-gain bandwidth	V_I = 10 mV, C_L = 20 pF,	See Figure 3	25°C		635		kHz
				0°C		710		
				70°C		510		
ϕ_m	Phase margin	V_I = 10 mV, f = B_1, C_L = 20 pF, See Figure 3		25°C		43°		
				0°C		44°		
				70°C		42°		

electrical characteristics, V_{DD} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	TLC252Y			TLC25L2Y			TLC25M2Y			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_O = 1.4 V, V_{IC} = 0 V, R_S = 50 Ω, See Note 6		1.1	10		1.1	10		1.1	10	mV
α_{VIO}	Average temperature coefficient of input offset voltage			1.8			1.1			1.7		µV/°C
I_{IO}	Input offset current (see Note 4)	V_O = V_{DD}/2, V_{IC} = V_{DD}/2		0.1			0.1			0.1		pA
I_{IB}	Input bias current (see Note 4)	V_O = V_{DD}/2, V_{IC} = V_{DD}/2		0.6			0.6			0.6		pA
V_{ICR}	Common-mode input voltage range (see Note 5)		−0.2 to 4	−0.3 to 4.2		−0.2 to 4	−0.3 to 4.2		−0.2 to 4	−0.3 to 4.2		V
V_{OH}	High-level output voltage	V_{ID} = 100 mV, See Note 6	3.2	3.8		3.2	4.1		3.2	3.9		V
V_{OL}	Low-level output voltage	V_{ID} = −100 mV, I_{OL} = 0		0	50		0	50		0	50	mV
A_{VD}	Large-signal differential voltage amplification	V_O = 0.25 V, See Note 6	5	23		50	700		25	170		V/mV
CMRR	Common-mode rejection ratio	V_{IC} = V_{ICR}min	65	80		65	94		65	91		dB
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)	V_{DD} = 5 V to 10 V, V_O = 1.4 V	65	95		70	97		70	93		dB
I_{DD}	Supply current	V_O = V_{DD}/2, V_{IC} = V_{DD}/2, No load		1.4	3.2		0.02	0.034		0.21	0.56	mA

operating characteristics, V_{DD} = 5 V, T_A = 25°C

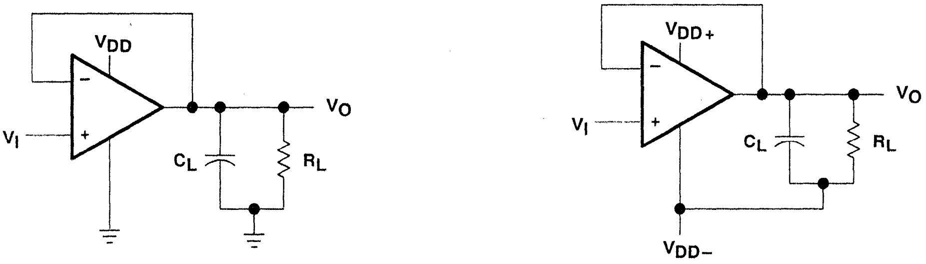
PARAMETER		TEST CONDITIONS		TLC252Y			TLC25L2Y			TLC25M2Y			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
SR	Slew rate at unity gain	C_L = 20 pF, See Note 6	$V_{I(PP)}$ = 1 V		3.6			0.03			0.43		V/µs
			$V_{I(PP)}$ = 2.5 V		2.9			0.03			0.40		
V_n	Equivalent input noise voltage	f = 1 kHz,	R_S = 100 Ω		2.5			68			32		nV/√Hz
B_{OM}	Maximum output swing bandwidth	V_O = V_{OH}, R_L = 10 kΩ	C_L = 20 pF,		320			5			55		kHz
B_1	Unity-gain bandwidth	V_I = 10 mV,	C_L = 20 pF		1.7			0.085			0.525		MHz
ϕ_m	Phase margin	f = B_1, C_L = 20 pF	V_I = 10 mV,		46°			34°			40°		

NOTES: 4. The typical values of input bias current and input offset current below 5 pA were determined mathematically.
5. This range also applies to each input individually.
6. For low-bias mode, R_L = 1 MΩ; for medium-bias mode, R_L = 100 kΩ, and for high-bias mode, R_L = 10 kΩ.

PARAMETER MEASUREMENT INFORMATION

single-supply versus split-supply test circuits

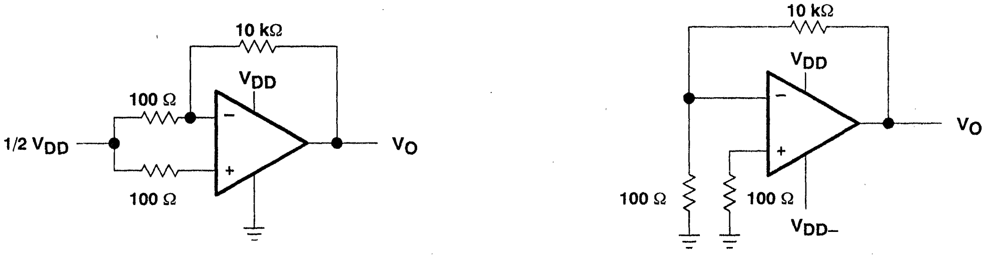
Because the TLC252C, TLC25L2C, and TLC25M2C are optimized for single-supply operation, circuit configurations used for the various tests often present some inconvenience since the input signal, in many cases, must be offset from ground. This inconvenience can be avoided by testing the device with split supplies and the output load tied to the negative rail. A comparison of single-supply versus split-supply test circuits is shown below. The use of either circuit will give the same result.



(a) SINGLE SUPPLY

(b) SPLIT SUPPLY

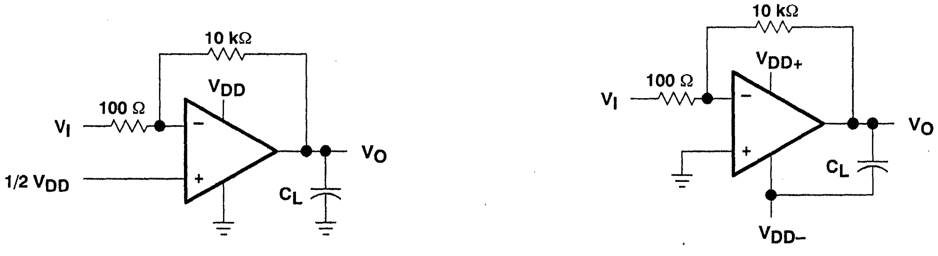
Figure 1. Unity-Gain Amplifier



(a) SINGLE SUPPLY

(a) SPLIT SUPPLY

Figure 2. Noise Test Circuit



(a) SINGLE SUPPLY

(a) SPLIT SUPPLY

Figure 3. Gain-of-100 Inverting Amplifier

TYPICAL CHARACTERISTICS

SUPPLY CURRENT
vs
SUPPLY VOLTAGE

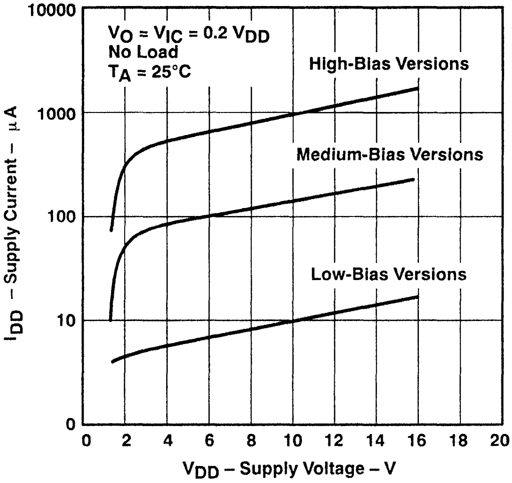


Figure 4

SUPPLY CURRENT
vs
FREE-AIR TEMPERATURE

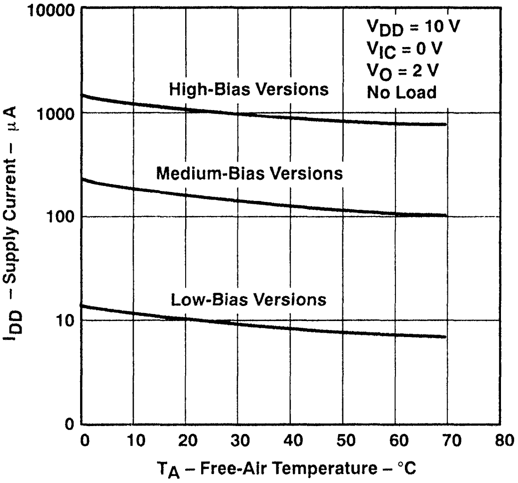


Figure 5

LOW BIAS
LARGE-SIGNAL
DIFFERENTIAL VOLTAGE AMPLIFICATION
and PHASE SHIFT
vs
FREQUENCY

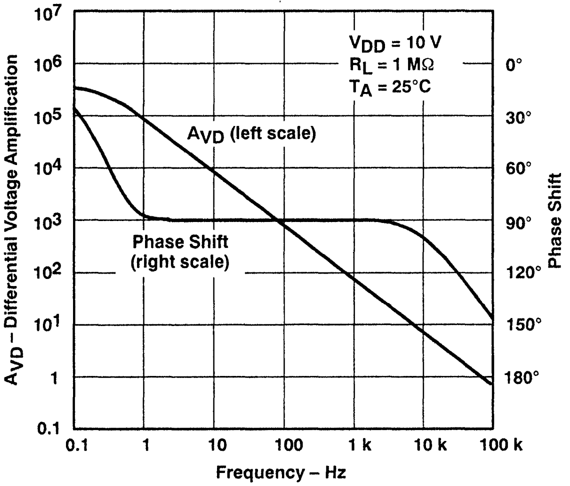


Figure 6

TYPICAL CHARACTERISTICS

MEDIUM BIAS
LARGE-SIGNAL
DIFFERENTIAL VOLTAGE AMPLIFICATION
and PHASE SHIFT
vs
FREQUENCY

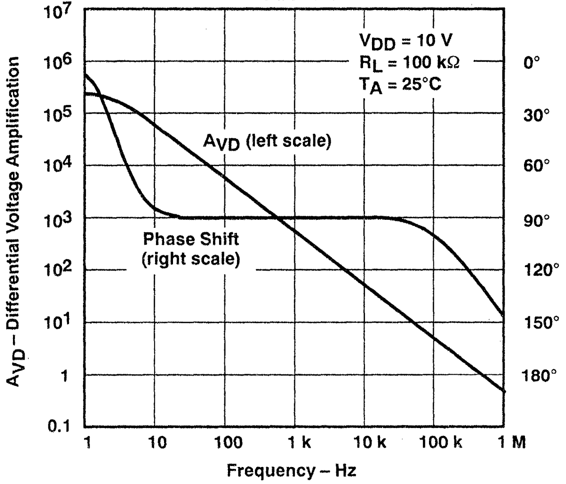


Figure 7

HIGH BIAS
LARGE-SIGNAL
DIFFERENTIAL VOLTAGE AMPLIFICATION
and PHASE SHIFT
vs
FREQUENCY

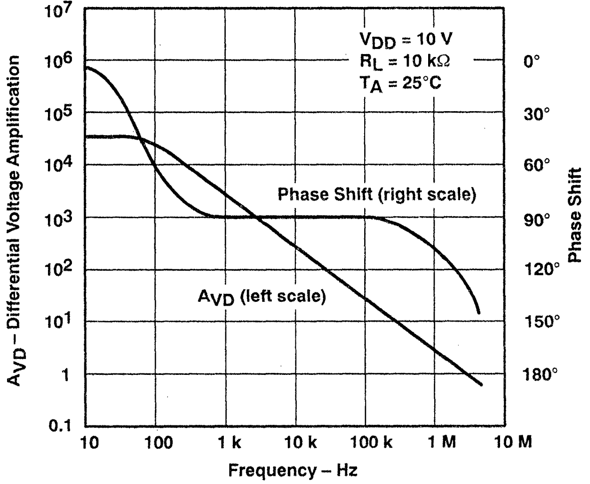


Figure 8

APPLICATION INFORMATION

latch-up avoidance

Junction-isolated CMOS circuits have an inherent parasitic PNPN structure that can function as an SCR. Under certain conditions, this SCR may be triggered into a low-impedance state, resulting in excessive supply current. To avoid such conditions, no voltage greater than 0.3 V beyond the supply rails should be applied to any pin. In general, the op amp supplies should be applied simultaneously with, or before, application of any input signals.

output stage considerations

The amplifier's output stage consists of a source-follower-connected pullup transistor and an open-drain pulldown transistor. The high-level output voltage (V_{OH}) is virtually independent of the I_{DD} selection and increases with higher values of V_{DD} and reduced output loading. The low-level output voltage (V_{OL}) decreases with reduced output current and higher input common-mode voltage. With no load, V_{OL} is essentially equal to the V_{DD-}/GND pin potential.

supply configurations

Even though the TLC25_2C series is characterized for single-supply operation, it can be used effectively in a split-supply configuration if the input common-mode voltage (V_{ICR}), output swing (V_{OL} and V_{OH}), and supply voltage limits are not exceeded.

circuit layout precautions

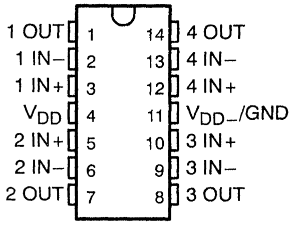
The user is cautioned that whenever extremely high circuit impedances are used, care must be exercised in layout, construction, board cleanliness, and supply filtering to avoid hum and noise pickup, as well as excessive dc leakages.

TLC254C, TLC25L4C, TLC25M4C, TLC254Y, TLC25L4Y, TLC25M4Y
LinCMOS™ QUAD OPERATIONAL AMPLIFIERS

D2753, JUNE 1983–REVISED NOVEMBER 1991

- **A-Suffix Versions Offer 5-mV V_{IO}**
- **B-Suffix Versions Offer 2-mV V_{IO}**
- **Wide Range of Supply Voltages 1.4 V to 16 V**
- **True Single-Supply Operation**
- **Common-Mode Input Voltage Includes the Negative Rail**
- **Low Noise . . . 30 $\text{nV}/\sqrt{\text{Hz}}$ Typ at f = 1 kHz (High-Bias Versions)**

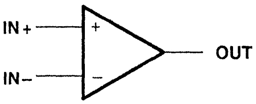
D OR N PACKAGE
(TOP VIEW)



description

The TLC254C, TLC25L4C, and TLC25M4C are low-cost, low-power quad operational amplifiers designed to operate with single or dual supplies. These devices utilize the Texas Instruments silicon gate LinCMOS™ process, giving them stable input offset voltages that are available in selected grades of 2, 5, or 10 mV maximum, very high input impedances, and extremely low input offset and bias currents. Because the input common-mode range extends to the negative rail and the power consumption is extremely low, this series is ideally suited for battery-powered or energy-conserving applications. The series offers operation down to a 1.4-V supply, is stable at unity gain, and has excellent noise characteristics.

symbol (each amplifier)



These devices have internal electrostatic-discharge (ESD) protection circuits that will prevent catastrophic failures at voltages up to 2000 V as tested under MIL-STD-883C, Method 3015.1. However, care should be exercised in handling these devices, as exposure to ESD may result in a degradation of the device parametric performance.

Because of the extremely high input impedance and low input bias and offset currents, applications for the TLC254C series include many areas that have previously been limited to BIFET and NFET product types. Any circuit using high-impedance elements and requiring small offset errors is a good candidate for cost-effective use of these devices. Many features associated with bipolar technology are available with LinCMOS™ operational amplifiers without the power penalties of traditional bipolar devices. General applications such as

AVAILABLE OPTIONS

T_A	V_{IO}max AT 25°C	PACKAGES		CHIP FORM (Y)
		SMALL OUTLINE (D)	PLASTIC DIP (N)	
0°C to 70°C	10 mV	TLC254CD	TLC254CN	TLC254Y TLC25L4Y TLC25M4Y
	5 mV	TLC254ACD	TLC254ACN	
	2 mV	TLC254BCD	TLC254BCN	
	10 mV	TLC25L4CD	TLC25L4CN	
	5 mV	TLC25L4ACD	TLC25L4ACN	
	2 mV	TLC25L2BCD	TLC25L4BCN	
	10 mV	TLC25M4CD	TLC25M4CN	
	5 mV	TLC25M4ACD	TLC25M4ACN	
	2 mV	TLC25M4BCD	TLC25M4BCN	

The D package is available taped and reeled. Add the suffix "R" to the device type (e.g., TLC254CDR). Chips are tested at 25°C.

LinCMOS is a trademark of Texas Instruments Incorporated.

description (continued)

transducer interfacing, analog calculations, amplifier blocks, active filters, and signal buffering are all easily designed with the TLC254C series devices. Remote and inaccessible equipment applications are possible using their low-voltage and low-power capabilities. The TLC254C series is well suited to solve the difficult problems associated with single-battery and solar-cell-powered applications. This series includes devices that are characterized for the commercial temperature range and are available in 14-pin plastic dip (N) and small-outline (D) packages. The device is also available in chip form (Y).

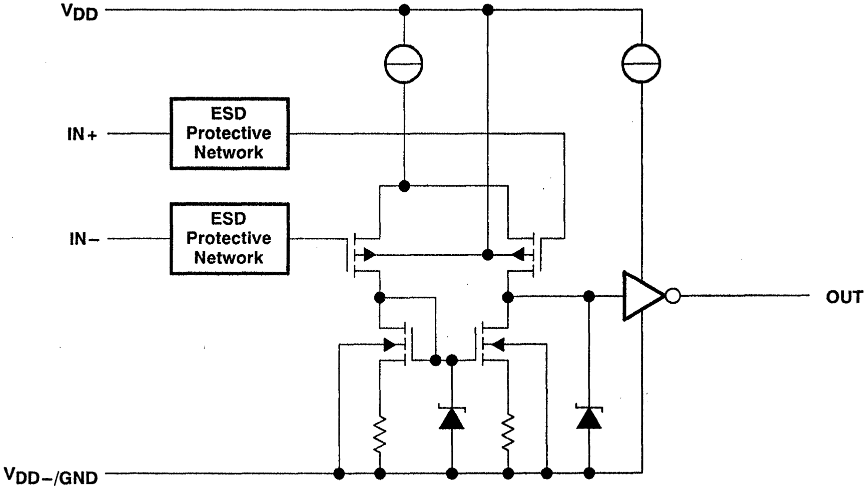
The TLC254C series is characterized for operation from 0°C to 70°C.

DEVICE FEATURES

PARAMETER	TLC25L4C (LOW BIAS)	TLC25M4C (MEDIUM BIAS)	TLC254C (HIGH BIAS)
Supply current (Typ)	40 µA	600 µA	4000 µA
Slew rate (Typ)	0.04 V/µA	0.6 V/µA	4.5 V/µA
Input offset voltage (Max)			
TLC254C, TLC25L4C, TLC25M4C	10 mV	10 mV	10 mV
TLC254AC, TLC25L4AC, TLC25M4AC	5 mV	5 mV	5 mV
TLC254BC, TLC25L4BC, TLC25M4BC	2 mV	2 mV	2 mV
Offset voltage drift (Typ)	0.1 µV/month†	0.1 µV/month†	0.1 µV/month†
Offset voltage temperature coefficient (Typ)	0.7 µV/°C	2 µV/°C	5 µV/°C
Input bias current (Typ)	1 pA	1 pA	1 pA
Input offset current (Typ)	1 pA	1 pA	1 pA

† The long-term drift value applies after the first month.

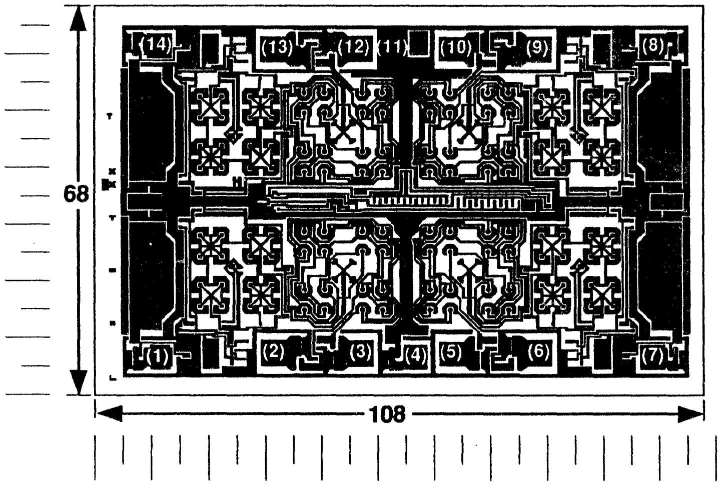
equivalent schematic (each amplifier)

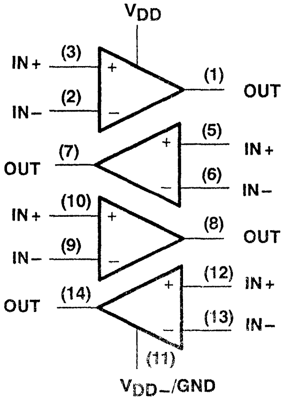


chip information

These chips, properly assembled, display characteristics similar to the TLC25_4C. Thermal compression or ultrasonic bonding may be used on the doped aluminum bonding pads. Chips may be mounted with conductive epoxy or a gold-silicon preform.

BONDING PAD ASSIGNMENTS





CHIP THICKNESS: 15 TYPICAL

BONDING PADS: 4 × 4 MINIMUM

T_{JMAX} = 150°C

TOLERANCES ARE ±10%

ALL DIMENSIONS ARE IN MILS

PIN (11) INTERNALLY CONNECTED TO BACKSIDE OF CHIP

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{DD} (see Note 1)	18 V
Differential input voltage (see Note 2)	±18 V
Input voltage range (any input)	−0.3 V to 18 V
Duration of short circuit at (or below) 25°C free-air temperature (see Note 3)	unlimited
Continuous total dissipation	See Dissipation Rating Table
Operating free-air temperature range	0°C to 70°C
Storage temperature range	−65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C

NOTES: 1. All voltage values, except differential voltages, are with respect to V_{DD-}/GND terminal.
2. Differential voltages are at the noninverting input terminal, with respect to the inverting input terminal.
3. The output may be shorted to either supply. Temperature and/or supply voltages must be limited to ensure the maximum dissipation rating is not exceeded.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING
D	725 mW	5.8 mW/°C	464 mW
N	1050 mW	9.2 mW/°C	736 mW

recommended operating conditions

		MIN	MAX	UNIT
Supply voltage, V_{DD}		1.4	16	V
Common-mode input voltage, V_{IC}	V_{DD} = 1.4 V	0	0.2	V
	V_{DD} = 5 V	−0.2	4	
	V_{DD} = 10 V	−0.2	9	
	V_{DD} = 16 V	−0.2	14	
Operating free-air temperature, T_A		0	70	°C

electrical characteristics at specified free-air temperature, V_{DD} = 1.4 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS†		TLC254_C			TLC25L4_C			TLC25M4_C			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	TLC25_4C	V_O = 0.2 V, R_S = 50 Ω	25°C			10			10			10	mV
				0°C to 70°C			12			12			12	
		TLC25_4AC		25°C			5			5			5	
				0°C to 70°C			6.5			6.5			6.5	
		TLC25_4BC		25°C			2			2			2	
				0°C to 70°C			3			3			3	
α_{VIO}	Average temperature coefficient of input offset voltage			25°C to 70°C		1			1			1		µV/°C
I_{IO}	Input offset current		V_O = 0.2 V	25°C		1			1			1		pA
				0°C to 70°C			300			300			300	
I_{IB}	Input bias current		V_O = 0.2 V	25°C		1			1			1		pA
				0°C to 70°C			600			600			600	
V_{ICR}	Common-mode input voltage range			25°C	0 to 0.2			0 to 0.2			0 to 0.2			V
V_{OM}	Peak output voltage swing‡		V_{ID} = 100 mV	25°C	450	700		450	700		450	700		mV
A_{VD}	Large-signal differential voltage amplification		VO = 100 to 300 mV, R_S = 50 Ω	25°C		10			20			20		V/mV
CMRR	Common-mode rejection ratio		V_O = 0.2 V, V_{IC} = V_{ICR}min	25°C	60	77		60	77		60	77		dB
I_{DD}	Supply current		No load, V_O = 0.2 V	25°C		600	750		50	68		400	500	µA

† All characteristics are measured under open-loop conditions with zero common-mode input voltage unless otherwise specified. Unless otherwise noted, an output load resistor is connected from the output to ground and has the following value: for low bias, R_L = 1 MΩ, for medium bias, R_L = 100 kΩ, and for high bias, R_L = 10 kΩ.

‡ The output will swing to the potential of the V_{DD-}/GND pin.

operating characteristics, V_{DD} = 1.4 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	TLC254_C			TLC25L4_C			TLC25M4_C			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
B_1	Unity-gain bandwidth	A_V = 40 dB, C_L = 10 pF, R_S = 50 Ω		12			12			12		kHz
SR	Slew rate at unity gain	See Figure 1		0.1			0.001			0.01		V/µs
	Overshoot factor	See Figure 1		30%			35%			35%		

electrical characteristics at specified free-air temperature, V_{DD} = 5 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS	T_A†	MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	TLC254C	V_O = 1.4 V, V_{IC} = 0, R_S = 50 Ω, R_L = 10 kΩ	25°C		1.1	10	mV
				Full range			12	
		TLC254AC	V_O = 1.4 V, V_{IC} = 0, R_S = 50 Ω, R_L = 10 kΩ	25°C		0.9	5	
				Full range			6.5	
		TLC254BC	V_O = 1.4 V, V_{IC} = 0, R_S = 50 Ω, R_L = 10 kΩ	25°C		0.34	2	
				Full range			3	
α_{VIO}	Average temperature coefficient of input offset voltage			25°C to 70°C		1.8		μV/°C
I_{IO}	Input offset current (see Note 4)		V_O = 2.5 V, V_{IC} = 2.5 V	25°C		0.1		pA
				70°C		7	300	
I_{IB}	Input bias current (see Note 4)		V_O = 2.5 V, V_{IC} = 2.5 V	25°C		0.6		pA
				70°C		40	600	
V_{ICR}	Common-mode input voltage range (see Note 5)			25°C	−0.2 to 4	−0.3 to 4.2		V
				Full range	−0.2 to 3.5			V
V_{OH}	High-level output voltage		V_{ID} = 100 mV, R_L = 10 kΩ	25°C	3.2	3.8		V
				0°C	3	3.8		
				70°C	3	3.8		
V_{OL}	Low-level output voltage		V_{ID} = −100 mV, I_{OL} = 0	25°C		0	50	mV
				0°C		0	50	
				70°C		0	50	
A_{VD}	Large-signal differential voltage amplification		V_O = 0.25 V to 2 V, R_L = 10 kΩ	25°C	5	23		V/mV
				0°C	4	27		
				70°C	4	20		
CMRR	Common-mode rejection ratio		V_{IC} = V_{ICR}min	25°C	65	80		dB
				0°C	60	84		
				70°C	60	85		
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)		V_{DD} = 5 V to 10 V, V_O = 1.4 V	25°C	65	95		dB
				0°C	60	94		
				70°C	60	96		
I_{DD}	Supply current (four amplifiers)		V_O = 2.5 V, V_{IC} = 2.5 V, No load	25°C		2.7	6.4	mA
				0°C		3.1	7.2	
				70°C		2.3	5.2	

† Full range is 0°C to 70°C.

NOTES: 4. The typical values of input bias current and input offset current below 5 pA were determined mathematically.

5. This range also applies to each input individually.

electrical characteristics at specified free-air temperature, V_{DD} = 10 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS	T_A†	MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	TLC254C	V_O = 1.4 V, V_{IC} = 0, R_S = 50 Ω, R_L = 10 kΩ	25°C		1.1	10	mV
				Full range			12	
		TLC254AC	V_O = 1.4 V, V_{IC} = 0, R_S = 50 Ω, R_L = 10 kΩ	25°C		0.9	5	
				Full range			6.5	
		TLC254BC	V_O = 1.4 V, V_{IC} = 0, R_S = 50 Ω, R_L = 10 kΩ	25°C		0.39	2	
				Full range			3	
α_{VIO}	Average temperature coefficient of input offset voltage			25°C to 70°C		2		μV/°C
I_{IO}	Input offset current (see Note 4)		V_O = 5 V, V_{IC} = 5 V	25°C		0.1		pA
				70°C		7	300	
I_{IB}	Input bias current (see Note 4)		V_O = 5 V, V_{IC} = 5 V	25°C		0.7		pA
				70°C		50	600	
V_{ICR}	Common-mode input voltage range (see Note 5)			25°C	−0.2 to 9	−0.3 to 9.2		V
				Full range	−0.2 to 8.5			V
V_{OH}	High-level output voltage		V_{ID} = 100 mV, R_L = 10 kΩ	25°C	8	8.5		V
				0°C	7.8	8.5		
				70°C	7.8	8.4		
V_{OL}	Low-level output voltage		V_{ID} = −100 mV, I_{OL} = 0	25°C		0	50	mV
				0°C		0	50	
				70°C		0	50	
A_{VD}	Large-signal differential voltage amplification		V_O = 1 V to 6 V, R_L = 10 kΩ	25°C	10	36		V/mV
				0°C	7.5	42		
				70°C	7.5	32		
CMRR	Common-mode rejection ratio		V_{IC} = V_{ICR}min	25°C	65	85		dB
				0°C	60	88		
				70°C	60	88		
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)		V_{DD} = 5 V to 10 V, V_O = 1.4 V	25°C	65	95		dB
				0°C	60	94		
				70°C	60	96		
I_{DD}	Supply current (four amplifiers)		V_O = 5 V, V_{IC} = 5 V, No load	25°C		3.8	8	mA
				0°C		4.5	8.8	
				70°C		3.2	6.8	

† Full range is 0°C to 70°C.

NOTES: 4. The typical values of input bias current and input offset current below 5 pA were determined mathematically.
5. This range also applies to each input individually.

operating characteristics, V_{DD} = 5 V

PARAMETER		TEST CONDITIONS		T_A	MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain	R_L = 10 kΩ, C_L = 20 pF, See Figure 1	$V_{I(PP)}$ = 1 V	25°C		3.6		V/μs
				0°C		4		
				70°C		3		
			$V_{I(PP)}$ = 2.5 V	25°C		2.9		
				0°C		3.1		
				70°C		2.5		
V_n	Equivalent input noise voltage	f = 1 kHz, R_S = 100 Ω, See Figure 2		25°C		25		nV/√Hz
B_{OM}	Maximum output swing bandwidth	V_O = V_{OH}, C_L = 20 pF, R_L = 10 kΩ, See Figure 1		25°C		320		kHz
				0°C		340		
				70°C		260		
B_1	Unity-gain bandwidth	V_I = 10 mV, C_L = 20 pF, See Figure 3		25°C		1.7		MHz
				0°C		2		
				70°C		1.3		
ϕ_m	Phase margin	V_I = 10 mV, f = B_1, C_L = 20 pF, See Figure 3		25°C		46°		
				0°C		47°		
				70°C		44°		

operating characteristics, V_{DD} = 10 V

PARAMETER		TEST CONDITIONS		T_A	MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain	R_L = 10 kΩ, C_L = 20 pF See Figure 1	$V_{I(PP)}$ = 1 V	25°C		5.3		V/μs
				0°C		5.9		
				70°C		4.3		
			$V_{I(PP)}$ = 5.5 V	25°C		4.6		
				0°C		5.1		
				70°C		3.8		
V_n	Equivalent input noise voltage	f = 1 kHz, R_S = 100 Ω, See Figure 2		25°C		25		nV/√Hz
B_{OM}	Maximum output swing bandwidth	V_O = V_{OH}, C_L = 20 pF, R_L = 10 kΩ, See Figure 1		25°C		200		kHz
				0°C		220		
				70°C		140		
B_1	Unity-gain bandwidth	V_I = 10 mV, C_L = 20 pF, See Figure 3		25°C		2.2		MHz
				0°C		2.5		
				70°C		1.8		
ϕ_m	Phase margin	V_I = 10 mV, f = B_1, C_L = 20 pF, See Figure 3		25°C		49°		
				0°C		50°		
				70°C		46°		

electrical characteristics at specified free-air temperature, V_{DD} = 5 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS	T_A†	MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	TLC25L4C	V_O = 1.4 V, V_{IC} = 0, R_S = 50 Ω, R_L = 1 MΩ	25°C		1.1	10	mV
				Full range			12	
		TLC25L4AC	V_O = 1.4 V, V_{IC} = 0, R_S = 50 Ω, R_L = 1 MΩ	25°C		0.9	5	
				Full range			6.5	
		TLC25L4BC	V_O = 1.4 V, V_{IC} = 0, R_S = 50 Ω, R_L = 1 MΩ	25°C		0.24	2	
				Full range			3	
α_{VIO}	Average temperature coefficient of input offset voltage			25°C to 70°C		1.1		µV/°C
I_{IO}	Input offset current (see Note 4)		V_O = 2.5 V, V_{IC} = 2.5 V	25°C		0.1		pA
				70°C		7	300	
I_{IB}	Input bias current (see Note 4)		V_O = 2.5 V, V_{IC} = 2.5 V	25°C		0.6		pA
				70°C		40	600	
V_{ICR}	Common-mode input voltage range (see Note 5)			25°C	−0.2 to 4	−0.3 to 4.2		V
				Full range	−0.2 to 3.5			V
V_{OH}	High-level output voltage		V_{ID} = 100 mV, R_L = 1 MΩ	25°C	3.2	4.1		V
				0°C	3	4.1		
				70°C	3	4.2		
V_{OL}	Low-level output voltage		V_{ID} = −100 mV, I_{OL} = 0	25°C		0	50	mV
				0°C		0	50	
				70°C		0	50	
A_{VD}	Large-signal differential voltage amplification		V_O = 0.25 V to 2 V, R_L = 1 MΩ	25°C	50	520		V/mV
				0°C	50	680		
				70°C	50	380		
CMRR	Common-mode rejection ratio		V_{IC} = V_{ICR}min	25°C	65	94		dB
				0°C	60	95		
				70°C	60	95		
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)		V_{DD} = 5 V to 10 V, V_O = 1.4 V	25°C	70	97		dB
				0°C	60	97		
				70°C	60	98		
I_{DD}	Supply current (four amplifiers)		V_O = 2.5 V, V_{IC} = 2.5 V, No load	25°C		40	68	µA
				0°C		48	84	
				70°C		31	56	

† Full range is 0°C to 70°C.

NOTES: 4. The typical values of input bias current and input offset current below 5 pA were determined mathematically.
5. This range also applies to each input individually.

electrical characteristics at specified free-air temperature, V_{DD} = 10 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS		T_A†	MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	TLC25L4C	V_O = 1.4 V, R_S = 50 Ω,	V_{IC} = 0, R_L = 1 MΩ	25°C		1.1	10	mV
					Full range			12	
		TLC25L4AC	V_O = 1.4 V, R_S = 50 Ω,	V_{IC} = 0, R_L = 1 MΩ	25°C		0.9	5	
					Full range			6.5	
		TLC25L4BC	V_O = 1.4 V, R_S = 50 Ω,	V_{IC} = 0, R_L = 1 MΩ	25°C		0.26	2	
					Full range			3	
α_{VIO}	Average temperature coefficient of input offset voltage				25°C to 70°C		1		µV/°C
I_{IO}	Input offset current (see Note 4)		V_O = 5 V,	V_{IC} = 5 V	25°C		0.1		pA
					70°C		7	300	
I_{IB}	Input bias current (see Note 4)		V_O = 5 V,	V_{IC} = 5 V	25°C		0.7		pA
					70°C		50	600	
V_{ICR}	Common-mode input voltage range (see Note 5)				25°C	−0.2 to 9	−0.3 to 9.2		V
					Full range	−0.2 to 8.5			V
V_{OH}	High-level output voltage		V_{ID} = 100 mV,	R_L = 1 MΩ	25°C	8	8.9		V
					0°C	7.8	8.9		
					70°C	7.8	8.9		
V_{OL}	Low-level output voltage		V_{ID} = −100 mV,	I_{OL} = 0	25°C		0	50	mV
					0°C		0	50	
					70°C		0	50	
A_{VD}	Large-signal differential voltage amplification		V_O = 1 V to 6 V,	R_L = 1 MΩ	25°C	50	870		V/mV
					0°C	50	1020		
					70°C	50	660		
CMRR	Common-mode rejection ratio		V_{IC} = V_{ICR}min		25°C	65	97		dB
					0°C	60	97		
					70°C	60	97		
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)		V_{DD} = 5 V to 10 V,	V_O = 1.4 V	25°C	70	97		dB
					0°C	60	97		
					70°C	60	98		
I_{DD}	Supply current (four amplifiers)		V_O = 5 V, No load	V_{IC} = 5 V,	25°C		57	92	µA
					0°C		72	132	
					70°C		44	80	

† Full range is 0°C to 70°C.

NOTES: 4. The typical values of input bias current and input offset current below 5 pA were determined mathematically.

5. This range also applies to each input individually.

operating characteristics, V_{DD} = 5 V

PARAMETER		TEST CONDITIONS		T_A	MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain	R_L = 1 MΩ, C_L = 20 pF, See Figure 1	$V_{I(PP)}$ = 1 V	25°C		0.03		V/μs
				0°C		0.04		
				70°C		0.03		
			$V_{I(PP)}$ = 2.5 V	25°C		0.03		
				0°C		0.03		
				70°C		0.02		
V_n	Equivalent input noise voltage	f = 1 kHz, R_S = 100 Ω, See Figure 2		25°C		70		nV/√Hz
B_{OM}	Maximum output swing bandwidth	V_O = V_{OH}, C_L = 20 pF, R_L = 1 MΩ, See Figure 1		25°C		5		kHz
				0°C		6		
				70°C		4.5		
B_1	Unity-gain bandwidth	V_I = 10 mV, C_L = 20 pF, See Figure 3		25°C		85		kHz
				0°C		100		
				70°C		65		
ϕ_m	Phase margin	V_I = 10 mV, f = B_1, C_L = 20 pF, See Figure 3		25°C		34°		
				0°C		36°		
				70°C		30°		

operating characteristics, V_{DD} = 10 V

PARAMETER		TEST CONDITIONS		T_A	MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain	R_L = 1 MΩ, C_L = 20 pF See Figure 1	$V_{I(PP)}$ = 1 V	25°C		0.05		V/μs
				0°C		0.05		
				70°C		0.04		
			$V_{I(PP)}$ = 5.5 V	25°C		0.04		
				0°C		0.05		
				70°C		0.04		
V_n	Equivalent input noise voltage	f = 1 kHz, R_S = 100 Ω, See Figure 2		25°C		70		nV/√Hz
B_{OM}	Maximum output swing bandwidth	V_O = V_{OH}, C_L = 20 pF, R_L = 1 MΩ, See Figure 1		25°C		1		kHz
				0°C		1.3		
				70°C		0.9		
B_1	Unity-gain bandwidth	V_I = 10 mV, C_L = 20 pF, See Figure 3		25°C		110		kHz
				0°C		125		
				70°C		90		
ϕ_m	Phase margin	V_I = 10 mV, f = B_1, C_L = 20 pF, See Figure 3		25°C		38°		
				0°C		40°		
				70°C		34°		

electrical characteristics at specified free-air temperature, V_{DD} = 5 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS		T_A†	MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	TLC25M4C	V_O = 1.4 V,	V_{IC} = 0,	25°C		1.1	10	mV
			R_S = 50 Ω,	R_L = 100 kΩ	Full range			12	
		TLC25M4AC	V_O = 1.4 V,	V_{IC} = 0,	25°C		0.9	5	
			R_S = 50 Ω,	R_L = 100 kΩ	Full range			6.5	
		TLC25M4BC	V_O = 1.4 V,	V_{IC} = 0,	25°C		0.25	2	
			R_S = 50 Ω,	R_L = 100 kΩ	Full range			3	
α_{VIO}	Average temperature coefficient of input offset voltage				25°C to 70°C		1.7		μV/°C
I_{IO}	Input offset current (see Note 4)		V_O = 2.5 V,	V_{IC} = 2.5 V	25°C		0.1		pA
					70°C		7	300	
I_{IB}	Input bias current (see Note 4)		V_O = 2.5 V,	V_{IC} = 2.5 V	25°C		0.6		pA
					70°C		40	600	
V_{ICR}	Common-mode input voltage range (see Note 5)				25°C	−0.2 to 4	−0.3 to 4.2		V
					Full range	−0.2 to 3.5			V
V_{OH}	High-level output voltage		V_{ID} = 100 mV,	R_L = 100 kΩ	25°C	3.2	3.9		V
					0°C	3	3.9		
					70°C	3	4		
V_{OL}	Low-level output voltage		V_{ID} = −100 mV,	I_{OL} = 0	25°C		0	50	mV
					0°C		0	50	
					70°C		0	50	
A_{VD}	Large-signal differential voltage amplification		V_O = 0.25 V to 2 V,	R_L = 100 kΩ	25°C	25	170		V/mV
					0°C	15	200		
					70°C	15	140		
CMRR	Common-mode rejection ratio		V_{IC} = V_{ICR}min		25°C	65	91		dB
					0°C	60	91		
					70°C	60	92		
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)		V_{DD} = 5 V to 10 V,	V_O = 1.4 V	25°C	70	93		dB
					0°C	60	92		
					70°C	60	94		
I_{DD}	Supply current (four amplifiers)		V_O = 2.5 V, No load	V_{IC} = 2.5 V,	25°C		420	1120	μA
					0°C		500	1280	
					70°C		340	880	

† Full range is 0°C to 70°C.

NOTES: 4. The typical values of input bias current and input offset current below 5 pA were determined mathematically.

5. This range also applies to each input individually.

electrical characteristics at specified free-air temperature, V_{DD} = 10 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS	T_A†	MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	TLC25M4C	V_O = 1.4 V, V_{IC} = 0, R_S = 50 Ω, R_L = 100 kΩ	25°C		1.1	10	mV
				Full range			12	
		TLC25M4AC	V_O = 1.4 V, V_{IC} = 0, R_S = 50 Ω, R_L = 100 kΩ	25°C		0.9	5	
				Full range			6.5	
		TLC25M4BC	V_O = 1.4 V, V_{IC} = 0, R_S = 50 Ω, R_L = 100 kΩ	25°C		0.26	2	
				Full range			3	
α_{VIO}	Average temperature coefficient of input offset voltage			25°C to 70°C		2.1		μV/°C
I_{IO}	Input offset current (see Note 4)		V_O = 5 V, V_{IC} = 5 V	25°C		0.1		pA
				70°C		7	300	
I_{IB}	Input bias current (see Note 4)		V_O = 5 V, V_{IC} = 5 V	25°C		0.7		pA
				70°C		50	600	
V_{ICR}	Common-mode input voltage range (see Note 5)			25°C	−0.2 to 9	−0.3 to 9.2		V
				Full range	−0.2 to 8.5			V
V_{OH}	High-level output voltage		V_{ID} = 100 mV, R_L = 100 kΩ	25°C	8	8.7		V
				0°C	7.8	8.7		
				70°C	7.8	8.7		
V_{OL}	Low-level output voltage		V_{ID} = −100 mV, I_{OL} = 0	25°C		0	50	mV
				0°C		0	50	
				70°C		0	50	
A_{VD}	Large-signal differential voltage amplification		V_O = 1 V to 6 V, R_L = 100 kΩ	25°C	25	275		V/mV
				0°C	15	320		
				70°C	15	230		
CMRR	Common-mode rejection ratio		$V_{IC} = V_{ICR}$min	25°C	65	94		dB
				0°C	60	94		
				70°C	60	94		
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)		V_{DD} = 5 V to 10 V, V_O = 1.4 V	25°C	70	93		dB
				0°C	60	92		
				70°C	60	94		
I_{DD}	Supply current (four amplifiers)		V_O = 5 V, V_{IC} = 5 V, No load	25°C		570	1200	μA
				0°C		690	1600	
				70°C		440	1120	

† Full range is 0°C to 70°C.

NOTES: 4. The typical values of input bias current and input offset current below 5 pA were determined mathematically.
5. This range also applies to each input individually.

operating characteristics, V_{DD} = 5 V

PARAMETER		TEST CONDITIONS		T_A	MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain	R_L = 100 kΩ, C_L = 20 pF, See Figure 1	$V_{I(PP)}$ = 1 V	25°C		0.43		V/μs
				0°C		0.46		
				70°C		0.36		
			$V_{I(PP)}$ = 2.5 V	25°C		0.40		
				0°C		0.43		
				70°C		0.34		
V_n	Equivalent input noise voltage	f = 1 kHz, R_S = 100 Ω,	See Figure 2	25°C		32		nV/√Hz
B_{OM}	Maximum output swing bandwidth	V_O = V_{OH}, C_L = 20 pF, R_L = 100 kΩ, See Figure 1		25°C		55		kHz
				0°C		60		
				70°C		50		
B_1	Unity-gain bandwidth	V_I = 10 mV, C_L = 20 pF,	See Figure 3	25°C		525		kHz
				0°C		610		
				70°C		400		
ϕ_m	Phase margin	V_I = 10 mV, f = B_1, C_L = 20 pF, See Figure 3		25°C		40°		
				0°C		41°		
				70°C		39°		

operating characteristics, V_{DD} = 10 V

PARAMETER		TEST CONDITIONS		T_A	MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain	R_L = 100 kΩ, C_L = 20 pF, See Figure 1	$V_{I(PP)}$ = 1 V	25°C		0.62		V/μs
				0°C		0.67		
				70°C		0.51		
			$V_{I(PP)}$ = 5.5 V	25°C		0.56		
				0°C		0.61		
				70°C		0.46		
V_n	Equivalent input noise voltage	f = 1 kHz, R_S = 100 Ω,	See Figure 2	25°C		32		nV/√Hz
B_{OM}	Maximum output swing bandwidth	V_O = V_{OH}, C_L = 20 pF, R_L = 100 kΩ, See Figure 1		25°C		35		kHz
				0°C		40		
				70°C		30		
B_1	Unity-gain bandwidth	V_I = 10 mV, C_L = 20 pF,	See Figure 3	25°C		635		kHz
				0°C		710		
				70°C		510		
ϕ_m	Phase margin	V_I = 10 mV, f = B_1, C_L = 20 pF, See Figure 3		25°C		43°		
				0°C		44°		
				70°C		42°		

electrical characteristics, V_{DD} = 5 V, T_A = 25°C

PARAMETER			TEST CONDITIONS	TLC254Y			TLC25L4Y			TLC25M4Y			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	TLC25_4Y	V_O = 1.4 V, V_{IC} = 0 V, R_S = 50 Ω, See Note 6		1.1	10		1.1	10		1.1	10	mV
α_{VIO}	Average temperature coefficient of input offset voltage				1.8			1.1			1.7		μV/°C
I_{IO}	Input offset current (see Note 4)		$V_O = V_{DD}/2$, $V_{IC} = V_{DD}/2$		0.1			0.1			0.1		pA
I_{IB}	Input bias current (see Note 4)		$V_O = V_{DD}/2$, $V_{IC} = V_{DD}/2$		0.6			0.6			0.6		pA
V_{ICR}	Common-mode input voltage range (see Note 5)			−0.2 to 4	−0.3 to 4.2		−0.2 to 4	−0.3 to 4.2		−0.2 to 4	−0.3 to 4.2		V
V_{OH}	High-level output voltage		V_{ID} = 100 mV, R_L = 100 kΩ	3.2	3.8		3.2	4.1		3.2	3.9		V
V_{OL}	Low-level output voltage		V_{ID} = −100 mV, I_{OL} = 0		0	50		0	50		0	50	mV
A_{VD}	Large-signal differential voltage amplification		V_O = 0.25 V, See Note 6	5	23		50	520		25	170		V/mV
CMRR	Common-mode rejection ratio		$V_{IC} = V_{ICR}$min	65	80		65	94		65	91		dB
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)		V_{DD} = 5 V to 10 V, V_O = 1.4 V	65	95		70	97		70	93		dB
I_{DD}	Supply current		$V_O = V_{DD}/2$, $V_{IC} = V_{DD}/2$, No load		2.7	6.4		0.04	0.068		0.42	1.12	mA

† For high-bias mode, R_L = 10 kΩ; for medium-bias mode, R_L = 100 kΩ; for low-bias mode, R_L = 1 MΩ.

NOTES: 4. The typical values of input bias current and input offset current below 5 pA were determined mathematically.

5. This range also applies to each input individually.

6. For low-biased mode, R_L = 1 MΩ; for medium-biased mode, R_L = 100 kΩ, and for high-biased mode, R_L = 10 kΩ.

operating characteristics, V_{DD} = 5 V, T_A = 25°C

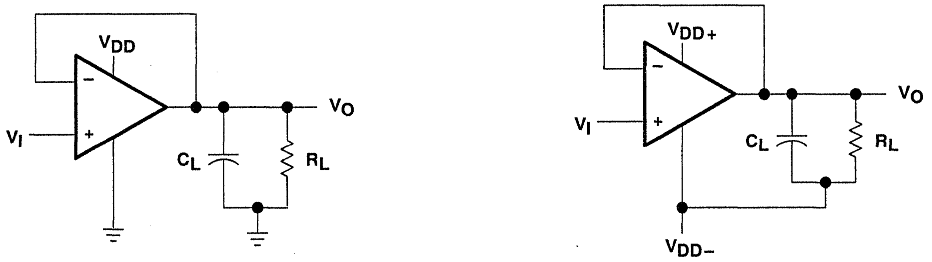
PARAMETER		TEST CONDITIONS		TLC252Y			TLC25L2Y			TLC25M2Y			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
SR	Slew rate at unity gain	C_L = 20 pF, See Note 6	$V_{I(PP)}$ = 1 V		3.6			0.03			0.43		V/μs
			$V_{I(PP)}$ = 2.5 V		2.9			0.03			0.40		
V_n	Equivalent input noise voltage	f = 1 kHz,	R_S = 100 Ω		25			70			32		nV/√Hz
B_{OM}	Maximum output swing bandwidth	$V_O = V_{OH}$, R_L = 10 kΩ	C_L = 20 pF,		320			5			55		kHz
B_1	Unity-gain bandwidth	V_I = 10 mV,	C_L = 20 pF		1.7			0.085			0.525		MHz
ϕ_m	Phase margin	f = B_1, C_L = 20 pF	V_I = 10 mV,		46°			34°			40°		

NOTE 6: For low-biased mode, R_L = 1 MΩ, for medium-biased mode, R_L = 100 kΩ, and for high-biased mode, R_L = 10 kΩ.

PARAMETER MEASUREMENT INFORMATION

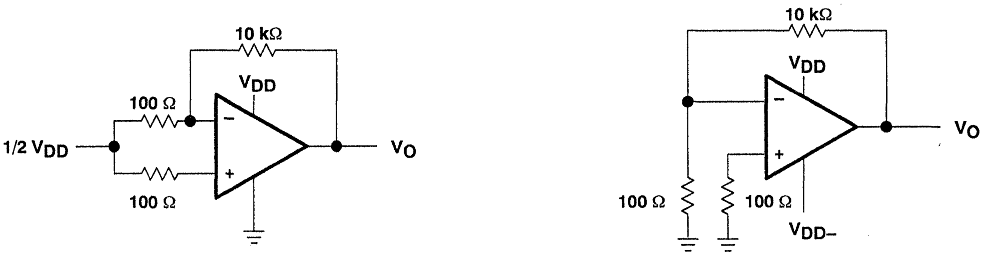
single-supply versus split-supply test circuits

Because the TLC254C, TLC25L4C, and TLC25M4C are optimized for single-supply operation, circuit configurations used for the various tests often present some inconvenience since the input signal, in many cases, must be offset from ground. This inconvenience can be avoided by testing the device with split supplies and the output load tied to the negative rail. A comparison of single-supply versus split-supply test circuits is shown below. The use of either circuit will give the same result.



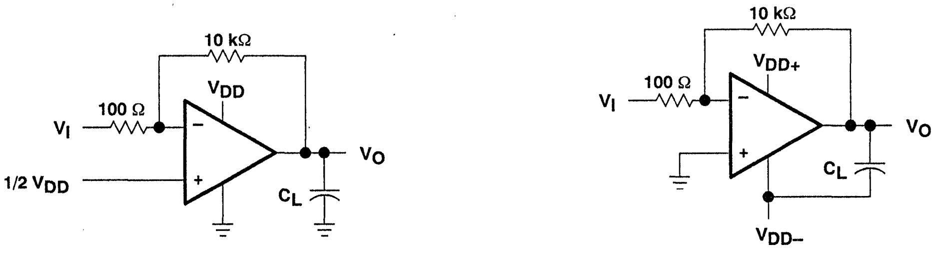
(a) SINGLE SUPPLY (b) SPLIT SUPPLY

Figure 1. Unity-Gain Amplifier



(a) SINGLE SUPPLY (a) SPLIT SUPPLY

Figure 2. Noise Test Circuit



(a) SINGLE SUPPLY (a) SPLIT SUPPLY

Figure 3. Gain-of-100 Inverting Amplifier

TYPICAL CHARACTERISTICS

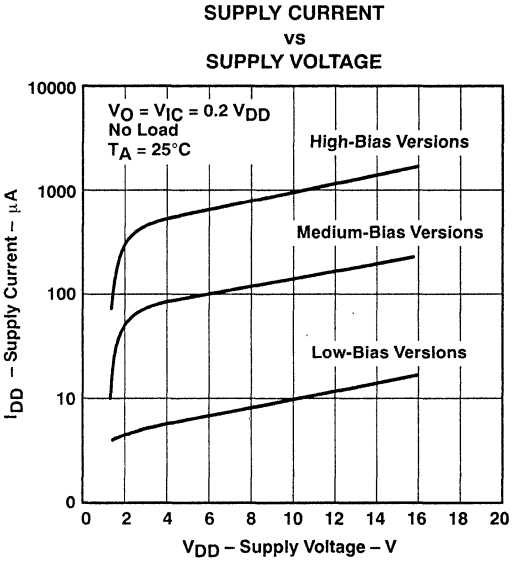


Figure 4

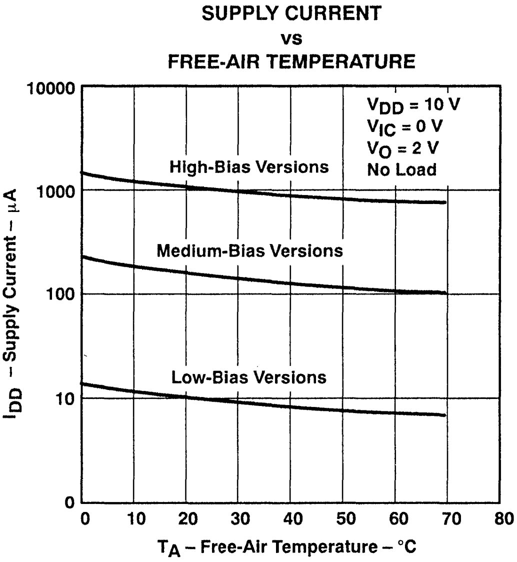


Figure 5

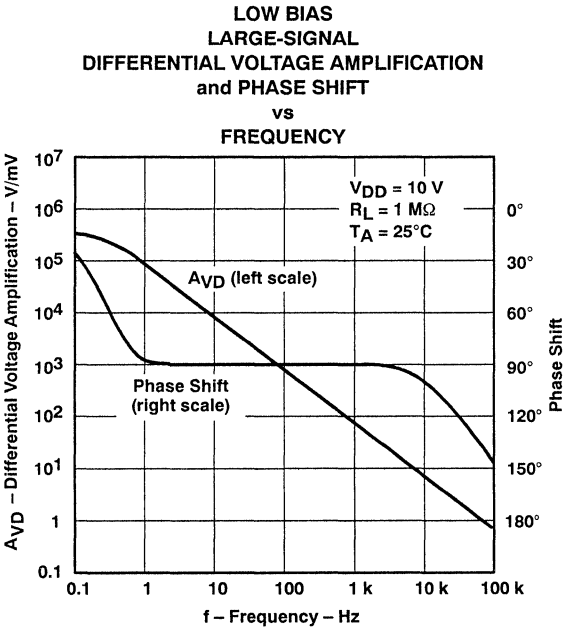


Figure 6

TYPICAL CHARACTERISTICS

MEDIUM BIAS
LARGE-SIGNAL
DIFFERENTIAL VOLTAGE AMPLIFICATION
and PHASE SHIFT
vs
FREQUENCY

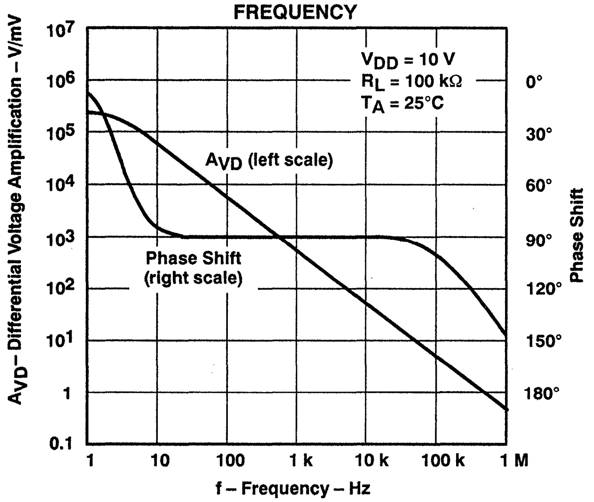


Figure 7

HIGH BIAS
LARGE-SIGNAL
DIFFERENTIAL VOLTAGE AMPLIFICATION
and PHASE SHIFT
vs
FREQUENCY

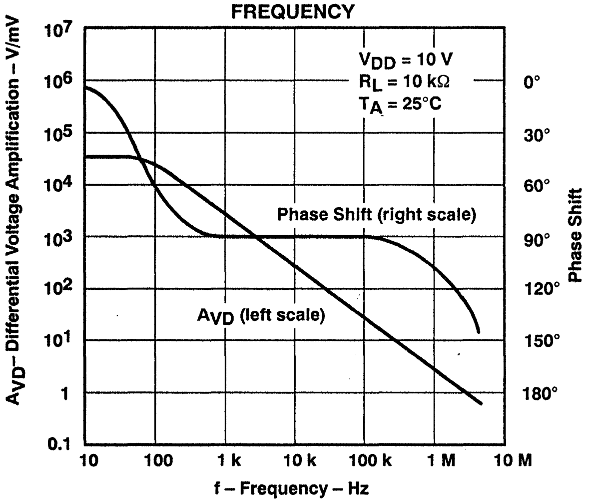


Figure 8

APPLICATION INFORMATION

latch-up avoidance

Junction-isolated CMOS circuits have an inherent parasitic PNPN structure that can function as an SCR. Under certain conditions, this SCR may be triggered into a low-impedance state, resulting in excessive supply current. To avoid such conditions, no voltage greater than 0.3 V beyond the supply rails should be applied to any pin. In general, the op amp supplies should be established simultaneously with, or before, application of any input signals.

output stage considerations

The amplifier's output stage consists of a source-follower-connected pullup transistor and an open-drain pulldown transistor. The high-level output voltage (V_{OH}) is virtually independent of the I_{DD} selection and increases with higher values of V_{DD} and reduced output loading. The low-level output voltage (V_{OL}) decreases with reduced output current and higher input common-mode voltage. With no load, V_{OL} is essentially equal to the V_{DD-}/GND pin potential.

supply configurations

Even though the TLC25_4C series is characterized for single-supply operation, it can be used effectively in a split-supply configuration if the input common-mode voltage (V_{ICR}), output swing (V_{OL} and V_{OH}), and supply voltage limits are not exceeded.

circuit layout precautions

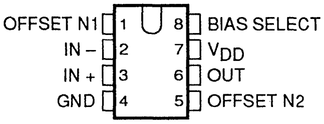
Whenever extremely high circuit impedances are used, care must be exercised in layout, construction, board cleanliness, and supply filtering to avoid hum and noise pickup as well as excessive dc leakages.

TLC271, TLC271A, TLC271B
LinCMOS™ PROGRAMMABLE LOW-POWER OPERATIONAL AMPLIFIERS

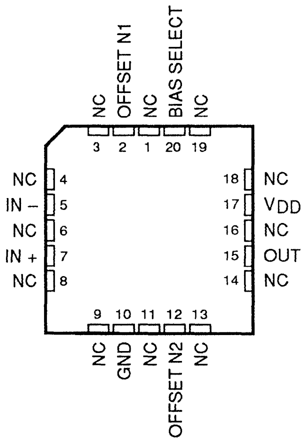
D3137, NOVEMBER 1987 – REVISED JUNE 1991

- Input Offset Voltage Drift . . . Typically 0.1 μV/Month, Including the First 30 Days
- Wide Range of Supply Voltages Over Specified Temperature Range:
  0°C to 70°C . . . 3 V to 16 V
  – 40°C to 85°C . . . 4 V to 16 V
  – 55°C to 125°C . . . 5 V to 16 V
- Single-Supply Operation
- Common-Mode Input Voltage Range Extends Below the Negative Rail (C-Suffix and I-Suffix Types)
- Low Noise . . . 25 nV/√Hz Typically at f = 1 kHz (High-Bias Mode)
- Output Voltage Range Includes Negative Rail
- High Input Impedance . . . 10^{12} Ω Typical
- ESD-Protection Circuitry
- Small-Outline Package Option Also Available In Tape and Reel
- Designed-In Latch-Up Immunity

D, JG, OR P PACKAGE
(TOP VIEW)



FK PACKAGE
(TOP VIEW)



NC – No internal connection

description

The TLC271 operational amplifier combines a wide range of input offset voltage grades with low offset voltage drift and high input impedance. In addition, the TLC271 offers a bias select mode that allows the user to select the best combination of power dissipation and ac performance for a particular application. These devices use Texas Instruments silicon-gate LinCMOS™ technology, which provides offset voltage stability far exceeding the stability available with conventional metal-gate processes.

AVAILABLE OPTIONS

T_A	V_{IO} MAX AT 25°C	PACKAGE			
		SMALL OUTLINE (D)	CHIP CARRIER (FK)	CERAMIC DIP (JG)	PLASTIC DIP (P)
0°C to 70°C	2 mV	TLC271BCD	–	–	TLC271BCP
	5 mV	TLC271ACD	–	–	TLC271ACP
	10 mV	TLC271CD	–	–	TLC271CP
– 40°C to 85°C	2 mV	TLC271BID	–	–	TLC271BIP
	5 mV	TLC271AID	–	–	TLC271AIP
	10 mV	TLC271ID	–	–	TLC271IP
– 55°C to 125°C	10 mV	TLC271MD	TLC271MFK	TLC271MJG	TLC271MP

The D package is available in tape and reel. Add R suffix to the device type (e.g., TLC271BCDR).

DEVICE FEATURES
TYPICAL AT V_{DD} = 5 V, T_A = 25°C

	BIAS-SELECT MODE			UNIT
	HIGH	MEDIUM	LOW	
P_D	3375	525	50	μW
S_R	3.6	0.4	0.03	V/μs
V_n	25	32	68	nV/√Hz
B_1	1.7	0.5	0.09	MHz
A_{VD}	23	170	480	V/mV

LinCMOS is a trademark of Texas Instruments Incorporated.

TEXAS INSTRUMENTS
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

description (continued)

Using the bias select option, these cost-effective devices can be "programmed" to span a wide range of applications which previously required BiFET, NFET or bipolar technology. Three offset voltage grades are available (C- suffix and I- suffix types), ranging from the low-cost TLC271 (10 mV) to the TLC271B (2 mV) low-offset version. The extremely high input impedance and low bias currents, in conjunction with good common-mode rejection and supply voltage rejection, make these devices a good choice for new state-of-the-art designs as well as for upgrading existing designs.

In general, many features associated with bipolar technology are available in LinCMOS™ operational amplifiers, without the power penalties of bipolar technology. General applications such as transducer interfacing, analog calculations, amplifier blocks, active filters, and signal buffering are all easily designed with the TLC271. The devices also exhibit low-voltage single-supply operation, making them ideally suited for remote and inaccessible battery-powered applications. The common-mode input voltage range includes the negative rail.

A wide range of packaging options is available, including small-outline and chip carrier versions for high-density system applications.

The device inputs and output are designed to withstand −100-mA surge currents without sustaining latchup.

The TLC271 incorporates internal ESD-protection circuits that will prevent functional failures at voltages up to 2000 V as tested under MIL-STD-883C, Method 3015.2; however, care should be exercised in handling these devices as exposure to ESD may result in the degradation of the device parametric performance.

The C-suffix devices are characterized for operation from 0°C to 70°C. The I-suffix devices are characterized for operation from − 40°C to 85°C. The M-suffix devices are characterized for operation over the full military temperature range of − 55°C to 125°C.

bias select feature

The TLC271 offers a bias select feature that allows the user to select any one of three bias levels, depending on the level of performance desired. The trade-offs between bias levels involve ac performance and power dissipation (see Table 1).

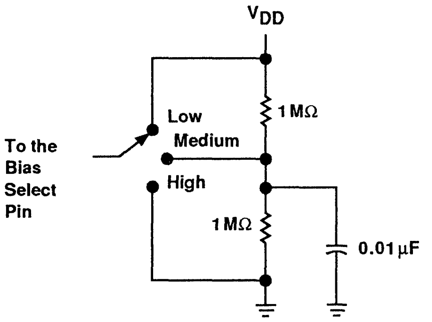
Table 1. Effect of Bias Selection on Performance

TYPICAL PARAMETER VALUES $T_A = 25°C, V_{DD} = 5$ V		MODE			UNIT
		HIGH-BIAS $R_L = 10$ kΩ	MEDIUM-BIAS $R_L = 100$ kΩ	LOW-BIAS $R_L = 1$ MΩ	
P_D	Power dissipation	3.4	0.5	0.05	mW
SR	Slew rate	3.6	0.4	0.03	V/µs
V_n	Equivalent input noise voltage at f = 1 kHz	25	32	68	nV/√Hz
B_1	Unity-gain bandwidth	1.7	0.5	0.09	MHz
ϕ_m	Phase margin	46°	40°	34°	
A_{VD}	Large-signal differential voltage amplification	23	170	480	V/mV

bias selection

Bias selection is achieved by connecting the bias select pin to one of three voltage levels (see Figure 1). For medium-bias applications, it is recommended that the bias select pin be connected to the midpoint between the supply rails. This procedure is simple in split-supply applications, since this point is ground. In single-supply applications, the medium-bias mode will necessitate using a voltage divider as indicated in Figure 1. The use of large-value resistors in the voltage divider will reduce the current drain of the divider from the supply line. However, large-value resistors used in conjunction with a large-value capacitor will require significant time to charge up to the supply midpoint after the supply is switched on. A voltage other than the midpoint may be used if it is within the voltages specified in the following table.

bias selection (continued)



BIAS MODE	BIAS SELECT VOLTAGE (Single Supply)
LOW	V_{DD}
MEDIUM	1 V to V_{DD} – 1 V
HIGH	GND

Figure 1. Bias Selection for Single-Supply Applications

high-bias mode

In the high-bias mode, the TLC271 series features low offset voltage drift, high input impedance, and low noise. Speed in this mode approaches that of BiFET devices, but at only a fraction of the power dissipation. Unity-gain bandwidth is typically greater than 1 MHz.

medium-bias mode

The TLC271 in the medium-bias mode features low offset voltage drift, high input impedance, and low noise. Speed in this mode is similar to general-purpose bipolar devices, but power dissipation is only a fraction of that consumed by bipolar devices.

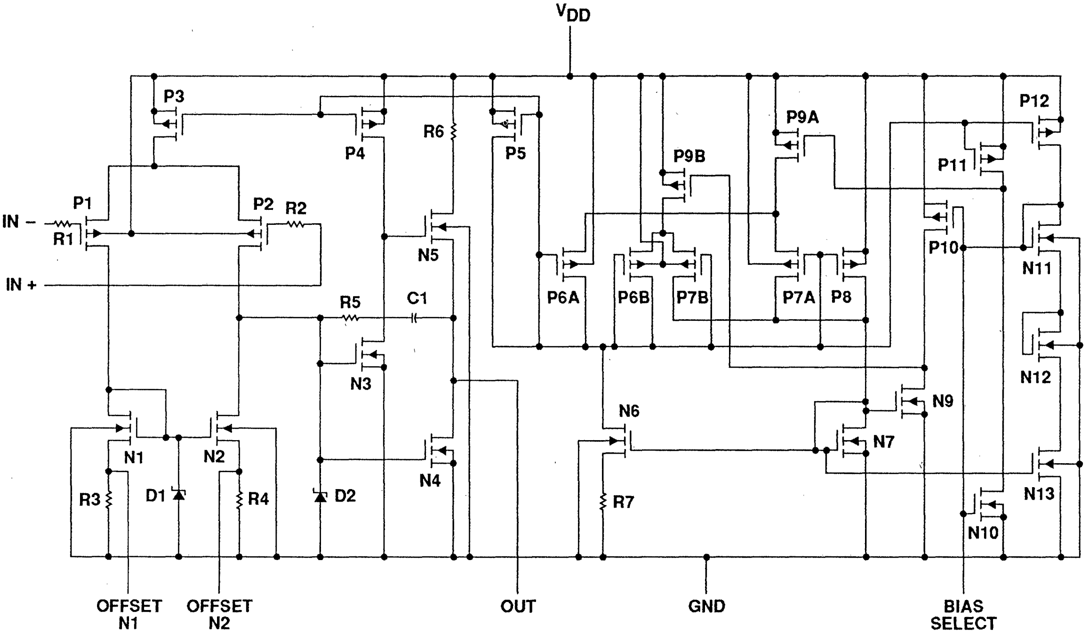
low-bias mode

In the low-bias mode, the TLC271 features low offset voltage drift, high input impedance, extremely low power consumption, and high differential voltage gain.

ORDER OF CONTENTS

TOPIC	BIAS-MODE
schematic	all
absolute maximum ratings	all
recommended operating conditions	all
electrical characteristics operating characteristics typical characteristics	high (Figures 2 – 33)
electrical characteristics operating characteristics typical characteristics	medium (Figures 34 – 65)
electrical characteristics operating characteristics typical characteristics	low (Figures 66 – 97)
parameter measurement information	all
application information	all

equivalent schematic



absolute maximum ratings over operating free-air temperature (unless otherwise noted)

Supply voltage, V_{DD} (see Note 1)	18 V
Differential input voltage (see Note 2)	± V_{DD}
Input voltage range, V_I (any input)	– 0.3 V to V_{DD}
Input current, I_I	± 5 mA
Output current, I_O	± 30 mA
Duration of short-circuit current at (or below) 25°C (see Note 3)	Unlimited
Continuous total dissipation	See Dissipation Rating Table
Operating free-air temperature, T_A: C-suffix	0°C to 70°C
I-suffix	– 40°C to 85°C
M-suffix	– 55°C to 125°C
Storage temperature range	– 65°C to 150°C
Case temperature for 60 seconds: FK package	260°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D and P package	260°C
Lead temperature 1,6mm (1/16 inch) from case for 60 seconds: JG package	300°C

NOTES:
1. All voltage values, except differential voltages, are with respect to network ground.
2. Differential voltages are at the noninverting input with respect to the inverting input.
3. The output may be shorted to either supply. Temperature and/or supply voltages must be limited to ensure that the maximum dissipation rating is not exceeded (see application section).

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING	$T_A = 125°C$ POWER RATING
D	725 mW	5.8 mW/°C	464 mW	377 mW	145 mW
FK	1375 mW	11 mW/°C	880 mW	715 mW	275 mW
JG	1050 mW	8.4 mW/°C	672 mW	546 mW	210 mW
P	1000 mW	8.0 mW/°C	640 mW	520 mW	200 mW

recommended operating conditions

		C-SUFFIX			I-SUFFIX			M-SUFFIX			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{DD}		3		16	4		16	5		16	V
Common-mode input voltage, V_{IC}	$V_{DD} = 5$ V	−0.2		3.5	−0.2		3.5	0		3.5	V
	$V_{DD} = 10$ V	−0.2		8.5	−0.2		8.5	0		8.5	
Operating free-air temperature, T_A		0		70	−40		85	−55		125	°C

HIGH-BIAS MODE

electrical characteristics over recommended free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS	T_A†	V_{DD} = 5 V			V_{DD} = 10 V			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	TLC271C	V_O = 1.4 V, V_{IC} = 0 V, R_S = 50 Ω, R_L = 10 kΩ	25°C		1.1	10		1.1	10	mV
				Full range			12			12	
		TLC271AC		25°C		0.9	5		0.9	5	
				Full range			6.5			6.5	
		TLC271BC		25°C		0.34	2		0.39	2	
				Full range			3			3	
α_{VIO}	Average temperature coefficient of input offset voltage			25°C to 70°C		1.8			2		μV/°C
I_{IO}	Input offset current (see Note 4)		V_O = V_{DD} / 2, V_{IC} = V_{DD} / 2	25°C		0.1			0.1		pA
				70°C		7	300		7	300	
I_{IB}	Input bias current (see Note 4)		V_O = V_{DD} / 2, V_{IC} = V_{DD} / 2	25°C		0.6			0.7		pA
				70°C		40	600		50	600	
V_{ICR}	Common-mode input voltage range (see Note 5)			25°C	−0.2 to 4	−0.3 to 4.2		−0.2 to 9	−0.3 to 9.2		V
				Full range	−0.2 to 3.5			−0.2 to 8.5			V
V_{OH}	High-level output voltage		V_{ID} = 100 mV, R_L = 10 kΩ	25°C	3.2	3.8		8	8.5		V
				0°C	3	3.8		7.8	8.5		
				70°C	3	3.8		7.8	8.4		
V_{OL}	Low-level output voltage		V_{ID} = − 100 mV, I_{OL} = 0	25°C		0	50		0	50	mV
				0°C		0	50		0	50	
				70°C		0	50		0	50	
A_{VD}	Large-signal differential voltage amplification		R_L = 10 kΩ, See Note 6	25°C	5	23		10	36		V/mV
				0°C	4	27		7.5	42		
				70°C	4	20		7.5	32		
CMRR	Common-mode rejection ratio		V_{IC} = V_{ICR}min	25°C	65	80		65	85		dB
				0°C	60	84		60	88		
				70°C	60	85		60	88		
k_{SVR}	Supply-voltage rejection ratio (ΔV_{DD} / ΔV_{IO})		V_{DD} = 5 V to 10 V, V_O = 1.4 V	25°C	65	95		65	95		dB
				0°C	60	94		60	94		
				70°C	60	96		60	96		
$I_{I(SEL)}$	Input current to bias select pin		$V_{I(SEL)}$ = 0	25°C		− 1.4			− 1.9		μA
I_{DD}	Supply current		V_O = V_{DD}/2, VIC = V_{DD}/2, No load	25°C		675	1600		950	2000	μA
				0°C		775	1800		1125	2200	
				70°C		575	1300		750	1700	

†Full range is 0°C to 70°C.

NOTES: 4. The typical values of input bias current and input offset current below 5 pA were determined mathematically.

5. This range also applies to each input individually.

6. At V_{DD} = 5 V, V_O = 0.25 V to 2 V; at V_{DD} = 10 V, V_O = 1 V to 6 V.

HIGH-BIAS MODE

electrical characteristics over recommended free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS	T_A†	V_{DD} = 5 V			V_{DD} = 10 V			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	TLC271I	V_O = 1.4 V, V_{IC} = 0 V, R_S = 50 Ω, R_L = 10 kΩ	25°C		1.1	10		1.1	10	mV
				Full range			13			13	
		TLC271AI		25°C		0.9	5		0.9	5	
				Full range			7			7	
		TLC271BI		25°C		0.34	2		0.39	2	
				Full range			3.5			3.5	
α_{VIO}	Average temperature coefficient of input offset voltage			25°C to 85°C		1.8			2		µV/°C
I_{IO}	Input offset current (see Note 4)		$V_O = V_{DD}/2$, $V_{IC} = V_{DD}/2$	25°C		0.1			0.1		pA
				85°C		24	1000		26	1000	
I_{IB}	Input bias current (see Note 4)		$V_O = V_{DD}/2$, $V_{IC} = V_{DD}/2$	25°C		0.6			0.7		pA
				85°C		200	2000		220	2000	
V_{ICR}	Common-mode input voltage range (see Note 5)			25°C	−0.2 to 4	−0.3 to 4.2		−0.2 to 9	−0.3 to 9.2		V
				Full range	−0.2 to 3.5			−0.2 to 8.5			V
V_{OH}	High-level output voltage		V_{ID} = 100 mV, R_L = 10 kΩ	25°C	3.2	3.8		8	8.5		V
				−40°C	3	3.8		7.8	8.5		
				85°C	3	3.8		7.8	8.5		
V_{OL}	Low-level output voltage		V_{ID} = −100 mV, I_{OL} = 0	25°C		0	50		0	50	mV
				−40°C		0	50		0	50	
				85°C		0	50		0	50	
A_{VD}	Large-signal differential voltage amplification		R_L = 10 kΩ, See Note 6	25°C	5	23		10	36		V/mV
				−40°C	3.5	32		7	46		
				85°C	3.5	19		7	31		
CMRR	Common-mode rejection ratio		$V_{IC} = V_{ICR}$min	25°C	65	80		65	85		dB
				−40°C	60	81		60	87		
				85°C	60	86		60	88		
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)		V_{DD} = 5 V to 10 V, V_O = 1.4 V	25°C	65	95		65	95		dB
				−40°C	60	92		60	92		
				85°C	60	96		60	96		
$I_{I(SEL)}$	Input current to bias select pin		$V_{I(SEL)}$ = 0	25°C		−1.4			−1.9		µA
I_{DD}	Supply current		$V_O = V_{DD}/2$, $V_{IC} = V_{DD}/2$, No load	25°C		675	1600		950	2000	µA
				−40°C		950	2200		1375	2500	
				85°C		525	1200		725	1600	

†Full range is −40°C to 85°C.

NOTES: 4. The typical values of input bias current and input offset current below 5 pA were determined mathematically.
5. This range also applies to each input individually.
6. At V_{DD} = 5 V, V_O = 0.25 V to 2 V; at V_{DD} = 10 V, V_O = 1 V to 6 V.

HIGH-BIAS MODE

electrical characteristics over recommended free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A†	V_{DD} = 5 V			V_{DD} = 10 V			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_O = 1.4 V, V_{IC} = 0 V, R_S = 50 Ω, R_L = 10 kΩ	25°C		1.1	10		1.1	10	mV
			Full range			12			12	
α_{VIO}	Average temperature coefficient of input offset voltage		25°C to 125°C		2.1			2.2		µV/°C
I_{IO}	Input offset current (see Note 4)	$V_O = V_{DD} / 2$, $V_{IC} = V_{DD} / 2$	25°C		0.1			0.1		pA
			125°C		1.4	15		1.8	15	nA
I_{IB}	Input bias current (see Note 4)	$V_O = V_{DD} / 2$, $V_{IC} = V_{DD} / 2$	25°C		0.6			0.7		pA
			125°C		9	35		10	35	nA
V_{ICR}	Common-mode input voltage range (see Note 5)		25°C	0 to 4	−0.3 to 4.2		0 to 9	−0.3 to 9.2		V
			Full range	0 to 3.5			0 to 8.5			V
V_{OH}	High-level output voltage	V_{ID} = 100 mV, R_L = 10 kΩ	25°C	3.2	3.8		8	8.5		V
			−55°C	3	3.8		7.8	8.5		
			125°C	3	3.8		7.8	8.4		
V_{OL}	Low-level output voltage	V_{ID} = −100 mV, I_{OL} = 0	25°C		0	50		0	50	mV
			−55°C		0	50		0	50	
			125°C		0	50		0	50	
A_{VD}	Large-signal differential voltage amplification	R_L = 10 kΩ, See Note 6	25°C	5	23		10	36		V/mV
			−55°C	3.5	35		7	50		
			125°C	3.5	16		7	27		
CMRR	Common-mode rejection ratio	$V_{IC} = V_{ICR}\text{min}$	25°C	65	80		65	85		dB
			−55°C	60	81		60	87		
			125°C	60	84		60	86		
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD} / \Delta V_{IO}$)	V_{DD} = 5 V to 10 V, V_O = 1.4 V	25°C	65	95		65	95		dB
			−55°C	60	90		60	90		
			125°C	60	97		60	97		
$I_{I(SEL)}$	Input current to bias select pin	$V_{I(SEL)}$ = 0	25°C		−1.4			−1.9		µA
I_{DD}	Supply current	$V_O = V_{DD} / 2$, $V_{IC} = V_{DD} / 2$, No load	25°C		675	1600		950	2000	µA
			−55°C		1000	2500		1475	3000	
			125°C		475	1100		625	1400	

†Full range is − 55°C to 125°C.

NOTES: 4. The typical values of input bias current and input offset current below 5 pA were determined mathematically.
5. This range also applies to each input individually.
6. At V_{DD} = 5 V, V_O = 0.25 V to 2 V; at V_{DD} = 10 V, V_O = 1 V to 6 V.

HIGH-BIAS MODE

operating characteristics, V_{DD} = 5 V

PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain	R_L = 10 kΩ, C_L = 20 pF, See Figure 98	V_{IPP} = 1 V	25°C		3.6		V/μs
				0°C		4		
				70°C		3		
			V_{IPP} = 2.5 V	25°C		2.9		
				0°C		3.1		
				70°C		2.5		
V_n	Equivalent input noise voltage	f = 1 kHz, R_S = 100 Ω, See Figure 99		25°C		25		nV/√Hz
B_{OM}	Maximum output swing bandwidth	V_O = V_{OH}, C_L = 20 pF, R_L = 10 kΩ, See Figure 98		25°C		320		kHz
				0°C		340		
				70°C		260		
B_1	Unity-gain bandwidth	V_i = 10 mV, C_L = 20 pF, See Figure 100		25°C		1.7		MHz
				0°C		2		
				70°C		1.3		
ϕ_m	Phase margin	V_i = 10 mV, f = B_1, C_L = 20 pF, See Figure 100		25°C		46°		
				0°C		47°		
				70°C		44°		

operating characteristics, V_{DD} = 10 V

PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain	R_L = 10 kΩ, C_L = 20 pF, See Figure 98	V_{IPP} = 1 V	25°C		5.3		V/μs
				0°C		5.9		
				70°C		4.3		
			V_{IPP} = 5.5 V	25°C		4.6		
				0°C		5.1		
				70°C		3.8		
V_n	Equivalent input noise voltage	f = 1 kHz, R_S = 100 Ω, See Figure 99		25°C		25		nV/√Hz
B_{OM}	Maximum output swing bandwidth	V_O = V_{OH}, C_L = 20 pF, R_L = 10 kΩ, See Figure 98		25°C		200		kHz
				0°C		220		
				70°C		140		
B_1	Unity-gain bandwidth	V_i = 10 mV, C_L = 20 pF, See Figure 100		25°C		2.2		MHz
				0°C		2.5		
				70°C		1.8		
ϕ_m	Phase margin	f = B_1, V_i = 10 mV, C_L = 20 pF, See Figure 100		25°C		49°		
				0°C		50°		
				70°C		46°		

HIGH-BIAS MODE

operating characteristics, V_{DD} = 5 V

PARAMETER		TEST CONDITIONS		T_A	MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain	R_L = 10 kΩ, C_L = 20 pF, See Figure 98	V_{IPP} = 1 V	25°C		3.6		V/µs
				– 40°C		4.5		
				85°C		2.8		
			V_{IPP} = 2.5 V	25°C		2.9		
				– 40°C		3.5		
				85°C		2.3		
V_n	Equivalent input noise voltage	f = 1 kHz, R_S = 100 Ω, See Figure 99		25°C		25		nV/√Hz
B_{OM}	Maximum output swing bandwidth	V_O = V_{OH}, C_L = 20 pF, R_L = 10 kΩ, See Figure 98		25°C		320		kHz
				– 40°C		380		
				85°C		250		
B_1	Unity-gain bandwidth	V_i = 10 mV, C_L = 20 pF, See Figure 100		25°C		1.7		MHz
				– 40°C		2.6		
				85°C		1.2		
ϕ_m	Phase margin	V_i = 10 mV, f = B_1, C_L = 20 pF, See Figure 100		25°C		46°		
				– 40°C		49°		
				85°C		43°		

operating characteristics, V_{DD} = 10 V

PARAMETER		TEST CONDITIONS		T_A	MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain	R_L = 10 kΩ, C_L = 20 pF, See Figure 98	V_{IPP} = 1 V	25°C		5.3		V/µs
				– 40°C		6.8		
				85°C		4		
			V_{IPP} = 5.5 V	25°C		4.6		
				– 40°C		5.8		
				85°C		3.5		
V_n	Equivalent input noise voltage	f = 1 kHz, R_S = 100 Ω, See Figure 99		25°C		25		nV/√Hz
B_{OM}	Maximum output swing bandwidth	V_O = V_{OH}, C_L = 20 pF, R_L = 10 kΩ, See Figure 98		25°C		200		kHz
				– 40°C		260		
				85°C		130		
B_1	Unity-gain bandwidth	V_i = 10 mV, C_L = 20 pF, See Figure 100		25°C		2.2		MHz
				– 40°C		3.1		
				85°C		1.7		
ϕ_m	Phase margin	V_i = 10 mV, f = B_1, C_L = 20 pF, See Figure 100		25°C		49°		
				– 40°C		52°		
				85°C		46°		

HIGH-BIAS MODE

operating characteristics, V_{DD} = 5 V

PARAMETER		TEST CONDITIONS		T_A	MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain	R_L = 10 kΩ, C_L = 20 pF, See Figure 98	V_{IPP} = 1 V	25°C		3.6		V/μs
				– 55°C		4.7		
				125°C		2.3		
			V_{IPP} = 2.5 V	25°C		2.9		
				– 55°C		3.7		
				125°C		2		
V_n	Equivalent input noise voltage	f = 1 kHz, R_S = 100 Ω, See Figure 99		25°C		25		nV/√Hz
B_{OM}	Maximum output swing bandwidth	V_O = V_{OH}, C_L = 20 pF, R_L = 10 kΩ, See Figure 98		25°C		320		kHz
				– 55°C		400		
				125°C		230		
B_1	Unity-gain bandwidth	V_i = 10 mV, C_L = 20 pF, See Figure 100		25°C		1.7		MHz
				– 55°C		2.9		
				125°C		1.1		
ϕ_m	Phase margin	V_i = 10 mV, f = B_1, C_L = 20 pF, See Figure 100		25°C		46°		
				– 55°C		49°		
				125°C		41°		

operating characteristics, V_{DD} = 10 V

PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain	R_L = 10 kΩ, C_L = 20 pF, See Figure 98	V_{IPP} = 1 V	25°C		5.3		V/μs
				– 55°C		7.1		
				125°C		3.1		
			V_{IPP} = 5.5 V	25°C		4.6		
				– 55°C		6.1		
				125°C		2.7		
V_n	Equivalent input noise voltage	f = 1 kHz, R_S = 100 Ω, See Figure 99		25°C		25		nV/√Hz
B_{OM}	Maximum output swing bandwidth	V_O = V_{OH}, C_L = 20 pF, R_L = 10 kΩ, See Figure 98		25°C		200		kHz
				– 55°C		280		
				125°C		110		
B_1	Unity-gain bandwidth	V_i = 10 mV, C_L = 20 pF, See Figure 100		25°C		2.2		MHz
				– 55°C		3.4		
				125°C		1.6		
ϕ_m	Phase margin	V_i = 10 mV, f = B_1, C_L = 20 pF, See Figure 100		25°C		49°		
				– 55°C		52°		
				125°C		44°		

TYPICAL CHARACTERISTICS (HIGH-BIAS MODE)†

DISTRIBUTION OF TLC271
INPUT OFFSET VOLTAGE

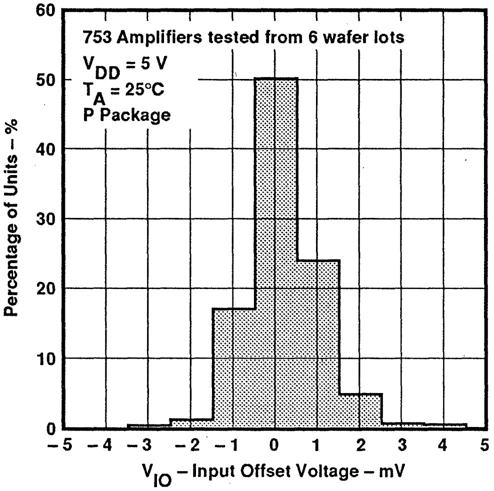


Figure 2

DISTRIBUTION OF TLC271
INPUT OFFSET VOLTAGE

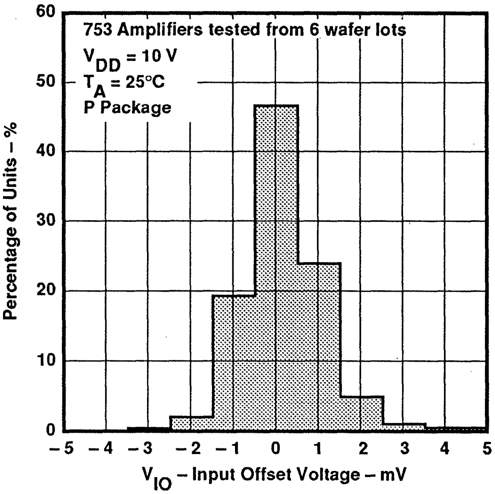


Figure 3

DISTRIBUTION OF TLC271
INPUT OFFSET VOLTAGE
TEMPERATURE COEFFICIENT

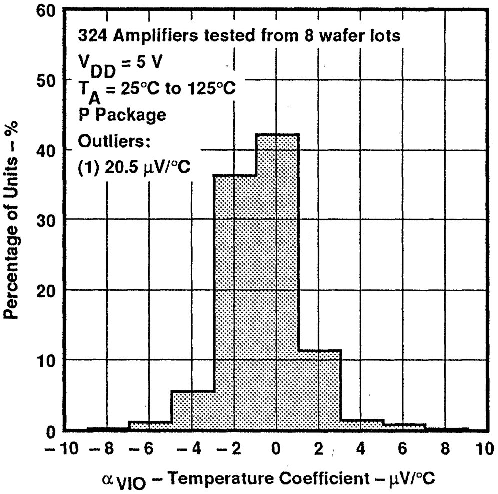


Figure 4

DISTRIBUTION OF TLC271
INPUT OFFSET VOLTAGE
TEMPERATURE COEFFICIENT

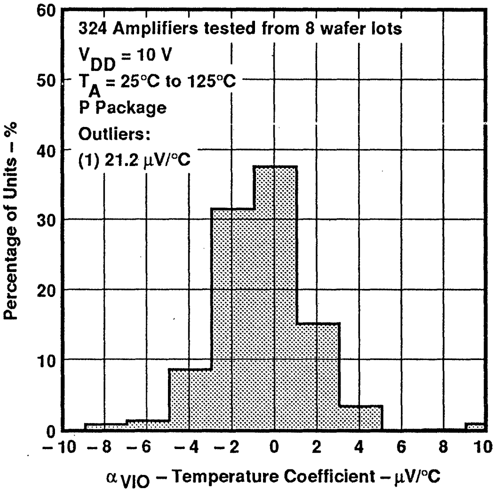
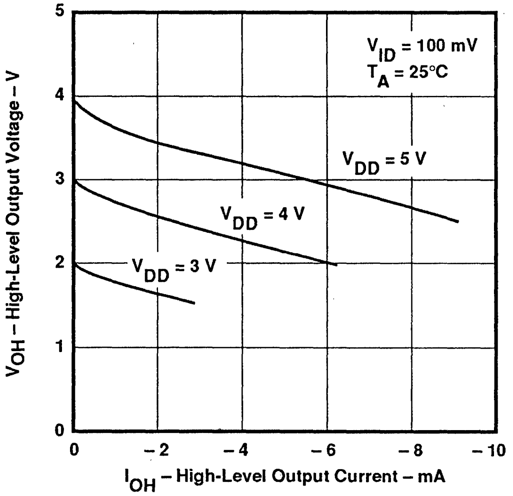


Figure 5

---

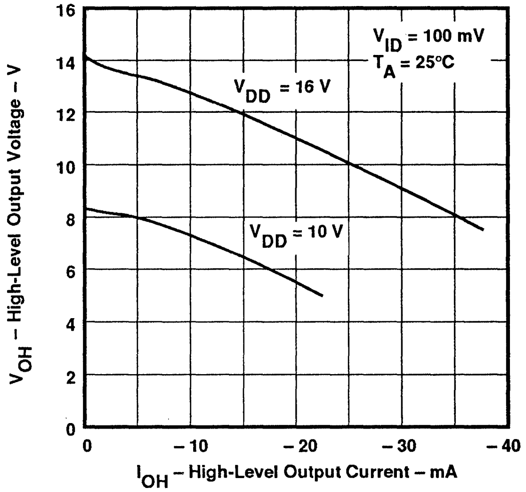
†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS (HIGH-BIAS MODE)†



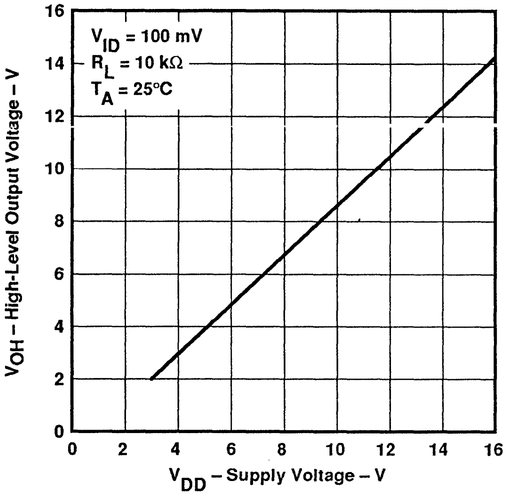
HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

Figure 6



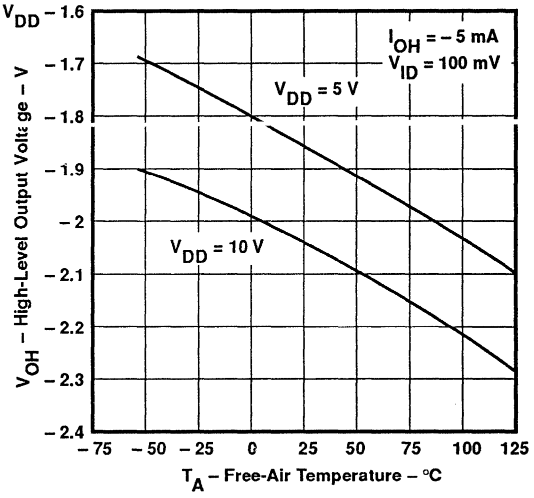
HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

Figure 7



HIGH-LEVEL OUTPUT VOLTAGE
vs
SUPPLY VOLTAGE

Figure 8



HIGH-LEVEL OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

Figure 9

---

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS (HIGH-BIAS MODE)†

LOW-LEVEL OUTPUT VOLTAGE
vs
COMMON-MODE INPUT VOLTAGE

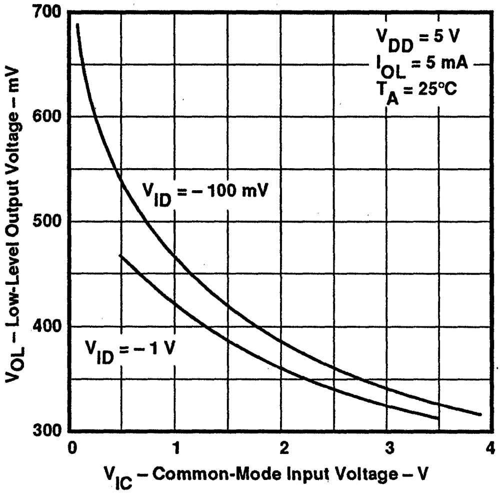


Figure 10

LOW-LEVEL OUTPUT VOLTAGE
vs
COMMON-MODE INPUT VOLTAGE

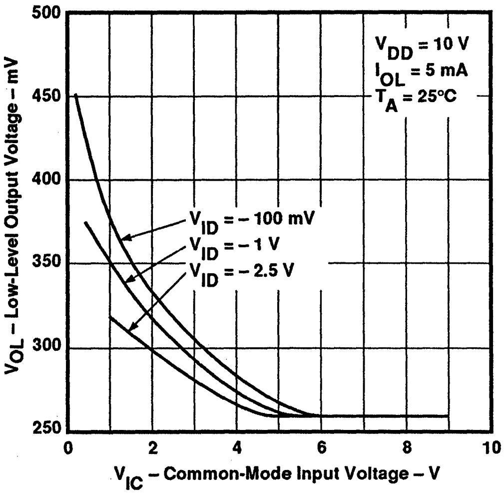


Figure 11

LOW-LEVEL OUTPUT VOLTAGE
vs
DIFFERENTIAL INPUT VOLTAGE

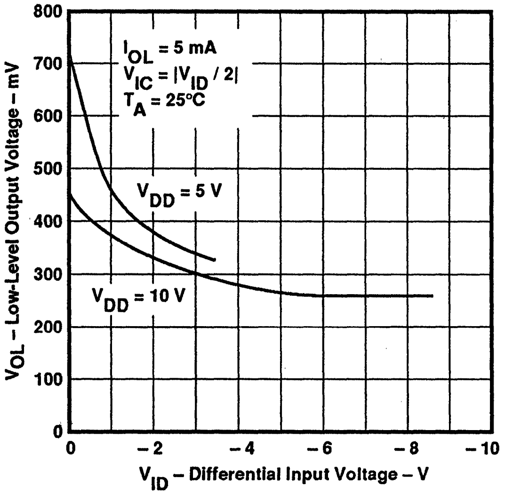


Figure 12

LOW-LEVEL OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

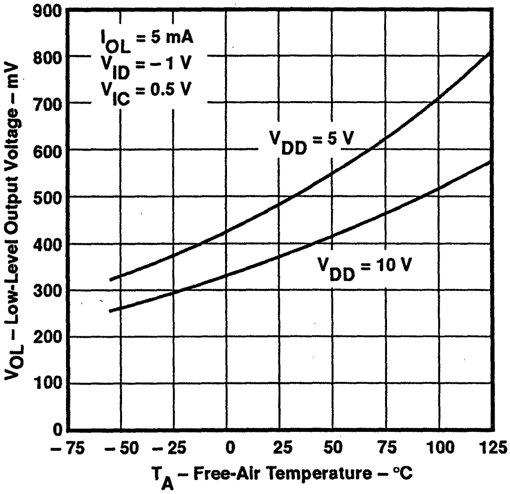


Figure 13

---

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS (HIGH-BIAS MODE)†

LOW-LEVEL OUTPUT VOLTAGE vs LOW-LEVEL OUTPUT CURRENT

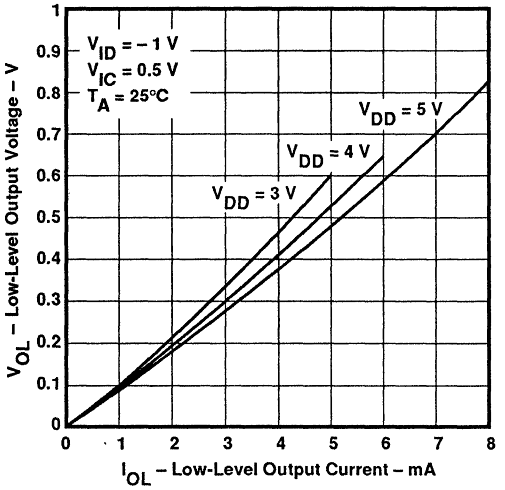


Figure 14

LOW-LEVEL OUTPUT VOLTAGE vs LOW-LEVEL OUTPUT CURRENT

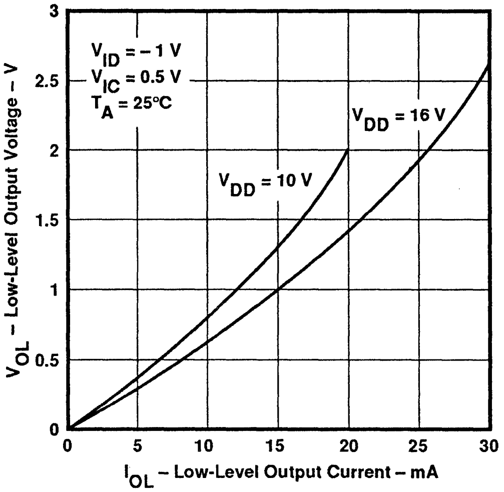


Figure 15

LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION vs SUPPLY VOLTAGE

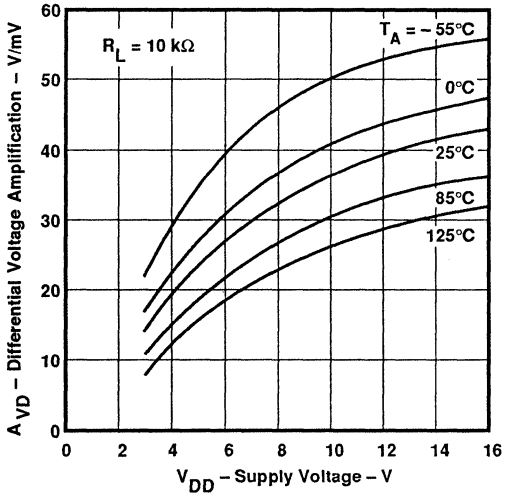


Figure 16

LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION vs FREE-AIR TEMPERATURE

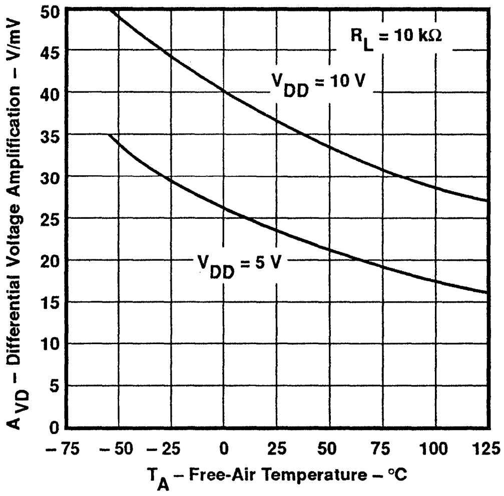


Figure 17

---

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS (HIGH-BIAS MODE)†

INPUT BIAS CURRENT AND INPUT OFFSET CURRENT vs FREE-AIR TEMPERATURE

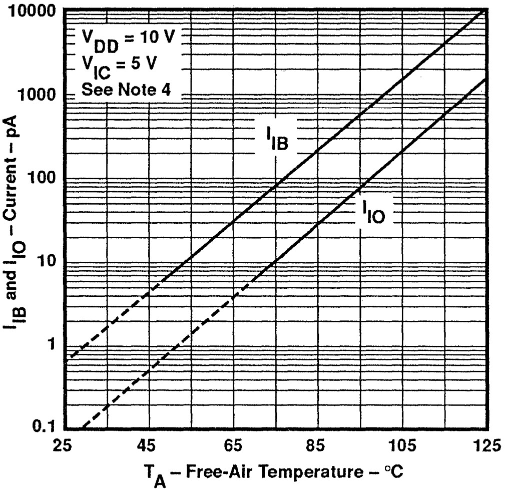


Figure 18

COMMON-MODE INPUT VOLTAGE POSITIVE LIMIT vs SUPPLY VOLTAGE

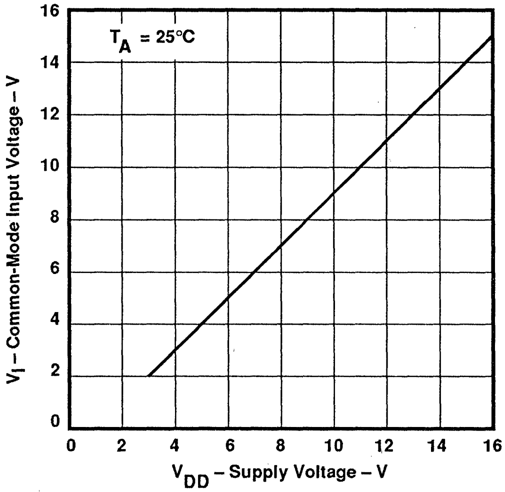


Figure 19

SUPPLY CURRENT vs SUPPLY VOLTAGE

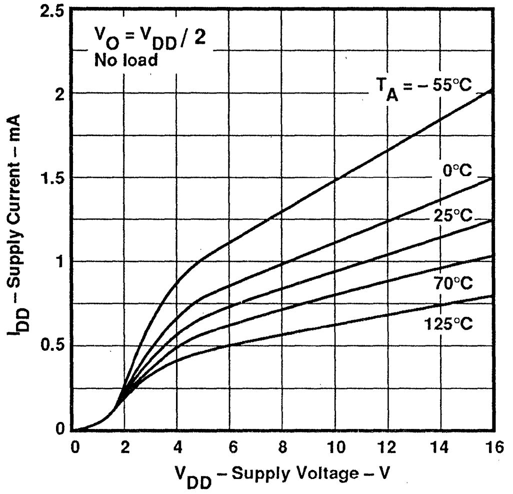


Figure 20

SUPPLY CURRENT vs FREE-AIR TEMPERATURE

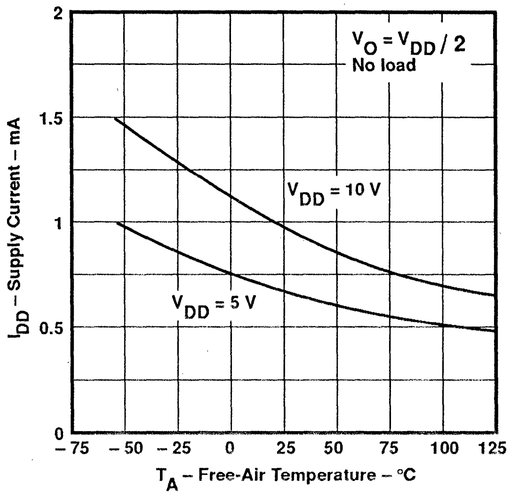


Figure 21

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.
NOTE 4: The typical values of input bias current and input offset current below 5 pA were determined mathematically.

TYPICAL CHARACTERISTICS (HIGH-BIAS MODE)†

SLEW RATE
vs
SUPPLY VOLTAGE

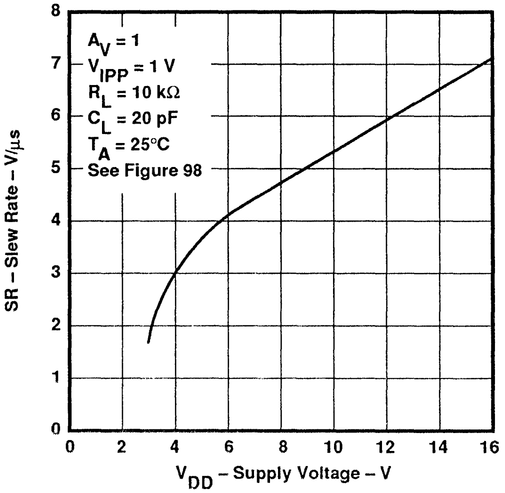


Figure 22

SLEW RATE
vs
FREE-AIR TEMPERATURE

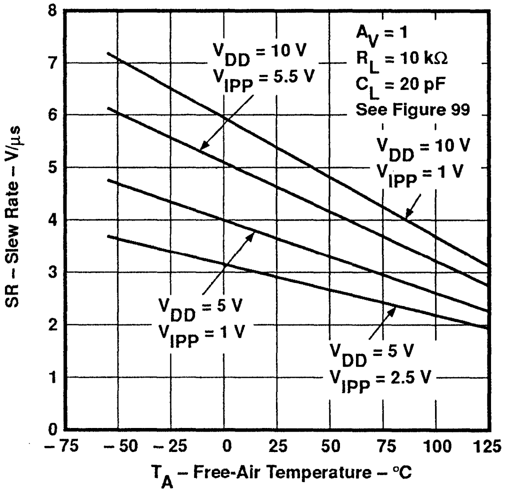


Figure 23

BIAS SELECT CURRENT
vs
SUPPLY VOLTAGE

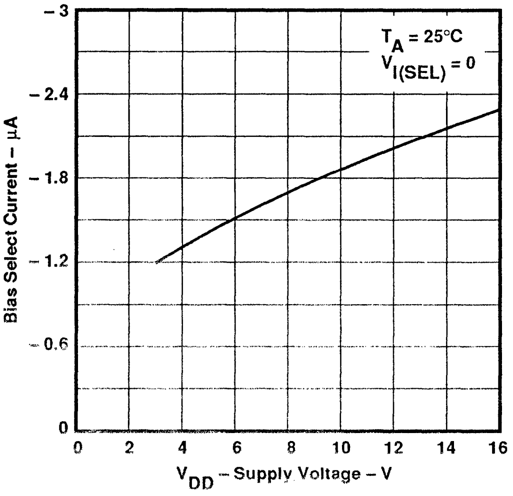


Figure 24

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE
vs
FREQUENCY

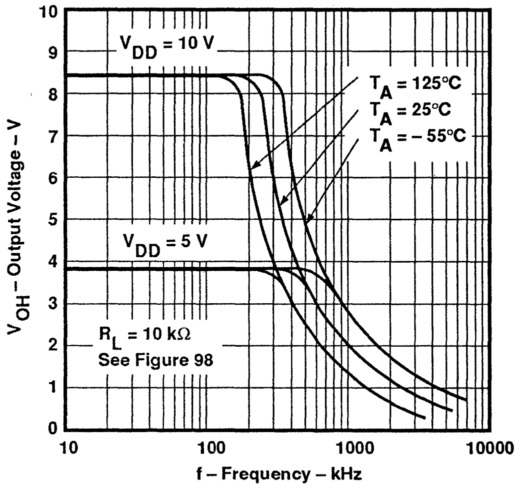


Figure 25

---

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS (HIGH-BIAS MODE)†

UNITY-GAIN BANDWIDTH
vs
FREE-AIR TEMPERATURE

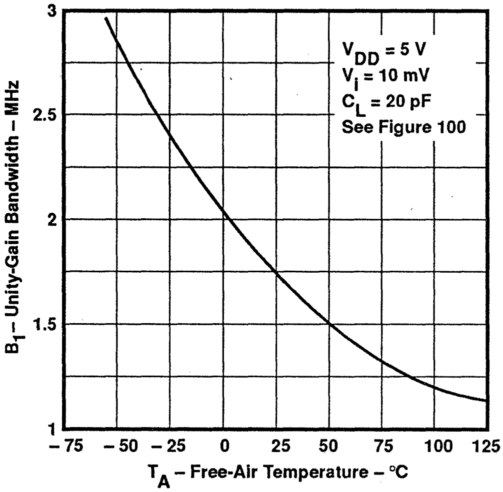


Figure 26

UNITY-GAIN BANDWIDTH
vs
SUPPLY VOLTAGE

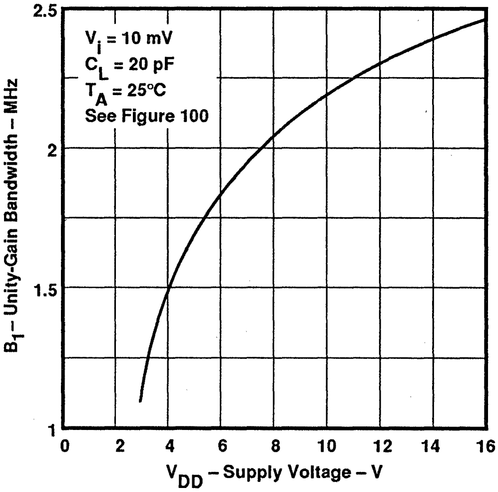


Figure 27

LARGE-SIGNAL DIFFERENTIAL VOLTAGE
AMPLIFICATION AND PHASE SHIFT
vs
FREQUENCY

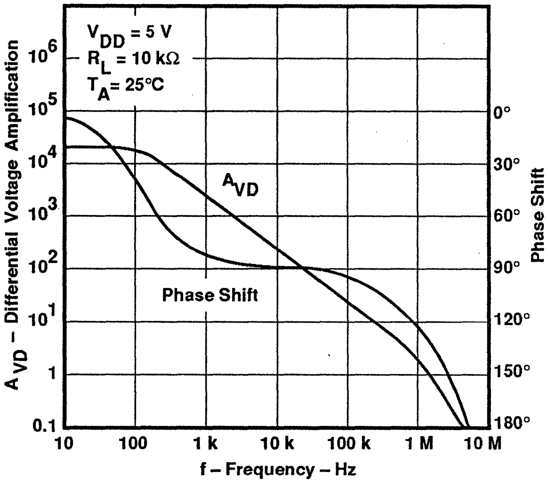


Figure 28

LARGE-SIGNAL DIFFERENTIAL VOLTAGE
AMPLIFICATION AND PHASE SHIFT
vs
FREQUENCY

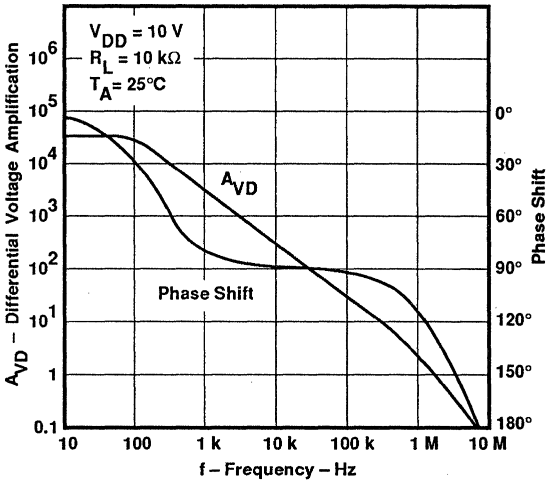


Figure 29

---

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS (HIGH-BIAS MODE)†

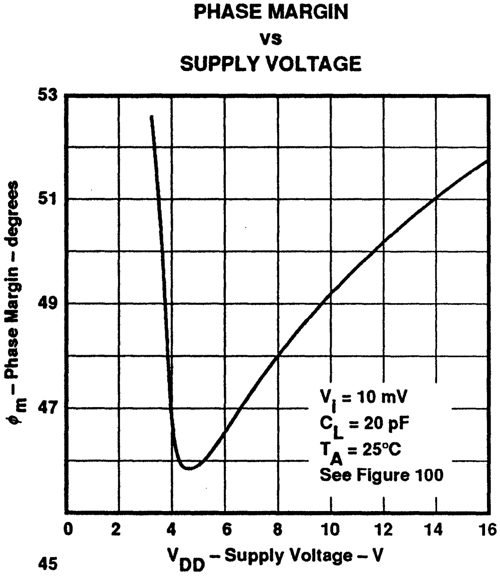


Figure 30

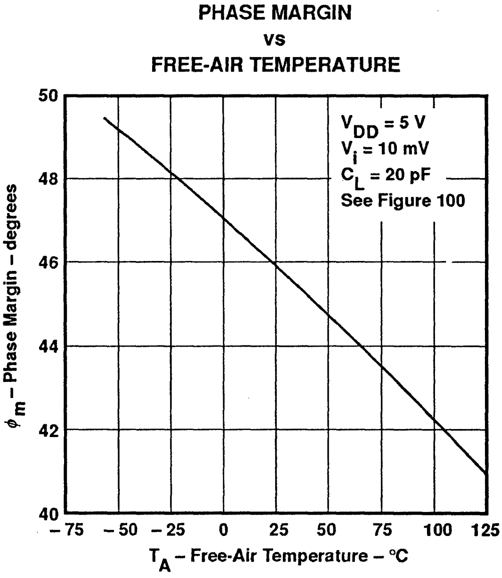


Figure 31

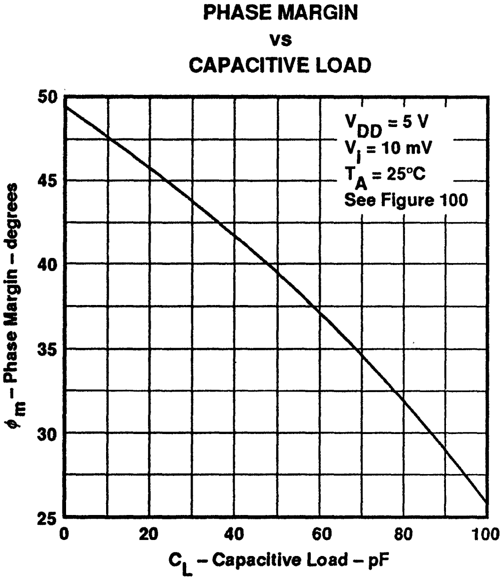


Figure 32

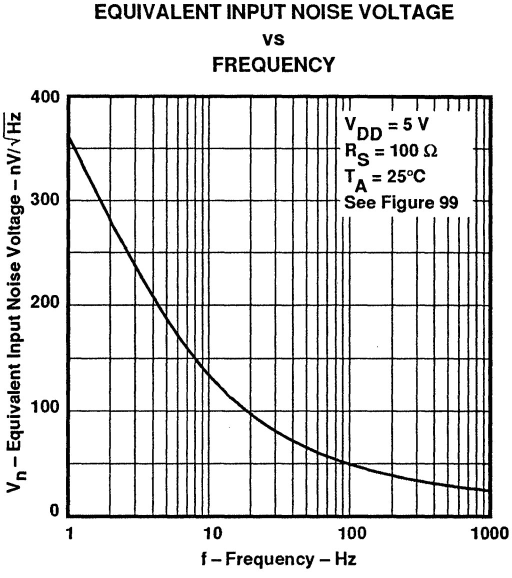


Figure 33

---

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

MEDIUM-BIAS MODE

electrical characteristics over recommended free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS	T_A†	V_{DD} = 5 V			V_{DD} = 10 V			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	TLC271C	V_O = 1.4 V, V_{IC} = 0 V, R_S = 50 Ω, R_L = 100 kΩ	25°C		1.1	10		1.1	10	mV
				Full range			12			12	
		TLC271AC		25°C		0.9	5		0.9	5	
				Full range			6.5			6.5	
		TLC271BC		25°C		0.25	2		0.26	2	
				Full range			3			3	
α_{VIO}	Average temperature coefficient of input offset voltage			25°C to 70°C		1.7			2.1		µV/°C
I_{IO}	Input offset current (see Note 4)		V_O = V_{DD} / 2, V_{IC} = V_{DD} / 2	25°C		0.1			0.1		pA
				70°C		7	300		7	300	
I_{IB}	Input bias current (see Note 4)		V_O = V_{DD} / 2, V_{IC} = V_{DD} / 2	25°C		0.6			0.7		pA
				70°C		40	600		50	600	
V_{ICR}	Common-mode input voltage range (see Note 5)			25°C	−0.2 to 4	−0.3 to 4.2		−0.2 to 9	−0.3 to 9.2		V
				Full range	−0.2 to 3.5			−0.2 to 8.5			V
V_{OH}	High-level output voltage		V_{ID} = 100 mV, R_L = 100 kΩ	25°C	3.2	3.9		8	8.7		V
				0°C	3	3.9		7.8	8.7		
				70°C	3	4		7.8	8.7		
V_{OL}	Low-level output voltage		V_{ID} = − 100 mV, I_{OL} = 0	25°C		0	50		0	50	mV
				0°C		0	50		0	50	
				70°C		0	50		0	50	
A_{VD}	Large-signal differential voltage amplification		R_L = 100 kΩ, See Note 6	25°C	25	170		25	275		V/mV
				0°C	15	200		15	320		
				70°C	15	140		15	230		
CMRR	Common-mode rejection ratio		V_{IC} = V_{ICR}min	25°C	65	91		65	94		dB
				0°C	60	91		60	94		
				70°C	60	92		60	94		
k_{SVR}	Supply-voltage rejection ratio (ΔV_{DD} / ΔV_{IO})		V_{DD} = 5 V to 10 V, V_O = 1.4 V	25°C	70	93		70	93		dB
				0°C	60	92		60	92		
				70°C	60	94		60	94		
$I_{I(SEL)}$	Input current to bias select pin		$V_{I(SEL)}$ = V_{DD} / 2	25°C		− 130			− 160		nA
I_{DD}	Supply current		V_O = V_{DD} / 2, V_{IC} = V_{DD} / 2 No load	25°C		105	280		143	300	µA
				0°C		125	320		173	400	
				70°C		85	220		110	280	

†Full range is 0°C to 70°C.

NOTES: 4. The typical values of input bias current and input offset current below 5 pA were determined mathematically.
5. This range also applies to each input individually.
6. At V_{DD} = 5 V, V_O = 0.25 V to 2 V; at V_{DD} = 10 V, V_O = 1 V to 6 V.

MEDIUM-BIAS MODE

electrical characteristics over recommended free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS	T_A†	V_{DD} = 5 V			V_{DD} = 10 V			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	TLC271I	V_O = 1.4 V, V_{IC} = 0 V, R_S = 50 Ω, R_L = 100 kΩ	25°C		1.1	10		1.1	10	mV
				Full range			13			13	
		TLC271AI		25°C		0.9	5		0.9	5	
				Full range			7			7	
		TLC271BI		25°C		0.25	2		0.26	2	
				Full range			3.5			3.5	
α_{VIO}	Average temperature coefficient of input offset voltage			25°C to 85°C		1.7			2.1		μV/°C
I_{IO}	Input offset current (see Note 4)		V_O = V_{DD} / 2, V_{IC} = V_{DD} / 2	25°C		0.1			0.1		pA
				85°C		24	1000		26	1000	
I_{IB}	Input bias current (see Note 4)		V_O = V_{DD} / 2, V_{IC} = V_{DD} / 2	25°C		0.6			0.7		pA
				85°C		200	2000		220	2000	
V_{ICR}	Common-mode input voltage range (see Note 5)			25°C	− 0.2 to 4	− 0.3 to 4.2		− 0.2 to 9	− 0.3 to 9.2		V
				Full range	− 0.2 to 3.5			− 0.2 to 8.5			V
V_{OH}	High-level output voltage		V_{ID} = 100 mV, R_L = 100 kΩ	25°C	3.2	3.9		8	8.7		V
				− 40°C	3	3.9		7.8	8.7		
				85°C	3	4		7.8	8.7		
V_{OL}	Low-level output voltage		V_{ID} = − 100 mV, I_{OL} = 0	25°C		0	50		0	50	mV
				− 40°C		0	50		0	50	
				85°C		0	50		0	50	
A_{VD}	Large-signal differential voltage amplification		R_L = 100 kΩ, See Note 6	25°C	25	170		25	275		V/mV
				− 40°C	15	270		15	390		
				85°C	15	130		15	220		
CMRR	Common-mode rejection ratio		V_{IC} = V_{ICR}min	25°C	65	91		65	94		dB
				− 40°C	60	90		60	93		
				85°C	60	90		60	94		
k_{SVR}	Supply-voltage rejection ratio (ΔV_{DD} / ΔV_{IO})		V_{DD} = 5 V to 10 V, V_O = 1.4 V	25°C	70	93		70	93		dB
				− 40°C	60	91		60	91		
				85°C	60	94		60	94		
$I_{I(SEL)}$	Input current to bias select pin		$V_{I(SEL)}$ = V_{DD} / 2	25°C		− 130			− 160		nA
I_{DD}	Supply current		V_O = V_{DD} / 2, V_{IC} = V_{DD} / 2, No load	25°C		105	280		143	300	μA
				− 40°C		158	400		225	450	
				85°C		80	200		103	260	

†Full range is – 40°C to 85°C.

NOTES: 4. The typical values of input bias current and input offset current below 5 pA were determined mathematically.

5. This range also applies to each input individually.

6. At V_{DD} = 5 V, V_O = 0.25 V to 2 V; at V_{DD} = 10 V, V_O = 1 V to 6 V.

MEDIUM-BIAS MODE

electrical characteristics over recommended free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A†	V_{DD} = 5 V			V_{DD} = 10 V			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_O = 1.4 V, V_{IC} = 0 V, R_S = 50 Ω, R_L = 100 kΩ	25°C		1.1	10		1.1	10	mV
			Full range			12			12	
α_{VIO}	Average temperature coefficient of input offset voltage		25°C to 125°C		1.7			2.1		µV/°C
I_{IO}	Input offset current (see Note 4)	V_O = V_{DD} / 2, V_{IC} = V_{DD} / 2	25°C		0.1			0.1		pA
			125°C		1.4	15		1.8	15	nA
I_{IB}	Input bias current (see Note 4)	V_O = V_{DD} / 2, V_{IC} = V_{DD} / 2	25°C		0.6			0.7		pA
			125°C		9	35		10	35	nA
V_{ICR}	Common-mode input voltage range (see Note 5)		25°C	0 to 4	−0.3 to 4.2		0 to 9	−0.3 to 9.2		V
			Full range	0 to 3.5			0 to 8.5			V
V_{OH}	High-level output voltage	V_{ID} = 100 mV, R_L = 100 kΩ	25°C	3.2	3.9		8	8.7		V
			−55°C	3	3.9		7.8	8.6		
			125°C	3	4		7.8	8.8		
V_{OL}	Low-level output voltage	V_{ID} = −100 mV, I_{OL} = 0	25°C		0	50		0	50	mV
			−55°C		0	50		0	50	
			125°C		0	50		0	50	
A_{VD}	Large-signal differential voltage amplification	R_L = 100 kΩ, See Note 6	25°C	25	170		25	275		V/mV
			−55°C	15	290		15	420		
			125°C	15	120		15	190		
CMRR	Common-mode rejection ratio	V_{IC} = V_{ICR}min	25°C	65	91		65	94		dB
			−55°C	60	89		60	93		
			125°C	60	91		60	93		
k_{SVR}	Supply-voltage rejection ratio (ΔV_{DD} / ΔV_{IO})	V_{DD} = 5 V to 10 V, V_O = 1.4 V	25°C	70	93		70	93		dB
			−55°C	60	91		60	91		
			125°C	60	94		60	94		
$I_{I(SEL)}$	Input current to bias select pin	$V_{I(SEL)}$ = V_{DD} / 2	25°C		−130			−160		nA
I_{DD}	Supply current	V_O = V_{DD} / 2, V_{IC} = V_{DD} / 2, No load	25°C		105	280		143	300	µA
			−55°C		170	440		245	500	
			125°C		70	180		90	240	

†Full range is – 55°C to 125°C.

NOTES: 4. The typical values of input bias current and input offset current below 5 pA were determined mathematically.
5. This range also applies to each input individually.
6. At V_{DD} = 5 V, V_O = 0.25 V to 2 V; at V_{DD} = 10 V, V_O = 1 V to 6 V.

MEDIUM-BIAS MODE

operating characteristics, V_{DD} = 5 V

PARAMETER		TEST CONDITIONS		T_A	MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain	R_L = 100 kΩ, C_L = 20 pF, See Figure 98	V_{IPP} = 1 V	25°C		0.43		V/µs
				0°C		0.46		
				70°C		0.36		
			V_{IPP} = 2.5 V	25°C		0.40		
				0°C		0.43		
				70°C		0.34		
V_n	Equivalent input noise voltage	f = 1 kHz, R_S = 100 Ω, See Figure 99		25°C		32		nV/√Hz
B_{OM}	Maximum output swing bandwidth	V_O = V_{OH}, C_L = 20 pF, R_L = 100 kΩ, See Figure 98		25°C		55		kHz
				0°C		60		
				70°C		50		
B_1	Unity-gain bandwidth	V_i = 10 mV, C_L = 20 pF, See Figure 100		25°C		525		kHz
				0°C		600		
				70°C		400		
ϕ_m	Phase margin	V_i = 10 mV, f = B_1, C_L = 20 pF, See Figure 100		25°C		40°		
				0°C		41°		
				70°C		39°		

operating characteristics, V_{DD} = 10 V

PARAMETER		TEST CONDITIONS		T_A	MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain	R_L = 100 kΩ, C_L = 20 pF, See Figure 98	V_{IPP} = 1 V	25°C		0.62		V/µs
				0°C		0.67		
				70°C		0.51		
			V_{IPP} = 5.5 V	25°C		0.56		
				0°C		0.61		
				70°C		0.46		
V_n	Equivalent input noise voltage	f = 1 kHz, R_S = 100 Ω, See Figure 99		25°C		32		nV/√Hz
B_{OM}	Maximum output swing bandwidth	V_O = V_{OH}, C_L = 20 pF, R_L = 100 kΩ, See Figure 98		25°C		35		kHz
				0°C		40		
				70°C		30		
B_1	Unity-gain bandwidth	V_i = 10 mV, C_L = 20 pF, See Figure 100		25°C		635		kHz
				0°C		710		
				70°C		510		
ϕ_m	Phase margin	V_i = 10 mV, f = B_1, C_L = 20 pF, See Figure 100		25°C		43°		
				0°C		44°		
				70°C		42°		

MEDIUM-BIAS MODE

operating characteristics, V_{DD} = 5 V

PARAMETER		TEST CONDITIONS		T_A†	MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain	R_L = 100 kΩ, C_L = 20 pF, See Figure 98	V_{IPP} = 1 V	25°C		0.43		V/µs
				– 40°C		0.51		
				85°C		0.35		
			V_{IPP} = 2.5 V	25°C		0.40		
				– 40°C		0.48		
				85°C		0.32		
V_n	Equivalent input noise voltage	f = 1 kHz, R_S = 100 Ω, See Figure 99		25°C		32		nV/√Hz
B_{OM}	Maximum output swing bandwidth	V_O = V_{OH}, C_L = 20 pF, R_L = 100 kΩ, See Figure 98		25°C		55		kHz
				– 40°C		75		
				85°C		45		
B_1	Unity-gain bandwidth	V_i = 10 mV, C_L = 20 pF, See Figure 100		25°C		525		kHz
				– 40°C		770		
				85°C		370		
ϕ_m	Phase margin	V_i = 10 mV, f = B_1, C_L = 20 pF, See Figure 100		25°C		40°		
				– 40°C		43°		
				85°C		38°		

operating characteristics, V_{DD} = 10 V

PARAMETER		TEST CONDITIONS		T_A†	MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain	R_L = 100 kΩ, C_L = 20 pF, See Figure 98	V_{IPP} = 1 V	25°C		0.62		V/µs
				– 40°C		0.77		
				85°C		0.47		
			V_{IPP} = 5.5 V	25°C		0.56		
				– 40°C		0.70		
				85°C		0.44		
V_n	Equivalent input noise voltage	f = 1 kHz, R_S = 100 Ω, See Figure 99		25°C		32		nV/√Hz
B_{OM}	Maximum output swing bandwidth	V_O = V_{OH}, C_L = 20 pF, R_L = 100 kΩ, See Figure 98		25°C		35		kHz
				– 40°C		45		
				85°C		25		
B_1	Unity-gain bandwidth	V_i = 10 mV, C_L = 20 pF, See Figure 100		25°C		635		kHz
				– 40°C		880		
				85°C		480		
ϕ_m	Phase margin	V_i = 10 mV, f = B_1, C_L = 20 pF, See Figure 100		25°C		43°		
				– 40°C		46°		
				85°C		41°		

MEDIUM-BIAS MODE

operating characteristics, V_{DD} = 5 V

PARAMETER		TEST CONDITIONS		T_A	MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain	R_L = 100 kΩ, C_L = 20 pF, See Figure 98	V_{IPP} = 1 V	25°C		0.43		V/μs
				– 55°C		0.54		
				125°C		0.29		
			V_{IPP} = 2.5 V	25°C		0.40		
				– 55°C		0.50		
				125°C		0.28		
V_n	Equivalent input noise voltage	f = 1 kHz, R_S = 100 Ω, See Figure 99		25°C		32		nV/√Hz
B_{OM}	Maximum output swing bandwidth	$V_O = V_{OH}$, C_L = 20 pF, R_L = 100 kΩ, See Figure 98		25°C		55		kHz
				– 55°C		80		
				125°C		40		
B_1	Unity-gain bandwidth	V_i = 10 mV, C_L = 20 pF, See Figure 100		25°C		525		kHz
				– 55°C		850		
				125°C		330		
ϕ_m	Phase margin	V_i = 10 mV, f = B_1, C_L = 20 pF, See Figure 100		25°C		40°		
				– 55°C		43°		
				125°C		36°		

operating characteristics, V_{DD} = 10 V

PARAMETER		TEST CONDITIONS		T_A	MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain	R_L = 100 kΩ, C_L = 20 pF, See Figure 98	V_{IPP} = 1 V	25°C		0.62		V/μs
				– 55°C		0.81		
				125°C		0.38		
			V_{IPP} = 5.5 V	25°C		0.56		
				– 55°C		0.73		
				125°C		0.35		
V_n	Equivalent input noise voltage	f = 1 kHz, R_S = 100 Ω, See Figure 99		25°C		32		nV/√Hz
B_{OM}	Maximum output swing bandwidth	$V_O = V_{OH}$, C_L = 20 pF, R_L = 100 kΩ, See Figure 98		25°C		35		kHz
				– 55°C		50		
				125°C		20		
B_1	Unity-gain bandwidth	V_i = 10 mV, C_L = 20 pF, See Figure 100		25°C		635		kHz
				– 55°C		960		
				125°C		440		
ϕ_m	Phase margin	V_i = 10 mV, f = B_1, C_L = 20 pF, See Figure 100		25°C		43°		
				– 55°C		47°		
				125°C		39°		

TYPICAL CHARACTERISTICS (MEDIUM-BIAS MODE)†

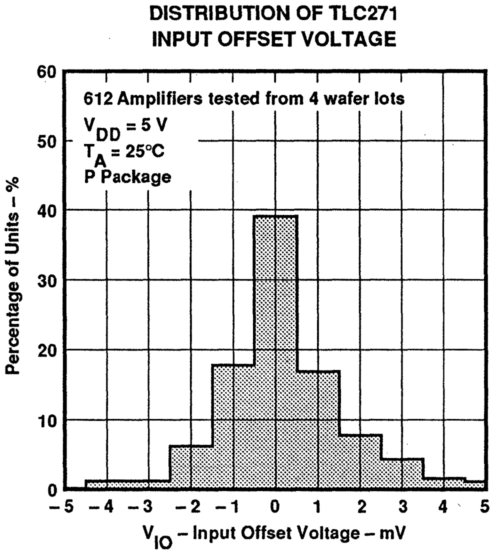

DISTRIBUTION OF TLC271
INPUT OFFSET VOLTAGE

Figure 34

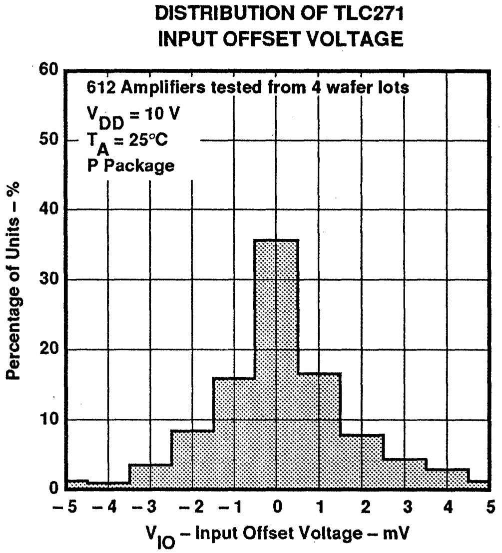

DISTRIBUTION OF TLC271
INPUT OFFSET VOLTAGE

Figure 35

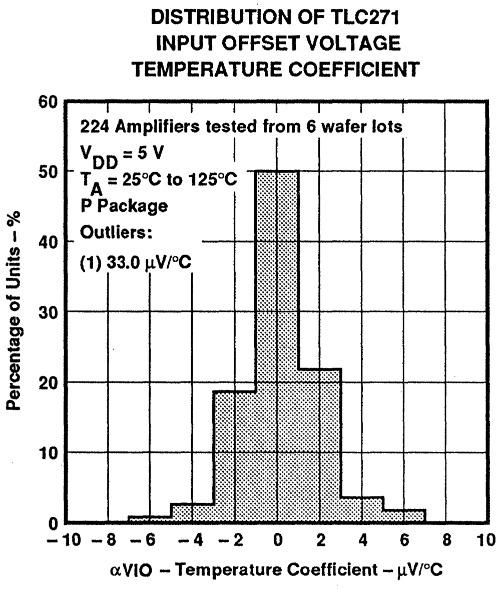

DISTRIBUTION OF TLC271
INPUT OFFSET VOLTAGE
TEMPERATURE COEFFICIENT

Figure 36

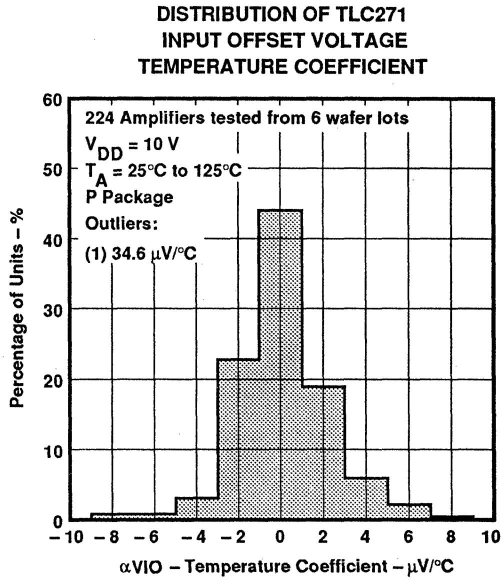

DISTRIBUTION OF TLC271
INPUT OFFSET VOLTAGE
TEMPERATURE COEFFICIENT

Figure 37

---

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS (MEDIUM-BIAS MODE)†

HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

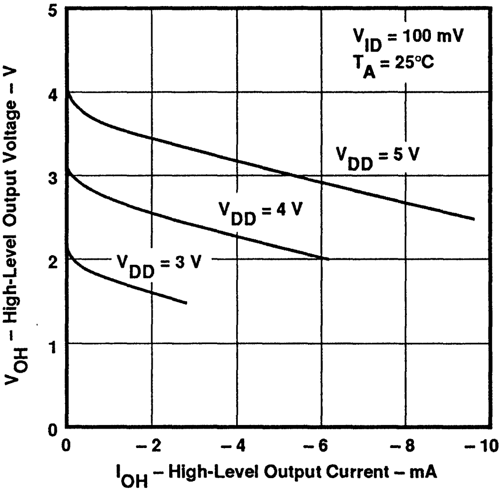


Figure 38

HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

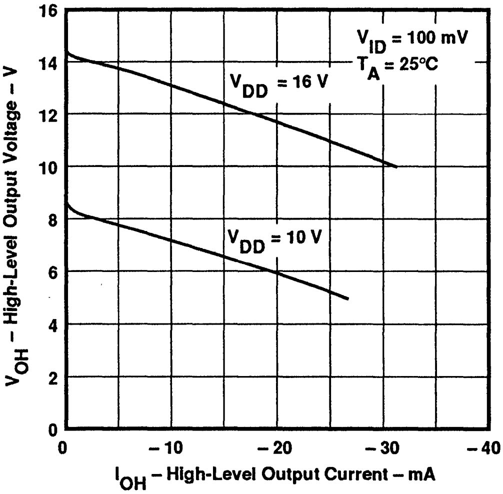


Figure 39

HIGH-LEVEL OUTPUT VOLTAGE
vs
SUPPLY VOLTAGE

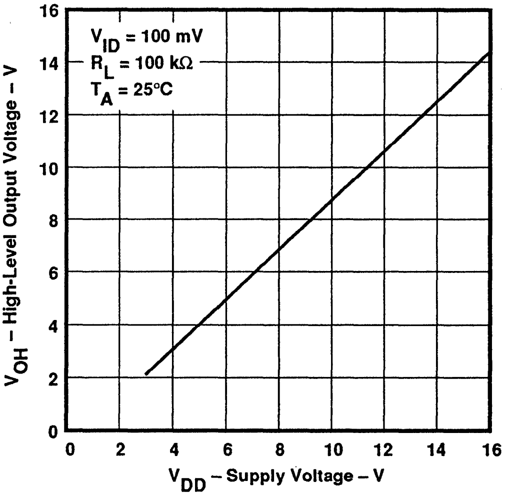


Figure 40

HIGH-LEVEL OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

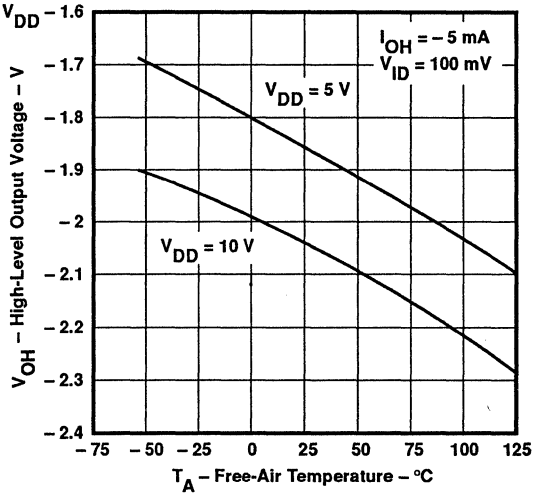


Figure 41

---

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS (MEDIUM-BIAS MODE)†

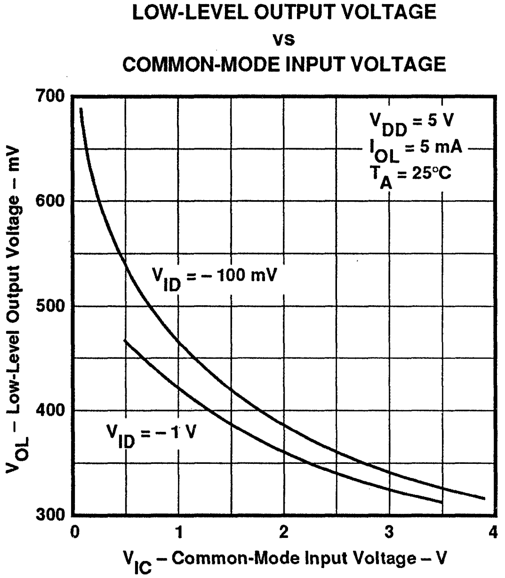

LOW-LEVEL OUTPUT VOLTAGE
vs
COMMON-MODE INPUT VOLTAGE

Figure 42

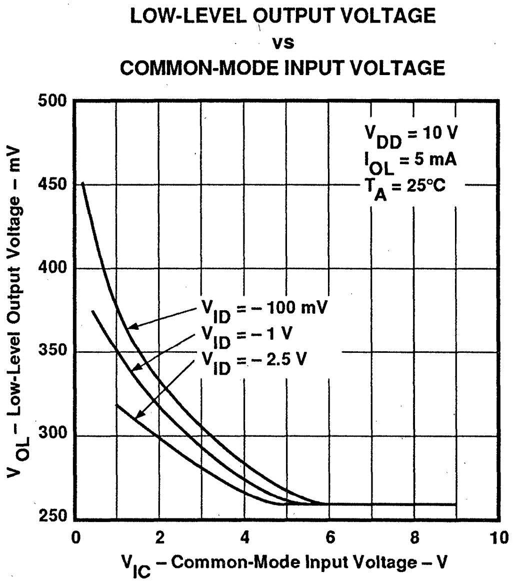

LOW-LEVEL OUTPUT VOLTAGE
vs
COMMON-MODE INPUT VOLTAGE

Figure 43

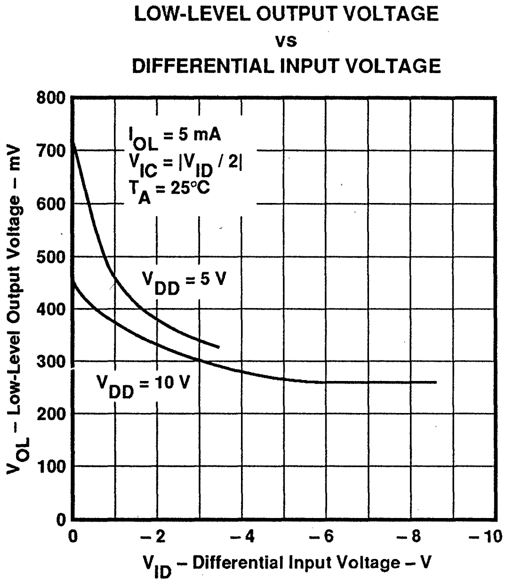

LOW-LEVEL OUTPUT VOLTAGE
vs
DIFFERENTIAL INPUT VOLTAGE

Figure 44

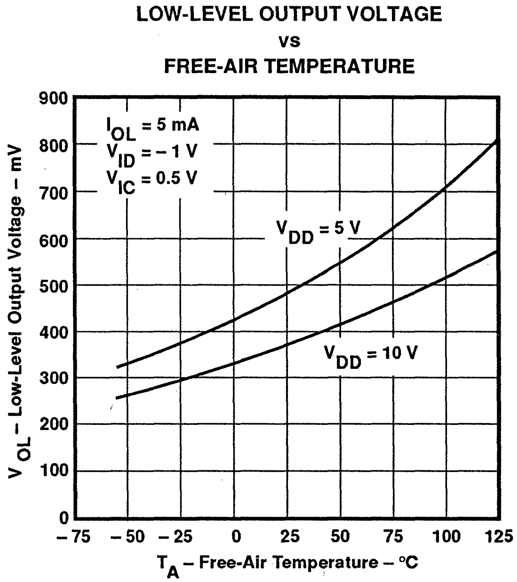

LOW-LEVEL OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

Figure 45

---

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS (MEDIUM-BIAS MODE)†

LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

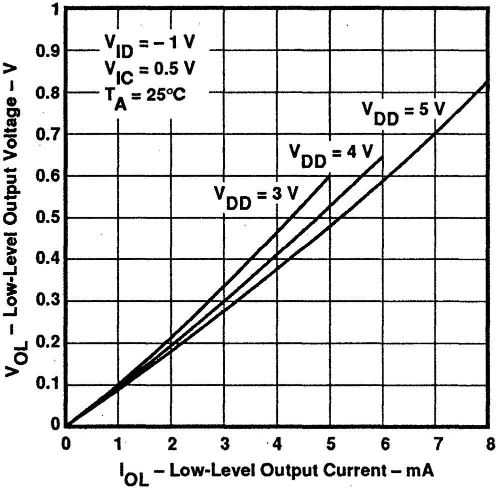


Figure 46

LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

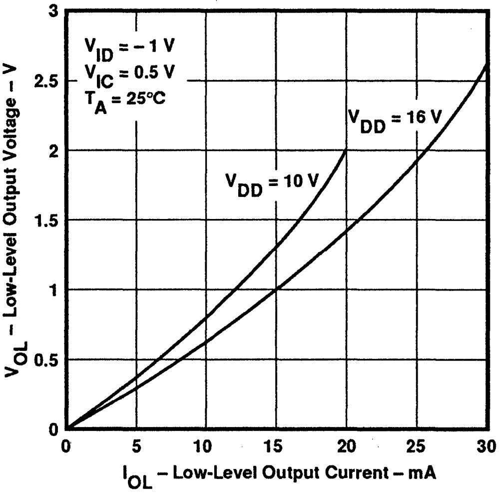


Figure 47

LARGE-SIGNAL
DIFFERENTIAL VOLTAGE AMPLIFICATION
vs
SUPPLY VOLTAGE

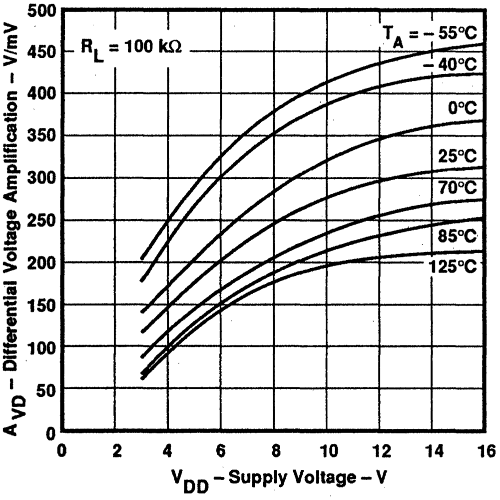


Figure 48

LARGE-SIGNAL
DIFFERENTIAL VOLTAGE AMPLIFICATION
vs
FREE-AIR TEMPERATURE

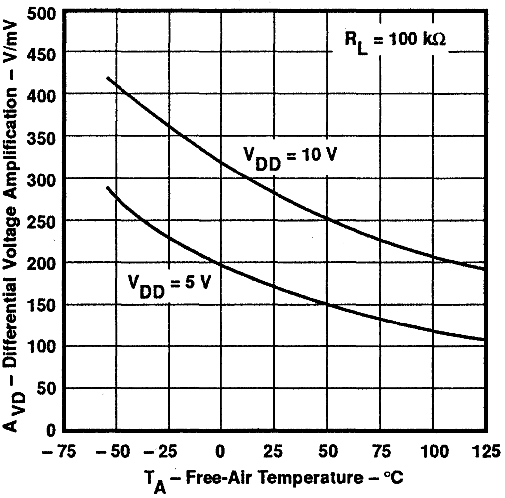


Figure 49

---

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS (MEDIUM-BIAS MODE)†

INPUT BIAS CURRENT AND INPUT OFFSET CURRENT vs FREE-AIR TEMPERATURE

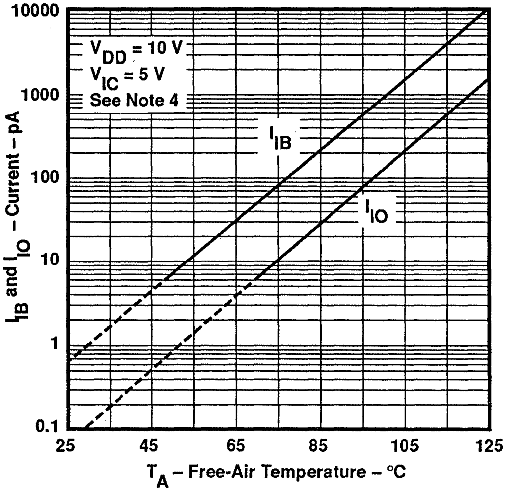


Figure 50

MAXIMUM INPUT VOLTAGE vs SUPPLY VOLTAGE

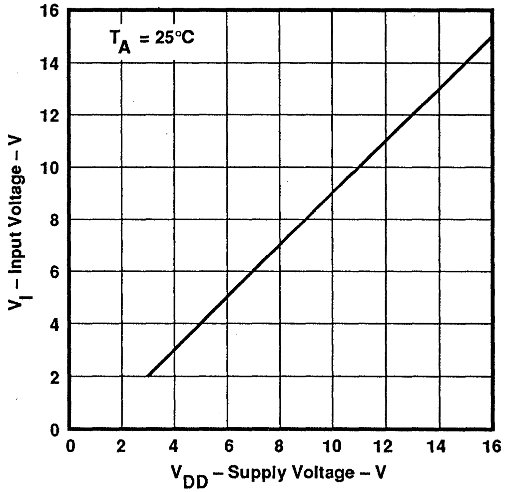


Figure 51

SUPPLY CURRENT vs SUPPLY VOLTAGE

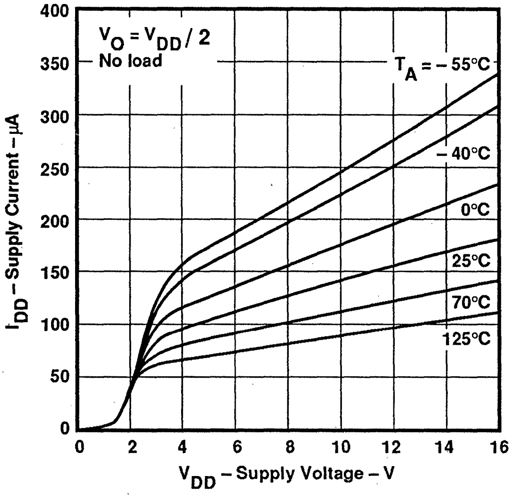


Figure 52

SUPPLY CURRENT vs FREE-AIR TEMPERATURE

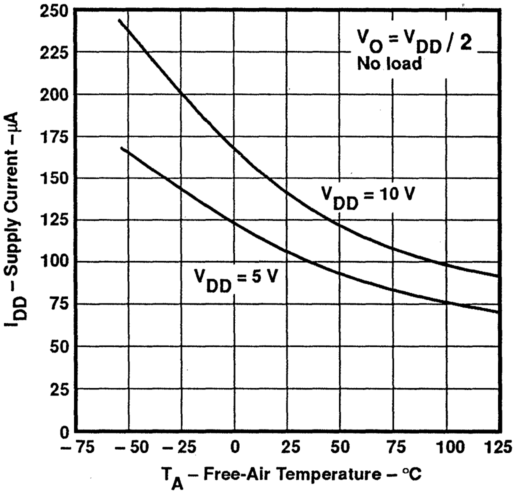


Figure 53

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

NOTE 4: The typical values of input bias current and input offset current below 5 pA were determined mathematically.

TYPICAL CHARACTERISTICS (MEDIUM-BIAS MODE)†

SLEW RATE
vs
SUPPLY VOLTAGE

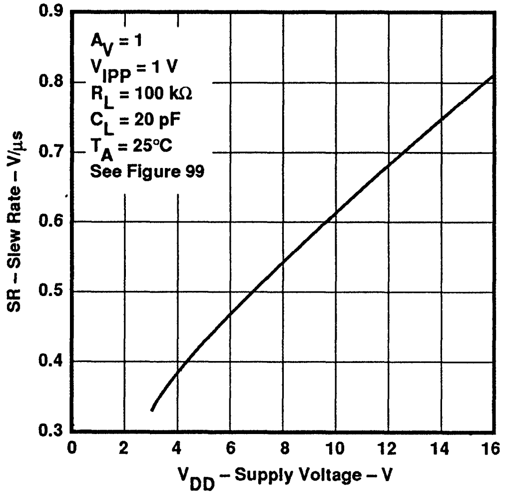


Figure 54

SLEW RATE
vs
FREE-AIR TEMPERATURE

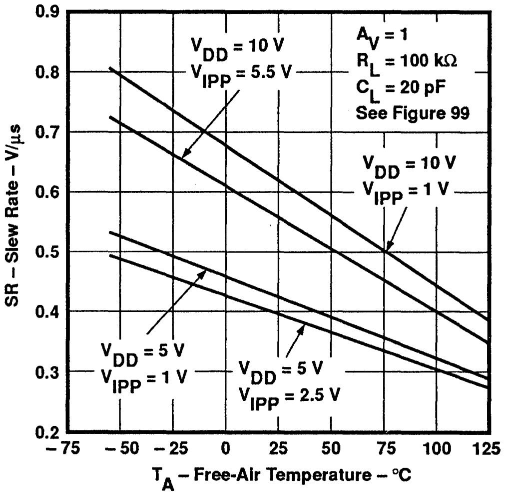


Figure 55

BIAS SELECT CURRENT
vs
SUPPLY VOLTAGE

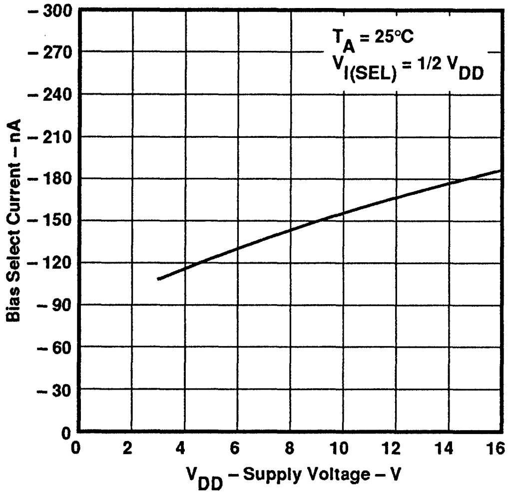


Figure 56

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE
vs
FREQUENCY

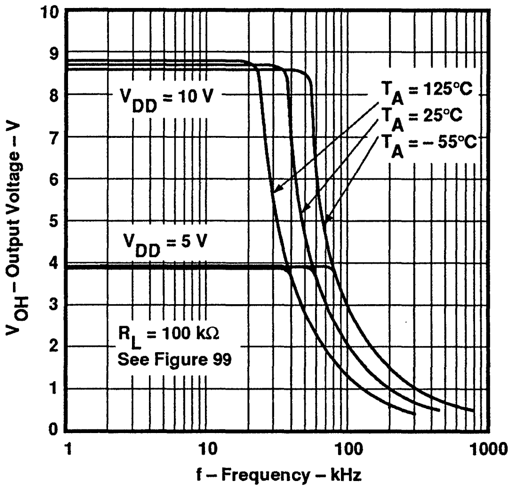


Figure 57

---

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS (MEDIUM-BIAS MODE)†

**UNITY-GAIN BANDWIDTH
vs
FREE-AIR TEMPERATURE**

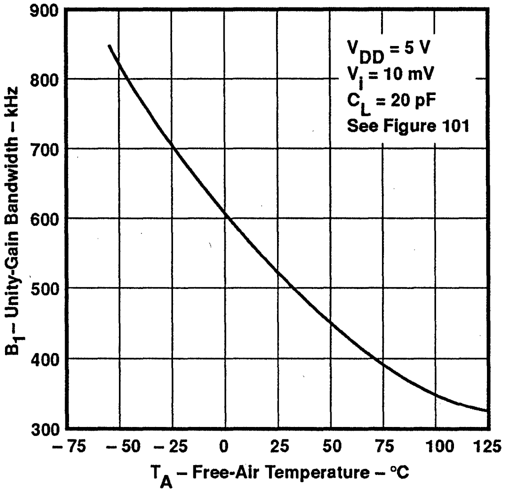


Figure 58

**UNITY-GAIN BANDWIDTH
vs
SUPPLY VOLTAGE**

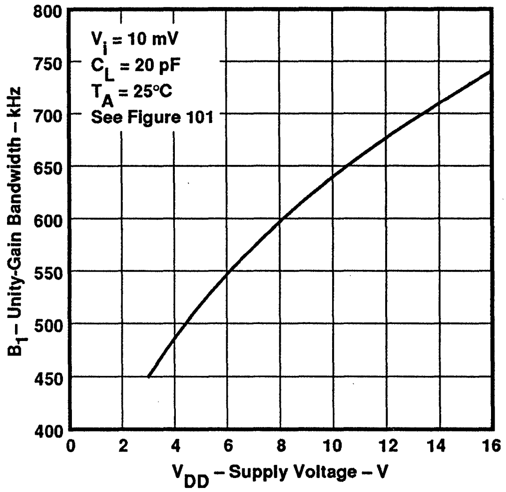


Figure 59

**LARGE-SIGNAL DIFFERENTIAL VOLTAGE
AMPLIFICATION AND PHASE SHIFT
vs
FREQUENCY**

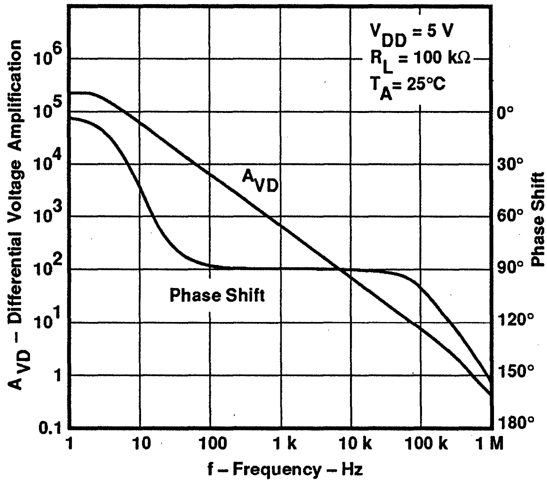


Figure 60

**LARGE-SIGNAL DIFFERENTIAL VOLTAGE
AMPLIFICATION AND PHASE SHIFT
vs
FREQUENCY**

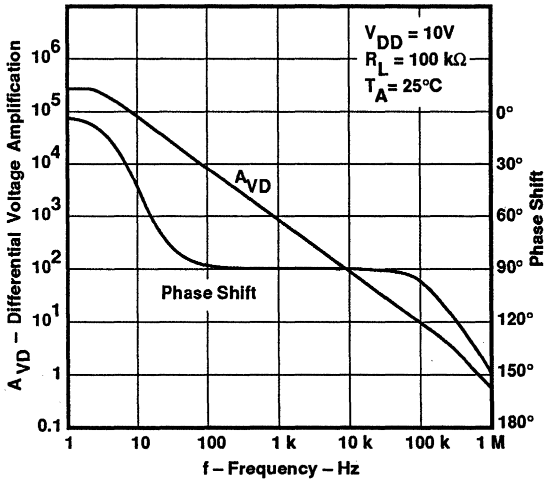


Figure 61

---

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS (MEDIUM-BIAS MODE)†

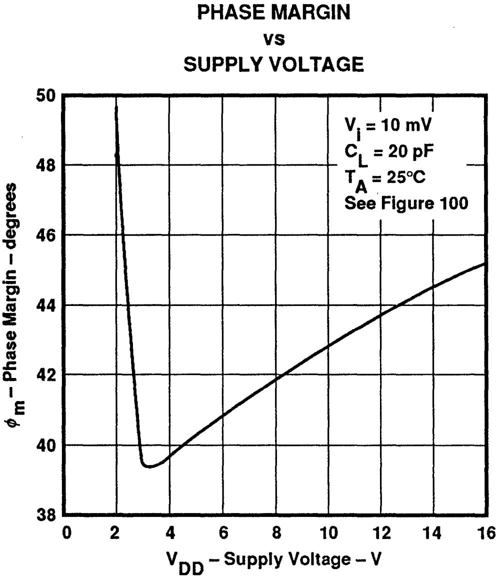


Figure 62

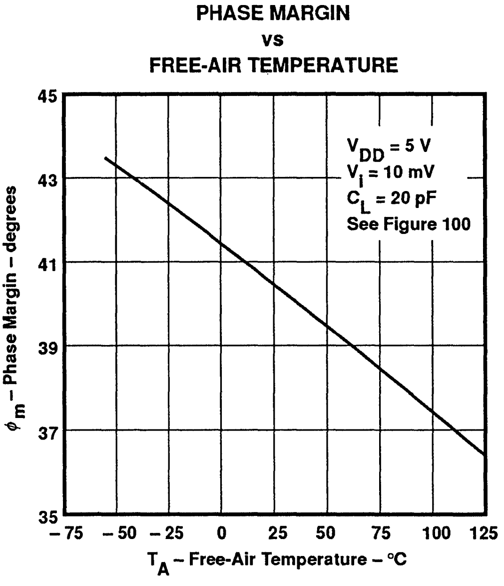


Figure 63

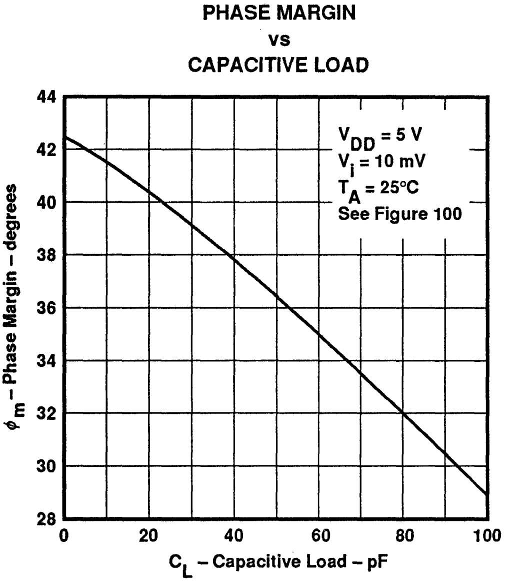


Figure 64

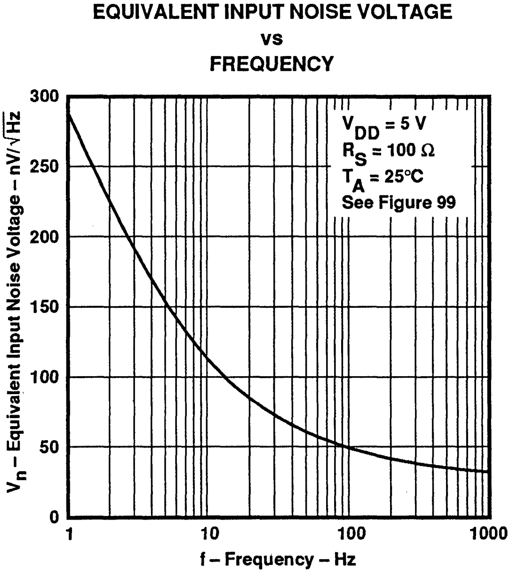


Figure 65

---

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

LOW-BIAS MODE

electrical characteristics over recommended free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS	T_A†	V_{DD} = 5 V			V_{DD} = 10 V			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	TLC271C	V_O = 1.4 V, V_{IC} = 0 V, R_S = 50 Ω, R_L = 1 MΩ	25°C		1.1	10		1.1	10	mV
				Full range			12			12	
		TLC271AC		25°C		0.9	5		0.9	5	
				Full range			6.5			6.5	
		TLC271BC		25°C		0.24	2		0.26	2	
				Full range			3			3	
α_{VIO}	Average temperature coefficient of input offset voltage			25°C to 70°C		1.1			1		µV/°C
I_{IO}	Input offset current (see Note 4)		V_O = V_{DD} / 2, V_{IC} = V_{DD} / 2	25°C		0.1			0.1		pA
				70°C		7	300		8	300	
I_{IB}	Input bias current (see Note 4)		V_O = V_{DD} / 2, V_{IC} = V_{DD} / 2	25°C		0.6			0.7		pA
				70°C		40	600		50	600	
V_{ICR}	Common-mode input voltage range (see Note 5)			25°C	−0.2 to 4	−0.3 to 4.2		−0.2 to 9	−0.3 to 9.2		V
				Full range	−0.2 to 3.5			−0.2 to 8.5			V
V_{OH}	High-level output voltage		V_{ID} = 100 mV, R_L = 1 MΩ	25°C	3.2	4.1		8	8.9		V
				0°C	3	4.1		7.8	8.9		
				70°C	3	4.2		7.8	8.9		
V_{OL}	Low-level output voltage		V_{ID} = − 100 mV, I_{OL} = 0	25°C		0	50		0	50	mV
				0°C		0	50		0	50	
				70°C		0	50		0	50	
A_{VD}	Large-signal differential voltage amplification		R_L = 1 MΩ, See Note 6	25°C	50	520		50	870		V/mV
				0°C	50	700		50	1030		
				70°C	50	380		50	660		
CMRR	Common-mode rejection ratio		V_{IC} = V_{ICR}min	25°C	65	94		65	97		dB
				0°C	60	95		60	97		
				70°C	60	95		60	97		
k_{SVR}	Supply-voltage rejection ratio (ΔV_{DD} / ΔV_{IO})		V_{DD} = 5 V to 10 V, V_O = 1.4 V	25°C	70	97		70	97		dB
				0°C	60	97		60	97		
				70°C	60	98		60	98		
$I_{I(SEL)}$	Input current to bias select pin		$V_{I(SEL)}$ = V_{DD}	25°C		65			95		nA
I_{DD}	Supply current		V_O = V_{DD} / 2, V_{IC} = V_{DD} / 2, No load	25°C		10	17		14	23	µA
				0°C		12	21		18	33	
				70°C		8	14		11	20	

†Full range is 0°C to 70°C.

NOTES:
4. The typical values of input bias current and input offset current below 5 pA were determined mathematically.
5. This range also applies to each input individually.
6. At V_{DD} = 5 V, V_O = 0.25 V to 2 V; at V_{DD} = 10 V, V_O = 1 V to 6 V.

LOW-BIAS MODE

electrical characteristics over recommended free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS	T_A†	V_{DD} = 5 V			V_{DD} = 10 V			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	TLC271I	V_O = 1.4 V, V_{IC} = 0 V, R_S = 50 Ω, R_L = 1 MΩ	25°C		1.1	10		1.1	10	mV
				Full range			13			13	
		TLC271AI		25°C		0.9	5		0.9	5	
				Full range			7			7	
		TLC271BI		25°C		0.24	2		0.26	2	
				Full range			3.5			3.5	
α_{VIO}	Average temperature coefficient of input offset voltage			25°C to 85°C		1.1			1		μV/°C
I_{IO}	Input offset current (see Note 4)		V_O = V_{DD} / 2, V_{IC} = V_{DD} / 2	25°C		0.1			0.1		pA
				85°C		24	1000		26	1000	
I_{IB}	Input bias current (see Note 4)		V_O = V_{DD} / 2, V_{IC} = V_{DD} / 2	25°C		0.6			0.7		pA
				85°C		200	2000		220	2000	
V_{ICR}	Common-mode input voltage range (see Note 5)			25°C	− 0.2 to 4	− 0.3 to 4.2		− 0.2 to 9	− 0.3 to 9.2		V
				Full range	− 0.2 to 3.5			− 0.2 to 8.5			V
V_{OH}	High-level output voltage		V_{ID} = 100 mV, R_L = 1 MΩ	25°C	3.2	4.1		8	8.9		V
				− 40°C	3	4.1		7.8	8.9		
				85°C	3	4.2		7.8	8.9		
V_{OL}	Low-level output voltage		V_{ID} = − 100 mV, I_{OL} = 0	25°C		0	50		0	50	mV
				− 40°C		0	50		0	50	
				85°C		0	50		0	50	
A_{VD}	Large-signal differential voltage amplification		R_L = 1 MΩ, See Note 6	25°C	50	520		50	870		V/mV
				− 40°C	50	900		50	1550		
				85°C	50	330		50	585		
CMRR	Common-mode rejection ratio		V_{IC} = V_{ICR}min	25°C	65	94		65	97		dB
				− 40°C	60	95		60	97		
				85°C	60	95		60	98		
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD} / \Delta V_{IO}$)		V_{DD} = 5 V to 10 V, V_O = 1.4 V	25°C	70	97		70	97		dB
				− 40°C	60	97		60	97		
				85°C	60	98		60	98		
$I_{I(SEL)}$	Input current to bias select pin		$V_{I(SEL)}$ = V_{DD}	25°C		65			95		nA
I_{DD}	Supply current		V_O = V_{DD} / 2, V_{IC} = V_{DD} / 2, No load	25°C		10	17		14	23	μA
				− 40°C		16	27		25	43	
				85°C		17	13		10	18	

†Full range is − 40 to 85°C.

NOTES: 4. The typical values of input bias current and input offset current below 5 pA were determined mathematically.

5. This range also applies to each input individually.

6. At V_{DD} = 5 V, V_O = 0.25 V to 2 V; at V_{DD} = 10 V, V_O = 1 V to 6 V.

LOW-BIAS MODE

electrical characteristics over recommended free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A†	V_{DD} = 5 V			V_{DD} = 10 V			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_O = 1.4 V, V_{IC} = 0 V, R_S = 50 Ω, R_L = 1 MΩ	25°C		1.1	10		1.1	10	mV
			Full range			12			12	
α_{VIO}	Average temperature coefficient of input offset voltage		25°C to 125°C		1.4			1.4		µV/°C
I_{IO}	Input offset current (see Note 4)	V_O = V_{DD} / 2, V_{IC} = V_{DD} / 2	25°C		0.1			0.1		pA
			125°C		1.4	15		1.8	15	nA
I_{IB}	Input bias current (see Note 4)	V_O = V_{DD} / 2, V_{IC} = V_{DD} / 2	25°C		0.6			0.7		pA
			125°C		9	35		10	35	nA
V_{ICR}	Common-mode input voltage range (see Note 5)		25°C	0 to 4	− 0.3 to 4.2		0 to 9	− 0.3 to 9.2		V
			Full range	0 to 3.5			0 to 8.5			V
V_{OH}	High-level output voltage	V_{ID} = 100 mV, R_L = 1 MΩ	25°C	3.2	4.1		8	8.9		V
			− 55°C	3	4.1		7.8	8.8		
			125°C	3	4.2		7.8	9		
V_{OL}	Low-level output voltage	V_{ID} = − 100 mV, I_{OL} = 0	25°C		0	50		0	50	mV
			− 55°C		0	50		0	50	
			125°C		0	50		0	50	
A_{VD}	Large-signal differential voltage amplification	R_L = 1 MΩ, See Note 6	25°C	50	520		50	870		V/mV
			− 55°C	25	1000		25	1775		
			125°C	25	200		25	380		
CMRR	Common-mode rejection ratio	V_{IC} = V_{ICR}min	25°C	65	94		65	97		dB
			− 55°C	60	95		60	97		
			125°C	60	85		60	91		
k_{SVR}	Supply-voltage rejection ratio (ΔV_{DD} / ΔV_{IO})	V_{DD} = 5 V to 10 V, V_O = 1.4 V	25°C	70	97		70	97		dB
			− 55°C	60	97		60	97		
			125°C	60	98		60	98		
$I_{I(SEL)}$	Input current to bias select pin	$V_{I(SEL)}$ = V_{DD}	25°C		65			95		nA
I_{DD}	Supply current	V_O = V_{DD} / 2, V_{IC} = V_{DD} / 2, No load	25°C		10	17		14	23	µA
			− 55°C		17	30		28	48	
			125 °C		7	12		9	15	

†Full range is − 55°C to 125°C.

NOTES: 4. The typical values of input bias current and input offset current below 5 pA were determined mathematically.
5. This range also applies to each input individually.
6. At V_{DD} = 5 V, V_O = 0.25 V to 2 V; at V_{DD} = 10 V, V_O = 1 V to 6 V.

LOW-BIAS MODE

operating characteristics, V_{DD} = 5 V

PARAMETER		TEST CONDITIONS		T_A	MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain	R_L = 1 MΩ, C_L = 20 pF, See Figure 98	V_{IPP} = 1 V	25°C		0.03		V/μs
				0°C		0.04		
				70°C		0.03		
			V_{IPP} = 2.5 V	25°C		0.03		
				0°C		0.03		
				70°C		0.02		
V_n	Equivalent input noise voltage	f = 1 kHz, R_S = 100 Ω, See Figure 99		25°C		68		nV/√Hz
B_{OM}	Maximum output swing bandwidth	$V_O = V_{OH}$, C_L = 20 pF, R_L = 1 MΩ, See Figure 98		25°C		5		kHz
				0°C		6		
				70°C		4.5		
B_1	Unity-gain bandwidth	V_i = 10 mV, C_L = 20 pF, See Figure 100		25°C		85		kHz
				0°C		100		
				70°C		65		
ϕ_m	Phase margin	V_i = 10 mV, f = B_1, C_L = 20 pF, See Figure 100		25°C		34°		
				0°C		36°		
				70°C		30°		

operating characteristics, V_{DD} = 10 V

PARAMETER		TEST CONDITIONS		T_A	MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain	R_L = 1 MΩ, C_L = 20 pF, See Figure 98	V_{IPP} = 1 V	25°C		0.05		V/μs
				0°C		0.05		
				70°C		0.04		
			V_{IPP} = 5.5 V	25°C		0.04		
				0°C		0.05		
				70°C		0.04		
V_n	Equivalent input noise voltage	f = 1 kHz, R_S = 100 Ω, See Figure 99		25°C		68		nV/√Hz
B_{OM}	Maximum output swing bandwidth	$V_O = V_{OH}$, C_L = 20 pF, R_L = 1 MΩ, See Figure 98		25°C		1		kHz
				0°C		1.3		
				70°C		0.9		
B_1	Unity-gain bandwidth	V_i = 10 mV, C_L = 20 pF, See Figure 100		25°C		110		kHz
				0°C		125		
				70°C		90		
ϕ_m	Phase margin	V_i = 10 mV, f = B_1, C_L = 20 pF, See Figure 100		25°C		38°		
				0°C		40°		
				70°C		34°		

LOW-BIAS MODE

operating characteristics, V_{DD} = 5 V

PARAMETER		TEST CONDITIONS		T_A	MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain	R_L = 1MΩ, C_L = 20 pF, See Figure 98	V_{IPP} = 1 V	25°C		0.03		V/µs
				– 40°C		0.04		
				85°C		0.03		
			V_{IPP} = 2.5 V	25°C		0.03		
				– 40°C		0.04		
				85°C		0.02		
V_n	Equivalent input noise voltage	f = 1 kHz, R_S = 100 Ω, See Figure 99		25°C		68		nV/√Hz
B_{OM}	Maximum output swing bandwidth	V_O = V_{OH}, C_L = 20 pF, R_L = 1MΩ, See Figure 98		25°C		5		kHz
				– 40°C		7		
				85°C		4		
B_1	Unity-gain bandwidth	V_i = 10 mV, C_L = 20 pF, See Figure 100		25°C		85		kHz
				– 40°C		130		
				85°C		55		
ϕ_m	Phase margin	V_i = 10 mV, f = B_1, C_L = 20 pF, See Figure 100		25°C		34°		
				– 40°C		38°		
				85°C		28°		

operating characteristics, V_{DD} = 10 V

PARAMETER		TEST CONDITIONS		T_A	MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain	R_L = 1 MΩ, C_L = 20 pF, See Figure 98	V_{IPP} = 1 V	25°C		0.05		V/µs
				– 40°C		0.06		
				85°C		0.03		
			V_{IPP} = 5.5 V	25°C		0.04		
				– 40°C		0.05		
				85°C		0.03		
V_n	Equivalent input noise voltage	f = 1 kHz, R_S = 100 Ω, See Figure 99		25°C		68		nV/√Hz
B_{OM}	Maximum output swing bandwidth	V_O = V_{OH}, C_L = 20 pF, R_L = 1 MΩ, See Figure 98		25°C		1		kHz
				– 40°C		1.4		
				85°C		0.8		
B_1	Unity-gain bandwidth	V_i = 10 mV, C_L = 20 pF, See Figure 100		25°C		110		kHz
				– 40°C		155		
				85°C		80		
ϕ_m	Phase margin	V_i = 10 mV, f = B_1, C_L = 20 pF, See Figure 100		25°C		38°		
				– 40°C		42°		
				85°C		32°		

LOW-BIAS MODE

operating characteristics, V_{DD} = 5 V

PARAMETER		TEST CONDITIONS		T_A	MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain	R_L = 1 MΩ, C_L = 20 pF, See Figure 98	V_{IPP} = 1 V	25°C		0.03		V/μs
				– 55°C		0.04		
				125°C		0.02		
			V_{IPP} = 2.5 V	25°C		0.03		
				– 55°C		0.04		
				125°C		0.02		
V_n	Equivalent input noise voltage	f = 1 kHz, R_S = 100 Ω, See Figure 99		25°C		68		nV/√Hz
B_{OM}	Maximum output swing bandwidth	V_O = V_{OH}, C_L = 20 pF, R_L = 1 MΩ, See Figure 98		25°C		5		kHz
				– 55°C		8		
				125°C		3		
B_1	Unity-gain bandwidth	V_i = 10 mV, C_L = 20 pF, See Figure 100		25°C		85		kHz
				– 55°C		140		
				125°C		45		
ϕ_m	Phase margin	V_i = 10 mV, f = B_1, C_L = 20 pF, See Figure 100		25°C		34°		
				– 55°C		39°		
				125°C		25°		

operating characteristics, V_{DD} = 10 V

PARAMETER		TEST CONDITIONS		T_A	MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain	R_L = 1 MΩ, C_L = 20 pF, See Figure 98	V_{IPP} = 1 V	25°C		0.05		V/μs
				– 55°C		0.06		
				125°C		0.03		
			V_{IPP} = 5.5 V	25°C		0.04		
				– 55°C		0.06		
				125°C		0.03		
V_n	Equivalent input noise voltage	f = 1 kHz, R_S = 100 Ω, See Figure 99		25°C		68		nV/√Hz
B_{OM}	Maximum output swing bandwidth	V_O = V_{OH}, C_L = 20 pF, R_L = 1 MΩ, See Figure 98		25°C		1		kHz
				–55°C		1.5		
				125°C		0.7		
B_1	Unity-gain bandwidth	V_i = 10 mV, C_L = 20 pF, See Figure 100		25°C		110		kHz
				– 55°C		165		
				125°C		70		
ϕ_m	Phase margin	V_i = 10 mV, f = B_1, C_L = 20 pF, See Figure 100		25°C		38°		
				– 55°C		43°		
				125°C		29°		

TYPICAL CHARACTERISTICS (LOW-BIAS MODE)†

DISTRIBUTION OF TLC271 INPUT OFFSET VOLTAGE

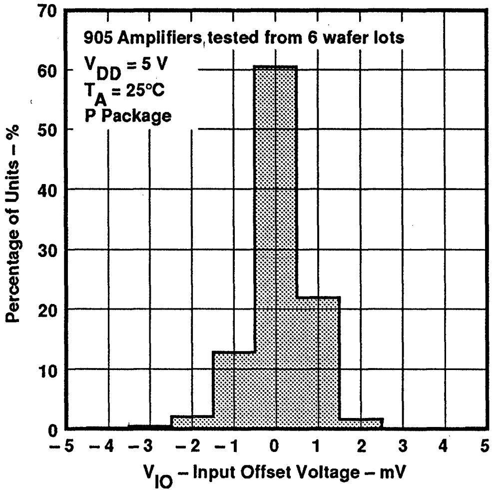


Figure 66

DISTRIBUTION OF TLC271 INPUT OFFSET VOLTAGE

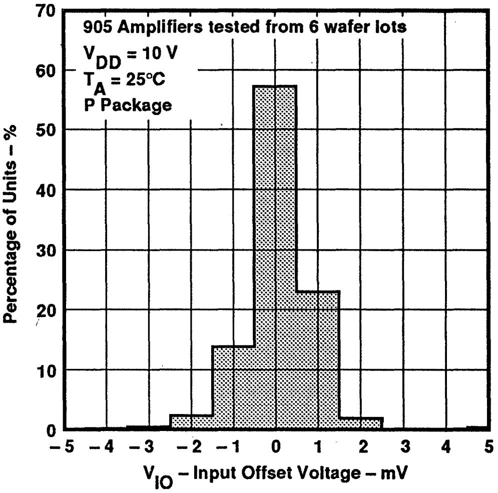


Figure 67

DISTRIBUTION OF TLC271 INPUT OFFSET VOLTAGE TEMPERATURE COEFFICIENT

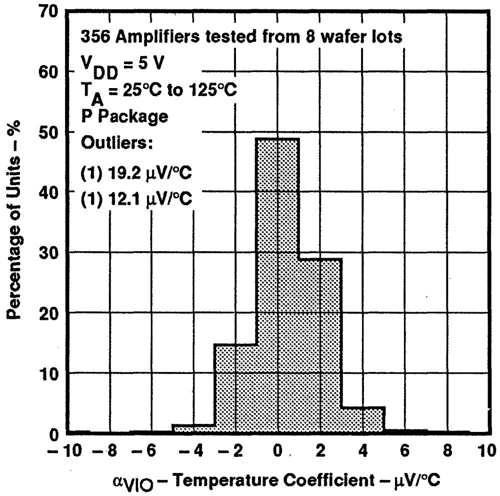


Figure 68

DISTRIBUTION OF TLC271 INPUT OFFSET VOLTAGE TEMPERATURE COEFFICIENT

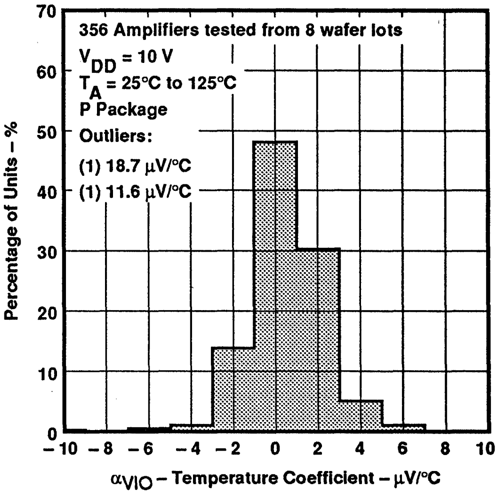


Figure 69

---

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS (LOW-BIAS MODE)†

HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

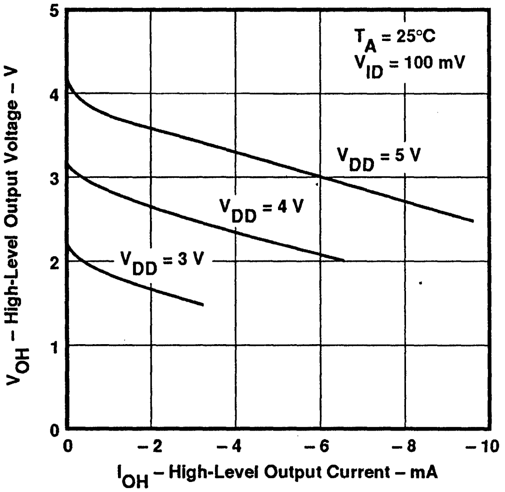


Figure 70

HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

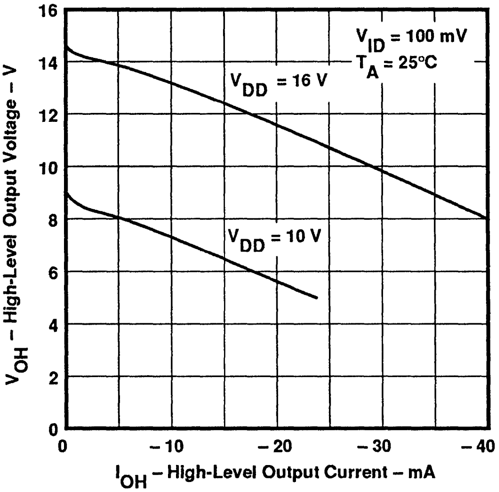


Figure 71

HIGH-LEVEL OUTPUT VOLTAGE
vs
SUPPLY VOLTAGE

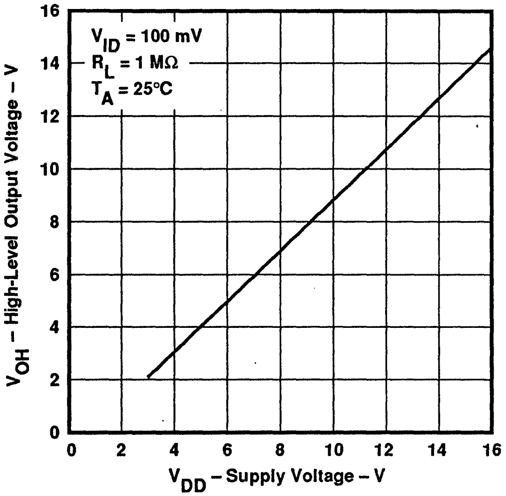


Figure 72

HIGH-LEVEL OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

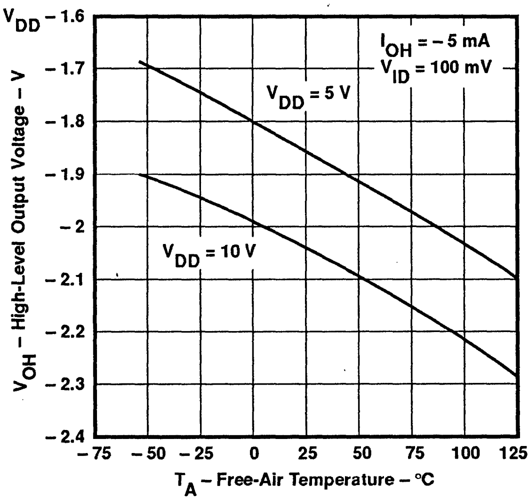


Figure 73

---

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS (LOW-BIAS MODE)†

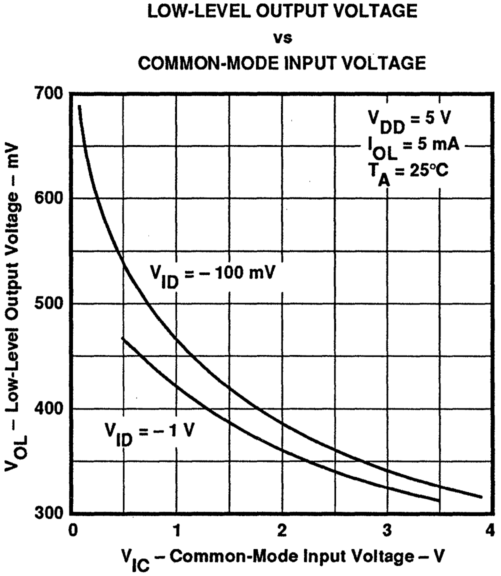


Figure 74

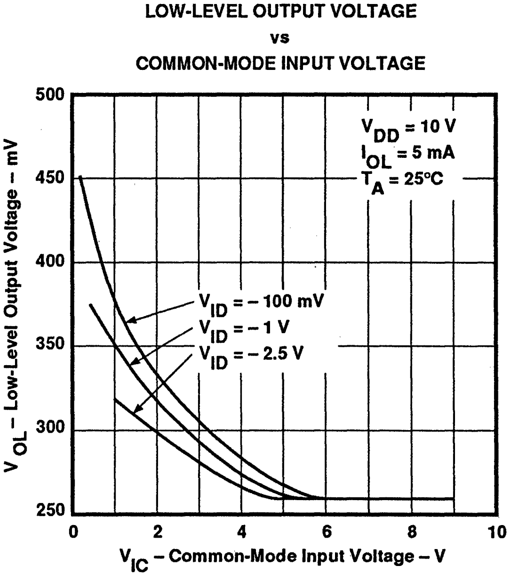


Figure 75

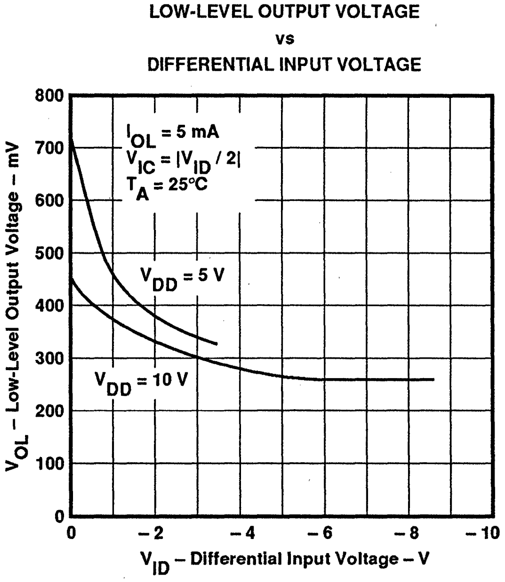


Figure 76

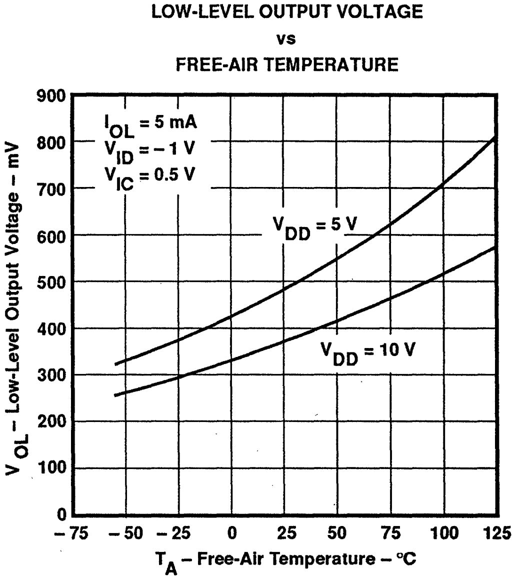


Figure 77

---

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS (LOW-BIAS MODE)†

LOW-LEVEL OUTPUT VOLTAGE vs LOW-LEVEL OUTPUT CURRENT

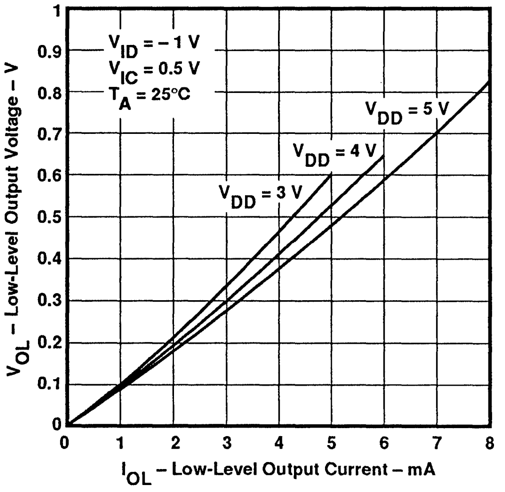


Figure 78

LOW-LEVEL OUTPUT VOLTAGE vs LOW-LEVEL OUTPUT CURRENT

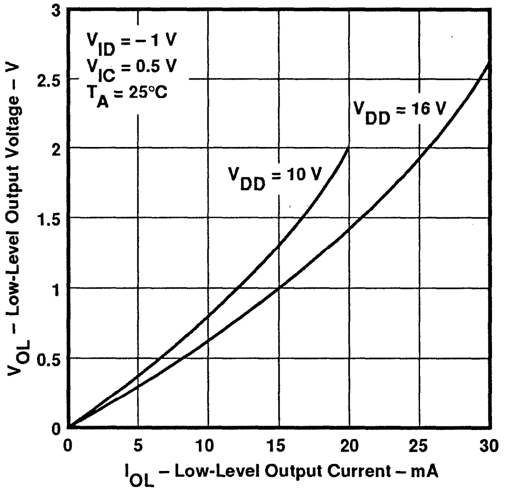


Figure 79

LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION vs SUPPLY VOLTAGE

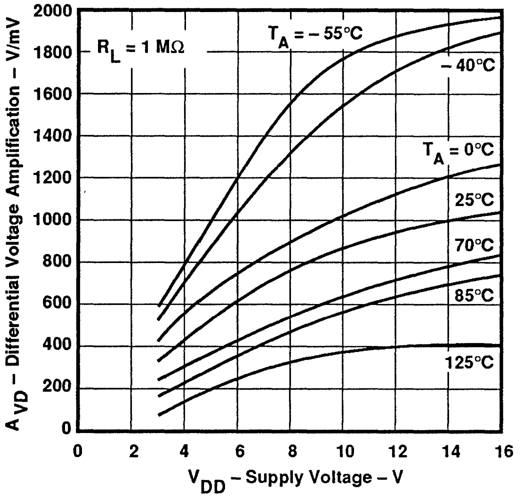


Figure 80

LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION vs FREE-AIR TEMPERATURE

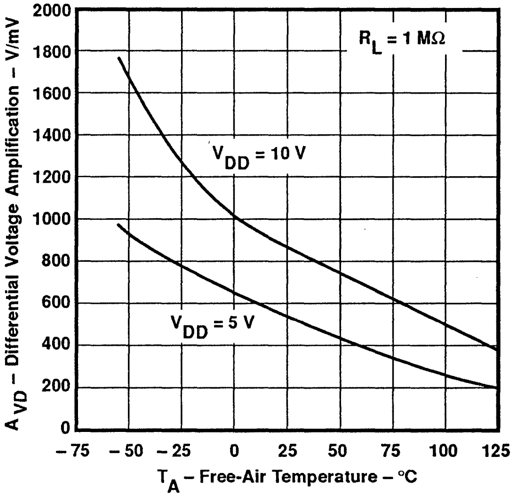


Figure 81

---

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS (LOW-BIAS MODE)†

INPUT BIAS CURRENT AND INPUT OFFSET CURRENT vs FREE-AIR TEMPERATURE

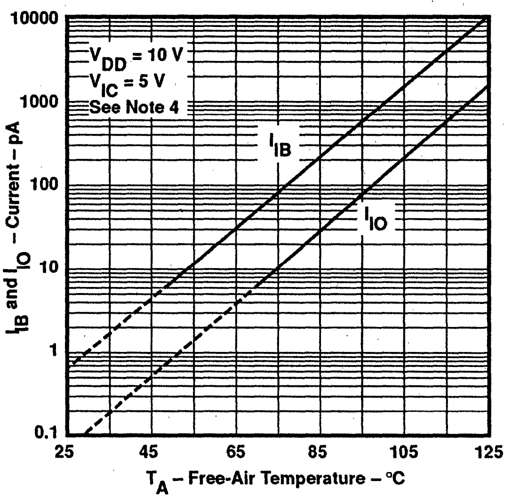


Figure 82

MAXIMUM INPUT VOLTAGE vs SUPPLY VOLTAGE

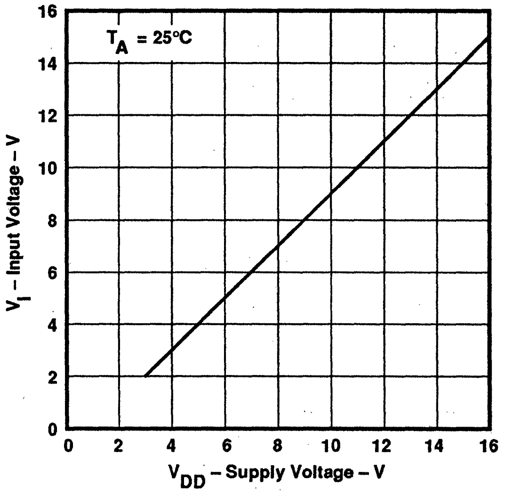


Figure 83

SUPPLY CURRENT vs SUPPLY VOLTAGE

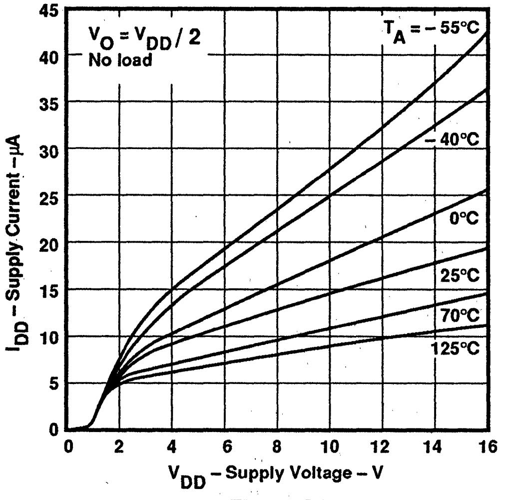


Figure 84

SUPPLY CURRENT vs FREE-AIR TEMPERATURE

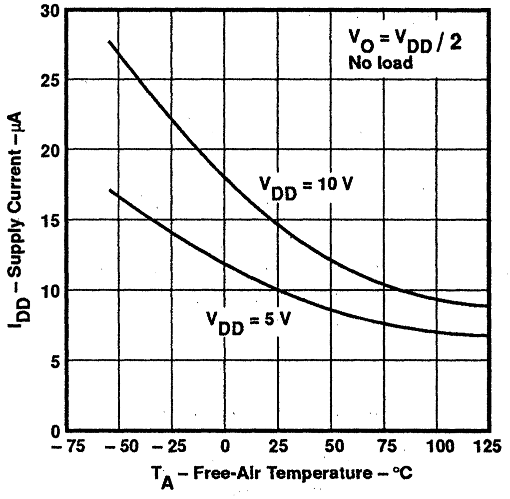


Figure 85

---

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

NOTE 4: The typical values of input bias current and input offset current below 5 pA were determined mathematically.

TYPICAL CHARACTERISTICS (LOW-BIAS MODE)†

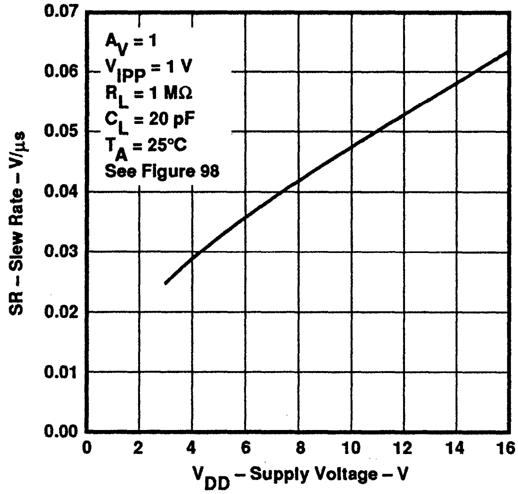

SLEW RATE
vs
SUPPLY VOLTAGE

Figure 86

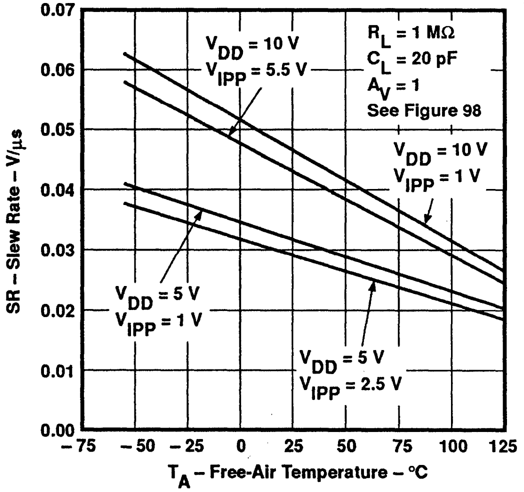

SLEW RATE
vs
FREE-AIR TEMPERATURE

Figure 87

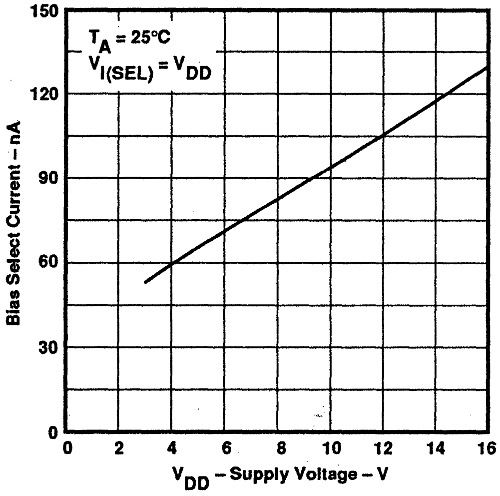

BIAS SELECT CURRENT
vs
SUPPLY VOLTAGE

Figure 88

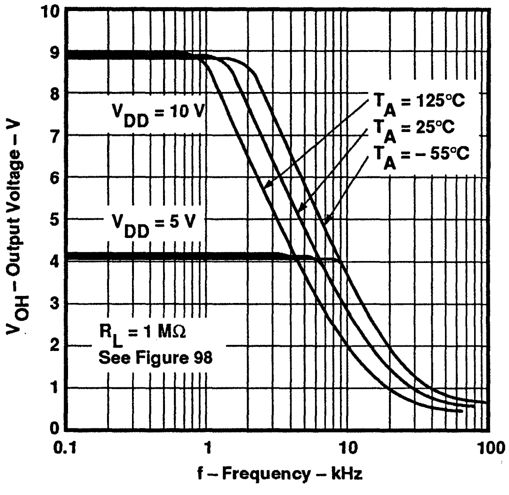

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE
vs
FREQUENCY

Figure 89

---

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS (LOW-BIAS MODE)†

UNITY-GAIN BANDWIDTH vs FREE-AIR TEMPERATURE

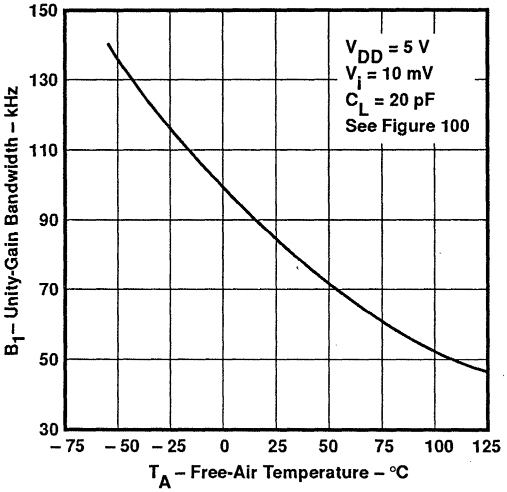


Figure 90

UNITY-GAIN BANDWIDTH vs SUPPLY VOLTAGE

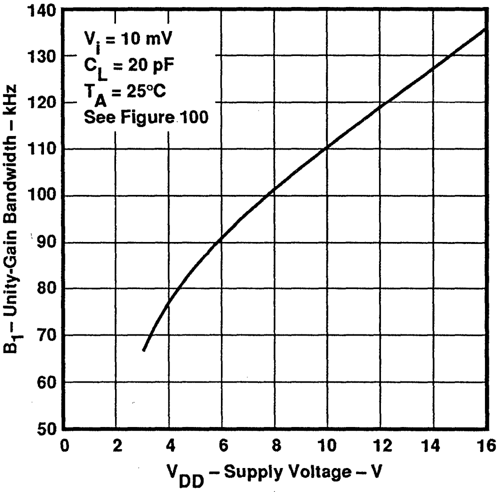


Figure 91

LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION AND PHASE SHIFT vs FREQUENCY

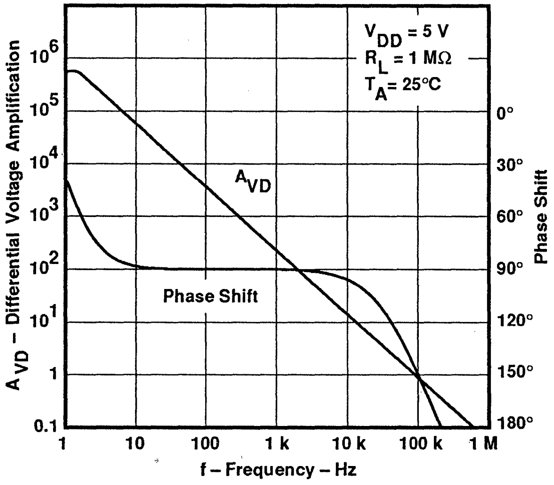


Figure 92

LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION AND PHASE SHIFT vs FREQUENCY

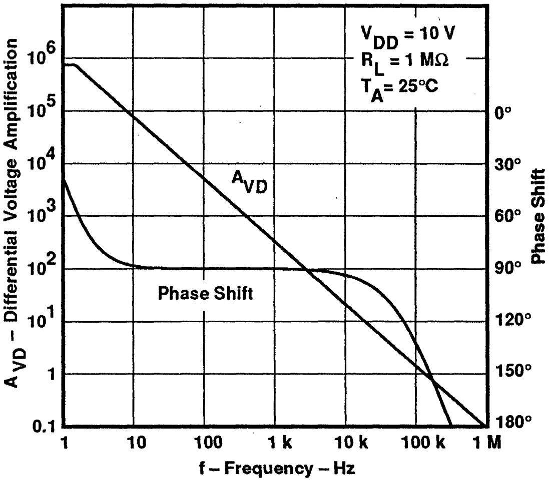


Figure 93

---

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS (LOW-BIAS MODE)†

PHASE MARGIN vs SUPPLY VOLTAGE

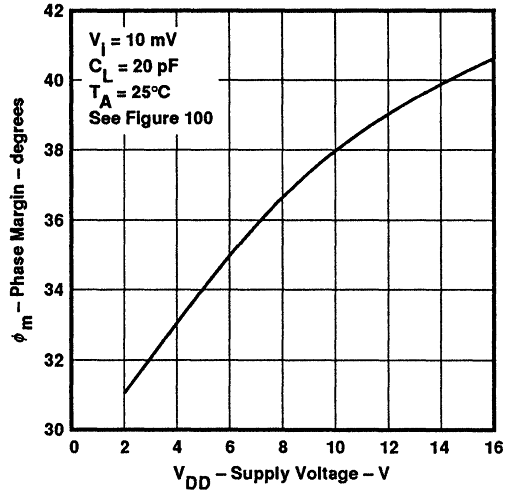


Figure 94

PHASE MARGIN vs FREE-AIR TEMPERATURE

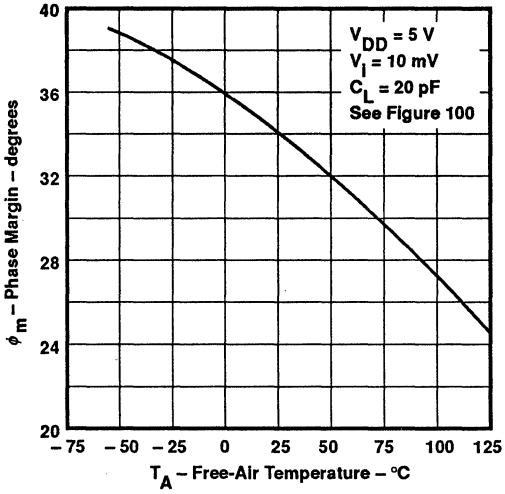


Figure 95

PHASE MARGIN vs CAPACITIVE LOAD

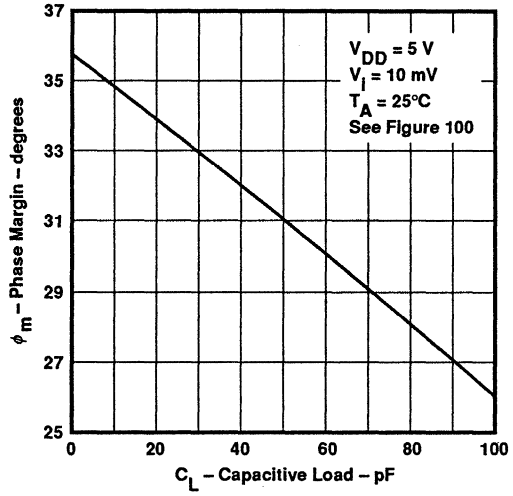


Figure 96

EQUIVALENT INPUT NOISE VOLTAGE vs FREQUENCY

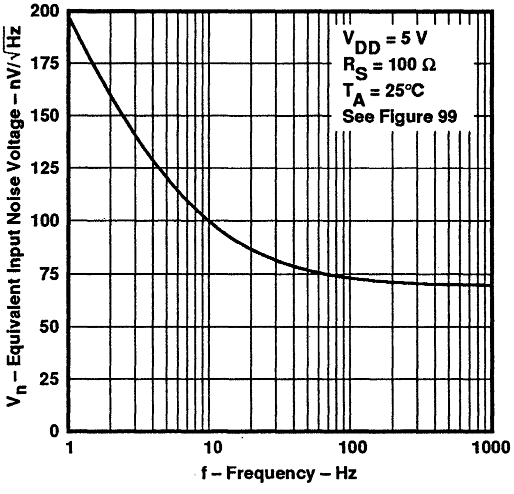


Figure 97

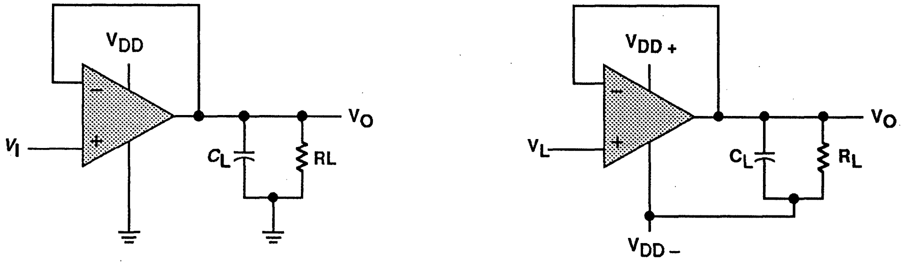
---

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

PARAMETER MEASUREMENT INFORMATION

single-supply versus split-supply test circuits

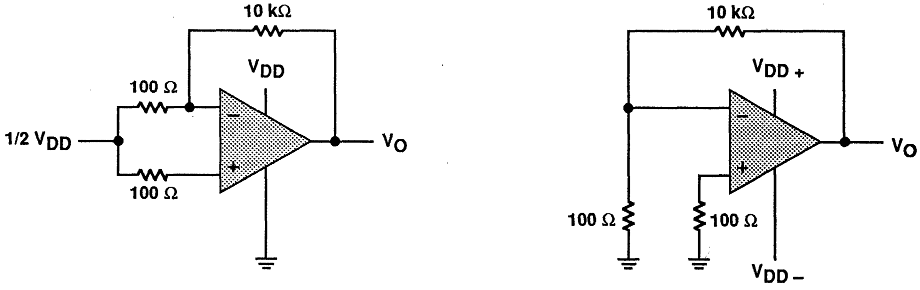
Because the TLC271 is optimized for single-supply operation, circuit configurations used for the various tests often present some inconvenience since the input signal, in many cases, must be offset from ground. This inconvenience can be avoided by testing the device with split supplies and the output load tied to the negative rail. A comparison of single-supply versus split-supply test circuits is shown below. The use of either circuit will give the same result.



(a) Single-Supply

(b) Split-Supply

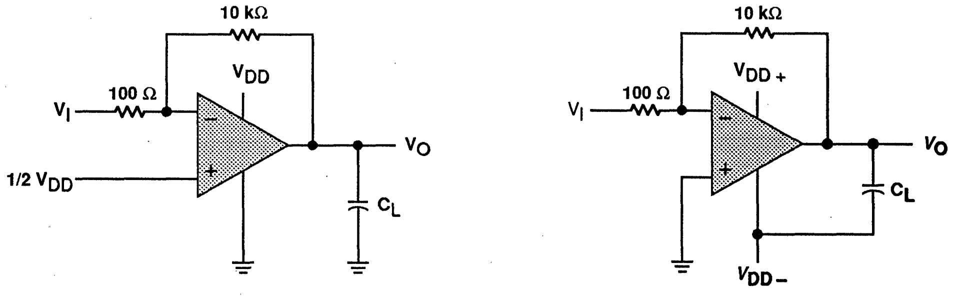
Figure 98. Unity-Gain Amplifier



(a) Single-Supply

(b) Split-Supply

Figure 99. Noise Test Circuit



(a) Single-Supply

(b) Split-Supply

Figure 100. Gain-of-100 Inverting Amplifier

PARAMETER MEASUREMENT INFORMATION

input bias current

Because of the high input impedance of the TLC271 op amp, attempts to measure the input bias current can result in erroneous readings. The bias current at normal room ambient temperature is typically less than 1 pA, a value that is easily exceeded by leakages on the test socket. Two suggestions are offered to avoid erroneous measurements:

1. Isolate the device from other potential leakage sources. Use a grounded shield around and between the device inputs (see Figure 101). Leakages that would otherwise flow to the inputs will be shunted away.
2. Compensate for the leakage of the test socket by actually performing an input bias current test (using a picoammeter) with no device in the test socket. The actual input bias current can then be calculated by subtracting the "open-socket" leakage readings from the readings obtained with a device in the test socket.

   One word of caution . . . many automatic testers as well as some bench-top op amp testers use the servo-loop technique with a resistor in series with the device input to measure the input bias current (the voltage drop across the series resistor is measured and the bias current is calculated). This method requires that a device be inserted into the test socket to obtain a correct reading; therefore, an "open-socket" reading is not feasible using this method.

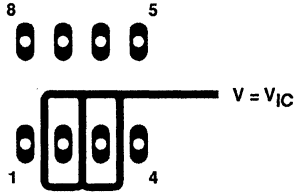


Figure 101. Isolation Metal Around Device Inputs
(JG and P Dual-In-Line Package)

low-level output voltage

To obtain low-supply-voltage operation, some compromise is necessary in the input stage. This compromise results in the device low-level output being dependent on both the common-mode input voltage level as well as the differential input voltage level. When attempting to correlate low-level output readings with those quoted in the electrical specifications, these two conditions should be observed. If conditions other than these are to be used, please refer to the Typical Characteristics section of this data sheet.

input offset voltage temperature coefficient

Erroneous readings often result from attempts to measure temperature coefficient of input offset voltage. This parameter is actually a calculation using input offset voltage measurements obtained at two different temperatures. When one (or both) of the temperatures is below freezing, moisture can collect on both the device and the test socket. This moisture will result in leakage and contact resistance which can cause erroneous input offset voltage readings. The isolation techniques previously mentioned have no effect on the leakage since the moisture also covers the isolation metal itself, thereby rendering it useless. It is suggested that these measurements be performed at temperatures above freezing to minimize error.

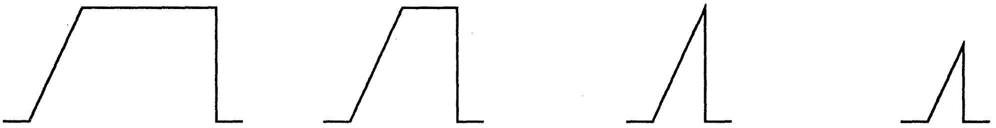
full power response

Full power response, the frequency above which the op amp slew rate limits the output voltage swing, is often specified two ways . . . full-linear response and full-peak response. The full-linear response is generally

PARAMETER MEASUREMENT INFORMATION

measured by monitoring the distortion level of the output while increasing the frequency of a sinusoidal input signal until the maximum frequency is found above which the output contains significant distortion. The full-peak response is defined as the maximum output frequency, without regard to distortion, above which full peak-to-peak output swing cannot be maintained.

Because there is no industry-wide accepted value for "significant" distortion, the full-peak response is specified in this data sheet and is measured using the circuit of Figure 98. The initial setup involves the use of a sinusoidal input to determine the maximum peak-to-peak output of the device (the amplitude of the sinusoidal wave is increased until clipping occurs). The sinusoidal wave is then replaced with a square wave of the same amplitude. The frequency is then increased until the maximum peak-to-peak output can no longer be maintained (Figure 102). A square wave is used to allow a more accurate determination of the point at which the maximum peak-to-peak output is reached.



(a) $f = 100$ Hz (b) $B_{OM} > f > 100$ Hz (c) $f = B_{OM}$ (d) $f > B_{OM}$

Figure 102. Full-Power-Response Output Signal

test time

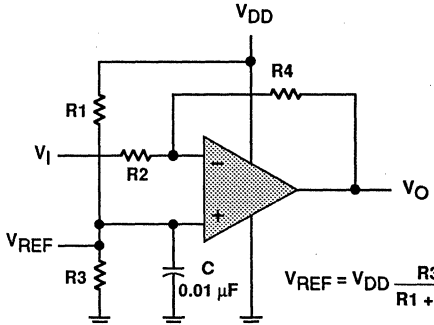
Inadequate test time is a frequent problem, especially when testing CMOS devices in a high-volume, short-test-time environment. Internal capacitances are inherently higher in CMOS than in bipolar and BiFET devices, and require longer test times than their bipolar and BiFET counterparts. The problem becomes more pronounced with reduced supply levels and lower temperatures.

TYPICAL APPLICATION DATA

single-supply operation

While the TLC271 will perform well using dual power supplies (also called balanced or split supplies), the design is optimized for single-supply operation. This includes an input common mode voltage range that encompasses ground as well as an output voltage range that pulls down to ground. The supply voltage range extends down to 3 V (C- suffix types), thus allowing operation with supply levels commonly available for TTL and HCMOS; however, for maximum dynamic range, 16-V single-supply operation is recommended.

Many single-supply applications require that a voltage be applied to one input to establish a reference level that is above ground. A resistive voltage divider is usually sufficient to establish this reference level (see Figure 103). The low input bias current consumption of the TLC271 permits the use of very large resistive values to implement the voltage divider, thus minimizing power consumption.



$$V_{REF} = V_{DD} \frac{R3}{R1 + R3}$$

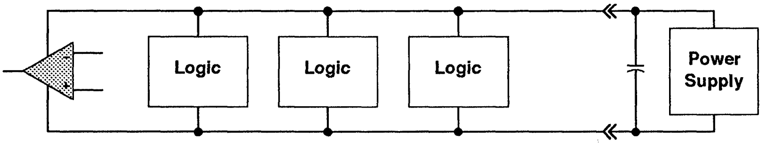
$$V_O = (V_{REF} - V_I) \frac{R4}{R2} + V_{REF}$$

Figure 103. Inverting Amplifier With Voltage Reference

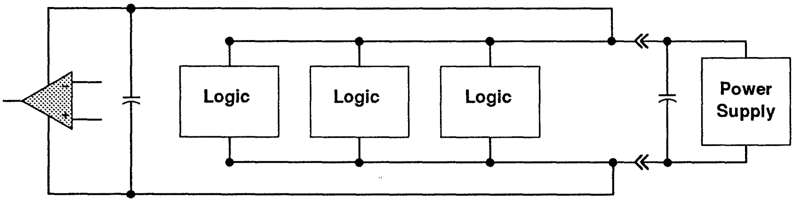
TYPICAL APPLICATION DATA

The TLC271 works well in conjunction with digital logic; however, when powering both linear devices and digital logic from the same power supply, the following precautions are recommended:

1. Power the linear devices from separate bypassed supply lines (see Figure 104); otherwise, the linear device supply rails can fluctuate due to voltage drops caused by high switching currents in the digital logic.
2. Use proper bypass techniques to reduce the probability of noise-induced errors. Single capacitive decoupling is often adequate; however, RC decoupling may be necessary in high-frequency applications.



(a) Common Supply Rails



(b) Separate Bypassed Supply Rails (preferred)

Figure 104. Common Versus Separate Supply Rails

input offset voltage nulling

The TLC271 offers external input offset null control. Nulling of the input offset voltage may be achieved by adjusting a 25-kΩ potentiometer connected between the offset null terminals with the wiper connected as shown in Figure 105. The amount of nulling range varies with the bias selection. In the high-bias mode, the nulling range will allow the maximum offset voltage specified to be trimmed to zero. In low-bias and medium-bias modes, total nulling may not be possible.

(a) Single-Supply

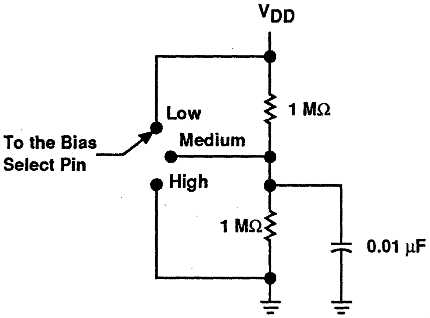
(b) Split-Supply

Figure 105. Input Offset Voltage Null Circuit

TYPICAL APPLICATION DATA

bias selection

Bias selection is achieved by connecting the bias select pin to one of the three voltage levels (see Figure 106). For medium-bias applications, it is recommended that the bias select pin be connected to the mid-point between the supply rails. This is a simple procedure in split-supply applications, since this point is ground. In single-supply applications, the medium-bias mode will necessitate using a voltage divider as indicated. The use of large-value resistors in the voltage divider will reduce the current drain of the divider from the supply line. However, large-value resistors used in conjunction with a large-value capacitor will require significant time to charge up to the supply midpoint after the supply is switched on. A voltage other than the mid-point may be used if it is within the voltages specified in the following table.



BIAS MODE	BIAS SELECT VOLTAGE (Single Supply)
LOW	V_{DD}
MEDIUM	1 V to $V_{DD} - 1$ V
HIGH	GND

Figure 106. Bias Selection for Single-Supply Applications

input characteristics

The TLC271 is specified with a minimum and a maximum input voltage that, if exceeded at either input, could cause the device to malfunction. Exceeding this specified range is a common problem, especially in single-supply operation. Note that the lower range limit includes the negative rail, while the upper range limit is specified at $V_{DD} - 1$ V at $T_A = 25°C$ and at $V_{DD} - 1.5$ V at all other temperatures.

The use of the polysilicon-gate process and the careful input circuit design gives the TLC271 very good input offset voltage drift characteristics relative to conventional metal-gate processes. Offset voltage drift in CMOS devices is highly influenced by threshold voltage shifts caused by polarization of the phosphorus dopant implanted in the oxide. Placing the phosphorus dopant in a conductor (such as a polysilicon gate) alleviates the polarization problem, thus reducing threshold voltage shifts by more than an order of magnitude. The offset voltage drift with time has been calculated to be typically 0.1 µV/month, including the first month of operation.

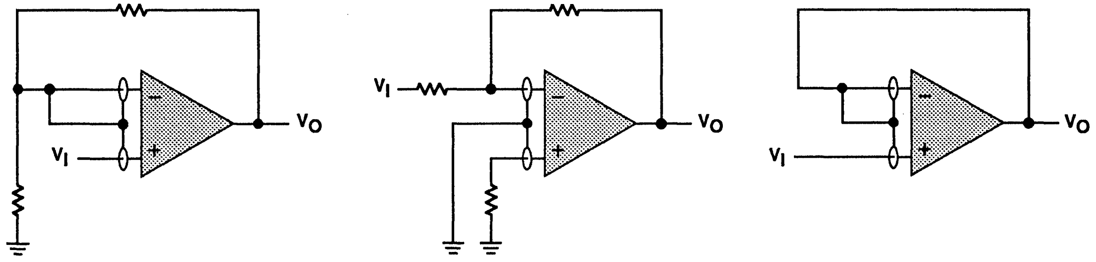
Because of the extremely high input impedance and resulting low bias current requirements, the TLC271 is well suited for low-level signal processing; however, leakage currents on printed circuit boards and sockets can easily exceed bias current requirements and cause a degradation in device performance. It is good practice to include guard rings around inputs (similar to those of Figure 101 in the Parameter Measurment Information section). These guards should be driven from a low-impedance source at the same voltage level as the common-mode input (see Figure 107).

The inputs of any unused amplifiers should be tied to ground to avoid possible oscillation.

noise performance

The noise specifications in op amp circuits are greatly dependent on the current in the first-stage differential amplifier. The low input bias current requirements of the TLC271 results in a very low noise current, which is insignificant in most applications. This feature makes the devices especially favorable over bipolar devices when using values of circuit impedance greater than 50 kΩ, since bipolar devices exhibit greater noise currents.

TYPICAL APPLICATION DATA



(a) Noninverting Amplifier (b) Inverting Amplifier (c) Unity Gain Amplifier

Figure 107. Guard Ring Schemes

feedback

Op amp circuits nearly always employ feedback, and since feedback is the first prerequisite for oscillation, a little caution is appropriate. Most oscillation problems result from driving capacitive loads and ignoring stray input capacitance. A small-value capacitor connected in parallel with the feedback resistor is an effective remedy (see Figure 108). The value of this capacitor is optimized empirically.

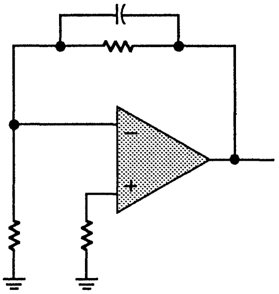


Figure 108. Compensation for Input Capacitance

electrostatic discharge protection

The TLC271 incorporates an internal electrostatic discharge (ESD) protection circuit that will prevent functional failures at voltages up to 2000 V as tested under MIL-STD-883C, Method 3015.2. Care should be exercised, however, when handling these devices as exposure to ESD may result in the degradation of the device parametric performance. The protection circuit also causes the input bias currents to be temperature dependent and have the characteristics of a reverse-biased diode.

latchup

Because CMOS devices are susceptible to latchup due to their inherent parasitic thyristors, the TLC271 inputs and output were designed to withstand −100-mA surge currents without sustaining latchup; however, techniques should be used to reduce the chance of latchup whenever possible. Internal protection diodes should not by design be forward biased. Applied input and output voltage should not exceed the supply voltage by more than 300 mV. Care should be exercised when using capacitive coupling on pulse generators. Supply transients should be shunted by the use of decoupling capacitors (0.1 µF typical) located across the supply rails as close to the device as possible.

The current path established if latchup occurs is usually between the positive supply rail and ground and can be triggered by surges on the supply lines and / or voltages on either the output or inputs that exceed the supply voltage. Once latchup occurs, the current flow is limited only by the impedance of the power supply and the forward resistance of the parasitic thyristor and usually results in the destruction of the device. The chance of latchup occuring increases with increasing temperature and supply voltages.

TYPICAL APPLICATION DATA

output characteristics

The output stage of the TLC271 is designed to sink and source relatively high amounts of current (see Typical Characteristics). If the output is subjected to a short-circuit condition, this high current capability can cause device damage under certain conditions. Output current capability increases with supply voltage.

All operating characteristics of the TLC271 were measured using a 20-pF load. The devices will drive higher capacitive loads; however, as output load capacitance increases, the resulting response pole occurs at lower frequencies, thereby causing ringing, peaking, or even oscillation (see Figures 110, 111, and 112). In many cases, adding some compensation in the form of a series resistor in the feedback loop will alleviate the problem.

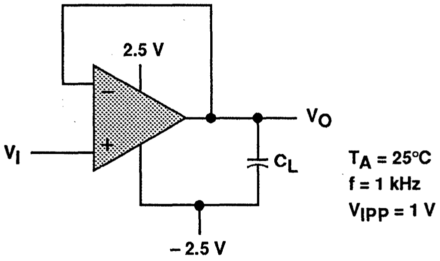
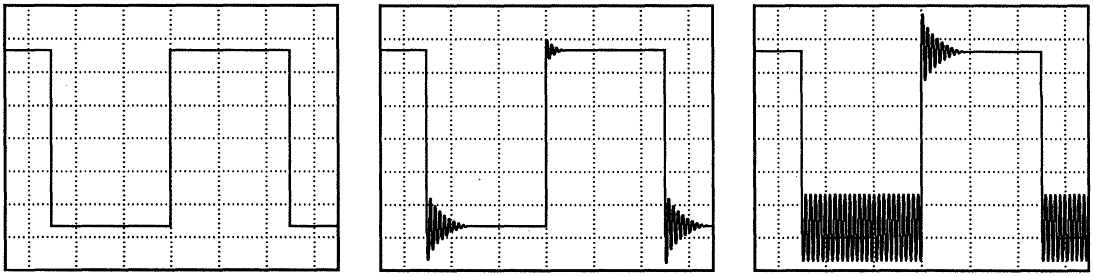


Figure 109. Test Circuit for Output Characteristics

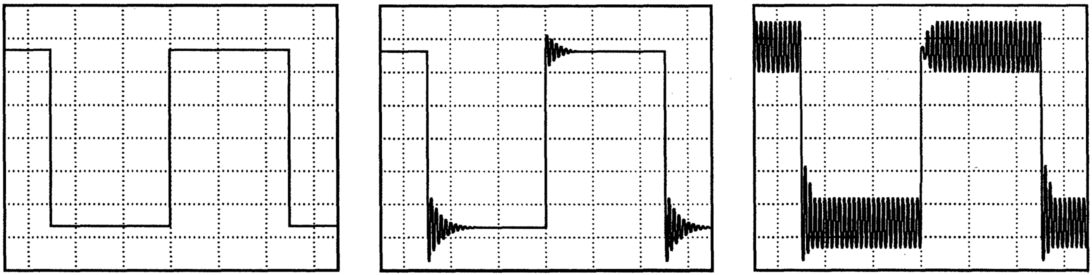


(a) C_L = 20 pF, R_L = No load

(a) C_L = 130 pF, R_L = No load

(a) C_L = 150 pF, R_L = No load

Figure 110. Effect of Capacitive Loads in High-Bias Mode



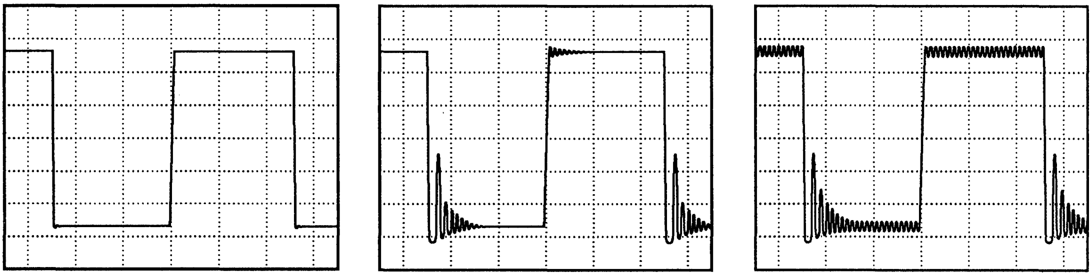
(a) C_L = 20 pF, R_L = No load

(a) C_L = 170 pF, R_L = No load

(a) C_L = 190 pF, R_L = No load

Figure 111. Effect of Capacitive Loads in Medium-Bias Mode

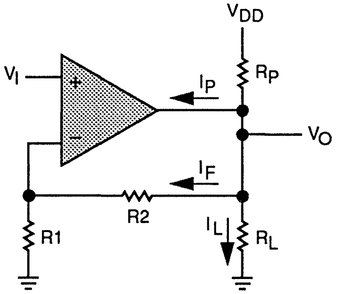
TYPICAL APPLICATION DATA



(a) C_L = 20 pF, R_L = No load (a) C_L = 260 pF, R_L = No load (a) C_L = 310 pF, R_L = No load

Figure 112. Effect of Capacitive Loads in Low-Bias Mode

Although the TLC271 possesses excellent high-level output voltage and current capability, methods are available for boosting this capability, if needed. The simplest method involves the use of a pullup resistor (R_P) connected from the output to the positive supply rail (see Figure 113). There are two disadvantages to the use of this circuit. First, the NMOS pulldown transistor, N4 (see equivalent schematic) must sink a comparatively large amount of current. In this circuit, N4 behaves like a linear resistor with an on-resistance between approximately 60 Ω and 180 Ω, depending on how hard the op amp input is driven. With very low values of R_P, a voltage offset from 0 V at the output will occur. Secondly, pullup resistor R_P acts as a drain load to N4 and the gain of the op amp is reduced at output voltage levels where N5 is not supplying the output current.

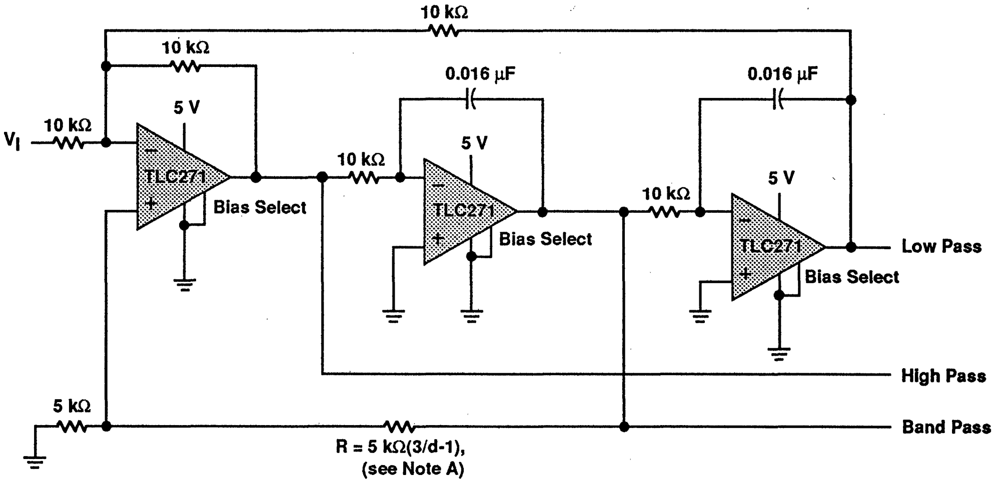


$$R_P = \frac{V_{DD} - V_O}{I_F + I_L + I_P}$$

I_P = Pull-up curent required by the op amp (typically 500 µA)

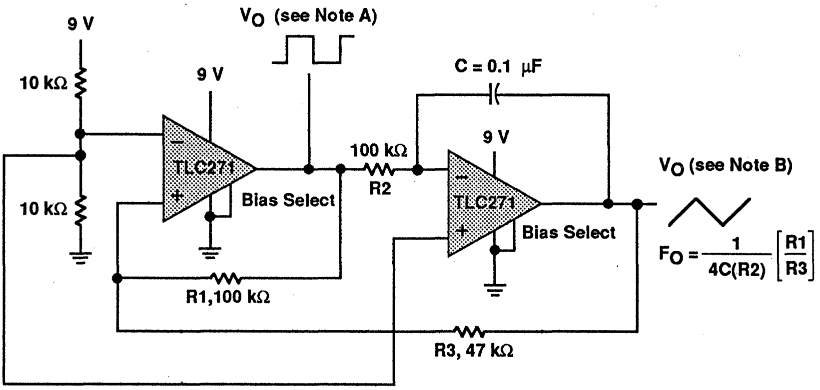
Figure 113. Resistive Pullup to Increase V_{OH}

TYPICAL APPLICATION DATA (HIGH-BIAS MODE)



NOTES: A. d = damping factor, 1/Q
B. Normalized to 10 kΩ and f_C = 1 kHz

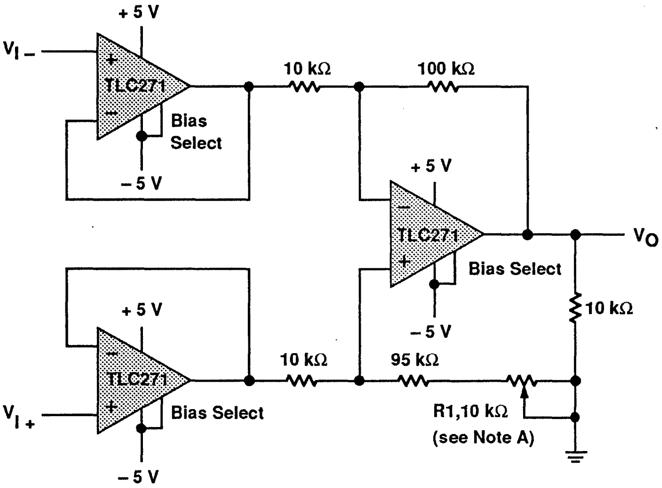
Figure 114. State Variable Filter



NOTES: A. V_{OPP} = 8 V
B. V_{OPP} = 4 V

Figure 115. Single-Supply Function Generator

TYPICAL APPLICATION DATA (HIGH-BIAS MODE)



NOTE A: CMRR adjustment (must be noninductive).

Figure 116. Low-Power Instrumentation Amplifier

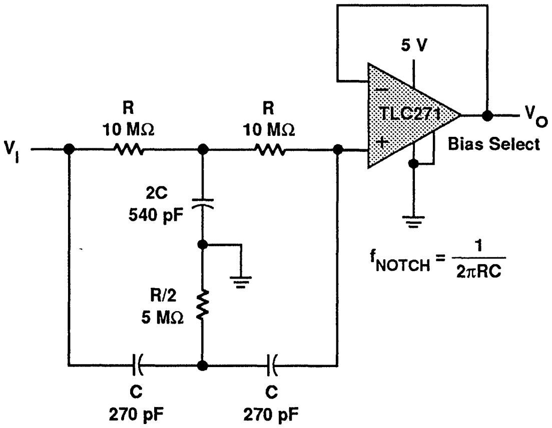
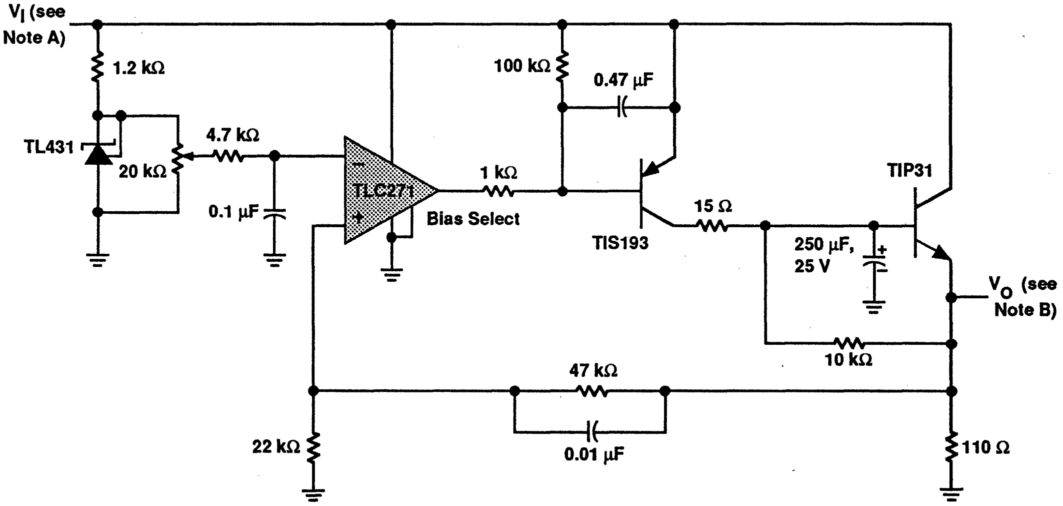


Figure 117. Single-Supply Twin-T Notch Filter

TYPICAL APPLICATION DATA (HIGH-BIAS MODE)



NOTES: A. V_I = 3.5 to 15 V
B. V_O = 2.0 V, 0 to 1 A

Figure 118. Logic-Array Power Supply

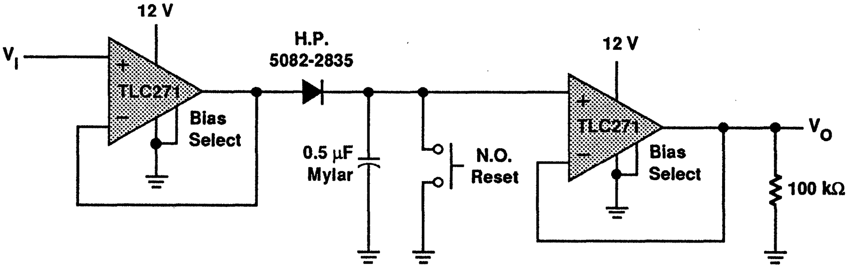


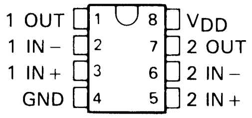
Figure 119. Positive-Peak Detector

TLC272, TLC272A, TLC272B, TLC277
LinCMOS™ PRECISION DUAL OPERATIONAL AMPLIFIERS

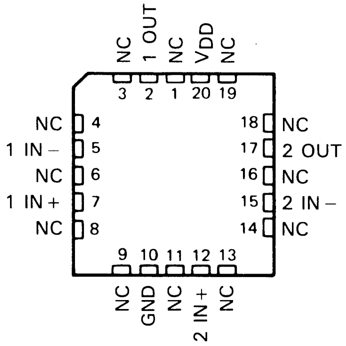
D3138, OCTOBER 1987–REVISED OCTOBER 1990

- **Trimmed Offset Voltage: TLC277 . . . 500 μV Max at 25 °C, V_{DD} = 5 V**
- **Input Offset Voltage Drift . . . Typically 0.1 μV/Month, Including the First 30 Days**
- **Wide Range of Supply Voltages Over Specified Temperature Range:**
  - **0 °C to 70 °C . . . 3 V to 16 V**
  - **−40 °C to 85 °C . . . 4 V to 16 V**
  - **−55 °C to 125 °C . . . 4 V to 16 V**
- **Single-Supply Operation**
- **Common-Mode Input Voltage Range Extends Below the Negative Rail (C-Suffix, I-Suffix types)**
- **Low Noise . . . Typically 25 nV/$\sqrt{Hz}$ at f = 1 kHz**
- **Output Voltage Range Includes Negative Rail**
- **High Input Impedance . . . 10^{12} Ω Typical**
- **ESD-Protection Circuitry**
- **Small-Outline Package Option Also Available in Tape and Reel**
- **Designed-In Latch-Up Immunity**

D, JG, OR P PACKAGE
(TOP VIEW)



FK PACKAGE
(TOP VIEW)



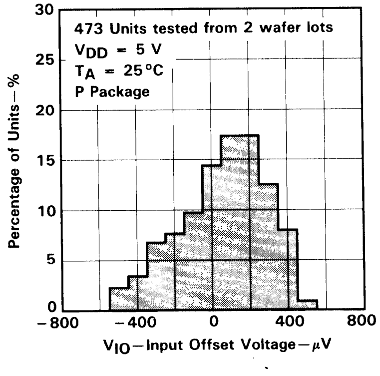
NC – No internal connection

AVAILABLE OPTIONS

T_A	V_{IO}max at 25 °C	PACKAGE			
		SMALL OUTLINE (D)	CHIP CARRIER (FK)	CERAMIC DIP (JG)	PLASTIC DIP (P)
0 °C to 70 °C	500 μV	TLC277CD	—	—	TLC277CP
	2 mV	TLC272BCD	—	—	TLC272BCP
	5 mV	TLC272ACD	—	—	TLC272ACP
	10 mV	TLC272CD	—	—	TLC272CP
−40 °C to 85 °C	500 μV	TLC277ID	—	—	TLC277IP
	2 mV	TLC272BID	—	—	TLC272BIP
	5 mV	TLC272AID	—	—	TLC272AIP
	10 mV	TLC272ID	—	—	TLC272IP
−55 °C to 125 °C	500 μV	TLC277MD	TLC277MFK	TLC277MJG	TLC277MP
	10 mV	TLC272MD	TLC272MFK	TLC272MJG	TLC272MP

The D package is available in tape and reel. Add R suffix to the device type, (e.g., TLC277CDR).

DISTRIBUTION OF TLC277
INPUT OFFSET VOLTAGE



LinCMOS is a trademark of Texas Instruments Incorporated

description

The TLC272 and TLC277 dual operational amplifiers combine a wide range of input offset voltage grades with low offset voltage drift, high input impedance, low noise, and speeds approaching that of general-purpose BiFET devices.

These devices use Texas Instruments silicon-gate LinCMOS™ technology, which provides offset voltage stability far exceeding the stability available with conventional metal-gate processes.

The extremely high input impedance, low bias currents, and high slew rates make these cost-effective devices ideal for applications which have previously been reserved for BiFET and NFET products. Four offset voltage grades are available (C-suffix and I-suffix types), ranging from the low-cost TLC272 (10 mV) to the high-precision TLC277 (500 μV). These advantages, in combination with good common-mode rejection and supply voltage rejection, make these devices a good choice for new state-of-the-art designs as well as for upgrading existing designs.

In general, many features associated with bipolar technology are available on LinCMOS™ operational amplifiers, without the power penalties of bipolar technology. General applications such as transducer interfacing, analog calculations, amplifier blocks, active filters, and signal buffering are easily designed with the TLC272 and TLC277. The devices also exhibit low voltage single-supply operation, making them ideally suited for remote and inaccessible battery-powered applications. The common-mode input voltage range includes the negative rail.

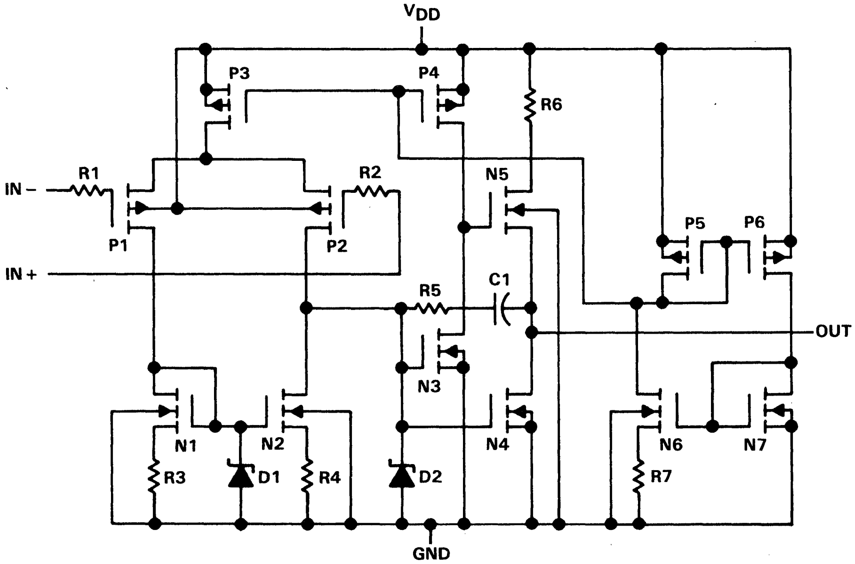
A wide range of packaging options is available, including small-outline and chip carrier versions for high-density system applications.

The device inputs and outputs are designed to withstand −100-mA surge currents without sustaining latch-up.

The TLC272 and TLC277 incorporate internal ESD-protection circuits that prevent functional failures at voltages up to 2000 V as tested under MIL-STD-883C, Method 3015.2; however, care should be exercised in handling these devices as exposure to ESD may result in the degradation of the device parametric performance.

C-suffix devices are characterized for operation from 0°C to 70°C. I-suffix devices are characterized for operation from −40°C to 85°C. M-suffix devices are characterized for operation over the full military temperature range of −55°C to 125°C.

equivalent schematic (each amplifier)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{DD} (see Note 1)	18 V
Differential input voltage (see Note 2)	$\pm V_{DD}$
Input voltage range, V_I (any input)	−0.3 V to V_{DD}
Input current, I_I	±5 mA
Output current, I_O (each output)	±30 mA
Total current into V_{DD} terminal	45 mA
Total current out of ground terminal	45 mA
Duration of short-circuit current at (or below) 25°C (see Note 3)	Unlimited
Continuous total dissipation	See Dissipation Rating Table
Operating free-air temperature, T_A: C-suffix	0°C to 70°C
I-suffix	−40°C to 85°C
M-suffix	−55°C to 125°C
Storage temperature range	−65°C to 150°C
Case temperature for 60 seconds: FK package	260°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D and P package	260°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: JG package	300°C

NOTES: 1. All voltage values, except differential voltages, are with respect to network ground.
2. Differential voltages are at the noninverting input with respect to the inverting input.
3. The output may be shorted to either supply. Temperature and/or supply voltages must be limited to ensure that the maximum dissipation rating is not exceeded (see application section).

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING	$T_A = 125°C$ POWER RATING
D	725 mW	5.8 mW/°C	464 mW	377 mW	
FK	1375 mW	11 mW/°C	880 mW	715 mW	275 mW
JG	1050 mW	8.4 mW/°C	672 mW	546 mW	210 mW
P	1000 mW	8.0 mW/°C	640 mW	520 mW	

recommended operating conditions

		C-SUFFIX			I-SUFFIX			M-SUFFIX			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{DD}		3		16	4		16	4		16	V
Common-mode input voltage, V_{IC}	$V_{DD} = 5$ V	−0.2		3.5	−0.2		3.5	0		3.5	V
	$V_{DD} = 10$ V	−0.2		8.5	−0.2		8.5	0		8.5	
Operating free-air temperature, T_A		0		70	−40		85	−55		125	°C

electrical characteristics at specified free-air temperature, V_{DD} = 5 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS	T_A†	MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	TLC272M	V_O = 1.4 V, V_{IC} = 0, R_S = 50 Ω, R_L = 10 kΩ	25°C		1.1	10	mV
				Full range			12	
		TLC277M	V_O = 1.4 V, V_{IC} = 0, R_S = 50 Ω, R_L = 10 kΩ	25°C		200	500	μV
				Full range			3750	
α_{VIO}	Average temperature coefficient of input offset voltage			25°C to 125°C		2.1		μV/°C
I_{IO}	Input offset current (see Note 4)		V_O = 2.5 V, V_{IC} = 2.5 V	25°C		0.1		pA
				125°C		1.4	15	nA
I_{IB}	Input bias current (see Note 4)		V_O = 2.5 V, V_{IC} = 2.5 V	25°C		0.6		pA
				125°C		9	35	nA
V_{ICR}	Common-mode input voltage range (see Note 5)			25°C	0 to 4	−0.3 to 4.2		V
				Full range	0 to 3.5			V
V_{OH}	High-level output voltage		V_{ID} = 100 mV, R_L = 10 kΩ	25°C	3.2	3.8		V
				−55°C	3	3.8		
				125°C	3	3.8		
V_{OL}	Low-level output voltage		V_{ID} = −100 mV, I_{OL} = 0	25°C		0	50	mV
				−55°C		0	50	
				125°C		0	50	
A_{VD}	Large-signal differential voltage amplification		V_O = 0.25 V to 2 V, R_L = 10 kΩ	25°C	5	23		V/mV
				−55°C	3.5	35		
				125°C	3.5	16		
CMRR	Common-mode rejection ratio		V_{IC} = V_{ICR} min	25°C	65	80		dB
				−55°C	60	81		
				125°C	60	84		
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)		V_{DD} = 5 V to 10 V, V_O = 1.4 V	25°C	65	95		dB
				−55°C	60	90		
				125°C	60	97		
I_{DD}	Supply current (two amplifiers)		V_O = 2.5 V, V_{IC} = 2.5 V, No load	25°C		1.4	3.2	mA
				−55°C		2	5	
				125°C		1	2.2	

† Full range is −55°C to 125°C.

NOTES: 4. The typical values of input bias current and input offset current below 5 pA were determined mathematically.
5. This range also applies to each input individually.

electrical characteristics at specified free-air temperature, V_{DD} = 10 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS		T_A†	MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	TLC272M	V_O = 1.4 V, R_S = 50 Ω,	V_{IC} = 0, R_L = 10 kΩ	25°C		1.1	10	mV
					Full range			12	
		TLC277M	V_O = 1.4 V, R_S = 50 Ω,	V_{IC} = 0, R_L = 10 kΩ	25°C		250	800	μV
					Full range			4300	
α_{VIO}	Average temperature coefficient of input offset voltage				25°C to 125°C		2.2		μV/°C
I_{IO}	Input offset current (see Note 4)		V_O = 5 V,	V_{IC} = 5 V	25°C		0.1		pA
					125°C		1.8	15	nA
I_{IB}	Input bias current (see Note 4)		V_O = 5 V,	V_{IC} = 5 V	25°C		0.7		pA
					125°C		10	35	nA
V_{ICR}	Common-mode input voltage range (see Note 5)				25°C	0 to 9	−0.3 to 9.2		V
					Full range	0 to 8.5			V
V_{OH}	High-level output voltage		V_{ID} = 100 mV,	R_L = 10 kΩ	25°C	8	8.5		V
					−55°C	7.8	8.5		
					125°C	7.8	8.4		
V_{OL}	Low-level output voltage		V_{ID} = −100 mV,	I_{OL} = 0	25°C		0	50	mV
					−55°C		0	50	
					125°C		0	50	
A_{VD}	Large-signal differential voltage amplification		V_O = 1 V to 6 V,	R_L = 10 kΩ	25°C	10	36		V/mV
					−55°C	7	50		
					125°C	7	27		
CMRR	Common-mode rejection ratio		$V_{IC} = V_{ICR}$ min		25°C	65	85		dB
					−55°C	60	87		
					125°C	60	86		
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)		V_{DD} = 5 V to 10 V,	V_O = 1.4 V	25°C	65	95		dB
					−55°C	60	90		
					125°C	60	97		
I_{DD}	Supply current (two amplifiers)		V_O = 5 V, No load	V_{IC} = 5 V,	25°C		1.9	4	mA
					−55°C		3	6	
					125°C		1.3	2.8	

† Full range is −55°C to 125°C.

NOTES: 4. The typical values of input bias current and input offset current below 5 pA were determined mathematically.
5. This range also applies to each input individually.

electrical characteristics at specified free-air temperature, V_{DD} = 5 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS		T_A†	MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	TLC272I	V_O = 1.4 V,	V_{IC} = 0,	25°C		1.1	10	mV
			R_S = 50 Ω,	R_L = 10 kΩ	Full range			13	
		TLC272AI	V_O = 1.4 V,	V_{IC} = 0,	25°C		0.9	5	
			R_S = 50 Ω,	R_L = 10 kΩ	Full range			7	
		TLC272BI	V_O = 1.4 V,	V_{IC} = 0,	25°C		230	2000	μV
			R_S = 50 Ω,	R_L = 10 kΩ	Full range			3500	
		TLC277I	V_O = 1.4 V,	V_{IC} = 0,	25°C		200	500	
			R_S = 50 Ω,	R_L = 10 kΩ	Full range			2000	
α_{VIO}	Average temperature coefficient of input offset voltage				25°C to 85°C		1.8		μV/°C
I_{IO}	Input offset current (see Note 4)		V_O = 2.5 V,	V_{IC} = 2.5 V	25°C		0.1		pA
					85°C		24	1000	
I_{IB}	Input bias current (see Note 4)		V_O = 2.5 V,	V_{IC} = 2.5 V	25°C		0.6		pA
					85°C		200	2000	
V_{ICR}	Common-mode input voltage range (see Note 5)				25°C	−0.2 to 4	−0.3 to 4.2		V
					Full range	−0.2 to 3.5			V
V_{OH}	High-level output voltage		V_{ID} = 100 mV,	R_L = 10 kΩ	25°C	3.2	3.8		V
					−40°C	3	3.8		
					85°C	3	3.8		
V_{OL}	Low-level output voltage		V_{ID} = −100 mV,	I_{OL} = 0	25°C		0	50	mV
					−40°C		0	50	
					85°C		0	50	
A_{VD}	Large-signal differential voltage amplification		V_O = 0.25 V to 2 V,	R_L = 10 kΩ	25°C	5	23		V/mV
					−40°C	3.5	32		
					85°C	3.5	19		
CMRR	Common-mode rejection ratio		V_{IC} = V_{ICR} min		25°C	65	80		dB
					−40°C	60	81		
					85°C	60	86		
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)		V_{DD} = 5 V to 10 V,	V_O = 1.4 V	25°C	65	95		dB
					−40°C	60	92		
					85°C	60	96		
I_{DD}	Supply current (two amplifiers)		V_O = 2.5 V, No load	V_{IC} = 2.5 V,	25°C		1.4	3.2	mA
					−40°C		1.9	4.4	
					85°C		1.1	2.4	

† Full range is −40°C to 85°C.

NOTES: 4. The typical values of input bias current and input offset current below 5 pA were determined mathematically.
5. This range also applies to each input individually.

electrical characteristics at specified free-air temperature, V_{DD} = 10 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS		T_A†	MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	TLC272I	V_O = 1.4 V, R_S = 50 Ω,	V_{IC} = 0, R_L = 10 kΩ	25°C		1.1	10	mV
					Full range			13	
		TLC272AI	V_O = 1.4 V, R_S = 50 Ω,	V_{IC} = 0, R_L = 10 kΩ	25°C		0.9	5	
					Full range			7	
		TLC272BI	V_O = 1.4 V, R_S = 50 Ω,	V_{IC} = 0, R_L = 10 kΩ	25°C		290	2000	µV
					Full range			3500	
		TLC277I	V_O = 1.4 V, R_S = 50 Ω,	V_{IC} = 0, R_L = 10 kΩ	25°C		250	800	
					Full range			2900	
α_{VIO}	Average temperature coefficient of input offset voltage				25°C to 85°C		2		µV/°C
I_{IO}	Input offset current (see Note 4)		V_O = 5 V,	V_{IC} = 5 V	25°C		0.1		pA
					85°C		26	1000	
I_{IB}	Input bias current (see Note 4)		V_O = 5 V,	V_{IC} = 5 V	25°C		0.7		pA
					85°C		220	2000	
V_{ICR}	Common-mode input voltage range (see Note 5)				25°C	−0.2 to 9	−0.3 to 9.2		V
					Full range	−0.2 to 8.5			V
V_{OH}	High-level output voltage		V_{ID} = 100 mV,	R_L = 10 kΩ	25°C	8	8.5		V
					−40°C	7.8	8.5		
					85°C	7.8	8.5		
V_{OL}	Low-level output voltage		V_{ID} = −100 mV,	I_{OL} = 0	25°C		0	50	mV
					−40°C		0	50	
					85°C		0	50	
A_{VD}	Large-signal differential voltage amplification		V_O = 1 V to 6 V,	R_L = 10 kΩ	25°C	10	36		V/mV
					−40°C	7	46		
					85°C	7	31		
CMRR	Common-mode rejection ratio		V_{IC} = V_{ICR} min		25°C	65	85		dB
					−40°C	60	87		
					85°C	60	88		
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)		V_{DD} = 5 V to 10 V,	V_O = 1.4 V	25°C	65	95		dB
					−40°C	60	92		
					85°C	60	96		
I_{DD}	Supply current (two amplifiers)		V_O = 5 V, No load	V_{IC} = 5 V,	25°C		1.9	4	mA
					−40°C		2.8	5	
					85°C		1.5	3.2	

† Full range is −40°C to 85°C.

NOTES: 4. The typical values of input bias current and input offset current below 5 pA were determined mathematically.
5. This range also applies to each input individually.

electrical characteristics at specified free-air temperature, V_{DD} = 5 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS		T_A†	MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	TLC272C	V_O = 1.4 V, R_S = 50 Ω,	V_{IC} = 0, R_L = 10 kΩ	25°C		1.1	10	mV
					Full range			12	
		TLC272AC	V_O = 1.4 V, R_S = 50 Ω,	V_{IC} = 0, R_L = 10 kΩ	25°C		0.9	5	
					Full range			6.5	
		TLC272BC	V_O = 1.4 V, R_S = 50 Ω,	V_{IC} = 0, R_L = 10 kΩ	25°C		230	2000	µV
					Full range			3000	
		TLC277C	V_O = 1.4 V, R_S = 50 Ω,	V_{IC} = 0, R_L = 10 kΩ	25°C		200	500	
					Full range			1500	
α_{VIO}	Average temperature coefficient of input offset voltage				25°C to 70°C		1.8		µV/°C
I_{IO}	Input offset current (see Note 4)		V_O = 2.5 V,	V_{IC} = 2.5 V	25°C		0.1		pA
					70°C		7	300	
I_{IB}	Input bias current (see Note 4)		V_O = 2.5 V,	V_{IC} = 2.5 V	25°C		0.6		pA
					70°C		40	600	
V_{ICR}	Common-mode input voltage range (see Note 5)				25°C	−0.2 to 4	−0.3 to 4.2		V
					Full range	−0.2 to 3.5			V
V_{OH}	High-level output voltage		V_{ID} = 100 mV,	R_L = 10 kΩ	25°C	3.2	3.8		V
					0°C	3	3.8		
					70°C	3	3.8		
V_{OL}	Low-level output voltage		V_{ID} = −100 mV,	I_{OL} = 0	25°C		0	50	mV
					0°C		0	50	
					70°C		0	50	
A_{VD}	Large-signal differential voltage amplification		V_O = 0.25 V to 2 V,	R_L = 10 kΩ	25°C	5	23		V/mV
					0°C	4	27		
					70°C	4	20		
CMRR	Common-mode rejection ratio		V_{IC} = V_{ICR} min		25°C	65	80		dB
					0°C	60	84		
					70°C	60	85		
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)		V_{DD} = 5 V to 10 V,	V_O = 1.4 V	25°C	65	95		dB
					0°C	60	94		
					70°C	60	96		
I_{DD}	Supply current (two amplifiers)		V_O = 2.5 V, No load	V_{IC} = 2.5 V,	25°C		1.4	3.2	mA
					0°C		1.6	3.6	
					70°C		1.2	2.6	

† Full range is 0°C to 70°C.

NOTES: 4. The typical values of input bias current and input offset current below 5 pA were determined mathematically.
5. This range also applies to each input individually.

electrical characteristics at specified free-air temperature, V_{DD} = 10 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS		T_A†	MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	TLC272C	V_O = 1.4 V, R_S = 50 Ω,	V_{IC} = 0, R_L = 10 kΩ	25°C		1.1	10	mV
					Full range			12	
		TLC272AC	V_O = 1.4 V, R_S = 50 Ω,	V_{IC} = 0, R_L = 10 kΩ	25°C		0.9	5	
					Full range			6.5	
		TLC272BC	V_O = 1.4 V, R_S = 50 Ω,	V_{IC} = 0, R_L = 10 kΩ	25°C		290	2000	μV
					Full range			3000	
		TLC277C	V_O = 1.4 V, R_S = 50 Ω,	V_{IC} = 0, R_L = 10 kΩ	25°C		250	800	
					Full range			1900	
α_{VIO}	Average temperature coefficient of input offset voltage				25°C to 70°C		2		μV/°C
I_{IO}	Input offset current (see Note 4)		V_O = 5 V,	V_{IC} = 5 V	25°C		0.1		pA
					70°C		7	300	
I_{IB}	Input bias current (see Note 4)		V_O = 5 V,	V_{IC} = 5 V	25°C		0.7		pA
					70°C		50	600	
V_{ICR}	Common-mode input voltage range (see Note 5)				25°C	−0.2 to 9	−0.3 to 9.2		V
					Full range	−0.2 to 8.5			V
V_{OH}	High-level output voltage		V_{ID} = 100 mV,	R_L = 10 kΩ	25°C	8	8.5		V
					0°C	7.8	8.5		
					70°C	7.8	8.4		
V_{OL}	Low-level output voltage		V_{ID} = −100 mV,	I_{OL} = 0	25°C		0	50	mV
					0°C		0	50	
					70°C		0	50	
A_{VD}	Large-signal differential voltage amplification		V_O = 1 V to 6 V,	R_L = 10 kΩ	25°C	10	36		V/mV
					0°C	7.5	42		
					70°C	7.5	32		
CMRR	Common-mode rejection ratio		V_{IC} = V_{ICR} min		25°C	65	85		dB
					0°C	60	88		
					70°C	60	88		
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)		V_{DD} = 5 V to 10 V,	V_O = 1.4 V	25°C	65	95		dB
					0°C	60	94		
					70°C	60	96		
I_{DD}	Supply current (two amplifiers)		V_O = 5 V, No load	V_{IC} = 5 V,	25°C		1.9	4	mA
					0°C		2.3	4.4	
					70°C		1.6	3.4	

† Full range is 0°C to 70°C.

NOTES: 4. The typical values of input bias current and input offset current below 5 pA were determined mathematically.
5. This range also applies to each input individually.

operating characteristics, V_{DD} = 5 V

PARAMETER		TEST CONDITIONS		T_A	MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain	R_L = 10 kΩ, C_L = 20 pF, See Figure 1	V_{IPP} = 1 V	25°C		3.6		V/μs
				−55°C		4.7		
				125°C		2.3		
			V_{IPP} = 2.5 V	25°C		2.9		
				−55°C		3.7		
				125°C		2		
V_n	Equivalent input noise voltage	f = 1 kHz, See Figure 2	R_S = 100 Ω,	25°C		25		nV/√Hz
B_{OM}	Maximum output swing bandwidth	V_O = V_{OH}, R_L = 10 kΩ,	C_L = 20 pF, See Figure 1	25°C		320		kHz
				−55°C		400		
				125°C		230		
B_1	Unity-gain bandwidth	V_i = 10 mV, See Figure 3	C_L = 20 pF,	25°C		1.7		MHz
				−55°C		2.9		
				125°C		1.1		
ϕ_m	Phase margin	V_i = 10 mV, C_L = 20 pF,	f = B_1, See Figure 3	25°C		46°		
				−55°C		49°		
				125°C		41°		

operating characteristics, V_{DD} = 10 V

PARAMETER		TEST CONDITIONS		T_A	MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain	R_L = 10 kΩ, C_L = 20 pF, See Figure 1	V_{IPP} = 1 V	25°C		5.3		V/μs
				−55°C		7.1		
				125°C		3.1		
			V_{IPP} = 5.5 V	25°C		4.6		
				−55°C		6.1		
				125°C		2.7		
V_n	Equivalent input noise voltage	f = 1 kHz, See Figure 2	R_S = 100 Ω,	25°C		25		nV/√Hz
B_{OM}	Maximum output swing bandwidth	V_O = V_{OH}, R_L = 10 kΩ,	C_L = 20 pF, See Figure 1	25°C		200		kHz
				−55°C		280		
				125°C		110		
B_1	Unity-gain bandwidth	V_i = 10 mV, See Figure 3	C_L = 20 pF,	25°C		2.2		MHz
				−55°C		3.4		
				125°C		1.6		
ϕ_m	Phase margin	V_i = 10 mV, C_L = 20 pF,	f = B_1, See Figure 3	25°C		49°		
				−55°C		52°		
				125°C		44°		

operating characteristics, V_{DD} = 5 V

PARAMETER		TEST CONDITIONS		T_A	MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain	R_L = 10 kΩ, C_L = 20 pF, See Figure 1	V_{IPP} = 1 V	25°C		3.6		V/μs
				−40°C		4.5		
				85°C		2.8		
			V_{IPP} = 2.5 V	25°C		2.9		
				−40°C		3.5		
				85°C		2.3		
V_n	Equivalent input noise voltage	f = 1 kHz, See Figure 2	R_S = 100 Ω,	25°C		25		nV/$\sqrt{Hz}$
B_{OM}	Maximum output swing bandwidth	V_O = V_{OH}, R_L = 10 kΩ,	C_L = 20 pF, See Figure 1	25°C		320		kHz
				−40°C		380		
				85°C		250		
B_1	Unity-gain bandwidth	V_i = 10 mV, See Figure 3	C_L = 20 pF,	25°C		1.7		MHz
				−40°C		2.6		
				85°C		1.2		
ϕ_m	Phase margin	V_i = 10 mV, C_L = 20 pF,	f = B_1, See Figure 3	25°C		46°		
				−40°C		49°		
				85°C		43°		

operating characteristics, V_{DD} = 10 V

PARAMETER		TEST CONDITIONS		T_A	MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain	R_L = 10 kΩ, C_L = 20 pF, See Figure 1	V_{IPP} = 1 V	25°C		5.3		V/μs
				−40°C		6.8		
				85°C		4		
			V_{IPP} = 5.5 V	25°C		4.6		
				−40°C		5.8		
				85°C		3.5		
V_n	Equivalent input noise voltage	f = 1 kHz, See Figure 2	R_S = 100 Ω,	25°C		25		nV/$\sqrt{Hz}$
B_{OM}	Maximum output swing bandwidth	V_O = V_{OH}, R_L = 10 kΩ,	C_L = 20 pF, See Figure 1	25°C		200		kHz
				−40°C		260		
				85°C		130		
B_1	Unity-gain bandwidth	V_i = 10 mV, See Figure 3	C_L = 20 pF,	25°C		2.2		MHz
				−40°C		3.1		
				85°C		1.7		
ϕ_m	Phase margin	V_i = 10 mV, C_L = 20 pF,	f = B_1, See Figure 3	25°C		49°		
				−40°C		52°		
				85°C		46°		

operating characteristics, V_{DD} = 5 V

PARAMETER		TEST CONDITIONS		T_A	MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain	R_L = 10 kΩ, C_L = 20 pF, See Figure 1	V_{IPP} = 1 V	25°C		3.6		V/µs
				0°C		4		
				70°C		3		
			V_{IPP} = 2.5 V	25°C		2.9		
				0°C		3.1		
				70°C		2.5		
V_n	Equivalent input noise voltage	f = 1 kHz, See Figure 2	R_S = 100 Ω,	25°C		25		$\text{nV}/\sqrt{\text{Hz}}$
B_{OM}	Maximum output swing bandwidth	$V_O = V_{OH}$, R_L = 10 kΩ,	C_L = 20 pF, See Figure 1	25°C		320		kHz
				0°C		340		
				70°C		260		
B_1	Unity-gain bandwidth	V_i = 10 mV, See Figure 3	C_L = 20 pF,	25°C		1.7		MHz
				0°C		2		
				70°C		1.3		
ϕ_m	Phase margin	V_i = 10 mV, C_L = 20 pF,	f = B_1, See Figure 3	25°C		46°		
				0°C		47°		
				70°C		43°		

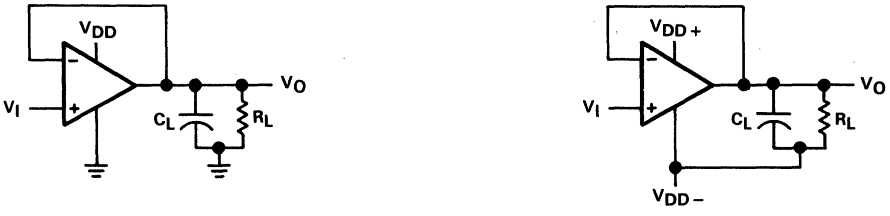
operating characteristics, V_{DD} = 10 V

PARAMETER		TEST CONDITIONS		T_A	MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain	R_L = 10 kΩ, C_L = 20 pF, See Figure 1	V_{IPP} = 1 V	25°C		5.3		V/µs
				0°C		5.9		
				70°C		4.3		
			V_{IPP} = 5.5 V	25°C		4.6		
				0°C		5.1		
				70°C		3.8		
V_n	Equivalent input noise voltage	f = 1 kHz, See Figure 2	R_S = 100 Ω,	25°C		25		$\text{nV}/\sqrt{\text{Hz}}$
B_{OM}	Maximum output swing bandwidth	$V_O = V_{OH}$, R_L = 10 kΩ,	C_L = 20 pF, See Figure 1	25°C		200		kHz
				0°C		220		
				70°C		140		
B_1	Unity-gain bandwidth	V_i = 10 mV, See Figure 3	C_L = 20 pF,	25°C		2.2		MHz
				0°C		2.5		
				70°C		1.8		
ϕ_m	Phase margin	V_i = 10 mV, C_L = 20 pF,	f = B_1, See Figure 3	25°C		49°		
				0°C		50°		
				70°C		46°		

PARAMETER MEASUREMENT INFORMATION

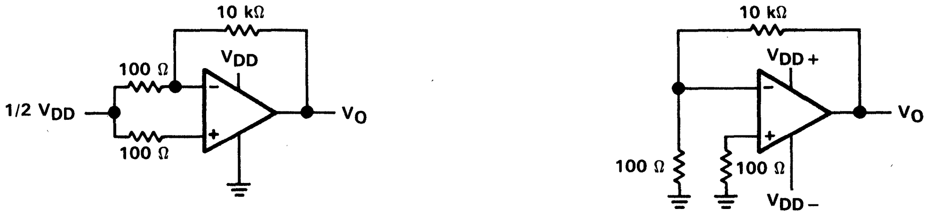
single-supply versus split-supply test circuits

Because the TLC272 and TLC277 are optimized for single-supply operation, circuit configurations used for the various tests often present some inconvenience since the input signal, in many cases, must be offset from ground. This inconvenience can be avoided by testing the device with split supplies and the output load tied to the negative rail. A comparison of single-supply versus split-supply test circuits is shown below. The use of either circuit will give the same result.



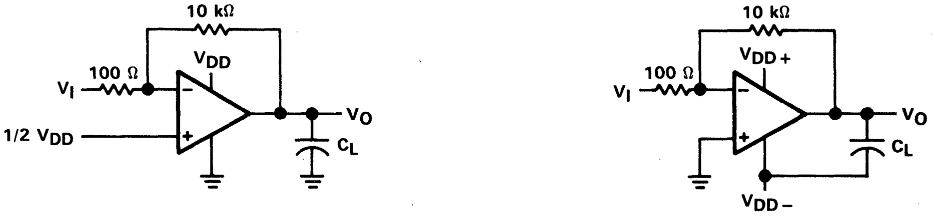
(a) Single-Supply
(b) Split-Supply

FIGURE 1. UNITY-GAIN AMPLIFIER



(a) Single-Supply
(b) Split-Supply

FIGURE 2. NOISE TEST CIRCUIT



(a) Single-Supply
(b) Split-Supply

FIGURE 3. GAIN-OF-100 INVERTING AMPLIFIER

PARAMETER MEASUREMENT INFORMATION

input bias current

Because of the high input impedance of the TLC272 and TLC277 op amps, attempts to measure the input bias current can result in erroneous readings. The bias current at normal room ambient temperature is typically less than 1 pA, a value that is easily exceeded by leakages on the test socket. Two suggestions are offered to avoid erroneous measurements:

1. Isolate the device from other potential leakage sources. Use a grounded shield around and between the device inputs (see Figure 4). Leakages that would otherwise flow to the inputs will be shunted away.
2. Compensate for the leakage of the test socket by actually performing an input bias current test (using a picoammeter) with no device in the test socket. The actual input bias current can then be calculated by subtracting the "open-socket" leakage readings from the readings obtained with a device in the test socket.

   One word of caution . . . many automatic testers as well as some bench-top op amp testers use the servo-loop technique with a resistor in series with the device input to measure the input bias current (the voltage drop across the series resistor is measured and the bias current is calculated). This method requires that a device be inserted into the test socket to obtain a correct reading; therefore, an "open-socket" reading is not feasible using this method.

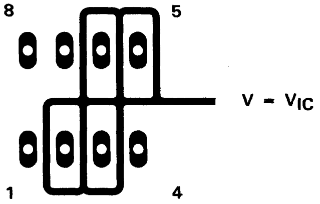


FIGURE 4. ISOLATION METAL AROUND DEVICE INPUTS
(JG AND P DUAL-IN-LINE-PACKAGE)

low-level output voltage

To obtain low-supply-voltage operation, some compromise was necessary in the input stage. This compromise results in the device low-level output being dependent on both the common-mode input voltage level as well as the differential input voltage level. When attempting to correlate low-level output readings with those quoted in the electrical specifications, these two conditions should be observed. If conditions other than these are to be used, please refer to Figures 14 through 19 in the Typical Characteristics of this data sheet.

input offset voltage temperature coefficient

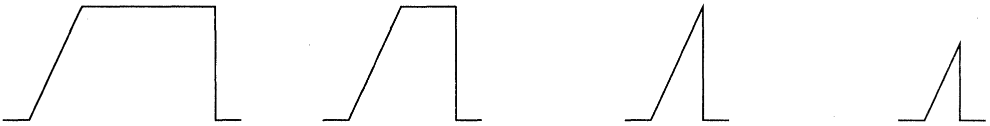
Erroneous readings often result from attempts to measure temperature coefficient of input offset voltage. This parameter is actually a calculation using input offset voltage measurements obtained at two different temperatures. When one (or both) of the temperatures is below freezing, moisture can collect on both the device and the test socket. This moisture will result in leakage and contact resistance, which can cause erroneous input offset voltage readings. The isolation techniques previously mentioned have no effect on the leakage since the moisture also covers the isolation metal itself, thereby rendering it useless. It is suggested that these measurements be performed at temperatures above freezing to minimize error.

PARAMETER MEASUREMENT INFORMATION

full-power response

Full-power response, the frequency above which the op amp slew rate limits the output voltage swing, is often specified two ways: full-linear response and full-peak response. The full-linear response is generally measured by monitoring the distortion level of the output while increasing the frequency of a sinusoidal input signal until the maximum frequency is found above which the output contains significant distortion. The full-peak response is defined as the maximum output frequency, without regard to distortion, above which full peak-to-peak output swing cannot be maintained.

Because there is no industry-wide accepted value for ''significant'' distortion, the full-peak response is specified in this data sheet and is measured using the circuit of Figure 1. The initial setup involves the use of a sinusoidal input to determine the maximum peak-to-peak output of the device (the amplitude of the sinusoidal wave is increased until clipping occurs). The sinusoidal wave is then replaced with a square wave of the same amplitude. The frequency is then increased until the maximum peak-to-peak output can no longer be maintained (Figure 5). A square wave is used to allow a more accurate determination of the point at which the maximum peak-to-peak output is reached.



(a) $f = 1$ kHz (b) $B_{OM} > f > 1$ kHz (c) $f = B_{OM}$ (d) $f > B_{OM}$

FIGURE 5. FULL-POWER-RESPONSE OUTPUT SIGNAL

test time

Inadequate test time is a frequent problem, especially when testing CMOS devices in a high-volume, short-test-time environment. Internal capacitances are inherently higher in CMOS than in bipolar and BiFET devices and require longer test times than their bipolar and BiFET counterparts. The problem becomes more pronounced with reduced supply levels and lower temperatures.

TYPICAL CHARACTERISTICS

DISTRIBUTION OF TLC272
INPUT OFFSET VOLTAGE

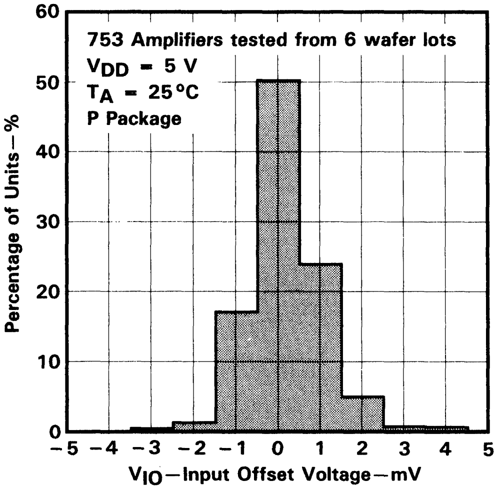


FIGURE 6

DISTRIBUTION OF TLC272
INPUT OFFSET VOLTAGE

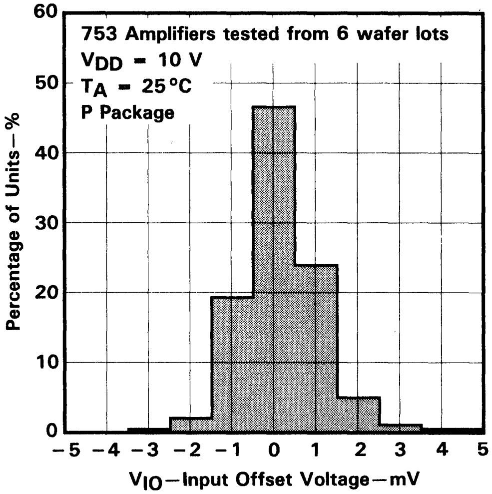


FIGURE 7

DISTRIBUTION OF TLC272 AND TLC277
INPUT OFFSET VOLTAGE
TEMPERATURE COEFFICIENT

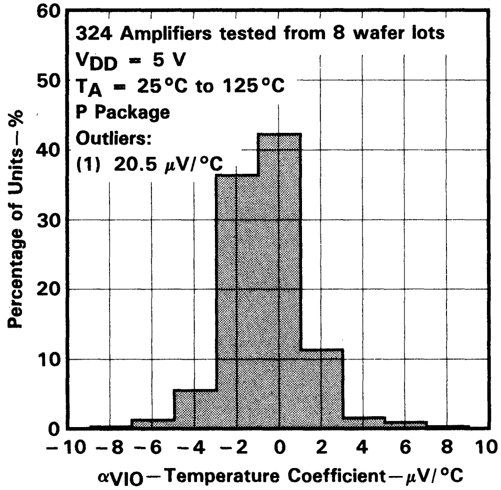


FIGURE 8

DISTRIBUTION OF TLC272 AND TLC277
INPUT OFFSET VOLTAGE
TEMPERATURE COEFFICIENT

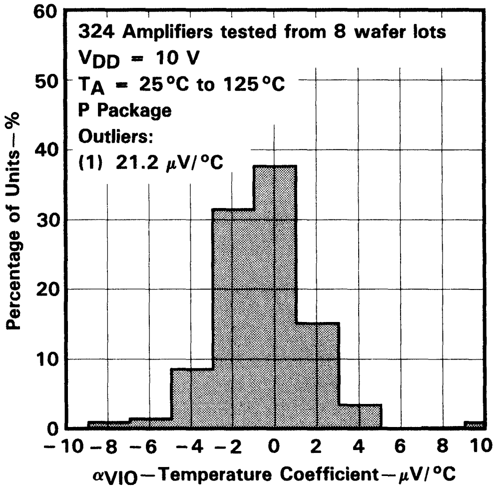


FIGURE 9

TYPICAL CHARACTERISTICS†

HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

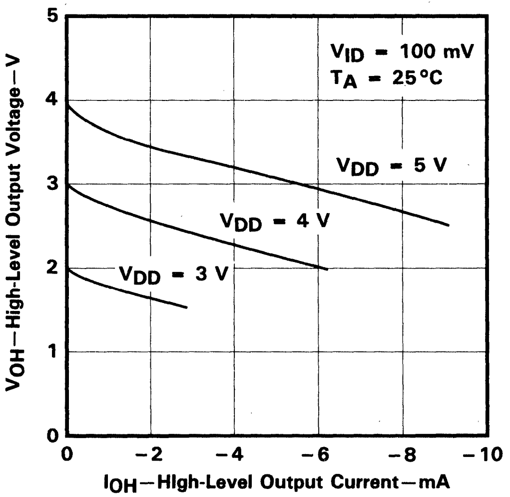


FIGURE 10

HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

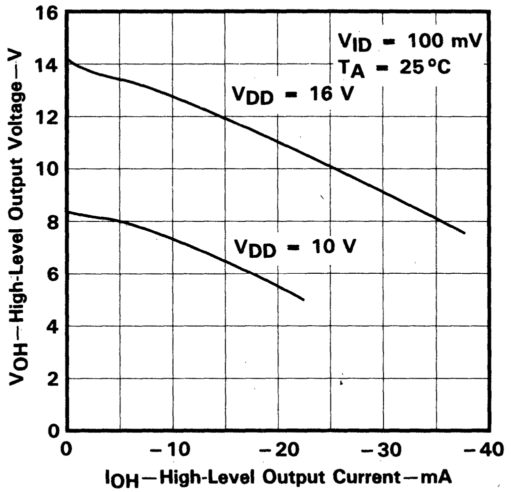


FIGURE 11

HIGH-LEVEL OUTPUT VOLTAGE
vs
SUPPLY VOLTAGE

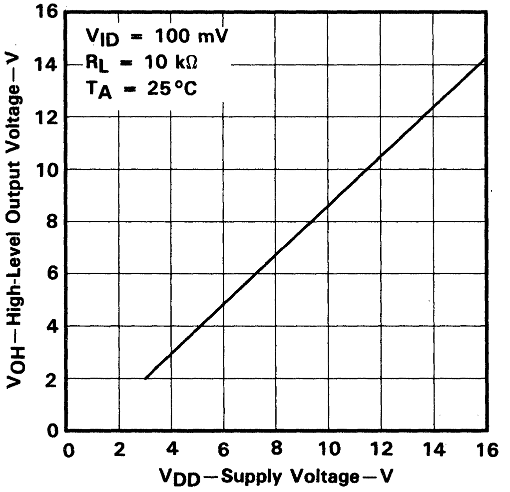


FIGURE 12

HIGH-LEVEL OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

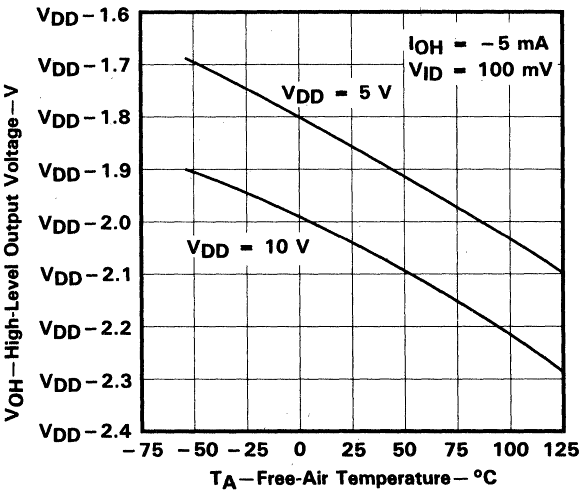


FIGURE 13

---

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

LOW-LEVEL OUTPUT VOLTAGE
vs
COMMON-MODE INPUT VOLTAGE

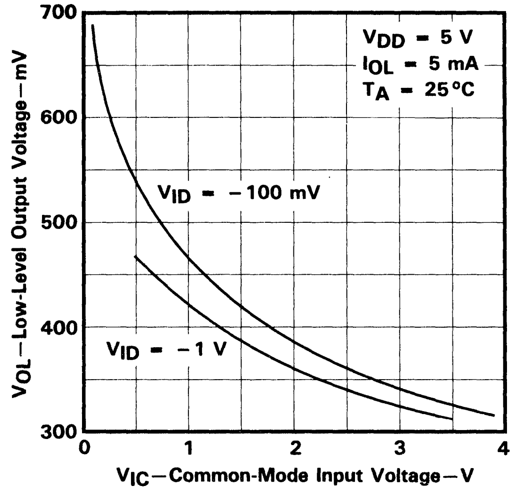


FIGURE 14

LOW-LEVEL OUTPUT VOLTAGE
vs
COMMON-MODE INPUT VOLTAGE

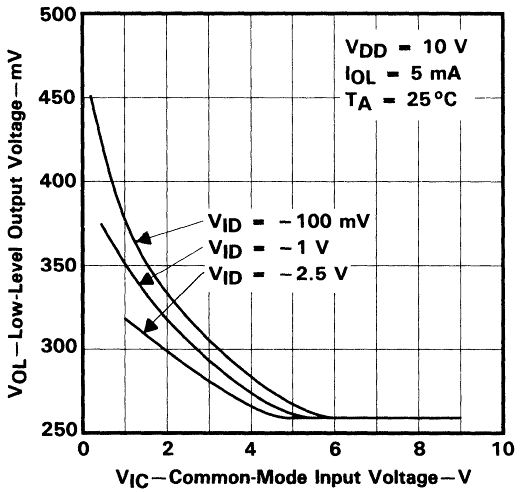


FIGURE 15

LOW-LEVEL OUTPUT VOLTAGE
vs
DIFFERENTIAL INPUT VOLTAGE

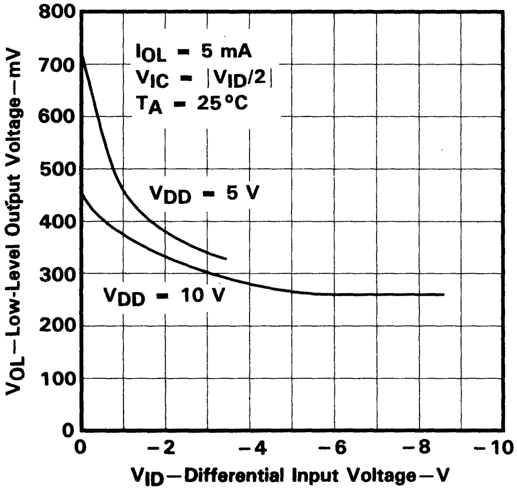


FIGURE 16

LOW-LEVEL OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

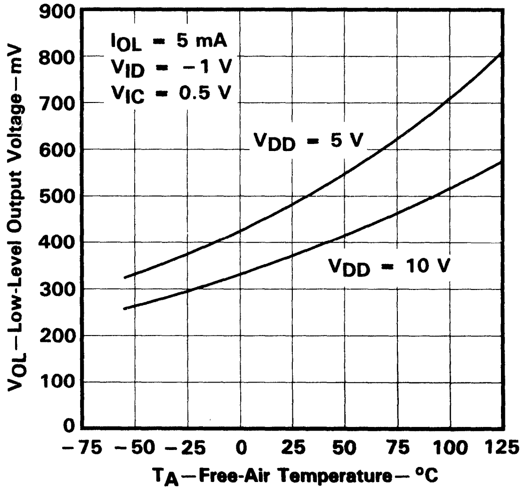


FIGURE 17

---

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

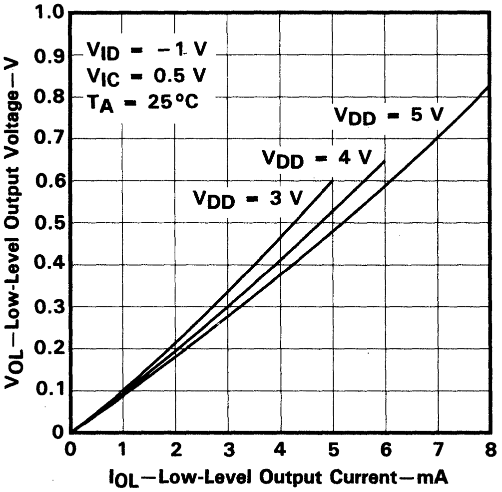


FIGURE 18

LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

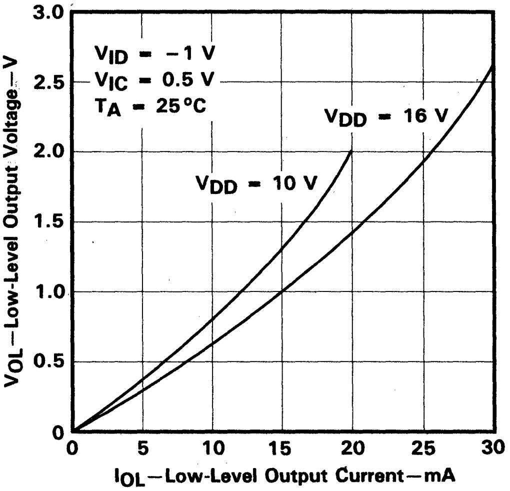


FIGURE 19

LARGE-SIGNAL
DIFFERENTIAL VOLTAGE AMPLIFICATION
vs
SUPPLY VOLTAGE

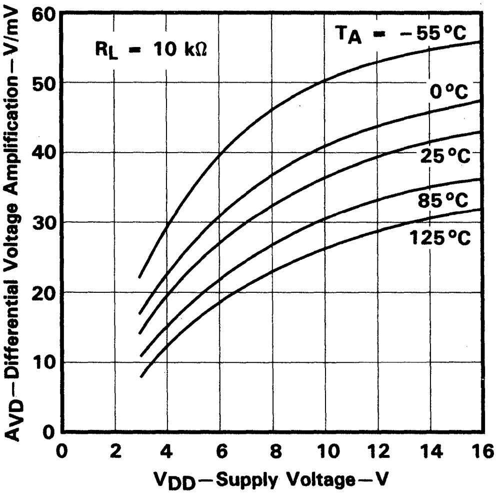


FIGURE 20

LARGE-SIGNAL
DIFFERENTIAL VOLTAGE AMPLIFICATION
vs
FREE-AIR TEMPERATURE

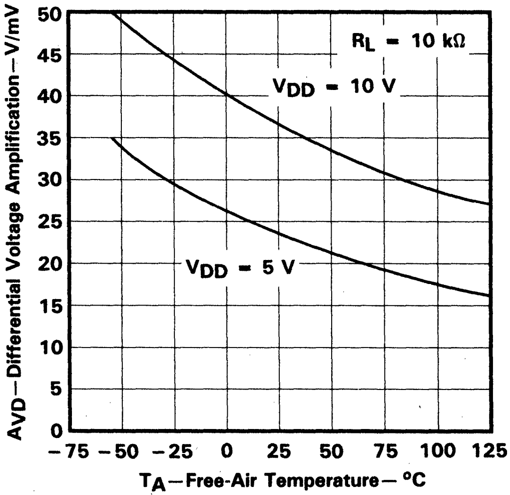


FIGURE 21

---

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

INPUT BIAS CURRENT AND INPUT OFFSET CURRENT
vs
FREE-AIR TEMPERATURE

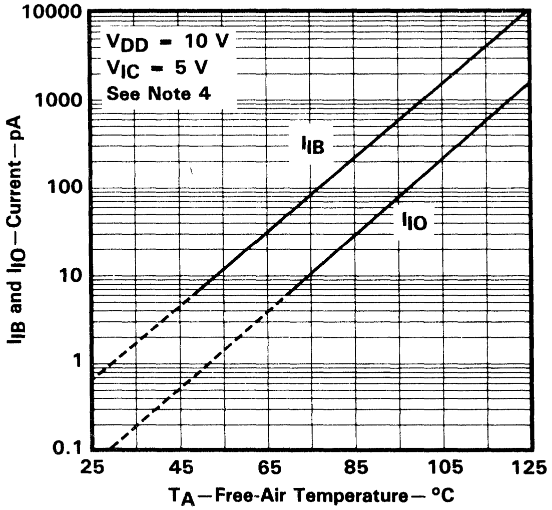


FIGURE 22

COMMON-MODE
INPUT VOLTAGE POSITIVE LIMIT
vs
SUPPLY VOLTAGE

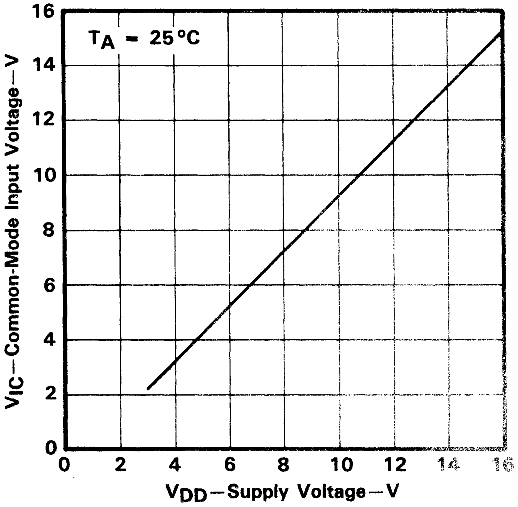


FIGURE 23

SUPPLY CURRENT
vs
SUPPLY VOLTAGE

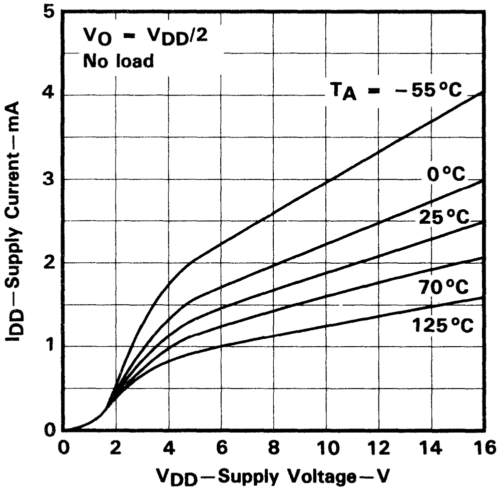


FIGURE 24

SUPPLY CURRENT
vs
FREE-AIR TEMPERATURE

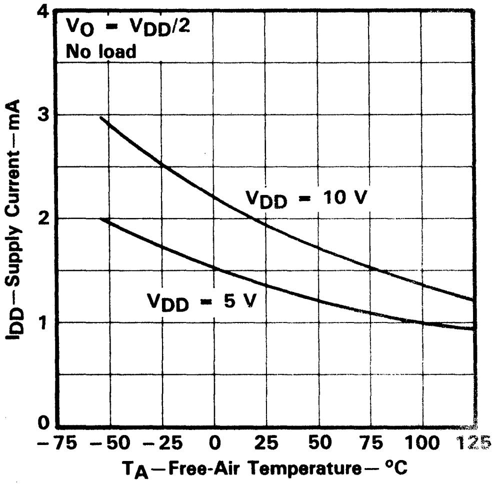


FIGURE 25

---

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

NOTE 4: The typical values of input bias current and input offset current below 5 pA were determined mathematically.

TYPICAL CHARACTERISTICS†

SLEW RATE
vs
SUPPLY VOLTAGE

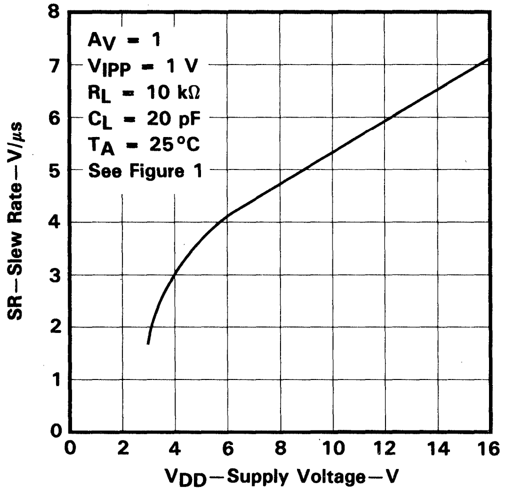


FIGURE 26

SLEW RATE
vs
FREE-AIR TEMPERATURE

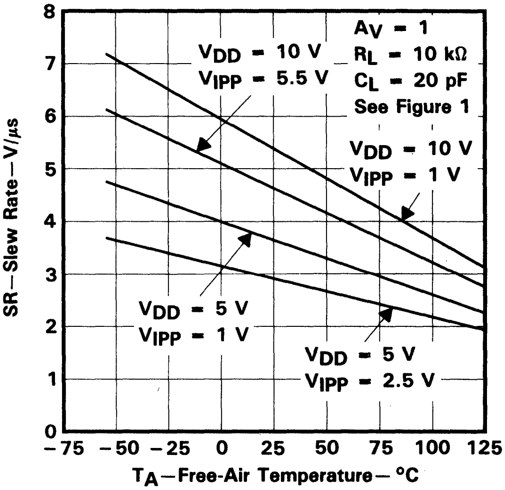


FIGURE 27

NORMALIZED SLEW RATE
vs
FREE-AIR TEMPERATURE

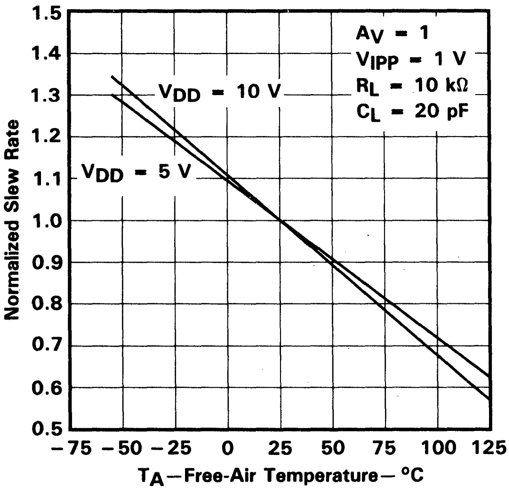


FIGURE 28

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE
vs
FREQUENCY

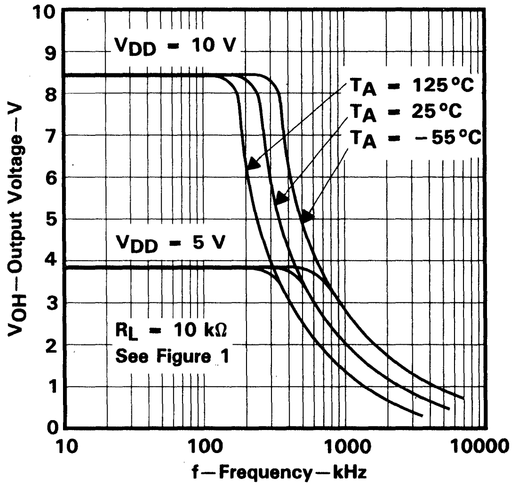


FIGURE 29

---

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

UNITY-GAIN BANDWIDTH
vs
FREE-AIR TEMPERATURE

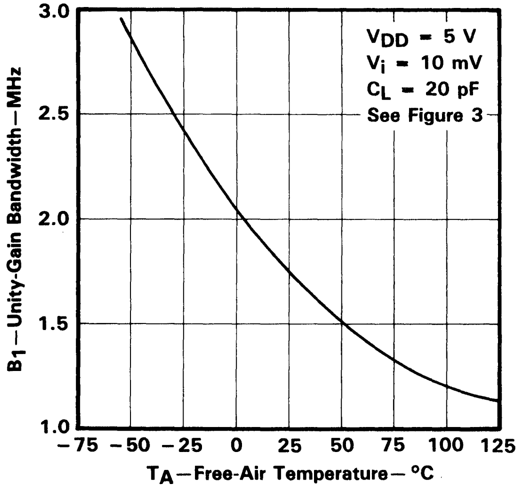


FIGURE 30

UNITY-GAIN BANDWIDTH
vs
SUPPLY VOLTAGE

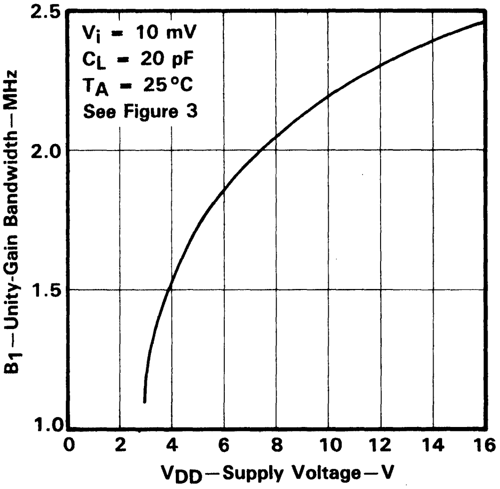


FIGURE 31

LARGE-SIGNAL DIFFERENTIAL VOLTAGE
AMPLIFICATION AND PHASE SHIFT
vs
FREQUENCY

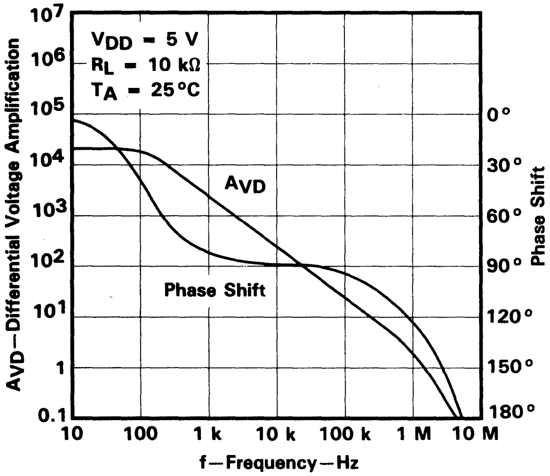


FIGURE 32

LARGE-SIGNAL DIFFERENTIAL VOLTAGE
AMPLIFICATION AND PHASE SHIFT
vs
FREQUENCY

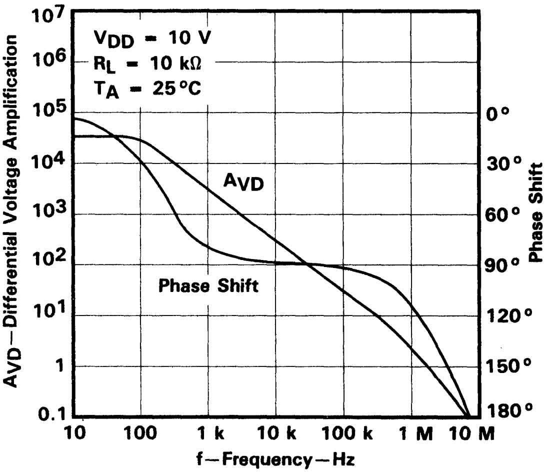
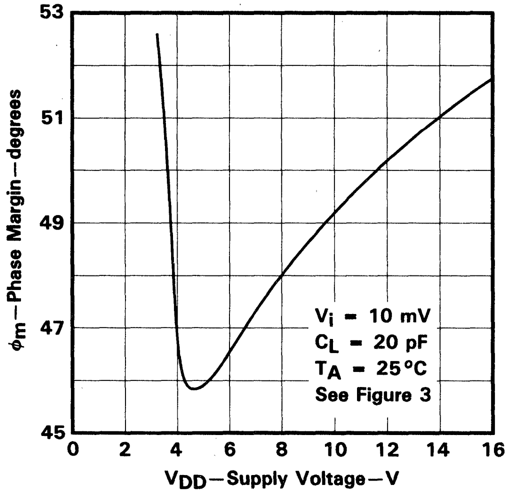


FIGURE 33

---

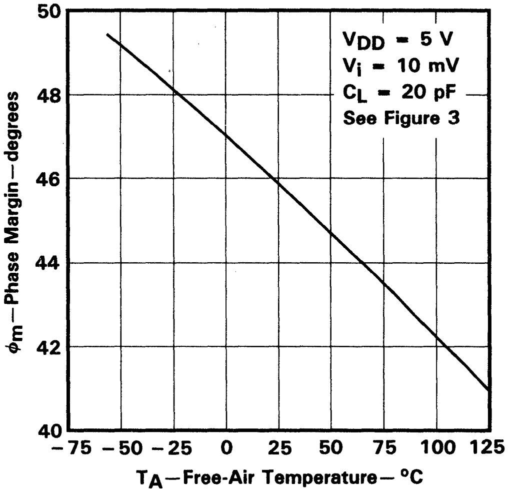
†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS[†]



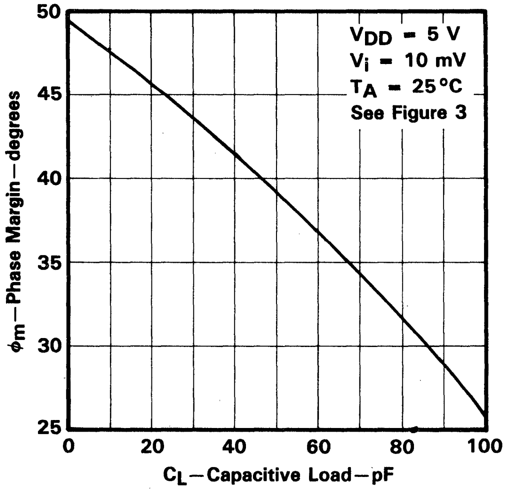
PHASE MARGIN
vs
SUPPLY VOLTAGE

FIGURE 34



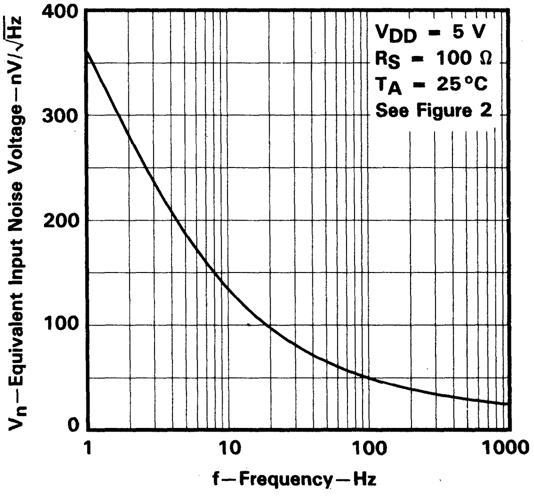
PHASE MARGIN
vs
FREE-AIR TEMPERATURE

FIGURE 35



PHASE MARGIN
vs
CAPACITIVE LOAD

FIGURE 36



EQUIVALENT INPUT NOISE VOLTAGE
vs
FREQUENCY

FIGURE 37

[†] Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL APPLICATION DATA

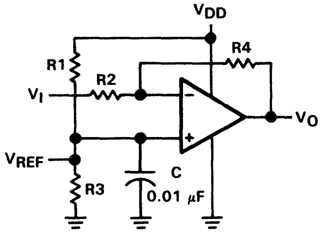
single-supply operation

While the TLC272 and TLC277 perform well using dual power supplies (also called balanced or split supplies), the design is optimized for single-supply operation. This design includes an input common-mode voltage range that encompasses ground as well as an output voltage range that pulls down to ground. The supply voltage range extends down to 3 V (C-suffix types), thus allowing operation with supply levels commonly available for TTL and HCMOS; however, for maximum dynamic range, 16-V single-supply operation is recommended.

Many single-supply applications require that a voltage be applied to one input to establish a reference level that is above ground. A resistive voltage divider is usually sufficient to establish this reference level (see Figure 38). The low input bias current of the TLC272 and TLC277 permits the use of very large resistive values to implement the voltage divider, thus minimizing power consumption.

The TLC272 and TLC277 work well in conjunction with digital logic; however, when powering both linear devices and digital logic from the same power supply, the following precautions are recommended:

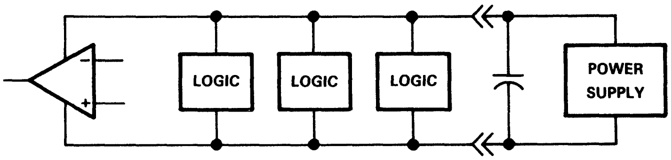
1. Power the linear devices from separate bypassed supply lines (see Figure 39); otherwise the linear device supply rails can fluctuate due to voltage drops caused by high switching currents in the digital logic.
2. Use proper bypass techniques to reduce the probability of noise-induced errors. Single capacitive decoupling is often adequate; however, high-frequency applications may require RC decoupling.



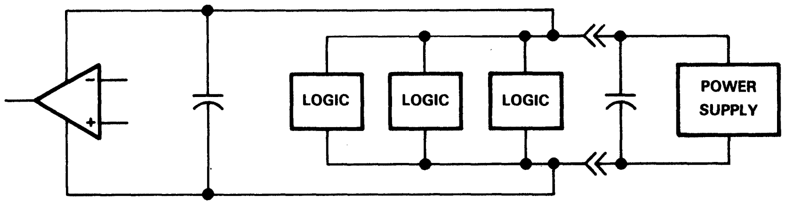
$$V_{REF} = V_{DD} \frac{R3}{R1 + R3}$$

$$V_O = \left(V_{REF} - V_I\right) \frac{R4}{R2} + V_{REF}$$

FIGURE 38. INVERTING AMPLIFIER WITH VOLTAGE REFERENCE



(a) Common Supply Rails



(b) Separate Bypassed Supply Rails (preferred)

FIGURE 39. COMMON VS SEPARATE SUPPLY RAILS

TYPICAL APPLICATION DATA

input characteristics

The TLC272 and TLC277 are specified with a minimum and a maximum input voltage that, if exceeded at either input, could cause the device to malfunction. Exceeding this specified range is a common problem, especially in single-supply operation. Note that the lower range limit includes the negative rail, while the upper range limit is specified at $V_{DD} - 1$ V at $T_A = 25\,°C$ and at $V_{DD} - 1.5$ V at all other temperatures.

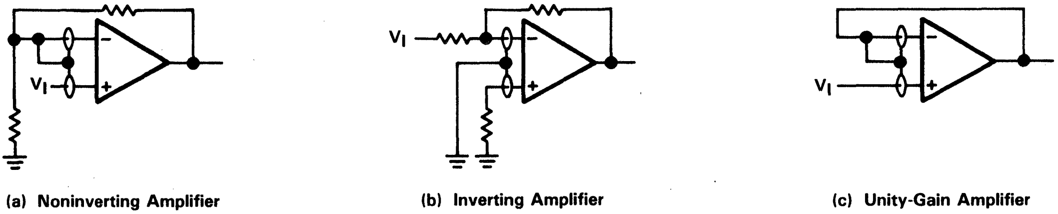
The use of the polysilicon-gate process and the careful input circuit design gives the TLC272 and TLC277 very good input offset voltage drift characteristics relative to conventional metal-gate processes. Offset voltage drift in CMOS devices is highly influenced by threshold voltage shifts caused by polarization of the phosphorus dopant implanted in the oxide. Placing the phosphorus dopant in a conductor (such as a polysilicon gate) alleviates the polarization problem, thus reducing threshold voltage shifts by more than an order of magnitude. The offset voltage drift with time has been calculated to be typically 0.1 μV/month, including the first month of operation.

Because of the extremely high input impedance and resulting low bias current requirements, the TLC272 and TLC277 are well suited for low-level signal processing; however, leakage currents on printed circuit boards and sockets can easily exceed bias current requirements and cause a degradation in device performance. It is good practice to include guard rings around inputs (similar to those of Figure 4 in the Parameter Measurement Information section). These guards should be driven from a low-impedance source at the same voltage level as the common-mode input (see Figure 40).

The inputs of any unused amplifiers should be tied to ground to avoid possible oscillation.

noise performance

The noise specifications in op amp circuits are greatly dependent on the current in the first-stage differential amplifier. The low input bias current requirements of the TLC272 and TLC277 result in a very low noise current, which is insignificant in most applications. This feature makes the devices especially favorable over bipolar devices when using values of circuit impedance greater than 50 kΩ, since bipolar devices exhibit greater noise currents.



(a) Noninverting Amplifier (b) Inverting Amplifier (c) Unity-Gain Amplifier

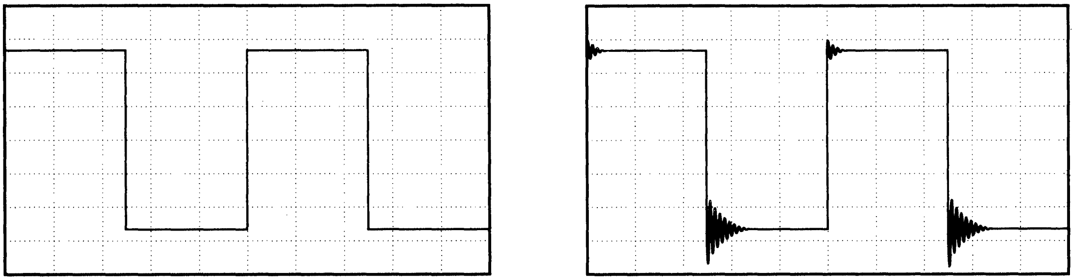
FIGURE 40. GUARD-RING SCHEMES

output characteristics

The output stage of the TLC272 and TLC277 is designed to sink and source relatively high amounts of current (see typical characteristics). If the output is subjected to a short-circuit condition, this high current capability can cause device damage under certain conditions. Output current capability increases with supply voltage.

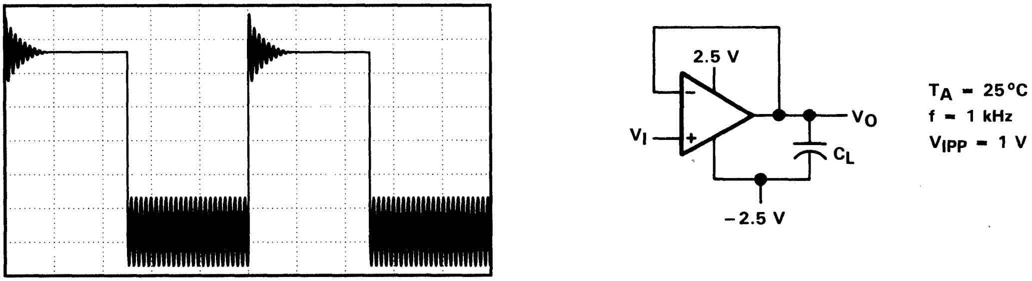
All operating characteristics of the TLC272 and TLC277 were measured using a 20-pF load. The devices will drive higher capacitive loads; however, as output load capacitance increases, the resulting response pole occurs at lower frequencies, thereby causing ringing, peaking, or even oscillation (see Figure 41). In many cases, adding a small amount of resistance in series with the load capacitance will alleviate the problem.

TYPICAL APPLICATION DATA



(a) C_L = 20 pF, R_L = No load

(b) C_L = 130 pF, R_L = No load



(c) C_L = 150 pF, R_L = No load

(d) Test Circuit

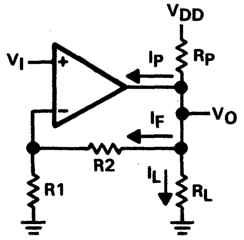
FIGURE 41. EFFECT OF CAPACITIVE LOADS AND TEST CIRCUIT

Although the TLC272 and TLC277 possess excellent high-level output voltage and current capability, methods for boosting this capability are available, if needed. The simplest method involves the use of a pullup resistor (R_P) connected from the output to the positive supply rail (see Figure 42). There are two disadvantages to the use of this circuit. First, the NMOS pulldown transistor N4 (see equivalent schematic) must sink a comparatively large amount of current. In this circuit, N4 behaves like a linear resistor with an on-resistance between approximately 60 Ω and 180 Ω, depending on how hard the op amp input is driven. With very low values of R_P, a voltage offset from 0 V at the output will occur. Second, pullup resistor R_P acts as a drain load to N4 and the gain of the op amp is reduced at output voltage levels where N5 is not supplying the output current.

feedback

Op amp circuits nearly always employ feedback, and since feedback is the first prerequisite for oscillation, some caution is appropriate. Most oscillation problems result from driving capacitive loads (discussed previously) and ignoring stray input capacitance. A small-value capacitor connected in parallel with the feedback resistor is an effective remedy (see Figure 43). The value of this capacitor is optimized empirically.

TYPICAL APPLICATION DATA



$$R_P = \frac{V_{DD} - V_O}{I_F + I_L + I_P}$$

I_P = Pullup current required by the op amp (typically 500 μA)

FIGURE 42. RESISTIVE PULLUP TO INCREASE V_{OH}

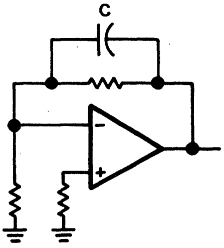


FIGURE 43. COMPENSATION FOR INPUT CAPACITANCE

electrostatic discharge protection

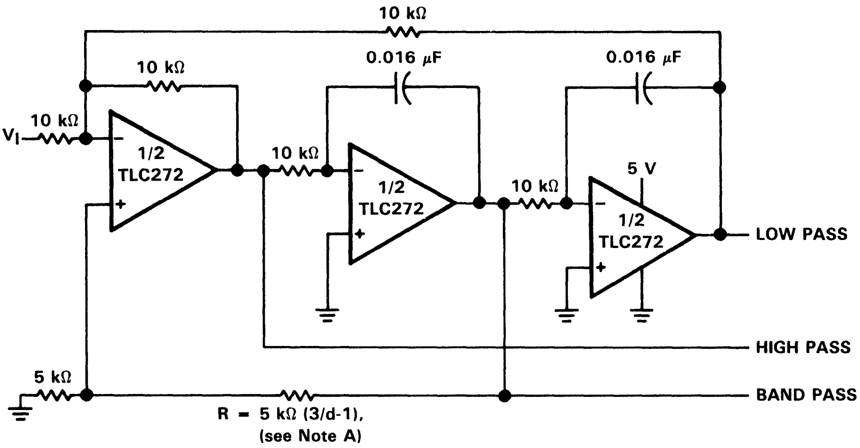
The TLC272 and TLC277 incorporate an internal electrostatic discharge (ESD) protection circuit that prevents functional failures at voltages up to 2000 V as tested under MIL-STD-883C, Method 3015.2. Care should be exercised, however, when handling these devices as exposure to ESD may result in the degradation of the device parametric performance. The protection circuit also causes the input bias currents to be temperature dependent and have the characteristics of a reverse-biased diode.

latch-up

Because CMOS devices are susceptible to latch-up due to their inherent parasitic thyristors, the TLC272 and TLC277 inputs and outputs were designed to withstand − 100-mA surge currents without sustaining latch-up; however, techniques should be used to reduce the chance of latch-up whenever possible. Internal protection diodes should not, by design, be forward biased. Applied input and output voltage should not exceed the supply voltage by more than 300 mV. Care should be exercised when using capacitive coupling on pulse generators. Supply transients should be shunted by the use of decoupling capacitors (0.1 μF typical) located across the supply rails as close to the device as possible.

The current path established if latch-up occurs is usually between the positive supply rail and ground and can be triggered by surges on the supply lines and/or voltages on either the output or inputs that exceed the supply voltage. Once latch-up occurs, the current flow is limited only by the impedance of the power supply and the forward resistance of the parasitic thyristor and usually results in the destruction of the device. The chance of latch-up occurring increases with increasing temperature and supply voltages.

TYPICAL APPLICATION DATA



NOTES: A. d = damping factor, 1/Q
B. Normalized to 10 kΩ and f_C = 1 kHz

FIGURE 44. STATE VARIABLE FILTER

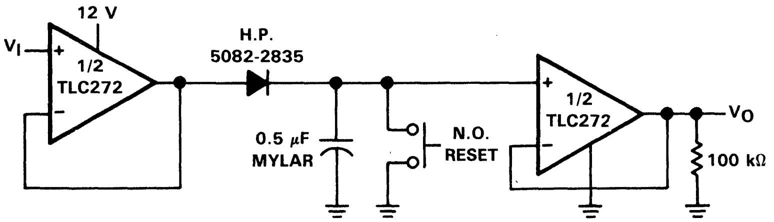
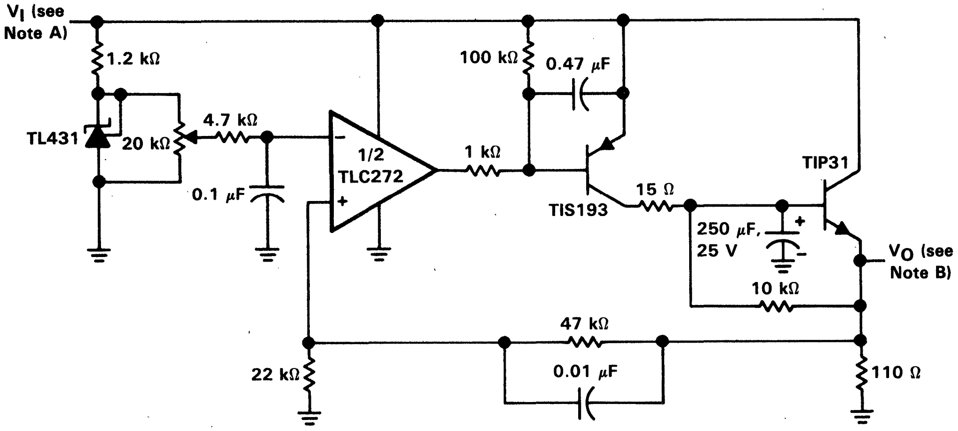


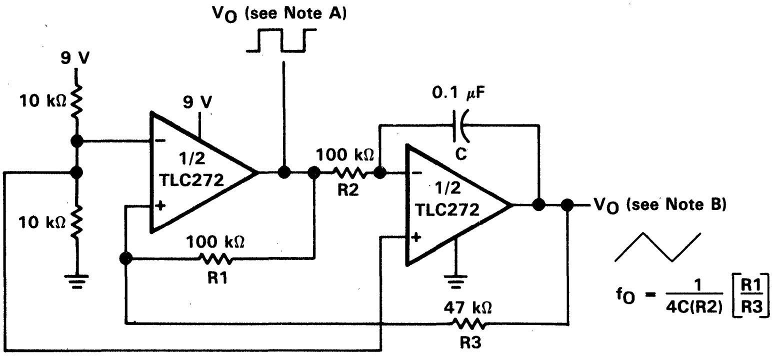
FIGURE 45. POSITIVE-PEAK DETECTOR

TYPICAL APPLICATION DATA



NOTES: A. V_I = 3.5 to 15 V
B. V_O = 2.0 V, 0 to 1 A

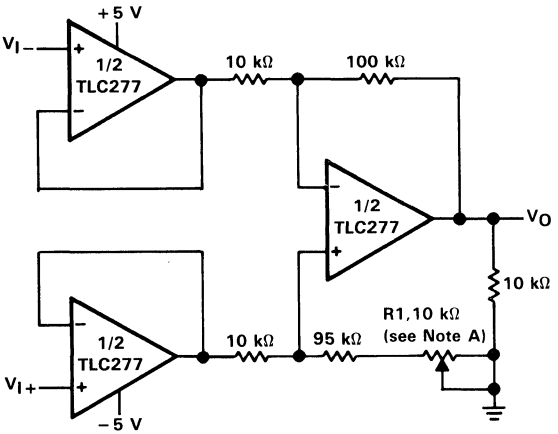
FIGURE 46. LOGIC ARRAY POWER SUPPLY



NOTES: A. V_{OPP} = 8 V
B. V_{OPP} = 4 V

FIGURE 47. SINGLE-SUPPLY FUNCTION GENERATOR

TYPICAL APPLICATION DATA



NOTE A: CMRR adjustment must be noninductive .

FIGURE 48. LOW-POWER INSTRUMENTATION AMPLIFIER

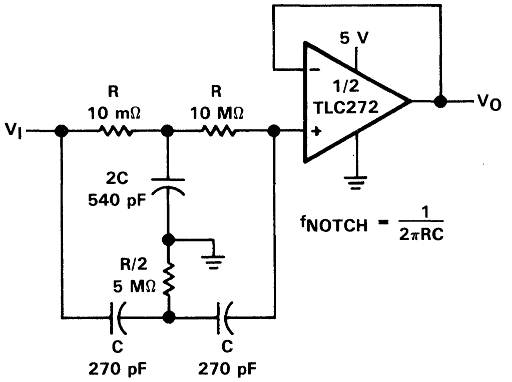


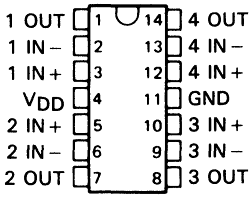
FIGURE 49. SINGLE-SUPPLY TWIN-T NOTCH FILTER

TLC274, TLC274A, TLC274B, TLC279
LinCMOS™ PRECISION QUAD OPERATIONAL AMPLIFIERS

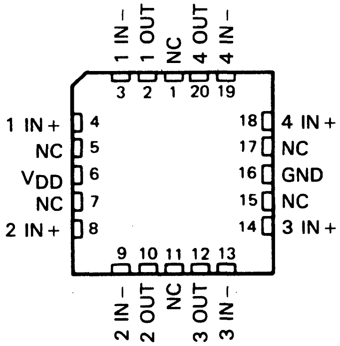
D3141, SEPTEMBER 1987—REVISED OCTOBER 1990

- **Trimmed Offset Voltage:**
  TLC279 . . . 900 μV Max at 25°C,
  V_{DD} = 5 V
- **Input Offset Voltage Drift . . . Typically 0.1 μV/Month, Including the First 30 Days**
- **Wide Range of Supply Voltages Over Specified Temperature Range:**
  0°C to 70°C . . . 3 V to 16 V
  −40°C to 85°C . . . 4 V to 16 V
  −55°C to 125°C . . . 4 V to 16 V
- **Single-Supply Operation**
- **Common-Mode Input Voltage Range Extends Below the Negative Rail (C-Suffix, I-Suffix types)**
- **Low Noise . . . Typically 25 nV/√Hz at f = 1 kHz**
- **Output Voltage Range Includes Negative Rail**
- **High Input Impedance . . . 10^{12} Ω Typical**
- **ESD-Protection Circuitry**
- **Small-Outline Package Option Also Available in Tape and Reel**
- **Designed-In Latch-Up Immunity**

D, J, OR N PACKAGE
(TOP VIEW)



FK PACKAGE
(TOP VIEW)



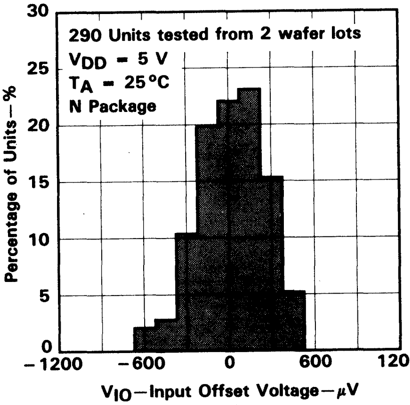
NC—No internal connection

AVAILABLE OPTIONS

T_A	V_{IO}max at 25°C	PACKAGE			
		SMALL OUTLINE (D)	CHIP CARRIER (FK)	CERAMIC DIP (J)	PLASTIC DIP (N)
0°C to 70°C	900 μV	TLC279CD	—	—	TLC279CN
	2 mV	TLC274BCD	—	—	TLC274BCN
	5 mV	TLC274ACD	—	—	TLC274ACN
	10 mV	TLC274CD	—	—	TLC274CN
−40°C to 85°C	900 μV	TLC279ID	—	—	TLC279IN
	2 mV	TLC274BID	—	—	TLC274BIN
	5 mV	TLC274AID	—	—	TLC274AIN
	10 mV	TLC274ID	—	—	TLC274IN
−55°C to 125°C	900 μV	TLC279MD	TLC279MFK	TLC279MJ	TLC279MN
	10 mV	TLC274MD	TLC274MFK	TLC274MJ	TLC274MN

The D package is available in tape and reel. Add R suffix to the device type, (e.g., TLC279CDR).

DISTRIBUTION OF TLC279
INPUT OFFSET VOLTAGE



LinCMOS is a trademark of Texas Instruments Incorporated

TEXAS INSTRUMENTS
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

description

The TLC274 and TLC279 quad operational amplifiers combine a wide range of input offset voltage grades with low offset voltage drift, high input impedance, low noise, and speeds approaching that of general-purpose BiFET devices.

These devices use Texas Instruments silicon-gate LinCMOS™ technology, which provides offset voltage stability far exceeding the stability available with conventional metal-gate processes.

The extremely high input impedance, low bias currents, and high slew rates make these cost-effective devices ideal for applications which have previously been reserved for BiFET and NFET products. Four offset voltage grades are available (C-suffix and I-suffix types), ranging from the low-cost TLC274 (10 mV) to the high-precision TLC279 (900 μV). These advantages, in combination with good common-mode rejection and supply voltage rejection, make these devices a good choice for new state-of-the-art designs as well as for upgrading existing designs.

In general, many features associated with bipolar technology are available on LinCMOS™ operational amplifiers, without the power penalties of bipolar technology. General applications such as transducer interfacing, analog calculations, amplifier blocks, active filters, and signal buffering are easily designed with the TLC274 and TLC279. The devices also exhibit low voltage single-supply operation, making them ideally suited for remote and inaccessible battery-powered applications. The common-mode input voltage range includes the negative rail.

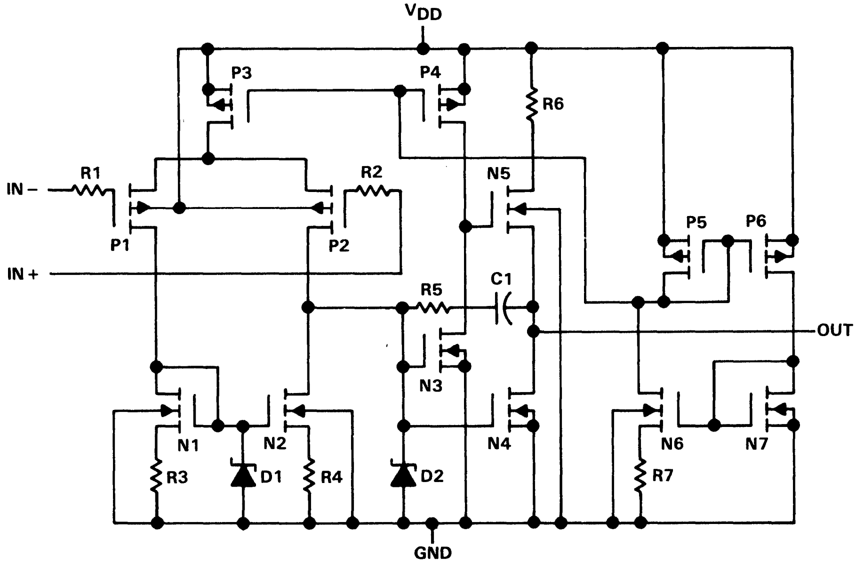
A wide range of packaging options is available, including small-outline and chip carrier versions for high-density system applications.

The device inputs and outputs are designed to withstand −100-mA surge currents without sustaining latch-up.

The TLC274 and TLC279 incorporate internal ESD-protection circuits that prevent functional failures at voltages up to 2000 V as tested under MIL-STD-883C, Method 3015.2; however, care should be exercised in handling these devices as exposure to ESD may result in the degradation of the device parametric performance.

C-suffix devices are characterized for operation from 0°C to 70°C. I-suffix devices are characterized for operation from −40°C to 85°C. M-suffix devices are characterized for operation over the full military temperature range of −55°C to 125°C.

equivalent schematic (each amplifier)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{DD} (see Note 1)	18 V
Differential input voltage (see Note 2)	$\pm V_{DD}$
Input voltage range, V_I (any input)	−0.3 V to V_{DD}
Input current, I_I	±5 mA
Output current, I_O (each output)	±30 mA
Total current into V_{DD} terminal	45 mA
Total current out of ground terminal	45 mA
Duration of short-circuit current at (or below) 25°C (see Note 3)	Unlimited
Continuous total dissipation	See Dissipation Rating Table
Operating free-air temperature, T_A: C-suffix	0°C to 70°C
I-suffix	−40°C to 85°C
M-suffix	−55°C to 125°C
Storage temperature range	−65°C to 150°C
Case temperature for 60 seconds: FK package	260°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D and N package	260°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: J package	300°C

NOTES: 1. All voltage values, except differential voltages, are with respect to network ground.
2. Differential voltages are at the noninverting input with respect to the inverting input.
3. The output may be shorted to either supply. Temperature and/or supply voltages must be limited to ensure that the maximum dissipation rating is not exceeded (see application section).

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING	$T_A = 125°C$ POWER RATING
D	950 mW	7.6 mW/°C	608 mW	494 mW	
FK	1375 mW	11 mW/°C	880 mW	715 mW	275 mW
J	1375 mW	11 mW/°C	880 mW	715 mW	275 mW
N	1575 mW	12.6 mW/°C	1008 mW	819 mW	

recommended operating conditions

		C-SUFFIX			I-SUFFIX			M-SUFFIX			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{DD}		3		16	4		16	4		16	V
Common-mode input voltage, V_{IC}	V_{DD} = 5 V	−0.2		3.5	−0.2		3.5	0		3.5	V
	V_{DD} = 10 V	−0.2		8.5	−0.2		8.5	0		8.5	
Operating free-air temperature, T_A		0		70	−40		85	−55		125	°C

electrical characteristics at specified free-air temperature, V_{DD} = 5 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS	T_A†	MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	TLC274M	V_O = 1.4 V, V_{IC} = 0, R_S = 50 Ω, R_L = 10 kΩ	25°C		1.1	10	mV
				Full range			12	
		TLC279M	V_O = 1.4 V, V_{IC} = 0, R_S = 50 Ω, R_L = 10 kΩ	25°C		320	900	µV
				Full range			3750	
α_{VIO}	Average temperature coefficient of input offset voltage			25°C to 125°C		2.1		µV/°C
I_{IO}	Input offset current (see Note 4)		V_O = 2.5 V, V_{IC} = 2.5 V	25°C		0.1		pA
				125°C		1.4	15	nA
I_{IB}	Input bias current (see Note 4)		V_O = 2.5 V, V_{IC} = 2.5 V	25°C		0.6		pA
				125°C		9	35	nA
V_{ICR}	Common-mode input voltage range (see Note 5)			25°C	0 to 4	−0.3 to 4.2		V
				Full range	0 to 3.5			V
V_{OH}	High-level output voltage		V_{ID} = 100 mV, R_L = 10 kΩ	25°C	3.2	3.8		V
				−55°C	3	3.8		
				125°C	3	3.8		
V_{OL}	Low-level output voltage		V_{ID} = −100 mV, I_{OL} = 0	25°C		0	50	mV
				−55°C		0	50	
				125°C		0	50	
A_{VD}	Large-signal differential voltage amplification		V_O = 0.25 V to 2 V, R_L = 10 kΩ	25°C	5	23		V/mV
				−55°C	3.5	35		
				125°C	3.5	16		
CMRR	Common-mode rejection ratio		V_{IC} = V_{ICR} min	25°C	65	80		dB
				−55°C	60	81		
				125°C	60	84		
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)		V_{DD} = 5 V to 10 V, V_O = 1.4 V	25°C	65	95		dB
				−55°C	60	90		
				125°C	60	97		
I_{DD}	Supply current (four amplifiers)		V_O = 2.5 V, V_{IC} = 2.5 V, No load	25°C		2.7	6.4	mA
				−55°C		4	10	
				125°C		1.9	4.4	

† Full range is −55°C to 125°C.

NOTES: 4. The typical values of input bias current and input offset current below 5 pA were determined mathematically.

5. This range also applies to each input individually.

electrical characteristics at specified free-air temperature, V_{DD} = 10 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS	T_A[†]	MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	TLC274M	V_O = 1.4 V, V_{IC} = 0, R_S = 50 Ω, R_L = 10 kΩ	25°C		1.1	10	mV
				Full range			12	
		TLC279M	V_O = 1.4 V, V_{IC} = 0, R_S = 50 Ω, R_L = 10 kΩ	25°C		370	1200	µV
				Full range			4300	
α_{VIO}	Average temperature coefficient of input offset voltage			25°C to 125°C		2.2		µV/°C
I_{IO}	Input offset current (see Note 4)		V_O = 5 V, V_{IC} = 5 V	25°C		0.1		pA
				125°C		1.8	15	nA
I_{IB}	Input bias current (see Note 4)		V_O = 5 V, V_{IC} = 5 V	25°C		0.7		pA
				125°C		10	35	nA
V_{ICR}	Common-mode input voltage range (see Note 5)			25°C	0 to 9	−0.3 to 9.2		V
				Full range	0 to 8.5			V
V_{OH}	High-level output voltage		V_{ID} = 100 mV, R_L = 10 kΩ	25°C	8	8.5		V
				−55°C	7.8	8.5		
				125°C	7.8	8.4		
V_{OL}	Low-level output voltage		V_{ID} = −100 mV, I_{OL} = 0	25°C		0	50	mV
				−55°C		0	50	
				125°C		0	50	
A_{VD}	Large-signal differential voltage amplification		V_O = 1 V to 6 V, R_L = 10 kΩ	25°C	10	36		V/mV
				−55°C	7	50		
				125°C	7	27		
CMRR	Common-mode rejection ratio		V_{IC} = V_{ICR} min	25°C	65	85		dB
				−55°C	60	87		
				125°C	60	86		
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)		V_{DD} = 5 V to 10 V, V_O = 1.4 V	25°C	65	95		dB
				−55°C	60	90		
				125°C	60	97		
I_{DD}	Supply current (four amplifiers)		V_O = 5 V, V_{IC} = 5 V, No load	25°C		3.8	8	mA
				−55°C		6.0	12	
				125°C		2.5	5.6	

[†] Full range is −55°C to 125°C.

NOTES: 4. The typical values of input bias current and input offset current below 5 pA were determined mathematically.
5. This range also applies to each input individually.

electrical characteristics at specified free-air temperature, V_{DD} = 5 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS		T_A†	MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	TLC274I	V_O = 1.4 V, R_S = 50 Ω,	V_{IC} = 0, R_L = 10 kΩ	25°C		1.1	10	mV
					Full range			13	
		TLC274AI	V_O = 1.4 V, R_S = 50 Ω,	V_{IC} = 0, R_L = 10 kΩ	25°C		0.9	5	
					Full range			7	
		TLC274BI	V_O = 1.4 V, R_S = 50 Ω,	V_{IC} = 0, R_L = 10 kΩ	25°C		340	2000	µV
					Full range			3500	
		TLC279I	V_O = 1.4 V, R_S = 50 Ω,	V_{IC} = 0, R_L = 10 kΩ	25°C		320	900	
					Full range			2000	
α_{VIO}	Average temperature coefficient of input offset voltage				25°C to 85°C		1.8		µV/°C
I_{IO}	Input offset current (see Note 4)		V_O = 2.5 V,	V_{IC} = 2.5 V	25°C		0.1		pA
					85°C		24	1000	
I_{IB}	Input bias current (see Note 4)		V_O = 2.5 V,	V_{IC} = 2.5 V	25°C		0.6		pA
					85°C		200	2000	
V_{ICR}	Common-mode input voltage range (see Note 5)				25°C	−0.2 to 4	−0.3 to 4.2		V
					Full range	−0.2 to 3.5			V
V_{OH}	High-level output voltage		V_{ID} = 100 mV,	R_L = 10 kΩ	25°C	3.2	3.8		V
					−40°C	3	3.8		
					85°C	3	3.8		
V_{OL}	Low-level output voltage		V_{ID} = −100 mV,	I_{OL} = 0	25°C		0	50	mV
					−40°C		0	50	
					85°C		0	50	
A_{VD}	Large-signal differential voltage amplification		V_O = 0.25 V to 2 V,	R_L = 10 kΩ	25°C	5	23		V/mV
					−40°C	3.5	32		
					85°C	3.5	19		
CMRR	Common-mode rejection ratio		V_{IC} = V_{ICR} min		25°C	65	80		dB
					−40°C	60	81		
					85°C	60	86		
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)		V_{DD} = 5 V to 10 V,	V_O = 1.4 V	25°C	65	95		dB
					−40°C	60	92		
					85°C	60	96		
I_{DD}	Supply current (four amplifiers)		V_O = 2.5 V, No load	V_{IC} = 2.5 V,	25°C		2.7	6.4	mA
					−40°C		3.8	8.8	
					85°C		2.1	4.8	

† Full range is −40°C to 85°C.

NOTES: 4. The typical values of input bias current and input offset current below 5 pA were determined mathematically.
5. This range also applies to each input individually.

electrical characteristics at specified free-air temperature, V_{DD} = 10 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS		T_A†	MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	TLC274I	V_O = 1.4 V, R_S = 50 Ω,	V_{IC} = 0, R_L = 10 kΩ	25°C		1.1	10	mV
					Full range			13	
		TLC274AI	V_O = 1.4 V, R_S = 50 Ω,	V_{IC} = 0, R_L = 10 kΩ	25°C		0.9	5	
					Full range			7	
		TLC274BI	V_O = 1.4 V, R_S = 50 Ω,	V_{IC} = 0, R_L = 10 kΩ	25°C		390	2000	µV
					Full range			3500	
		TLC279I	V_O = 1.4 V, R_S = 50 Ω,	V_{IC} = 0, R_L = 10 kΩ	25°C		370	1200	
					Full range			2900	
α_{VIO}	Average temperature coefficient of input offset voltage				25°C to 85°C		2		µV/°C
I_{IO}	Input offset current (see Note 4)		V_O = 5 V,	V_{IC} = 5 V	25°C		0.1		pA
					85°C		26	1000	
I_{IB}	Input bias current (see Note 4)		V_O = 5 V,	V_{IC} = 5 V	25°C		0.7		pA
					85°C		220	2000	
V_{ICR}	Common-mode input voltage range (see Note 5)				25°C	−0.2 to 9	−0.3 to 9.2		V
					Full range	−0.2 to 8.5			V
V_{OH}	High-level output voltage		V_{ID} = 100 mV,	R_L = 10 kΩ	25°C	8	8.5		V
					−40°C	7.8	8.5		
					85°C	7.8	8.5		
V_{OL}	Low-level output voltage		V_{ID} = −100 mV,	I_{OL} = 0	25°C		0	50	mV
					−40°C		0	50	
					85°C		0	50	
A_{VD}	Large-signal differential voltage amplification		V_O = 1 V to 6 V,	R_L = 10 kΩ	25°C	10	36		V/mV
					−40°C	7	47		
					85°C	7	31		
CMRR	Common-mode rejection ratio		V_{IC} = V_{ICR} min		25°C	65	85		dB
					−40°C	60	87		
					85°C	60	88		
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)		V_{DD} = 5 V to 10 V,	V_O = 1.4 V	25°C	65	95		dB
					−40°C	60	92		
					85°C	60	96		
I_{DD}	Supply current (four amplifiers)		V_O = 5 V, No load	V_{IC} = 5 V,	25°C		3.8	8	mA
					−40°C		5.5	10	
					85°C		2.9	6.4	

† Full range is −40°C to 85°C.

NOTES: 4. The typical values of input bias current and input offset current below 5 pA were determined mathematically.
5. This range also applies to each input individually.

electrical characteristics at specified free-air temperature, V_{DD} = 5 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS	T_A†	MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	TLC274C	V_O = 1.4 V, V_{IC} = 0, R_S = 50 Ω, R_L = 10 kΩ	25°C		1.1	10	mV
				Full range			12	
		TLC274AC	V_O = 1.4 V, V_{IC} = 0, R_S = 50 Ω, R_L = 10 kΩ	25°C		0.9	5	
				Full range			6.5	
		TLC274BC	V_O = 1.4 V, V_{IC} = 0, R_S = 50 Ω, R_L = 10 kΩ	25°C		340	2000	μV
				Full range			3000	
		TLC279C	V_O = 1.4 V, V_{IC} = 0, R_S = 50 Ω, R_L = 10 kΩ	25°C		320	900	
				Full range			1500	
α_{VIO}	Average temperature coefficient of input offset voltage			25°C to 70°C		1.8		μV/°C
I_{IO}	Input offset current (see Note 4)		V_O = 2.5 V, V_{IC} = 2.5 V	25°C		0.1		pA
				70°C		7	300	
I_{IB}	Input bias current (see Note 4)		V_O = 2.5 V, V_{IC} = 2.5 V	25°C		0.6		pA
				70°C		40	600	
V_{ICR}	Common-mode input voltage range (see Note 5)			25°C	−0.2 to 4	−0.3 to 4.2		V
				Full range	−0.2 to 3.5			V
V_{OH}	High-level output voltage		V_{ID} = 100 mV, R_L = 10 kΩ	25°C	3.2	3.8		V
				0°C	3	3.8		
				70°C	3	3.8		
V_{OL}	Low-level output voltage		V_{ID} = −100 mV, I_{OL} = 0	25°C		0	50	mV
				0°C		0	50	
				70°C		0	50	
A_{VD}	Large-signal differential voltage amplification		V_O = 0.25 V to 2 V, R_L = 10 kΩ	25°C	5	23		V/mV
				0°C	4	27		
				70°C	4	20		
CMRR	Common-mode rejection ratio		V_{IC} = V_{ICR} min	25°C	65	80		dB
				0°C	60	84		
				70°C	60	85		
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)		V_{DD} = 5 V to 10 V, V_O = 1.4 V	25°C	65	95		dB
				0°C	60	94		
				70°C	60	96		
I_{DD}	Supply current (four amplifiers)		V_O = 2.5 V, V_{IC} = 2.5 V, No load	25°C		2.7	6.4	mA
				0°C		3.1	7.2	
				70°C		2.3	5.2	

† Full range is 0°C to 70°C.

NOTES: 4. The typical values of input bias current and input offset current below 5 pA were determined mathematically.

5. This range also applies to each input individually.

electrical characteristics at specified free-air temperature, V_{DD} = 10 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS	T_A†	MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	TLC274C	V_O = 1.4 V, V_{IC} = 0, R_S = 50 Ω, R_L = 10 kΩ	25°C		1.1	10	mV
				Full range			12	
		TLC274AC	V_O = 1.4 V, V_{IC} = 0, R_S = 50 Ω, R_L = 10 kΩ	25°C		0.9	5	
				Full range			6.5	
		TLC274BC	V_O = 1.4 V, V_{IC} = 0, R_S = 50 Ω, R_L = 10 kΩ	25°C		390	2000	μV
				Full range			3000	
		TLC279C	V_O = 1.4 V, V_{IC} = 0, R_S = 50 Ω, R_L = 10 kΩ	25°C		370	1200	
				Full range			1900	
α_{VIO}	Average temperature coefficient of input offset voltage			25°C to 70°C		2		μV/°C
I_{IO}	Input offset current (see Note 4)		V_O = 5 V, V_{IC} = 5 V	25°C		0.1		pA
				70°C		7	300	
I_{IB}	Input bias current (see Note 4)		V_O = 5 V, V_{IC} = 5 V	25°C		0.7		pA
				70°C		50	600	
V_{ICR}	Common-mode input voltage range (see Note 5)			25°C	−0.2 to 9	−0.3 to 9.2		V
				Full range	−0.2 to 8.5			V
V_{OH}	High-level output voltage		V_{ID} = 100 mV, R_L = 10 kΩ	25°C	8	8.5		V
				0°C	7.8	8.5		
				70°C	7.8	8.4		
V_{OL}	Low-level output voltage		V_{ID} = −100 mV, I_{OL} = 0	25°C		0	50	mV
				0°C		0	50	
				70°C		0	50	
A_{VD}	Large-signal differential voltage amplification		V_O = 1 V to 6 V, R_L = 10 kΩ	25°C	10	36		V/mV
				0°C	7.5	42		
				70°C	7.5	32		
CMRR	Common-mode rejection ratio		V_{IC} = V_{ICR} min	25°C	65	85		dB
				0°C	60	88		
				70°C	60	88		
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)		V_{DD} = 5 V to 10 V, V_O = 1.4 V	25°C	65	95		dB
				0°C	60	94		
				70°C	60	96		
I_{DD}	Supply current (four amplifiers)		V_O = 5 V, V_{IC} = 5 V, No load	25°C		3.8	8	mA
				0°C		4.5	8.8	
				70°C		3.2	6.8	

† Full range is 0°C to 70°C.

NOTES: 4. The typical values of input bias current and input offset current below 5 pA were determined mathematically.
5. This range also applies to each input individually.

operating characteristics, V_{DD} = 5 V

PARAMETER		TEST CONDITIONS		T_A	MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain	R_L = 10 kΩ, C_L = 20 pF, See Figure 1	V_{IPP} = 1 V	25°C		3.6		V/μs
				−55°C		4.7		
				125°C		2.3		
			V_{IPP} = 2.5 V	25°C		2.9		
				−55°C		3.7		
				125°C		2		
V_n	Equivalent input noise voltage	f = 1 kHz, See Figure 2	R_S = 100 Ω,	25°C		25		nV/$\sqrt{Hz}$
B_{OM}	Maximum output swing bandwidth	V_O = V_{OH}, R_L = 10 kΩ,	C_L = 20 pF, See Figure 1	25°C		320		kHz
				−55°C		400		
				125°C		230		
B_1	Unity-gain bandwidth	V_i = 10 mV, See Figure 3	C_L = 20 pF,	25°C		1.7		MHz
				−55°C		2.9		
				125°C		1.1		
ϕ_m	Phase margin	V_i = 10 mV, C_L = 20 pF,	f = B_1, See Figure 3	25°C		46°		
				−55°C		49°		
				125°C		41°		

operating characteristics, V_{DD} = 10 V

PARAMETER		TEST CONDITIONS		T_A	MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain	R_L = 10 kΩ, C_L = 20 pF, See Figure 1	V_{IPP} = 1 V	25°C		5.3		V/μs
				−55°C		7.1		
				125°C		3.1		
			V_{IPP} = 5.5 V	25°C		4.6		
				−55°C		6.1		
				125°C		2.7		
V_n	Equivalent input noise voltage	f = 1 kHz, See Figure 2	R_S = 100 Ω,	25°C		25		nV/$\sqrt{Hz}$
B_{OM}	Maximum output swing bandwidth	V_O = V_{OH}, R_L = 10 kΩ,	C_L = 20 pF, See Figure 1	25°C		200		kHz
				−55°C		280		
				125°C		110		
B_1	Unity-gain bandwidth	V_i = 10 mV, See Figure 3	C_L = 20 pF,	25°C		2.2		MHz
				−55°C		3.4		
				125°C		1.6		
ϕ_m	Phase margin	V_i = 10 mV, C_L = 20 pF,	f = B_1, See Figure 3	25°C		49°		
				−55°C		52°		
				125°C		44°		

operating characteristics, V_{DD} = 5 V

PARAMETER		TEST CONDITIONS		T_A	MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain	R_L = 10 kΩ, C_L = 20 pF, See Figure 1	V_{IPP} = 1 V	25°C		3.6		V/μs
				−40°C		4.5		
				85°C		2.8		
			V_{IPP} = 2.5 V	25°C		2.9		
				−40°C		3.5		
				85°C		2.3		
V_n	Equivalent input noise voltage	f = 1 kHz, See Figure 2	R_S = 100 Ω,	25°C		25		$\mathrm{nV}/\sqrt{\mathrm{Hz}}$
B_{OM}	Maximum output swing bandwidth	V_O = V_{OH}, R_L = 10 kΩ,	C_L = 20 pF, See Figure 1	25°C		320		kHz
				−40°C		380		
				85°C		250		
B_1	Unity-gain bandwidth	V_i = 10 mV, See Figure 3	C_L = 20 pF,	25°C		1.7		MHz
				−40°C		2.6		
				85°C		1.2		
ϕ_m	Phase margin	V_i = 10 mV, C_L = 20 pF,	f = B_1, See Figure 3	25°C		46°		
				−40°C		49°		
				85°C		43°		

operating characteristics, V_{DD} = 10 V

PARAMETER		TEST CONDITIONS		T_A	MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain	R_L = 10 kΩ, C_L = 20 pF, See Figure 1	V_{IPP} = 1 V	25°C		5.3		V/μs
				−40°C		6.7		
				85°C		4		
			V_{IPP} = 5.5 V	25°C		4.6		
				−40°C		5.8		
				85°C		3.5		
V_n	Equivalent input noise voltage	f = 1 kHz, See Figure 2	R_S = 100 Ω,	25°C		25		$\mathrm{nV}/\sqrt{\mathrm{Hz}}$
B_{OM}	Maximum output swing bandwidth	V_O = V_{OH}, R_L = 10 kΩ,	C_L = 20 pF, See Figure 1	25°C		200		kHz
				−40°C		260		
				85°C		130		
B_1	Unity-gain bandwidth	V_i = 10 mV, See Figure 3	C_L = 20 pF,	25°C		2.2		MHz
				−40°C		3.1		
				85°C		1.7		
ϕ_m	Phase margin	V_i = 10 mV, C_L = 20 pF,	f = B_1, See Figure 3	25°C		49°		
				−40°C		52°		
				85°C		46°		

operating characteristics, V_{DD} = 5 V

PARAMETER		TEST CONDITIONS		T_A	MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain	R_L = 10 kΩ, C_L = 20 pF, See Figure 1	V_{IPP} = 1 V	25°C		3.6		V/μs
				0°C		4		
				70°C		3		
			V_{IPP} = 2.5 V	25°C		2.9		
				0°C		3.1		
				70°C		2.5		
V_n	Equivalent input noise voltage	f = 1 kHz, See Figure 2	R_S = 100 Ω,	25°C		25		nV/√Hz
B_{OM}	Maximum output swing bandwidth	V_O = V_{OH}, R_L = 10 kΩ,	C_L = 20 pF, See Figure 1	25°C		320		kHz
				0°C		340		
				70°C		260		
B_1	Unity-gain bandwidth	V_i = 10 mV, See Figure 3	C_L = 20 pF,	25°C		1.7		MHz
				0°C		2		
				70°C		1.3		
ϕ_m	Phase margin	V_i = 10 mV, C_L = 20 pF,	f = B_1, See Figure 3	25°C		46°		
				0°C		47°		
				70°C		44°		

operating characteristics, V_{DD} = 10 V

PARAMETER		TEST CONDITIONS		T_A	MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain	R_L = 10 kΩ, C_L = 20 pF, See Figure 1	V_{IPP} = 1 V	25°C		5.3		V/μs
				0°C		5.9		
				70°C		4.3		
			V_{IPP} = 5.5 V	25°C		4.6		
				0°C		5.1		
				70°C		3.8		
V_n	Equivalent input noise voltage	f = 1 kHz, See Figure 2	R_S = 100 Ω,	25°C		25		nV/√Hz
B_{OM}	Maximum output swing bandwidth	V_O = V_{OH}, R_L = 10 kΩ,	C_L = 20 pF, See Figure 1	25°C		200		kHz
				0°C		220		
				70°C		140		
B_1	Unity-gain bandwidth	V_i = 10 mV, See Figure 3	C_L = 20 pF,	25°C		2.2		MHz
				0°C		2.5		
				70°C		1.8		
ϕ_m	Phase margin	V_i = 10 mV, C_L = 20 pF,	f = B_1, See Figure 3	25°C		49°		
				0°C		50°		
				70°C		46°		

PARAMETER MEASUREMENT INFORMATION

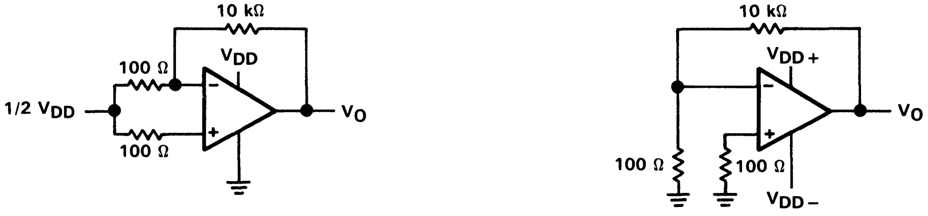
single-supply versus split-supply test circuits

Because the TLC274 and TLC279 are optimized for single-supply operation, circuit configurations used for the various tests often present some inconvenience since the input signal, in many cases, must be offset from ground. This inconvenience can be avoided by testing the device with split supplies and the output load tied to the negative rail. A comparison of single-supply versus split-supply test circuits is shown below. The use of either circuit will give the same result.

(a) Single-Supply

(b) Split-Supply

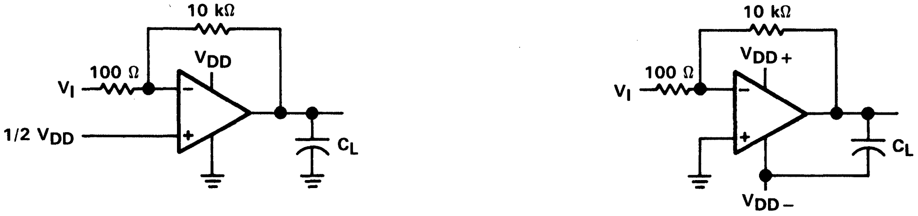
FIGURE 1. UNITY-GAIN AMPLIFIER



(a) Single-Supply

(b) Split-Supply

FIGURE 2. NOISE TEST CIRCUIT



(a) Single-Supply

(b) Split-Supply

FIGURE 3. GAIN-OF-100 INVERTING AMPLIFIER

PARAMETER MEASUREMENT INFORMATION

input bias current

Because of the high input impedance of the TLC274 and TLC279 op amps, attempts to measure the input bias current can result in erroneous readings. The bias current at normal room ambient temperature is typically less than 1 pA, a value that is easily exceeded by leakages on the test socket. Two suggestions are offered to avoid erroneous measurements:

1. Isolate the device from other potential leakage sources. Use a grounded shield around and between the device inputs (see Figure 4). Leakages that would otherwise flow to the inputs will be shunted away.
2. Compensate for the leakage of the test socket by actually performing an input bias current test (using a picoammeter) with no device in the test socket. The actual input bias current can then be calculated by subtracting the ''open-socket'' leakage readings from the readings obtained with a device in the test socket.

   One word of caution . . . many automatic testers as well as some bench-top op amp testers use the servo-loop technique with a resistor in series with the device input to measure the input bias current (the voltage drop across the series resistor is measured and the bias current is calculated). This method requires that a device be inserted into the test socket to obtain a correct reading; therefore, an ''open-socket'' reading is not feasible using this method.

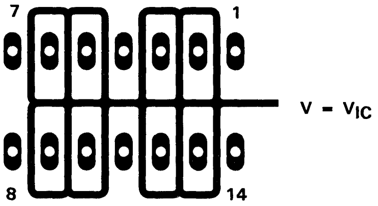


FIGURE 4. ISOLATION METAL AROUND DEVICE INPUTS
(J AND N DUAL-IN-LINE-PACKAGE)

low-level output voltage

To obtain low-supply-voltage operation, some compromise was necessary in the input stage. This compromise results in the device low-level output being dependent on both the common-mode input voltage level as well as the differential input voltage level. When attempting to correlate low-level output readings with those quoted in the electrical specifications, these two conditions should be observed. If conditions other than these are to be used, please refer to Figures 14 through 19 in the Typical Characteristics of this data sheet.

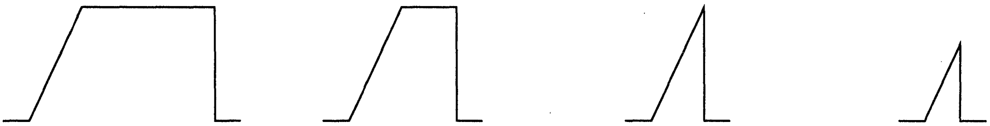
input offset voltage temperature coefficient

Erroneous readings often result from attempts to measure temperature coefficient of input offset voltage. This parameter is actually a calculation using input offset voltage measurements obtained at two different temperatures. When one (or both) of the temperatures is below freezing, moisture can collect on both the device and the test socket. This moisture will result in leakage and contact resistance, which can cause erroneous input offset voltage readings. The isolation techniques previously mentioned have no effect on the leakage since the moisture also covers the isolation metal itself, thereby rendering it useless. It is suggested that these measurements be performed at temperatures above freezing to minimize error.

full-power response

Full-power response, the frequency above which the op amp slew rate limits the output voltage swing, is often specified two ways . . . full-linear response and full-peak response. The full-linear response is generally measured by monitoring the distortion level of the output while increasing the frequency of a sinusoidal input signal until the maximum frequency is found above which the output contains significant distortion. The full-peak response is defined as the maximum output frequency, without regard to distortion, above which full peak-to-peak output swing cannot be maintained.

Because there is no industry-wide accepted value for "significant" distortion, the full-peak response is specified in this data sheet and is measured using the circuit of Figure 1. The initial setup involves the use of a sinusoidal input to determine the maximum peak-to-peak output of the device (the amplitude of the sinusoidal wave is increased until clipping occurs). The sinusoidal wave is then replaced with a square wave of the same amplitude. The frequency is then increased until the maximum peak-to-peak output can no longer be maintained (Figure 5). A square wave is used to allow a more accurate determination of the point at which the maximum peak-to-peak output is reached.



(a) f = 1 kHz (b) $B_{OM} > f > 1$ kHz (c) $f = B_{OM}$ (d) $f > B_{OM}$

FIGURE 5. FULL-POWER-RESPONSE OUTPUT SIGNAL

test time

Inadequate test time is a frequent problem, especially when testing CMOS devices in a high-volume, short-test-time environment. Internal capacitances are inherently higher in CMOS than in bipolar and BiFET devices and require longer test times than their bipolar and BiFET counterparts. The problem becomes more pronounced with reduced supply levels and lower temperatures.

TYPICAL CHARACTERISTICS

DISTRIBUTION OF TLC274
INPUT OFFSET VOLTAGE

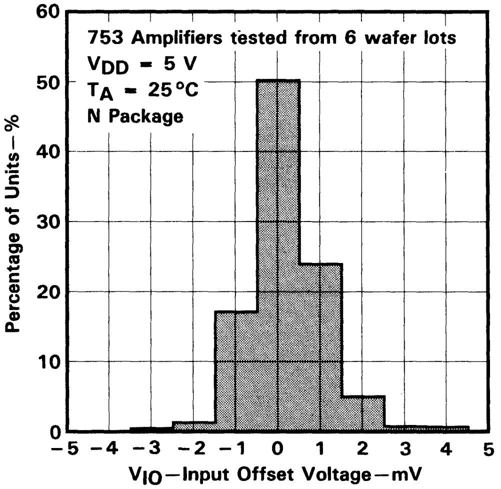


FIGURE 6

DISTRIBUTION OF TLC274
INPUT OFFSET VOLTAGE

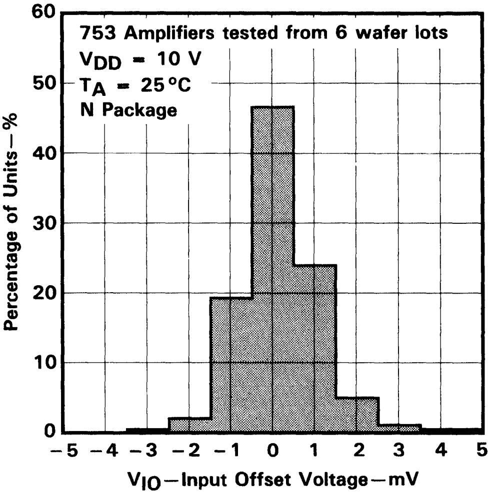


FIGURE 7

DISTRIBUTION OF TLC274 AND TLC279
INPUT OFFSET VOLTAGE
TEMPERATURE COEFFICIENT

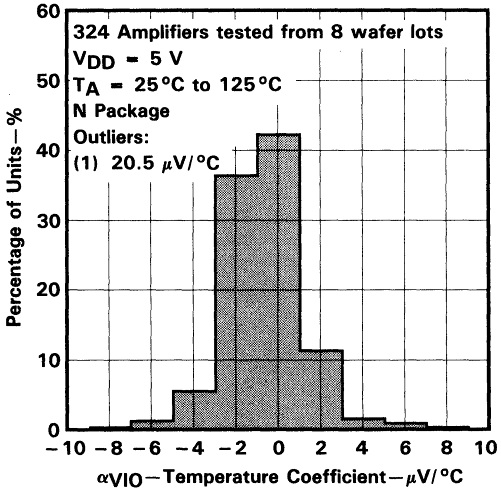


FIGURE 8

DISTRIBUTION OF TLC274 AND TLC279
INPUT OFFSET VOLTAGE
TEMPERATURE COEFFICIENT

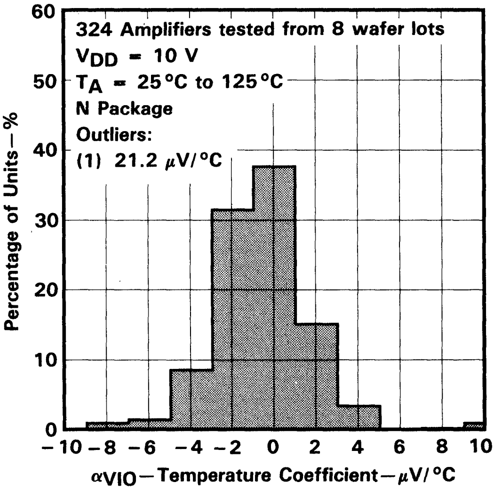


FIGURE 9

TYPICAL CHARACTERISTICS†

HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

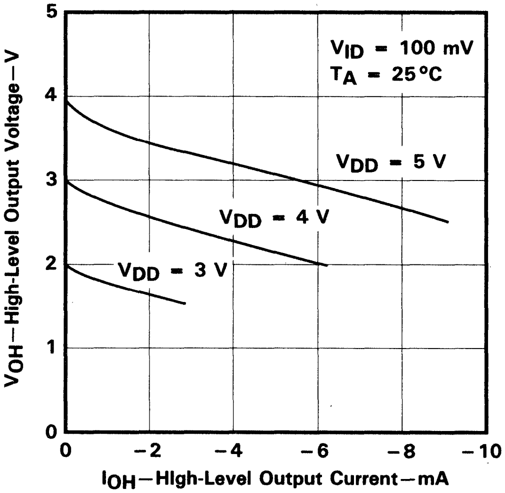


FIGURE 10

HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

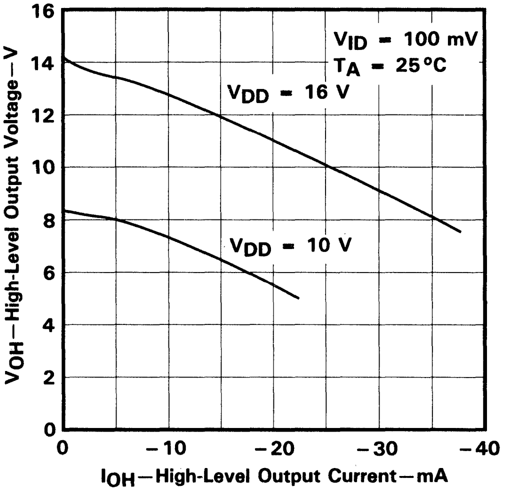


FIGURE 11

HIGH-LEVEL OUTPUT VOLTAGE
vs
SUPPLY VOLTAGE

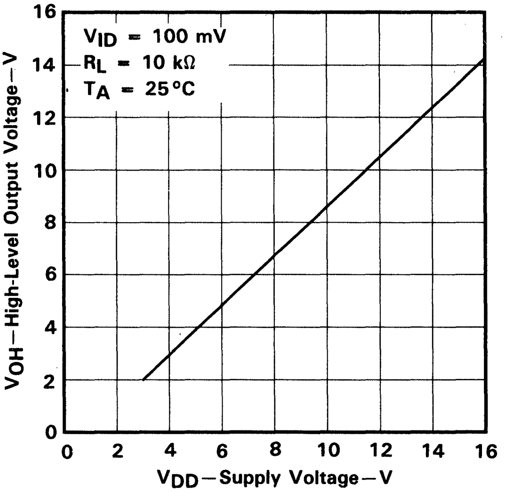


FIGURE 12

HIGH-LEVEL OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

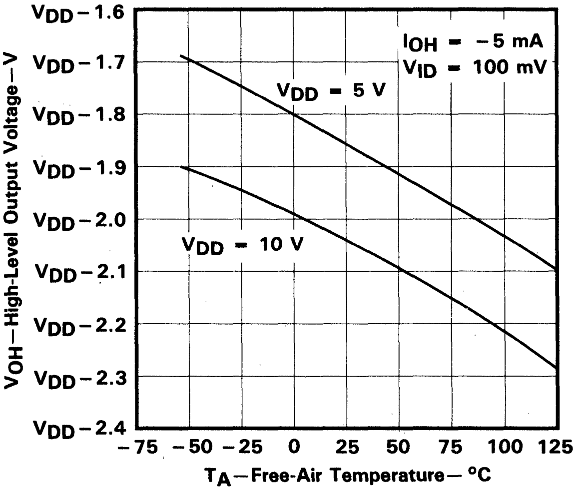


FIGURE 13

---

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

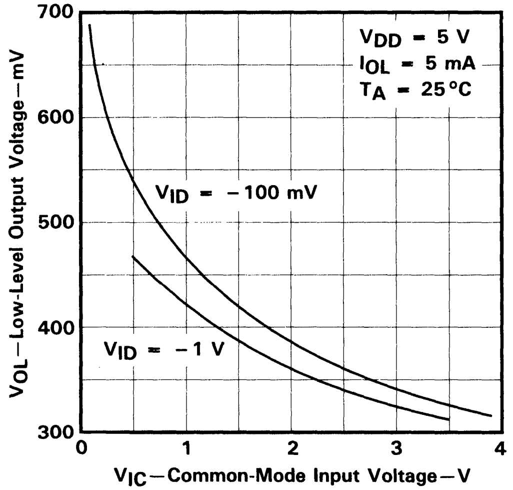

LOW-LEVEL OUTPUT VOLTAGE
vs
COMMON-MODE INPUT VOLTAGE

FIGURE 14

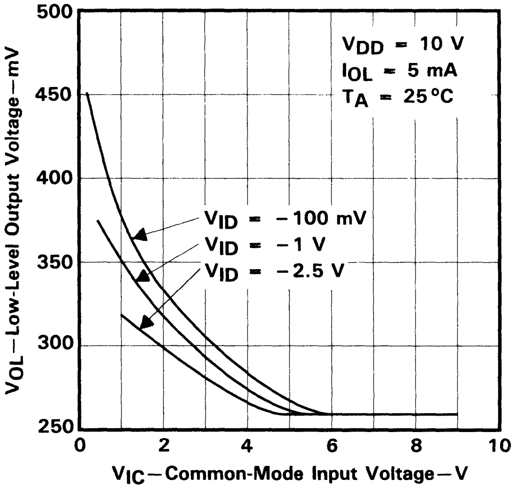

LOW-LEVEL OUTPUT VOLTAGE
vs
COMMON-MODE INPUT VOLTAGE

FIGURE 15

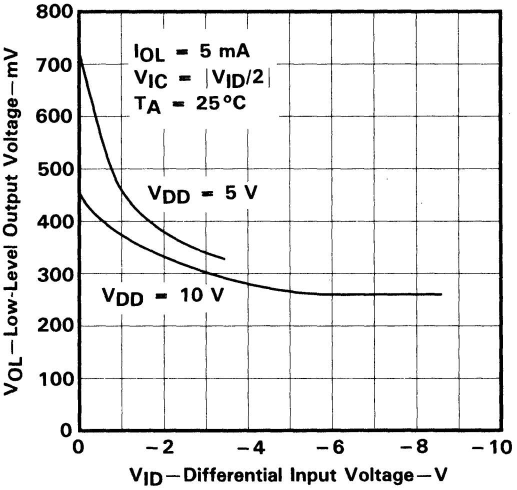

LOW-LEVEL OUTPUT VOLTAGE
vs
DIFFERENTIAL INPUT VOLTAGE

FIGURE 16

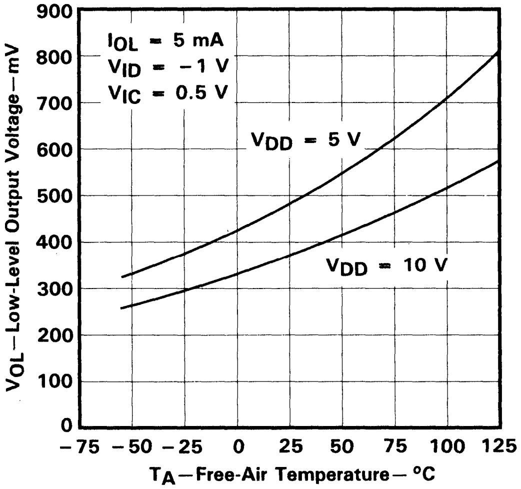

LOW-LEVEL OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

FIGURE 17

---

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

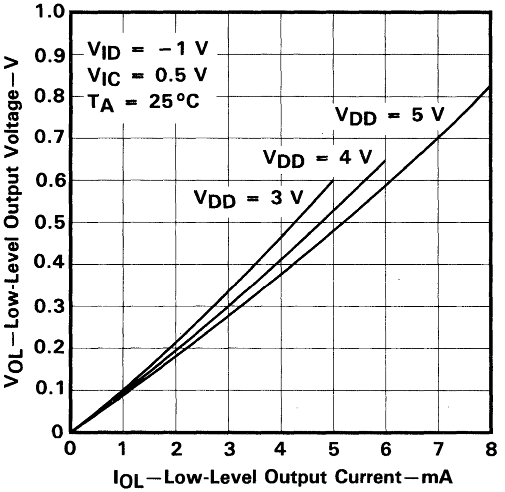

LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

FIGURE 18

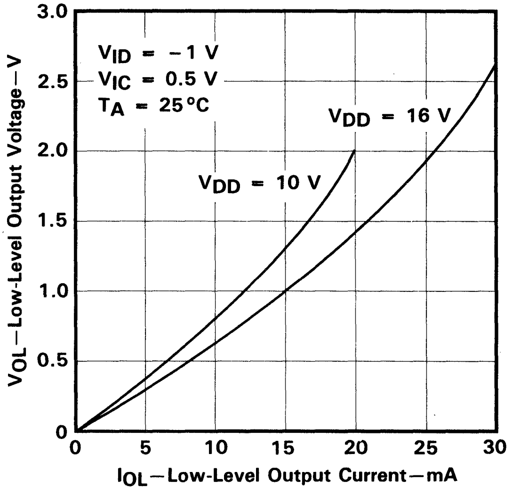

LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

FIGURE 19

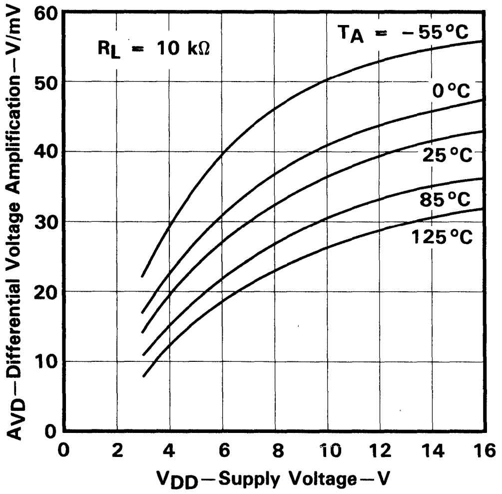

LARGE-SIGNAL
DIFFERENTIAL VOLTAGE AMPLIFICATION
vs
SUPPLY VOLTAGE

FIGURE 20

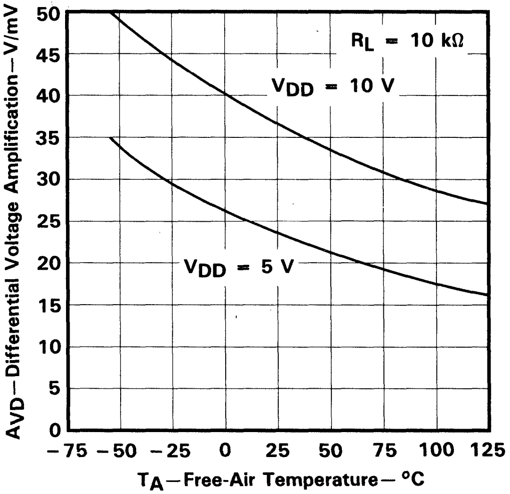

LARGE-SIGNAL
DIFFERENTIAL VOLTAGE AMPLIFICATION
vs
FREE-AIR TEMPERATURE

FIGURE 21

---

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS[†]

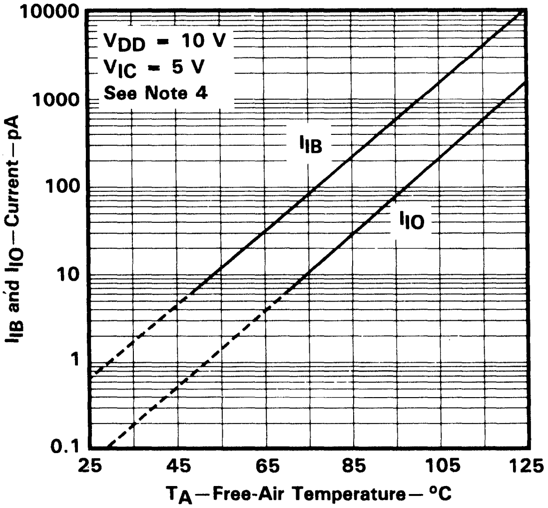

INPUT BIAS CURRENT AND INPUT OFFSET CURRENT
vs
FREE-AIR TEMPERATURE

FIGURE 22

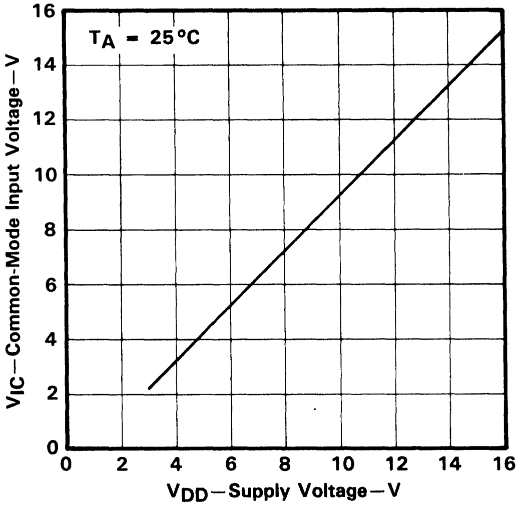

COMMON-MODE
INPUT VOLTAGE POSITIVE LIMIT
vs
SUPPLY VOLTAGE

FIGURE 23

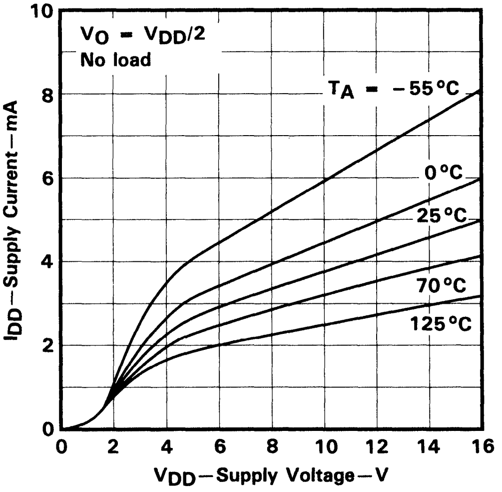

SUPPLY CURRENT
vs
SUPPLY VOLTAGE

FIGURE 24

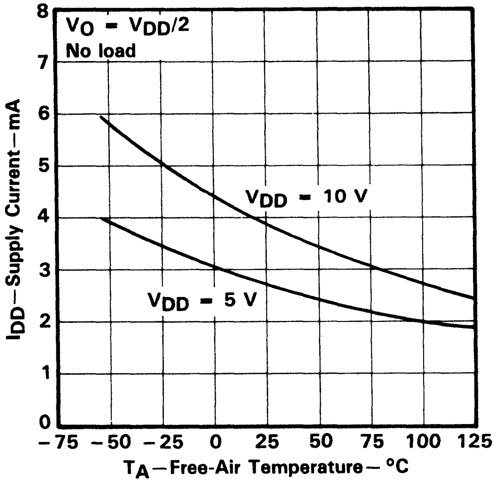

SUPPLY CURRENT
vs
FREE-AIR TEMPERATURE

FIGURE 25

[†] Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

NOTE 4: The typical values of input bias current and input offset current below 5 pA were determined mathematically.

TYPICAL CHARACTERISTICS†

SLEW RATE
vs
SUPPLY VOLTAGE

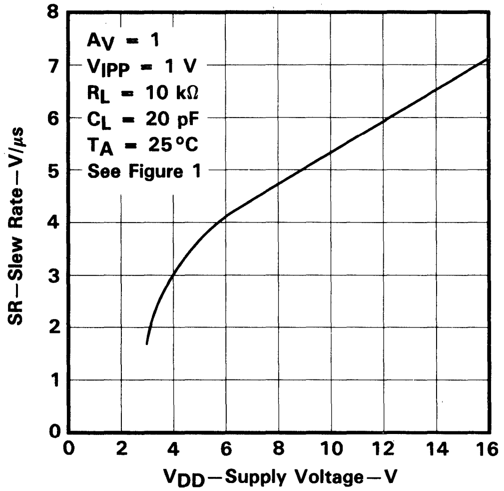


FIGURE 26

SLEW RATE
vs
FREE-AIR TEMPERATURE

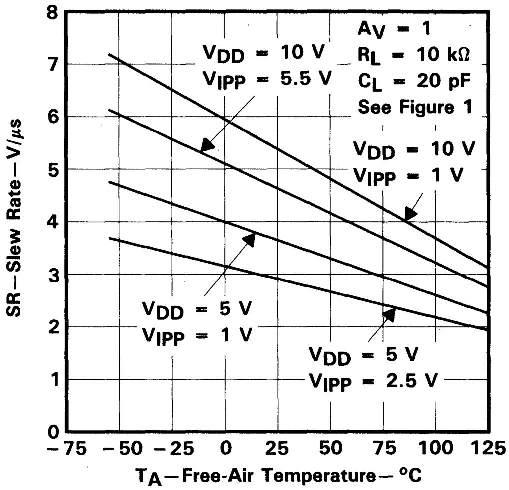


FIGURE 27

NORMALIZED SLEW RATE
vs
FREE-AIR TEMPERATURE

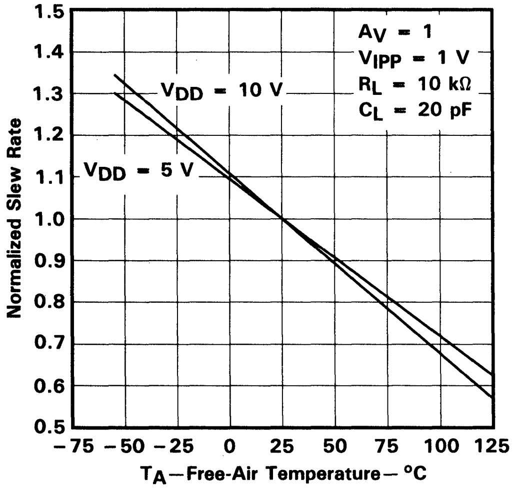


FIGURE 28

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE
vs
FREQUENCY

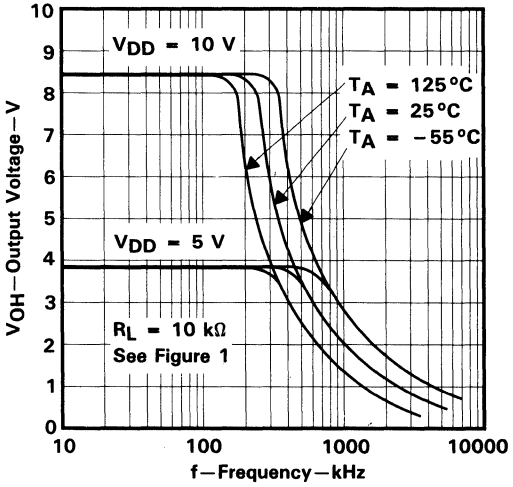


FIGURE 29

---

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS[†]

UNITY-GAIN BANDWIDTH
vs
FREE-AIR TEMPERATURE

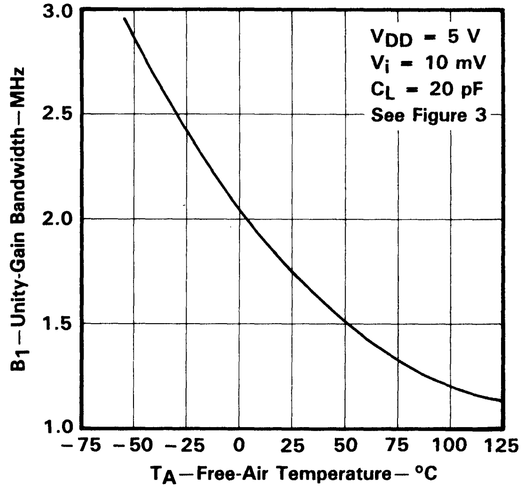


FIGURE 30

UNITY-GAIN BANDWIDTH
vs
SUPPLY VOLTAGE

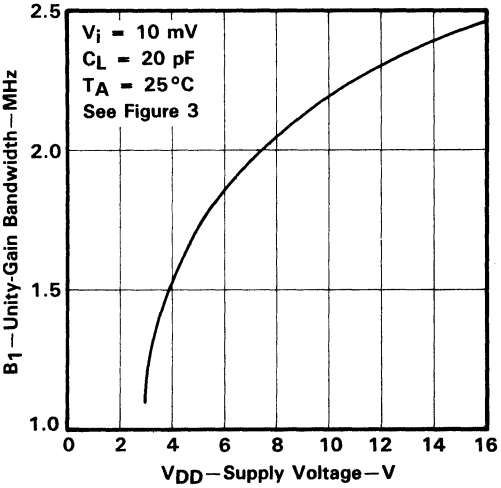


FIGURE 31

LARGE-SIGNAL DIFFERENTIAL VOLTAGE
AMPLIFICATION AND PHASE SHIFT
vs
FREQUENCY

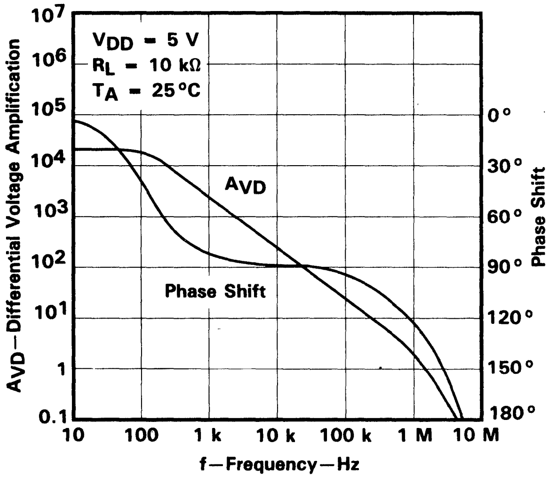


FIGURE 32

LARGE-SIGNAL DIFFERENTIAL VOLTAGE
AMPLIFICATION AND PHASE SHIFT
vs
FREQUENCY

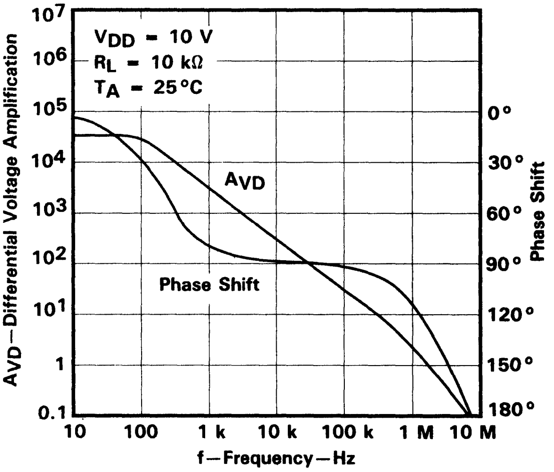


FIGURE 33

[†] Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

PHASE MARGIN
vs
SUPPLY VOLTAGE

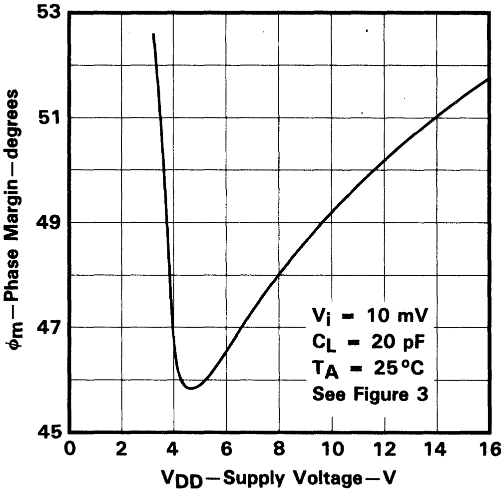


FIGURE 34

PHASE MARGIN
vs
FREE-AIR TEMPERATURE

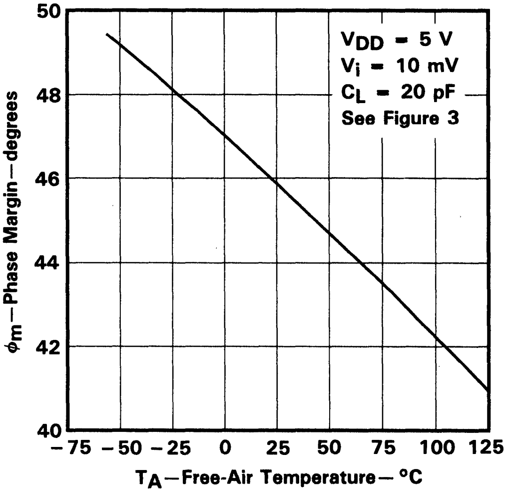


FIGURE 35

PHASE MARGIN
vs
CAPACITIVE LOAD

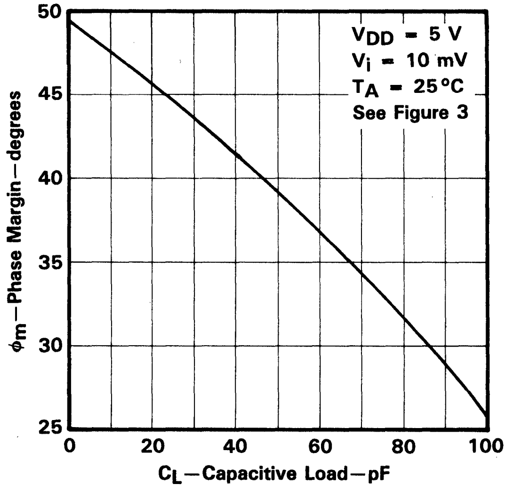


FIGURE 36

EQUIVALENT INPUT NOISE VOLTAGE
vs
FREQUENCY

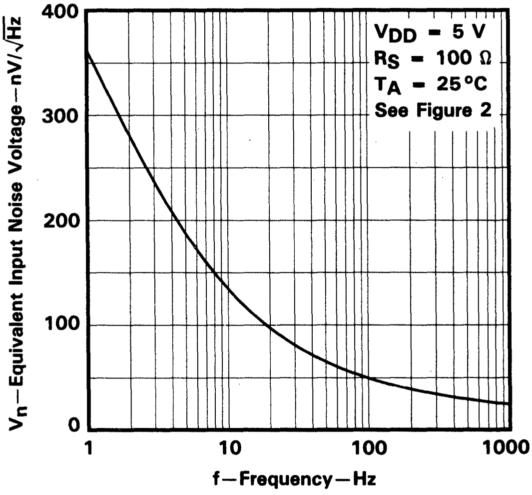


FIGURE 37

---

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL APPLICATION DATA

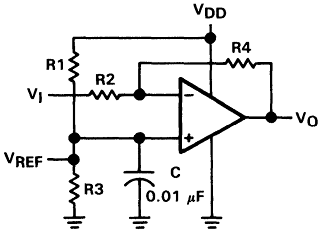
single-supply operation

While the TLC274 and TLC279 perform well using dual power supplies (also called balanced or split supplies), the design is optimized for single-supply operation. This design includes an input common-mode voltage range that encompasses ground as well as an output voltage range that pulls down to ground. The supply voltage range extends down to 3 V (C-suffix types), thus allowing operation with supply levels commonly available for TTL and HCMOS; however, for maximum dynamic range, 16-V single-supply operation is recommended.

Many single-supply applications require that a voltage be applied to one input to establish a reference level that is above ground. A resistive voltage divider is usually sufficient to establish this reference level (see Figure 38). The low input bias current of the TLC274 and TLC279 permits the use of very large resistive values to implement the voltage divider, thus minimizing power consumption.

The TLC274 and TLC279 work well in conjunction with digital logic; however, when powering both linear devices and digital logic from the same power supply, the following precautions are recommended:

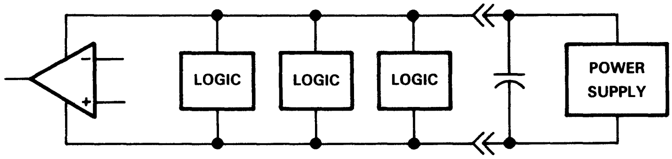
1. Power the linear devices from separate bypassed supply lines (see Figure 39); otherwise the linear device supply rails can fluctuate due to voltage drops caused by high switching currents in the digital logic.
2. Use proper bypass techniques to reduce the probability of noise-induced errors. Single capacitive decoupling is often adequate; however, high-frequency applications may require RC decoupling.



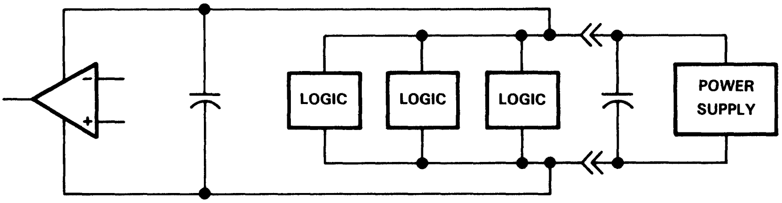
$$V_{REF} = V_{DD} \frac{R3}{R1 + R3}$$

$$V_O = \left(V_{REF} - V_I\right) \frac{R4}{R2} + V_{REF}$$

FIGURE 38. INVERTING AMPLIFIER WITH VOLTAGE REFERENCE



(a) Common Supply Rails



(b) Separate Bypassed Supply Rails (preferred)

FIGURE 39. COMMON VS SEPARATE SUPPLY RAILS

TYPICAL APPLICATION DATA

input characteristics

The TLC274 and TLC279 are specified with a minimum and a maximum input voltage that, if exceeded at either input, could cause the device to malfunction. Exceeding this specified range is a common problem, especially in single-supply operation. Note that the lower range limit includes the negative rail, while the upper range limit is specified at $V_{DD} - 1$ V at $T_A = 25\,^{\circ}C$ and at $V_{DD} - 1.5$ V at all other temperatures.

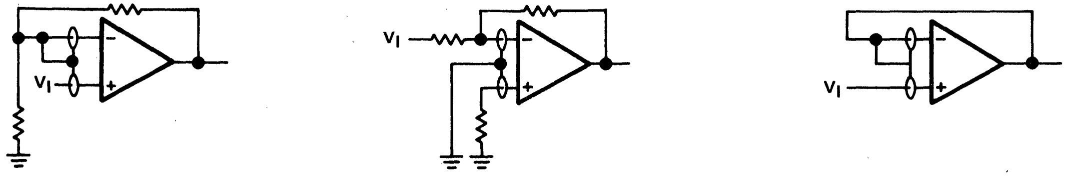
The use of the polysilicon-gate process and the careful input circuit design gives the TLC274 and TLC279 very good input offset voltage drift characteristics relative to conventional metal-gate processes. Offset voltage drift in CMOS devices is highly influenced by threshold voltage shifts caused by polarization of the phosphorus dopant implanted in the oxide. Placing the phosphorus dopant in a conductor (such as a polysilicon gate) alleviates the polarization problem, thus reducing threshold voltage shifts by more than an order of magnitude. The offset voltage drift with time has been calculated to be typically 0.1 μV/month, including the first month of operation.

Because of the extremely high input impedance and resulting low bias current requirements, the TLC274 and TLC279 are well suited for low-level signal processing; however, leakage currents on printed circuit boards and sockets can easily exceed bias current requirements and cause a degradation in device performance. It is good practice to include guard rings around inputs (similar to those of Figure 4 in the Parameter Measurement Information section). These guards should be driven from a low-impedance source at the same voltage level as the common-mode input (see Figure 40).

The inputs of any unused amplifiers should be tied to ground to avoid possible oscillation.

noise performance

The noise specifications in op amp circuits are greatly dependent on the current in the first-stage differential amplifier. The low input bias current requirements of the TLC274 and TLC279 result in a very low noise current, which is insignificant in most applications. This feature makes the devices especially favorable over bipolar devices when using values of circuit impedance greater than 50 kΩ, since bipolar devices exhibit greater noise currents.



(a) Noninverting Amplifier (b) Inverting Amplifier (c) Unity-Gain Amplifier

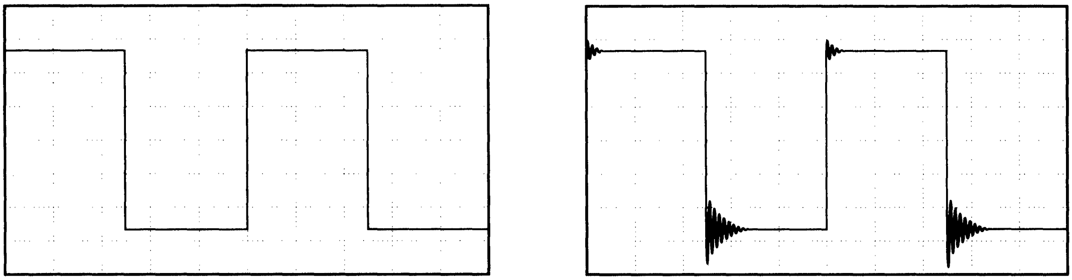
FIGURE 40. GUARD-RING SCHEMES

output characteristics

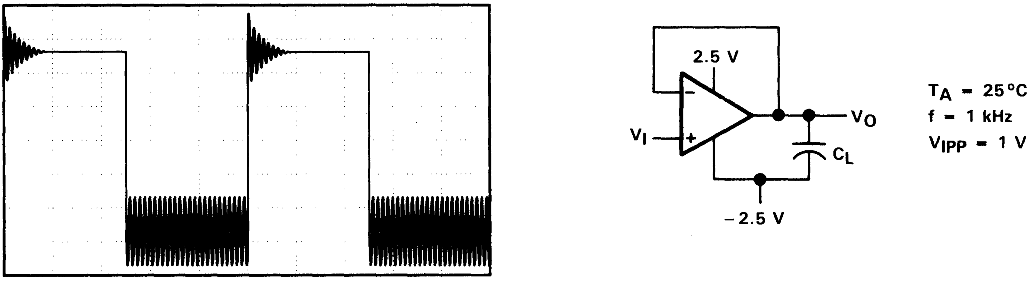
The output stage of the TLC274 and TLC279 is designed to sink and source relatively high amounts of current (see typical characteristics). If the output is subjected to a short-circuit condition, this high current capability can cause device damage under certain conditions. Output current capability increases with supply voltage.

All operating characteristics of the TLC274 and TLC279 were measured using a 20-pF load. The devices will drive higher capacitive loads; however, as output load capacitance increases, the resulting response pole occurs at lower frequencies, thereby causing ringing, peaking, or even oscillation (see Figure 41). In many cases, adding a small amount of resistance in series with the load capacitance will alleviate the problem.

TYPICAL APPLICATION DATA



(a) C_L = 20 pF, R_L = No load (b) C_L = 130 pF, R_L = No load



(c) C_L = 150 pF, R_L = No load (d) Test Circuit

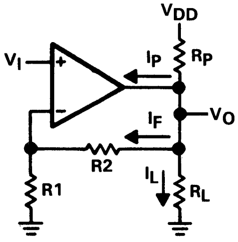
FIGURE 41. EFFECT OF CAPACITIVE LOADS AND TEST CIRCUIT

Although the TLC274 and TLC279 possess excellent high-level output voltage and current capability, methods for boosting this capability are available, if needed. The simplest method involves the use of a pullup resistor (R_P) connected from the output to the positive supply rail (see Figure 42). There are two disadvantages to the use of this circuit. First, the NMOS pulldown transistor N4 (see equivalent schematic) must sink a comparatively large amount of current. In this circuit, N4 behaves like a linear resistor with an on-resistance between approximately 60 Ω and 180 Ω, depending on how hard the op amp input is driven. With very low values of R_P, a voltage offset from 0 V at the output will occur. Second, pullup resistor R_P acts as a drain load to N4 and the gain of the op amp is reduced at output voltage levels where N5 is not supplying the output current.

feedback

Op amp circuits nearly always employ feedback, and since feedback is the first prerequisite for oscillation, some caution is appropriate. Most oscillation problems result from driving capacitive loads (discussed previously) and ignoring stray input capacitance. A small-value capacitor connected in parallel with the feedback resistor is an effective remedy (see Figure 43). The value of this capacitor is optimized empirically.

TYPICAL APPLICATION DATA



$$R_P = \frac{V_{DD} - V_O}{I_F + I_L + I_P}$$

I_P = Pullup current required by the op amp (typically 500 μA)

FIGURE 42. RESISTIVE PULLUP TO INCREASE V_{OH}

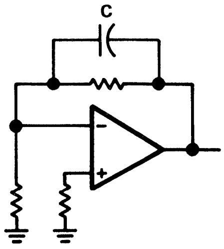


FIGURE 43. COMPENSATION FOR INPUT CAPACITANCE

electrostatic discharge protection

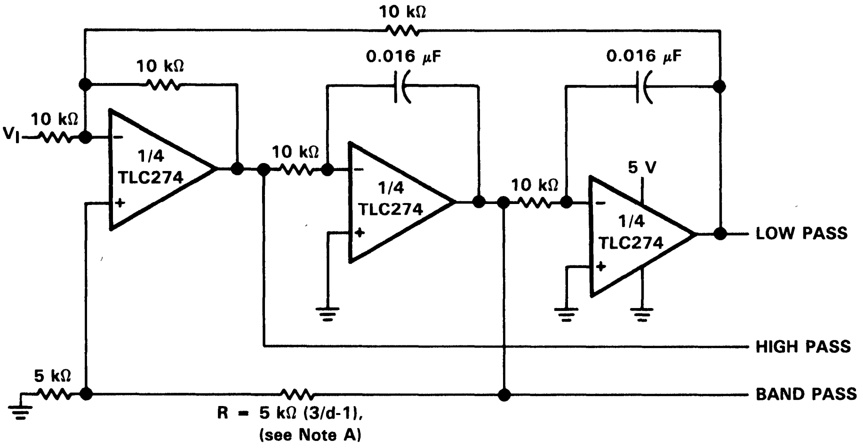
The TLC274 and TLC279 incorporate an internal electrostatic discharge (ESD) protection circuit that prevents functional failures at voltages up to 2000 V as tested under MIL-STD-883C, Method 3015.2. Care should be exercised, however, when handling these devices as exposure to ESD may result in the degradation of the device parametric performance. The protection circuit also causes the input bias currents to be temperature-dependent and have the characteristics of a reverse-biased diode.

latch-up

Because CMOS devices are susceptible to latch-up due to their inherent parasitic thyristors, the TLC274 and TLC279 inputs and outputs were designed to withstand −100-mA surge currents without sustaining latch-up; however, techniques should be used to reduce the chance of latch-up whenever possible. Internal protection diodes should not, by design, be forward biased. Applied input and output voltage should not exceed the supply voltage by more than 300 mV. Care should be exercised when using capacitive coupling on pulse generators. Supply transients should be shunted by the use of decoupling capacitors (0.1 μF typical) located across the supply rails as close to the device as possible.

The current path established if latch-up occurs is usually between the positive supply rail and ground and can be triggered by surges on the supply lines and/or voltages on either the output or inputs that exceed the supply voltage. Once latch-up occurs, the current flow is limited only by the impedance of the power supply and the forward resistance of the parasitic thyristor and usually results in the destruction of the device. The chance of latch-up occurring increases with increasing temperature and supply voltages.

TYPICAL APPLICATION DATA



NOTES: A. d = damping factor, 1/Q
B. Normalized to 10 kΩ and f_C = 1 kHz

FIGURE 44. STATE VARIABLE FILTER

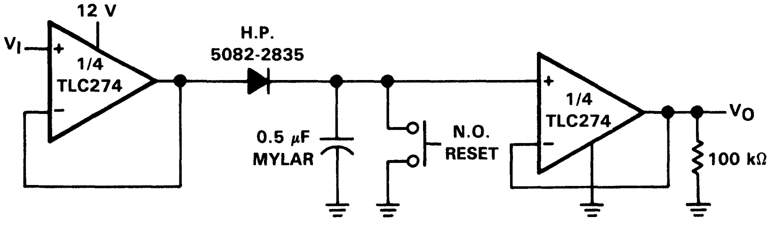
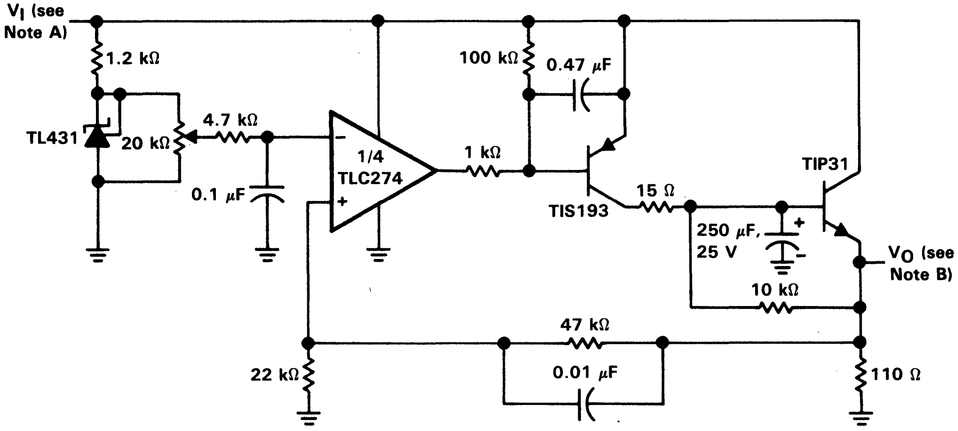


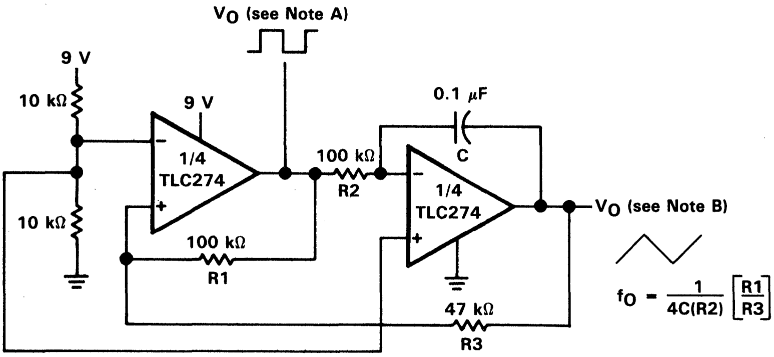
FIGURE 45. POSITIVE-PEAK DETECTOR

TYPICAL APPLICATION DATA



NOTES: A. V_I = 3.5 to 15 V
B. V_O = 2.0 V, 0 to 1 A

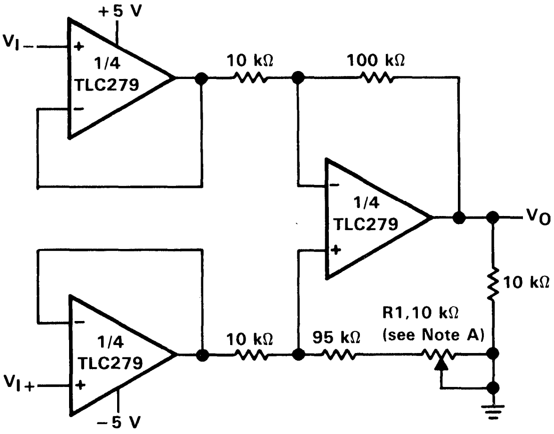
FIGURE 46. LOGIC ARRAY POWER SUPPLY



NOTES: A. V_{OPP} = 8 V
B. V_{OPP} = 4 V

FIGURE 47. SINGLE-SUPPLY FUNCTION GENERATOR

TYPICAL APPLICATION DATA



NOTE A: CMRR adjustment (must be noninductive).

FIGURE 48. LOW-POWER INSTRUMENTATION AMPLIFIER

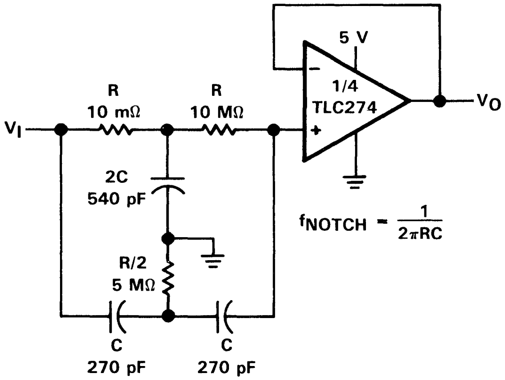


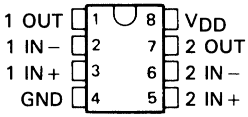
FIGURE 49. SINGLE-SUPPLY TWIN-T NOTCH FILTER

TLC27L2, TLC27L2A, TLC27L2B, TLC27L7
LinCMOS™ PRECISION DUAL OPERATIONAL AMPLIFIERS

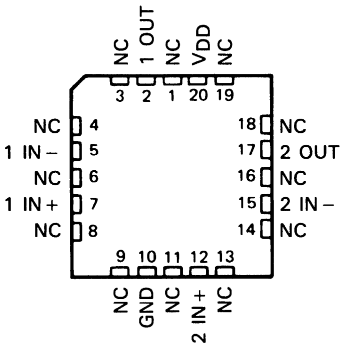
D3139, OCTOBER 1987—REVISED OCTOBER 1990

- **Trimmed Offset Voltage:**
  TLC27L7 . . . 500 μV Max at 25°C,
  V_{DD} = 5 V
- **Input Offset Voltage Drift . . . Typically 0.1 μV/Month, Including the First 30 Days**
- **Wide Range of Supply Voltages over Specified Temperature Range:**
  0°C to 70°C . . . 3 V to 16 V
  −40°C to 85°C . . . 4 V to 16 V
  −55°C to 125°C . . . 4 V to 16 V
- **Single-Supply Operation**
- **Common-Mode Input Voltage Range Extends Below the Negative Rail (C-Suffix, I-Suffix types)**
- **Ultralow Power . . . Typically 95 μW at 25°C, V_{DD} = 5 V**
- **Output Voltage Range Includes Negative Rail**
- **High Input Impedance . . . 10^{12} Ω Typical**
- **ESD-Protection Circuitry**
- **Small-Outline Package Option Also Available in Tape and Reel**
- **Designed-In Latch-Up Immunity**

D, JG, OR P PACKAGE
(TOP VIEW)



FK PACKAGE
(TOP VIEW)



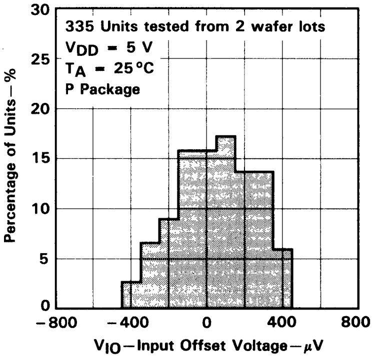
NC—No internal connection

AVAILABLE OPTIONS

T_A	V_{IO}max at 25°C	PACKAGE			
		SMALL OUTLINE (D)	CHIP CARRIER (FK)	CERAMIC DIP (JG)	PLASTIC DIP (P)
0°C to 70°C	500 μV	TLC27L7CD	—	—	TLC27L7CP
	2 mV	TLC27L2BCD	—	—	TLC27L2BCP
	5 mV	TLC27L2ACD	—	—	TLC27L2ACP
	10 mV	TLC27L2CD	—	—	TLC27L2CP
−40°C to 85°C	500 μV	TLC27L7ID	—	—	TLC27L7IP
	2 mV	TLC27L2BID	—	—	TLC27L2BIP
	5 mV	TLC27L2AID	—	—	TLC27L2AIP
	10 mV	TLC27L2ID	—	—	TLC27L2IP
−55°C to 125°C	500 μV	TLC27L7MD	TLC27L7MFK	TLC27L7MJG	TLC27L7MP
	10 mV	TLC27L2MD	TLC27L2MFK	TLC27L2MJG	TLC27L2MP

The D package is available in tape and reel. Add R suffix to the device type, (e.g., TLC27L7CDR).

DISTRIBUTION OF TLC27L7
INPUT OFFSET VOLTAGE



LinCMOS is a trademark of Texas Instruments Incorporated

description

The TLC27L2 and TLC27L7 dual operational amplifiers combine a wide range of input offset voltage grades with low offset voltage drift, high input impedance, extremely low power, and high gain.

These devices use Texas Instruments silicon-gate LinCMOS™ technology, which provides offset voltage stability far exceeding the stability available with conventional metal-gate processes.

The extremely high input impedance, low bias currents, and low power consumption make these cost-effective devices ideal for high gain, low frequency, low power applications. Four offset voltage grades are available (C-suffix and I-suffix types), ranging from the low-cost TLC27L2 (10 mV) to the high-precision TLC27L7 (500 μV). These advantages, in combination with good common-mode rejection and supply voltage rejection, make these devices a good choice for new state-of-the-art designs as well as for upgrading existing designs.

In general, many features associated with bipolar technology are available on LinCMOS™ operational amplifiers, without the power penalties of bipolar technology. General applications such as transducer interfacing, analog calculations, amplifier blocks, active filters, and signal buffering are easily designed with the TLC27L2 and TLC27L7. The devices also exhibit low voltage single-supply operation and ultra-low power consumption, making them ideally suited for remote and inaccessible battery-powered applications. The common-mode input voltage range includes the negative rail.

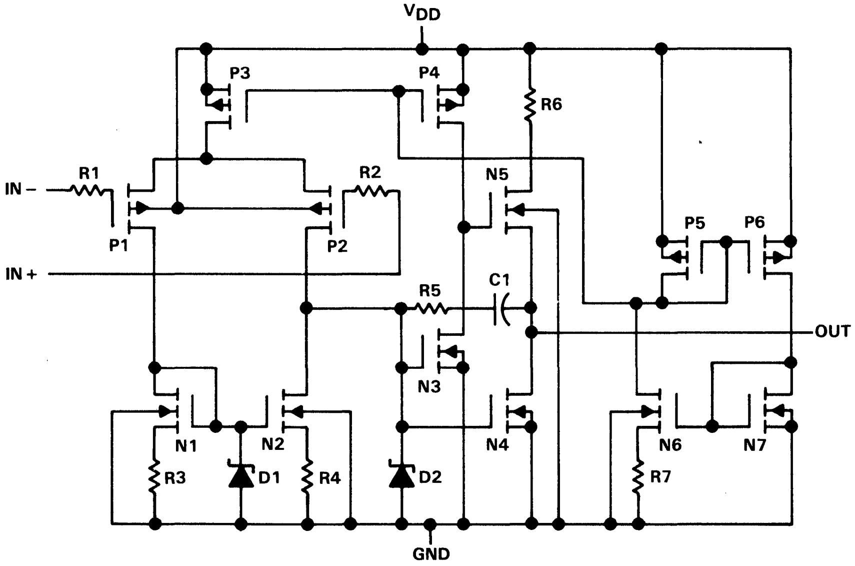
A wide range of packaging options is available, including small-outline and chip carrier versions for high-density system applications.

The device inputs and outputs are designed to withstand −100-mA surge currents without sustaining latch-up.

The TLC27L2 and TLC27L7 incorporate internal ESD-protection circuits that prevent functional failures at voltages up to 2000 V as tested under MIL-STD-883C, Method 3015.2; however, care should be exercised in handling these devices as exposure to ESD may result in the degradation of the device parametric performance.

C-suffix devices are characterized for operation from 0 °C to 70 °C. I-suffix devices are characterized for operation from −40 °C to 85 °C. M-suffix devices are characterized for operation over the full military temperature range of −55 °C to 125 °C.

equivalent schematic (each amplifier)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{DD} (see Note 1)	18 V
Differential input voltage (see Note 2)	$\pm V_{DD}$
Input voltage range, V_I (any input)	-0.3 V to V_{DD}
Input current, I_I	±5 mA
Output current, I_O (each output)	±30 mA
Total current into V_{DD} terminal	45 mA
Total current out of ground terminal	45 mA
Duration of short-circuit current at (or below) 25°C (see Note 3)	Unlimited
Continuous total dissipation	See Dissipation Rating Table
Operating free-air temperature, T_A: C-suffix	0°C to 70°C
I-suffix	−40°C to 85°C
M-suffix	−55°C to 125°C
Storage temperature range	−65°C to 150°C
Case temperature for 60 seconds: FK package	260°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D and P package	260°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: JG package	300°C

NOTES: 1. All voltage values, except differential voltages, are with respect to network ground.
2. Differential voltages are at the noninverting input with respect to the inverting input.
3. The output may be shorted to either supply. Temperature and/or supply voltages must be limited to ensure that the maximum dissipation rating is not exceeded (see application section).

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING	$T_A = 125°C$ POWER RATING
D	725 mW	5.8 mW/°C	464 mW	377 mW	
FK	1375 mW	11 mW/°C	880 mW	715 mW	275 mW
JG	1050 mW	8.4 mW/°C	672 mW	546 mW	210 mW
P	1000 mW	8.0 mW/°C	640 mW	520 mW	

recommended operating conditions

		C-SUFFIX			I-SUFFIX			M-SUFFIX			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{DD}		3		16	4		16	4		16	V
Common-mode input voltage, V_{IC}	$V_{DD} = 5$ V	−0.2		3.5	−0.2		3.5	0		3.5	V
	$V_{DD} = 10$ V	−0.2		8.5	−0.2		8.5	0		8.5	
Operating free-air temperature, T_A		0		70	−40		85	−55		125	°C

electrical characteristics at specified free-air temperature, V_{DD} = 5 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS	T_A†	MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	TLC27L2C	V_O = 1.4 V, V_{IC} = 0, R_S = 50 Ω, R_L = 1 MΩ	25°C		1.1	10	mV
				Full range			12	
		TLC27L2AC	V_O = 1.4 V, V_{IC} = 0, R_S = 50 Ω, R_L = 1 MΩ	25°C		0.9	5	
				Full range			6.5	
		TLC27L2BC	V_O = 1.4 V, V_{IC} = 0, R_S = 50 Ω, R_L = 1 MΩ	25°C		204	2000	μV
				Full range			3000	
		TLC27L7C	V_O = 1.4 V, V_{IC} = 0, R_S = 50 Ω, R_L = 1 MΩ	25°C		170	500	
				Full range			1500	
α_{VIO}	Average temperature coefficient of input offset voltage			25°C to 70°C		1.1		μV/°C
I_{IO}	Input offset current (see Note 4)		V_O = 2.5 V, V_{IC} = 2.5 V	25°C		0.1		pA
				70°C		7	300	
I_{IB}	Input bias current (see Note 4)		V_O = 2.5 V, V_{IC} = 2.5 V	25°C		0.6		pA
				70°C		50	600	
V_{ICR}	Common-mode input voltage range (see Note 5)			25°C	−0.2 to 4	−0.3 to 4.2		V
				Full range	−0.2 to 3.5			V
V_{OH}	High-level output voltage		V_{ID} = 100 mV, R_L = 1 MΩ	25°C	3.2	4.1		V
				0°C	3	4.1		
				70°C	3	4.2		
V_{OL}	Low-level output voltage		V_{ID} = −100 mV, I_{OL} = 0	25°C		0	50	mV
				0°C		0	50	
				70°C		0	50	
A_{VD}	Large-signal differential voltage amplification		V_O = 0.25 V to 2 V, R_L = 1 MΩ	25°C	50	700		V/mV
				0°C	50	700		
				70°C	50	380		
CMRR	Common-mode rejection ratio		V_{IC} = V_{ICR} min	25°C	65	94		dB
				0°C	60	95		
				70°C	60	95		
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)		V_{DD} = 5 V to 10 V, V_O = 1.4 V	25°C	70	97		dB
				0°C	60	97		
				70°C	60	98		
I_{DD}	Supply current (two amplifiers)		V_O = 2.5 V, V_{IC} = 2.5 V, No load	25°C		20	34	μA
				0°C		24	42	
				70°C		16	28	

†Full range is 0°C to 70°C.

NOTES: 4. The typical values of input bias current and input offset current below 5 pA were determined mathematically.
5. This range also applies to each input individually.

electrical characteristics at specified free-air temperature, V_{DD} = 10 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS	T_A†	MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	TLC27L2C	V_O = 1.4 V, V_{IC} = 0, R_S = 50 Ω, R_L = 1 MΩ	25°C		1.1	10	mV
				Full range			12	
		TLC27L2AC	V_O = 1.4 V, V_{IC} = 0, R_S = 50 Ω, R_L = 1 MΩ	25°C		0.9	5	
				Full range			6.5	
		TLC27L2BC	V_O = 1.4 V, V_{IC} = 0, R_S = 50 Ω, R_L = 1 MΩ	25°C		235	2000	μV
				Full range			3000	
		TLC27L7C	V_O = 1.4 V, V_{IC} = 0, R_S = 50 Ω, R_L = 1 MΩ	25°C		190	800	
				Full range			1900	
α_{VIO}	Average temperature coefficient of input offset voltage			25°C to 70°C		1		μV/°C
I_{IO}	Input offset current (see Note 4)		V_O = 5 V, V_{IC} = 5 V	25°C		0.1		pA
				70°C		8	300	
I_{IB}	Input bias current (see Note 4)		V_O = 5 V, V_{IC} = 5 V	25°C		0.7		pA
				70°C		50	600	
V_{ICR}	Common-mode input voltage range (see Note 5)			25°C	−0.2 to 9	−0.3 to 9.2		V
				Full range	−0.2 to 8.5			V
V_{OH}	High-level output voltage		V_{ID} = 100 mV, R_L = 1 MΩ	25°C	8	8.9		V
				0°C	7.8	8.9		
				70°C	7.8	8.9		
V_{OL}	Low-level output voltage		V_{ID} = −100 mV, I_{OL} = 0	25°C		0	50	mV
				0°C		0	50	
				70°C		0	50	
A_{VD}	Large-signal differential voltage amplification		V_O = 1 V to 6 V, R_L = 1 MΩ	25°C	50	860		V/mV
				0°C	50	1025		
				70°C	50	660		
CMRR	Common-mode rejection ratio		V_{IC} = V_{ICR} min	25°C	65	97		dB
				0°C	60	97		
				70°C	60	97		
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)		V_{DD} = 5 V to 10 V, V_O = 1.4 V	25°C	70	97		dB
				0°C	60	97		
				70°C	60	98		
I_{DD}	Supply current (two amplifiers)		V_O = 5 V, V_{IC} = 5 V, No load	25°C		29	46	μA
				0°C		36	66	
				70°C		22	40	

†Full range is 0°C to 70°C.

NOTES: 4. The typical values of input bias current and input offset current below 5 pA were determined mathematically.

5. This range also applies to each input individually.

electrical characteristics at specified free-air temperature, V_{DD} = 5 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS	T_A†	MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	TLC27L2I	V_O = 1.4 V, V_{IC} = 0, R_S = 50 Ω, R_L = 1 MΩ	25°C		1.1	10	mV
				Full range			13	
		TLC27L2AI	V_O = 1.4 V, V_{IC} = 0, R_S = 50 Ω, R_L = 1 MΩ	25°C		0.9	5	
				Full range			7	
		TLC27L2BI	V_O = 1.4 V, V_{IC} = 0, R_S = 50 Ω, R_L = 1 MΩ	25°C		240	2000	μV
				Full range			3500	
		TLC27L7I	V_O = 1.4 V, V_{IC} = 0, R_S = 50 Ω, R_L = 1 MΩ	25°C		200	900	
				Full range			2000	
α_{VIO}	Average temperature coefficient of input offset voltage			25°C to 85°C		1.1		μV/°C
I_{IO}	Input offset current (see Note 4)		V_O = 2.5 V, V_{IC} = 2.5 V	25°C		0.1		pA
				85°C		24	1000	
I_{IB}	Input bias current (see Note 4)		V_O = 2.5 V, V_{IC} = 2.5 V	25°C		0.6		pA
				85°C		200	2000	
V_{ICR}	Common-mode input voltage range (see Note 5)			25°C	−0.2 to 4	−0.3 to 4.2		V
				Full range	−0.2 to 3.5			V
V_{OH}	High-level output voltage		V_{ID} = 100 mV, R_L = 1 MΩ	25°C	3.2	4.1		V
				−40°C	3	4.1		
				85°C	3	4.2		
V_{OL}	Low-level output voltage		V_{ID} = −100 mV, I_{OL} = 0	25°C		0	50	mV
				−40°C		0	50	
				85°C		0	50	
A_{VD}	Large-signal differential voltage amplification		V_O = 0.25 V to 2 V, R_L = 1 MΩ	25°C	50	480		V/mV
				−40°C	50	900		
				85°C	50	330		
CMRR	Common-mode rejection ratio		V_{IC} = V_{ICR} min	25°C	65	94		dB
				−40°C	60	95		
				85°C	60	95		
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)		V_{DD} = 5 V to 10 V, V_O = 1.4 V	25°C	70	97		dB
				−40°C	60	97		
				85°C	60	98		
I_{DD}	Supply current (two amplifiers)		V_O = 2.5 V, V_{IC} = 2.5 V, No load	25°C		20	34	μA
				−40°C		31	54	
				85°C		15	26	

†Full range is −40°C to 85°C.

NOTES: 4. The typical values of input bias current and input offset current below 5 pA were determined mathematically.
5. This range also applies to each input individually.

electrical characteristics at specified free-air temperature, V_{DD} = 10 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS		T_A†	MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	TLC27L2I	V_O = 1.4 V,	V_{IC} = 0,	25°C		1.1	10	mV
			R_S = 50 Ω,	R_L = 1 MΩ	Full range			13	
		TLC27L2AI	V_O = 1.4 V,	V_{IC} = 0,	25°C		0.9	5	
			R_S = 50 Ω,	R_L = 1 MΩ	Full range			7	
		TLC27L2BI	V_O = 1.4 V,	V_{IC} = 0,	25°C		235	2000	µV
			R_S = 50 Ω,	R_L = 1 MΩ	Full range			3500	
		TLC27L7I	V_O = 1.4 V,	V_{IC} = 0,	25°C		190	800	
			R_S = 50 Ω,	R_L = 1 MΩ	Full range			2900	
α_{VIO}	Average temperature coefficient of input offset voltage				25°C to 85°C		1		µV/°C
I_{IO}	Input offset current (see Note 4)		V_O = 5 V,	V_{IC} = 5 V	25°C		0.1		pA
					85°C		26	1000	
I_{IB}	Input bias current (see Note 4)		V_O = 5 V,	V_{IC} = 5 V	25°C		0.7		pA
					85°C		220	2000	
V_{ICR}	Common-mode input voltage range (see Note 5)				25°C	−0.2 to 9	−0.3 to 9.2		V
					Full range	−0.2 to 8.5			V
V_{OH}	High-level output voltage		V_{ID} = 100 mV,	R_L = 1 MΩ	25°C	8	8.9		V
					−40°C	7.8	8.9		
					85°C	7.8	8.9		
V_{OL}	Low-level output voltage		V_{ID} = −100 mV,	I_{OL} = 0	25°C		0	50	mV
					−40°C		0	50	
					85°C		0	50	
A_{VD}	Large-signal differential voltage amplification		V_O = 1 V to 6 V,	R_L = 1 MΩ	25°C	50	860		V/mV
					−40°C	50	1550		
					85°C	50	585		
CMRR	Common-mode rejection ratio		V_{IC} = V_{ICR} min		25°C	65	97		dB
					−40°C	60	97		
					85°C	60	98		
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)		V_{DD} = 5 V to 10 V,	V_O = 1.4 V	25°C	70	97		dB
					−40°C	60	97		
					85°C	60	98		
I_{DD}	Supply current (two amplifiers)		V_O = 5 V, No load	V_{IC} = 5 V,	25°C		29	46	µA
					−40°C		49	86	
					85°C		20	36	

† Full range is −40°C to 85°C.

NOTES: 4. The typical values of input bias current and input offset current below 5 pA were determined mathematically.
5. This range also applies to each input individually.

electrical characteristics at specified free-air temperature, V_{DD} = 5 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS	T_A†	MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	TLC27L2M	V_O = 1.4 V, V_{IC} = 0, R_S = 50 Ω, R_L = 1 MΩ	25°C		1.1	10	mV
				Full range			12	
		TLC27L7M	V_O = 1.4 V, V_{IC} = 0, R_S = 50 Ω, R_L = 1 MΩ	25°C		170	500	µV
				Full range			3750	
α_{VIO}	Average temperature coefficient of input offset voltage			25°C to 125°C		1.4		µV/°C
I_{IO}	Input offset current (see Note 4)		V_O = 2.5 V, V_{IC} = 2.5 V	25°C		0.1		pA
				125°C		1.4	15	nA
I_{IB}	Input bias current (see Note 4)		V_O = 2.5 V, V_{IC} = 2.5 V	25°C		0.6		pA
				125°C		9	35	nA
V_{ICR}	Common-mode input voltage range (see Note 5)			25°C	0 to 4	−0.3 to 4.2		V
				Full range	0 to 3.5			V
V_{OH}	High-level output voltage		V_{ID} = 100 mV, R_L = 1 MΩ	25°C	3.2	4.1		V
				−55°C	3	4.1		
				125°C	3	4.2		
V_{OL}	Low-level output voltage		V_{ID} = −100 mV, I_{OL} = 0	25°C		0	50	mV
				−55°C		0	50	
				125°C		0	50	
A_{VD}	Large-signal differential voltage amplification		V_O = 0.25 V to 2 V, R_L = 1 MΩ	25°C	50	500		V/mV
				−55°C	25	1000		
				125°C	25	200		
CMRR	Common-mode rejection ratio		V_{IC} = V_{ICR} min	25°C	65	94		dB
				−55°C	60	95		
				125°C	60	85		
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)		V_{DD} = 5 V to 10 V, V_O = 1.4 V	25°C	70	97		dB
				−55°C	60	97		
				125°C	60	98		
I_{DD}	Supply current (two amplifiers)		V_O = 2.5 V, V_{IC} = 2.5 V, No load	25°C		20	34	µA
				−55°C		35	60	
				125°C		14	24	

†Full range is −55°C to 125°C.

NOTES: 4. The typical values of input bias current and input offset current below 5 pA were determined mathematically.

5. This range also applies to each input individually.

electrical characteristics at specified free-air temperature, V_{DD} = 10 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS		T_A†	MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	TLC27L2M	V_O = 1.4 V, R_S = 50 Ω,	V_{IC} = 0, R_L = 1 MΩ	25°C		1.1	10	mV
					Full range			12	
		TLC27L7M	V_O = 1.4 V, R_S = 50 Ω,	V_{IC} = 0, R_L = 1 MΩ	25°C		190	800	µV
					Full range			4300	
α_{VIO}	Average temperature coefficient of input offset voltage				25°C to 125°C		1.4		µV/°C
I_{IO}	Input offset current (see Note 4)		V_O = 5 V,	V_{IC} = 5 V	25°C		0.1		pA
					125°C		1.8	15	nA
I_{IB}	Input bias current (see Note 4)		V_O = 5 V,	V_{IC} = 5 V	25°C		0.7		pA
					125°C		10	35	nA
V_{ICR}	Common-mode input voltage range (see Note 5)				25°C	0 to 9	−0.3 to 9.2		V
					Full range	0 to 8.5			V
V_{OH}	High-level output voltage		V_{ID} = 100 mV,	R_L = 1 MΩ	25°C	8	8.9		V
					−55°C	7.8	8.8		
					125°C	7.8	9		
V_{OL}	Low-level output voltage		V_{ID} = −100 mV,	I_{OL} = 0	25°C		0	50	mV
					−55°C		0	50	
					125°C		0	50	
A_{VD}	Large-signal differential voltage amplification		V_O = 1 V to 6 V,	R_L = 1 MΩ	25°C	50	860		V/mV
					−55°C	25	1750		
					125°C	25	380		
CMRR	Common-mode rejection ratio		$V_{IC} = V_{ICR}$ min		25°C	65	97		dB
					−55°C	60	97		
					125°C	60	91		
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)		V_{DD} = 5 V to 10 V,	V_O = 1.4 V	25°C	70	97		dB
					−55°C	60	97		
					125°C	60	98		
I_{DD}	Supply current (two amplifiers)		V_O = 5 V, No load	V_{IC} = 5 V,	25°C		29	46	µA
					−55°C		56	96	
					125°C		18	30	

†Full range is −55°C to 125°C.

NOTES: 4. The typical values of input bias current and input offset current below 5 pA were determined mathematically.
5. This range also applies to each input individually.

operating characteristics, V_{DD} = 5 V

PARAMETER		TEST CONDITIONS		T_A	MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain	R_L = 1 MΩ, C_L = 20 pF, See Figure 1	V_{IPP} = 1 V	25°C		0.03		V/μs
				0°C		0.04		
				70°C		0.03		
			V_{IPP} = 2.5 V	25°C		0.03		
				0°C		0.03		
				70°C		0.02		
V_n	Equivalent input noise voltage	f = 1 kHz, See Figure 2	R_S = 100 Ω,	25°C		68		nV/$\sqrt{Hz}$
B_{OM}	Maximum output swing bandwidth	V_O = V_{OH}, R_L = 1 MΩ,	C_L = 20 pF, See Figure 1	25°C		5		kHz
				0°C		6		
				70°C		4.5		
B_1	Unity-gain bandwidth	V_i = 10 mV, See Figure 3	C_L = 20 pF,	25°C		85		kHz
				0°C		100		
				70°C		65		
ϕ_m	Phase margin	V_i = 10 mV, C_L = 20 pF,	f = B_1, See Figure 3	25°C		34°		
				0°C		36°		
				70°C		30°		

operating characteristics, V_{DD} = 10 V

PARAMETER		TEST CONDITIONS		T_A	MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain	R_L = 1 MΩ, C_L = 20 pF, See Figure 1	V_{IPP} = 1 V	25°C		0.05		V/μs
				0°C		0.05		
				70°C		0.04		
			V_{IPP} = 5.5 V	25°C		0.04		
				0°C		0.05		
				70°C		0.04		
V_n	Equivalent input noise voltage	f = 1 kHz, See Figure 2	R_S = 100 Ω,	25°C		68		nV/$\sqrt{Hz}$
B_{OM}	Maximum output swing bandwidth	V_O = V_{OH}, R_L = 1 MΩ,	C_L = 20 pF, See Figure 1	25°C		1		kHz
				0°C		1.3		
				70°C		0.9		
B_1	Unity-gain bandwidth	V_i = 10 mV, See Figure 3	C_L = 20 pF,	25°C		110		kHz
				0°C		125		
				70°C		90		
ϕ_m	Phase margin	V_i = 10 mV, C_L = 20 pF,	f = B_1, See Figure 3	25°C		38°		
				0°C		40°		
				70°C		34°		

operating characteristics, V_{DD} = 5 V

PARAMETER		TEST CONDITIONS		T_A	MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain	R_L = 1 MΩ, C_L = 20 pF, See Figure 1	V_{IPP} = 1 V	25°C		0.03		V/μs
				−40°C		0.04		
				85°C		0.03		
			V_{IPP} = 2.5 V	25°C		0.03		
				−40°C		0.04		
				85°C		0.02		
V_n	Equivalent input noise voltage	f = 1 kHz, See Figure 2	R_S = 100 Ω,	25°C		68		nV/√Hz
B_{OM}	Maximum output swing bandwidth	$V_O = V_{OH}$, R_L = 1 MΩ,	C_L = 20 pF, See Figure 1	25°C		5		kHz
				−40°C		7		
				85°C		4		
B_1	Unity-gain bandwidth	V_i = 10 mV, See Figure 3	C_L = 20 pF,	25°C		85		kHz
				−40°C		130		
				85°C		55		
ϕ_m	Phase margin	V_i = 10 mV, C_L = 20 pF,	f = B_1, See Figure 3	25°C		34°		
				−40°C		38°		
				85°C		29°		

operating characteristics, V_{DD} = 10 V

PARAMETER		TEST CONDITIONS		T_A	MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain	R_L = 1 MΩ, C_L = 20 pF, See Figure 1	V_{IPP} = 1 V	25°C		0.05		V/μs
				−40°C		0.06		
				85°C		0.03		
			V_{IPP} = 5.5 V	25°C		0.04		
				−40°C		0.05		
				85°C		0.03		
V_n	Equivalent input noise voltage	f = 1 kHz, See Figure 2	R_S = 100 Ω,	25°C		68		nV/√Hz
B_{OM}	Maximum output swing bandwidth	$V_O = V_{OH}$, R_L = 1 MΩ,	C_L = 20 pF, See Figure 1	25°C		1		kHz
				−40°C		1.4		
				85°C		0.8		
B_1	Unity-gain bandwidth	V_i = 10 mV, See Figure 3	C_L = 20 pF,	25°C		110		kHz
				−40°C		155		
				85°C		80		
ϕ_m	Phase margin	V_i = 10 mV, C_L = 20 pF,	f = B_1, See Figure 3	25°C		38°		
				−40°C		42°		
				85°C		32°		

operating characteristics, V_{DD} = 5 V

PARAMETER		TEST CONDITIONS		T_A	MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain	R_L = 1 MΩ, C_L = 20 pF, See Figure 1	V_{IPP} = 1 V	25°C		0.03		V/μs
				−55°C		0.04		
				125°C		0.02		
			V_{IPP} = 2.5 V	25°C		0.03		
				−55°C		0.04		
				125°C		0.02		
V_n	Equivalent input noise voltage	f = 1 kHz, See Figure 2	R_S = 100 Ω,	25°C		68		nV/√Hz
B_{OM}	Maximum output swing bandwidth	V_O = V_{OH}, R_L = 1 MΩ,	C_L = 20 pF, See Figure 1	25°C		5		kHz
				−55°C		8		
				125°C		3		
B_1	Unity-gain bandwidth	V_i = 10 mV, See Figure 3	C_L = 20 pF,	25°C		85		kHz
				−55°C		140		
				125°C		45		
ϕ_m	Phase margin	V_i = 10 mV, C_L = 20 pF,	f = B_1, See Figure 3	25°C		34°		
				−55°C		39°		
				125°C		25°		

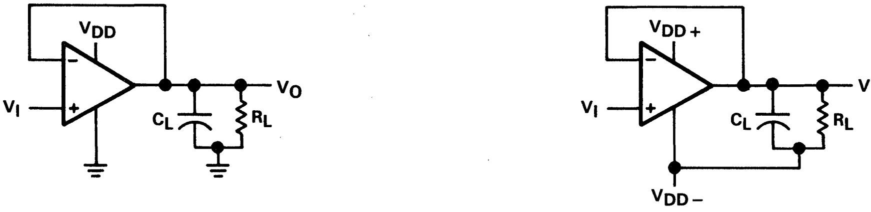
operating characteristics, V_{DD} = 10 V

PARAMETER		TEST CONDITIONS		T_A	MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain	R_L = 1 MΩ, C_L = 20 pF, See Figure 1	V_{IPP} = 1 V	25°C		0.05		V/μs
				−55°C		0.06		
				125°C		0.03		
			V_{IPP} = 5.5 V	25°C		0.04		
				−55°C		0.06		
				125°C		0.03		
V_n	Equivalent input noise voltage	f = 1 kHz, See Figure 2	R_S = 100 Ω,	25°C		68		nV/√Hz
B_{OM}	Maximum output swing bandwidth	V_O = V_{OH}, R_L = 1 MΩ,	C_L = 20 pF, See Figure 1	25°C		1		kHz
				−55°C		1.5		
				125°C		0.7		
B_1	Unity-gain bandwidth	V_i = 10 mV, See Figure 3	C_L = 20 pF,	25°C		110		kHz
				−55°C		165		
				125°C		70		
ϕ_m	Phase margin	V_i = 10 mV, C_L = 20 pF,	f = B_1, See Figure 3	25°C		38°		
				−55°C		43°		
				125°C		29°		

PARAMETER MEASUREMENT INFORMATION

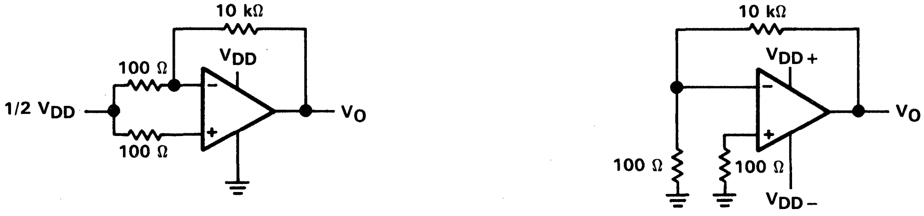
single-supply versus split-supply test circuits

Because the TLC27L2 and TLC27L7 are optimized for single-supply operation, circuit configurations used for the various tests often present some inconvenience since the input signal, in many cases, must be offset from ground. This inconvenience can be avoided by testing the device with split supplies and the output load tied to the negative rail. A comparison of single-supply versus split-supply test circuits is shown below. The use of either circuit will give the same result.



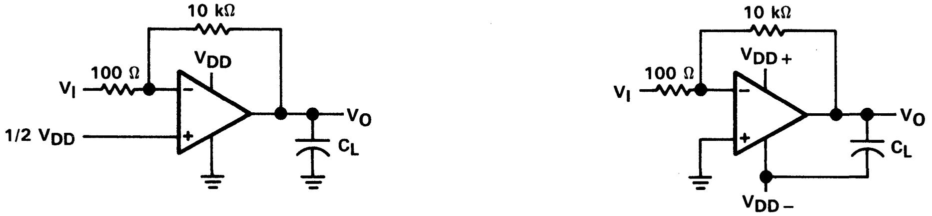
(a) Single-Supply (b) Split-Supply

FIGURE 1. UNITY-GAIN AMPLIFIER



(a) Single-Supply (b) Split-Supply

FIGURE 2. NOISE TEST CIRCUIT



(a) Single-Supply (b) Split-Supply

FIGURE 3. GAIN-OF-100 INVERTING AMPLIFIER

PARAMETER MEASUREMENT INFORMATION

input bias current

Because of the high input impedance of the TLC27L2 and TLC27L7 op amps, attempts to measure the input bias current can result in erroneous readings. The bias current at normal room ambient temperature is typically less than 1 pA, a value that is easily exceeded by leakages on the test socket. Two suggestions are offered to avoid erroneous measurements:

1. Isolate the device from other potential leakage sources. Use a grounded shield around and between the device inputs (see Figure 4). Leakages that would otherwise flow to the inputs will be shunted away.
2. Compensate for the leakage of the test socket by actually performing an input bias current test (using a picoammeter) with no device in the test socket. The actual input bias current can then be calculated by subtracting the ''open-socket'' leakage readings from the readings obtained with a device in the test socket.

One word of caution . . . many automatic testers as well as some bench-top op amp testers use the servo-loop technique with a resistor in series with the device input to measure the input bias current (the voltage drop across the series resistor is measured and the bias current is calculated). This method requires that a device be inserted into the test socket to obtain a correct reading; therefore, an ''open-socket'' reading is not feasible using this method.

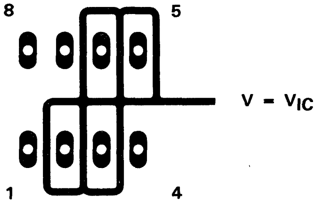


FIGURE 4. ISOLATION METAL AROUND DEVICE INPUTS
(JG AND P DUAL-IN-LINE-PACKAGE)

low-level output voltage

To obtain low-supply-voltage operation, some compromise was necessary in the input stage. This compromise results in the device low-level output being dependent on both the common-mode input voltage level as well as the differential input voltage level. When attempting to correlate low-level output readings with those quoted in the electrical specifications, these two conditions should be observed. If conditions other than these are to be used, please refer to Figures 14 through 19 in the Typical Characteristics of this data sheet.

input offset voltage temperature coefficient

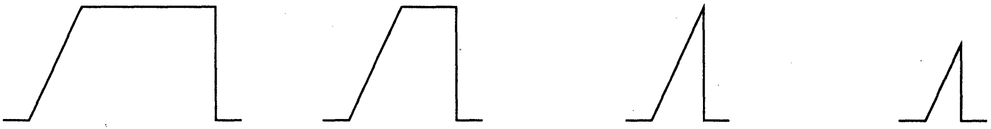
Erroneous readings often result from attempts to measure temperature coefficient of input offset voltage. This parameter is actually a calculation using input offset voltage measurements obtained at two different temperatures. When one (or both) of the temperatures is below freezing, moisture can collect on both the device and the test socket. This moisture will result in leakage and contact resistance, which can cause erroneous input offset voltage readings. The isolation techniques previously mentioned have no effect on the leakage since the moisture also covers the isolation metal itself, thereby rendering it useless. It is suggested that these measurements be performed at temperatures above freezing to minimize error.

PARAMETER MEASUREMENT INFORMATION

full-power response

Full-power response, the frequency above which the op amp slew rate limits the output voltage swing, is often specified two ways . . . full-linear response and full-peak response. The full-linear response is generally measured by monitoring the distortion level of the output while increasing the frequency of a sinusoidal input signal until the maximum frequency is found above which the output contains significant distortion. The full-peak response is defined as the maximum output frequency, without regard to distortion, above which full peak-to-peak output swing cannot be maintained.

Because there is no industry-wide accepted value for "significant" distortion, the full-peak response is specified in this data sheet and is measured using the circuit of Figure 1. The initial setup involves the use of a sinusoidal input to determine the maximum peak-to-peak output of the device (the amplitude of the sinusoidal wave is increased until clipping occurs). The sinusoidal wave is then replaced with a square wave of the same amplitude. The frequency is then increased until the maximum peak-to-peak output can no longer be maintained (Figure 5). A square wave is used to allow a more accurate determination of the point at which the maximum peak-to-peak output is reached.



(a) $f = 100$ Hz (b) $B_{OM} > f > 100$ Hz (c) $f = B_{OM}$ (d) $f > B_{OM}$

FIGURE 5. FULL-POWER-RESPONSE OUTPUT SIGNAL

test time

Inadequate test time is a frequent problem, especially when testing CMOS devices in a high-volume, short-test-time environment. Internal capacitances are inherently higher in CMOS than in bipolar and BiFET devices and require longer test times than their bipolar and BiFET counterparts. The problem becomes more pronounced with reduced supply levels and lower temperatures.

TYPICAL CHARACTERISTICS

DISTRIBUTION OF TLC27L2
INPUT OFFSET VOLTAGE

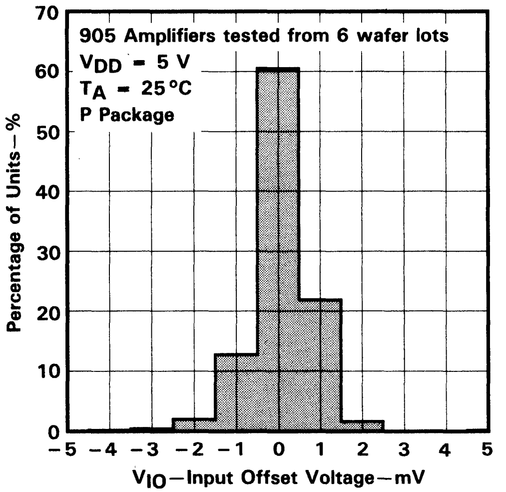


FIGURE 6

DISTRIBUTION OF TLC27L2
INPUT OFFSET VOLTAGE

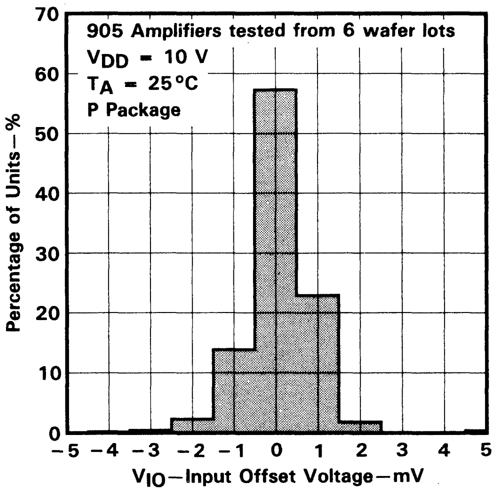


FIGURE 7

DISTRIBUTION OF TLC27L2 AND TLC27L7
INPUT OFFSET VOLTAGE
TEMPERATURE COEFFICIENT

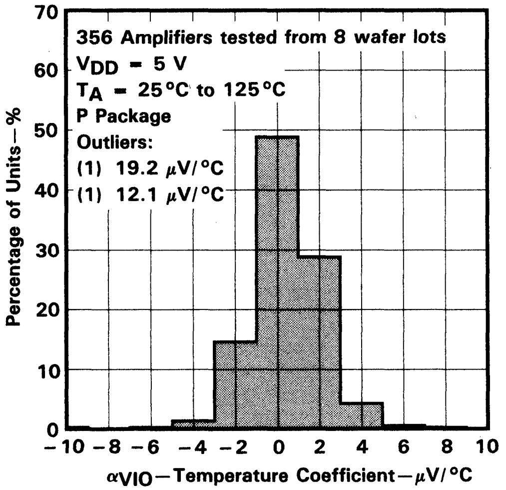


FIGURE 8

DISTRIBUTION OF TLC27L2 AND TLC27L7
INPUT OFFSET VOLTAGE
TEMPERATURE COEFFICIENT

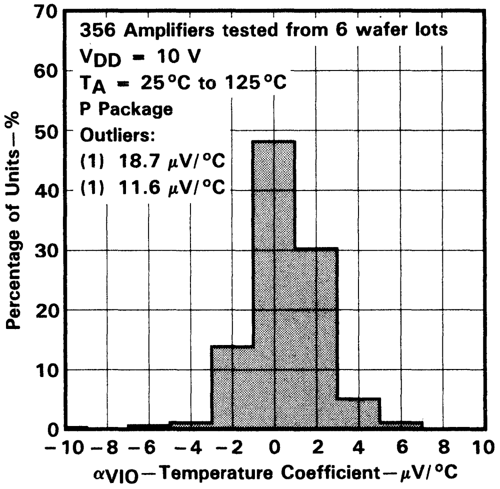


FIGURE 9

TYPICAL CHARACTERISTICS†

HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

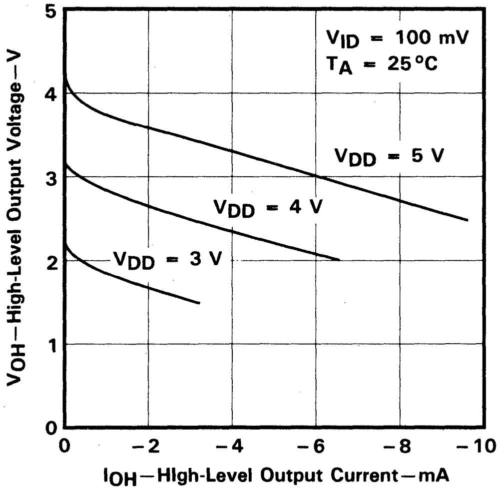


FIGURE 10

HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

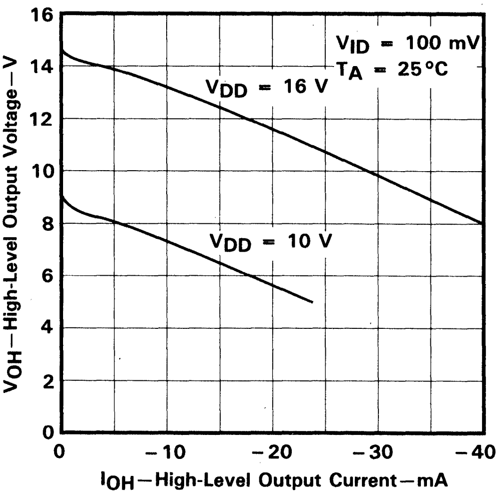


FIGURE 11

HIGH-LEVEL OUTPUT VOLTAGE
vs
SUPPLY VOLTAGE

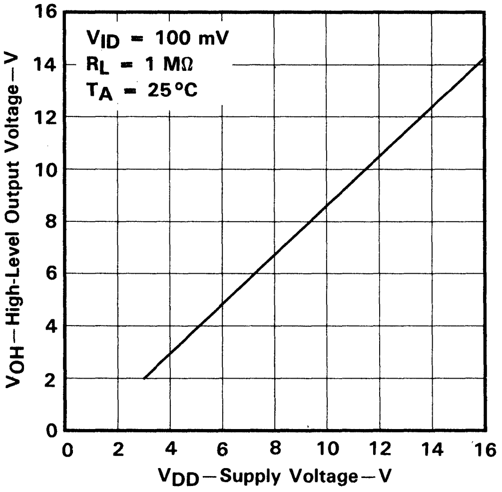


FIGURE 12

HIGH-LEVEL OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

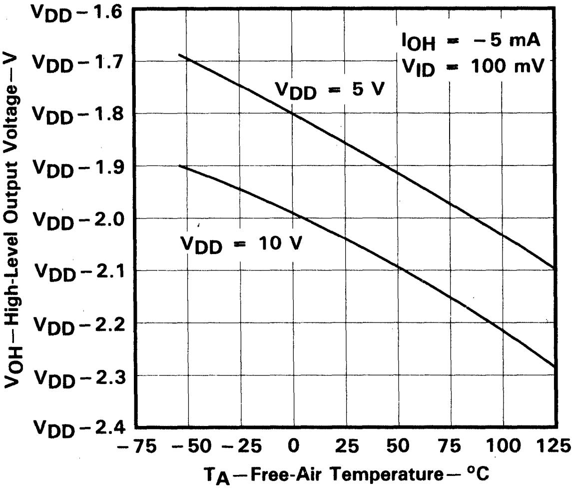


FIGURE 13

---

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

LOW-LEVEL OUTPUT VOLTAGE
vs
COMMON-MODE INPUT VOLTAGE

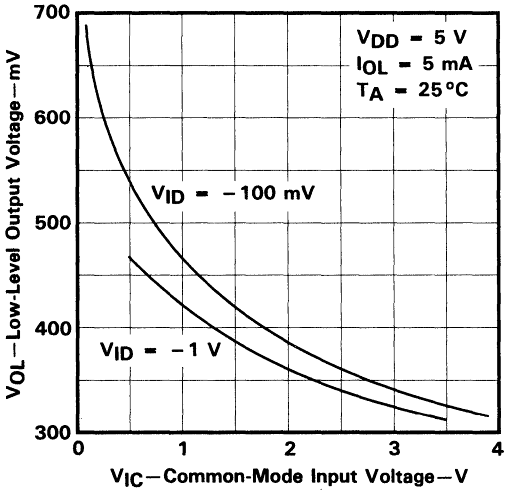


FIGURE 14

LOW-LEVEL OUTPUT VOLTAGE
vs
COMMON-MODE INPUT VOLTAGE

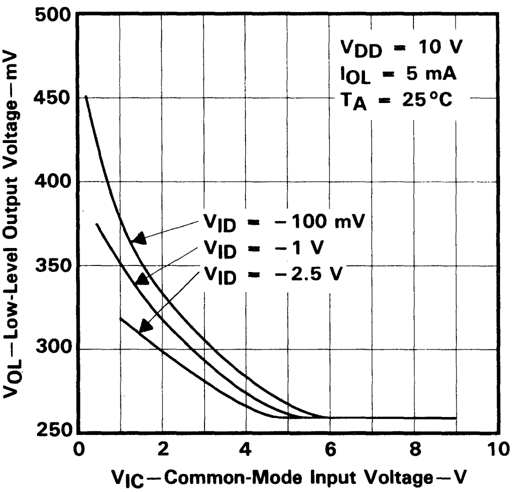


FIGURE 15

LOW-LEVEL OUTPUT VOLTAGE
vs
DIFFERENTIAL INPUT VOLTAGE

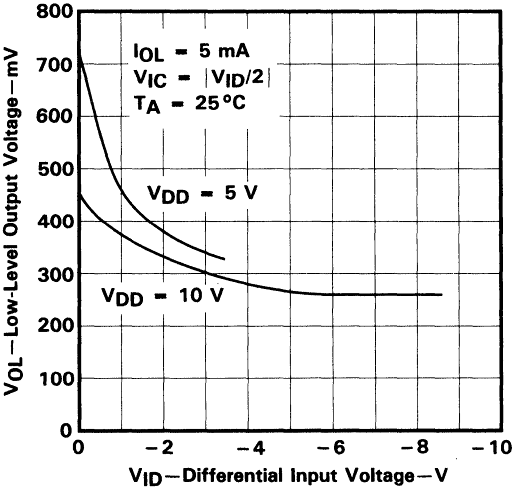


FIGURE 16

LOW-LEVEL OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

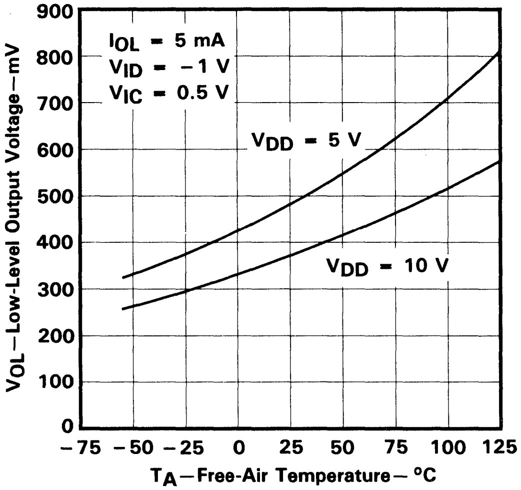


FIGURE 17

---

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS[†]

LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

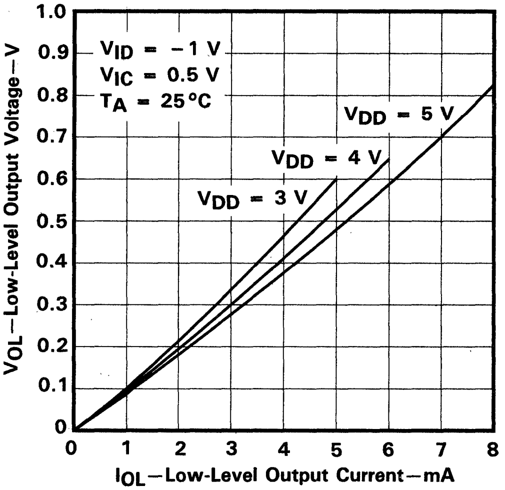


FIGURE 18

LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

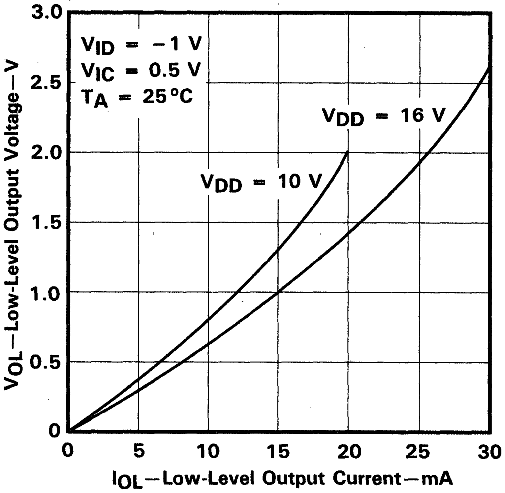


FIGURE 19

LARGE-SIGNAL
DIFFERENTIAL VOLTAGE AMPLIFICATION
vs
SUPPLY VOLTAGE

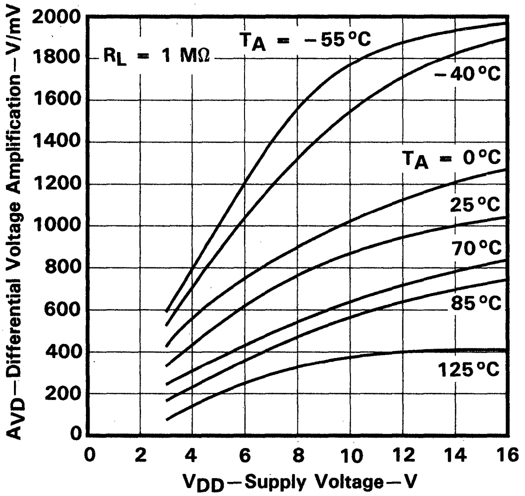


FIGURE 20

LARGE-SIGNAL
DIFFERENTIAL VOLTAGE AMPLIFICATION
vs
FREE-AIR TEMPERATURE

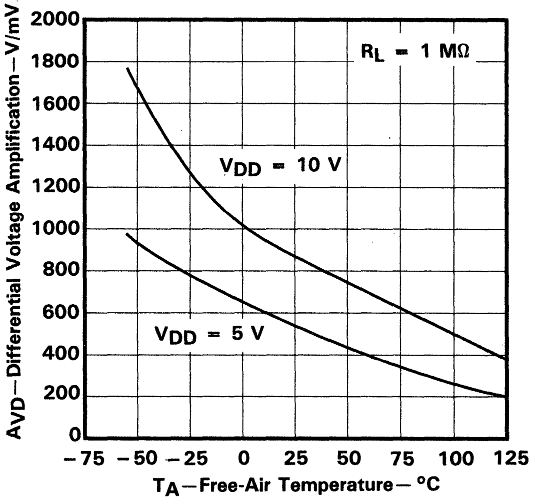


FIGURE 21

[†] Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

INPUT BIAS CURRENT AND INPUT OFFSET CURRENT
vs
FREE-AIR TEMPERATURE

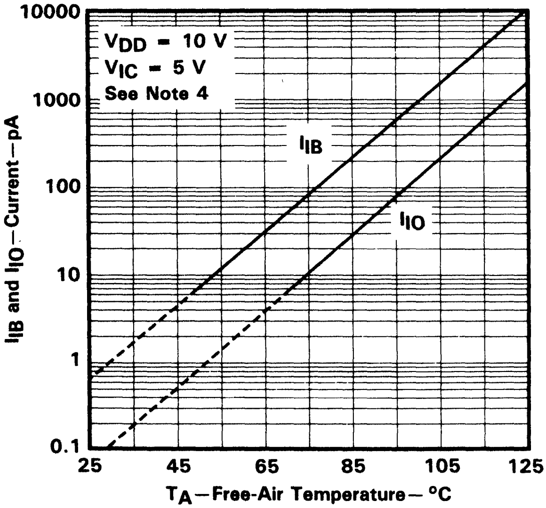


FIGURE 22

COMMON-MODE
INPUT VOLTAGE POSITIVE LIMIT
vs
SUPPLY VOLTAGE

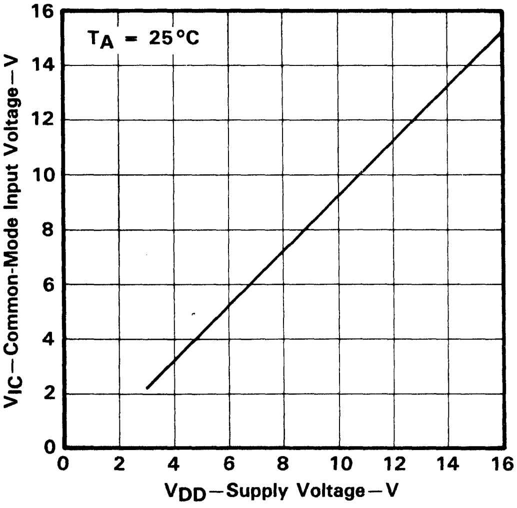


FIGURE 23

SUPPLY CURRENT
vs
SUPPLY VOLTAGE

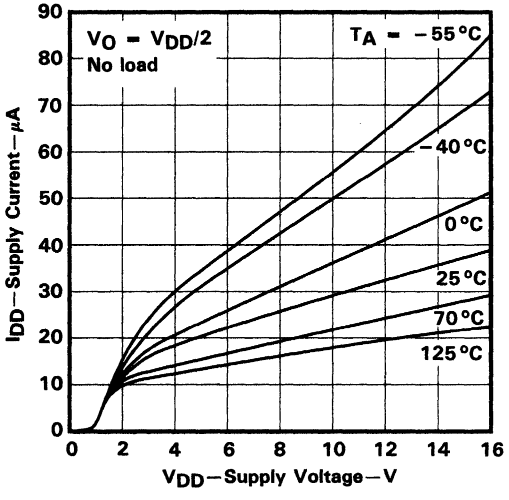


FIGURE 24

SUPPLY CURRENT
vs
FREE-AIR TEMPERATURE

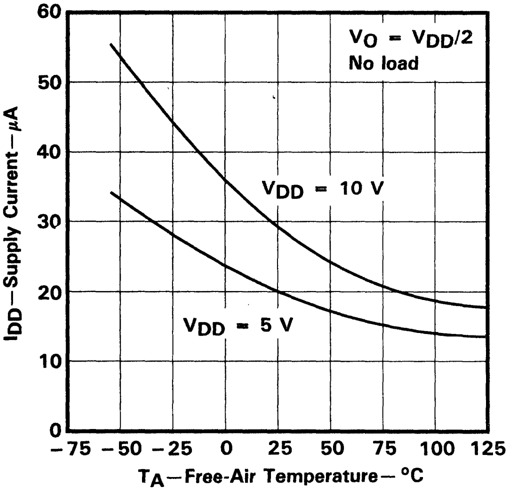


FIGURE 25

---

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

NOTE 4: The typical values of input bias current and input offset current below 5 pA were determined mathematically.

TYPICAL CHARACTERISTICS†

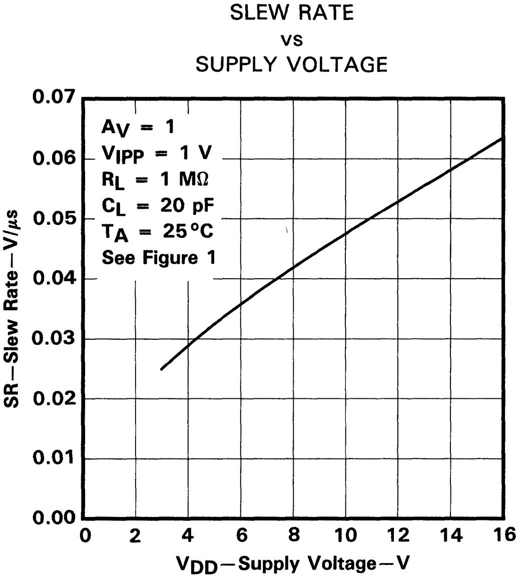


FIGURE 26

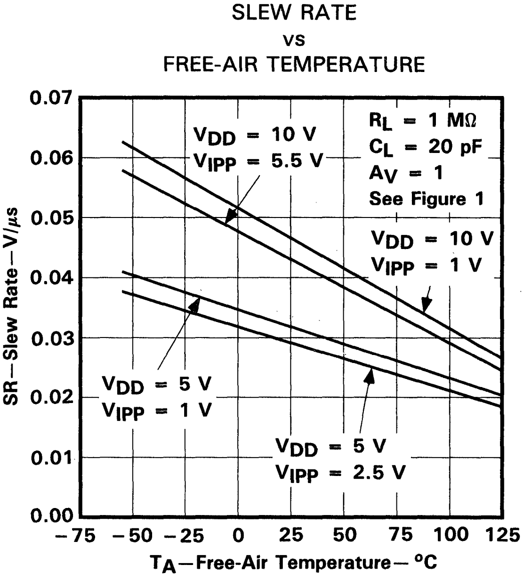


FIGURE 27

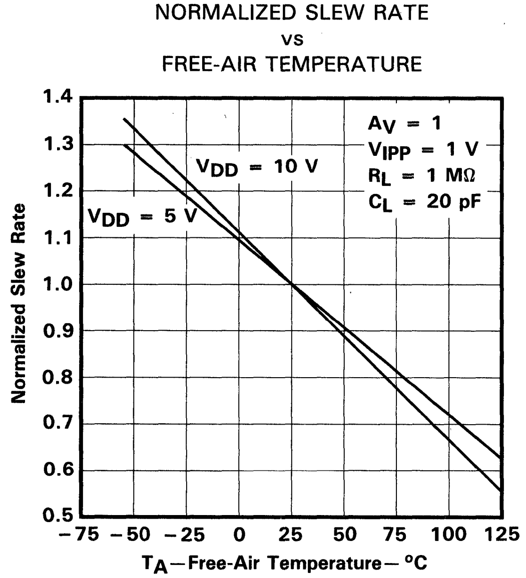


FIGURE 28

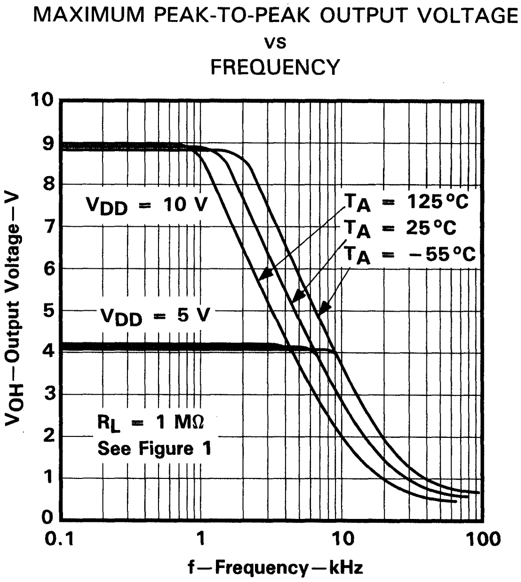


FIGURE 29

---

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

UNITY-GAIN BANDWIDTH
vs
FREE-AIR TEMPERATURE

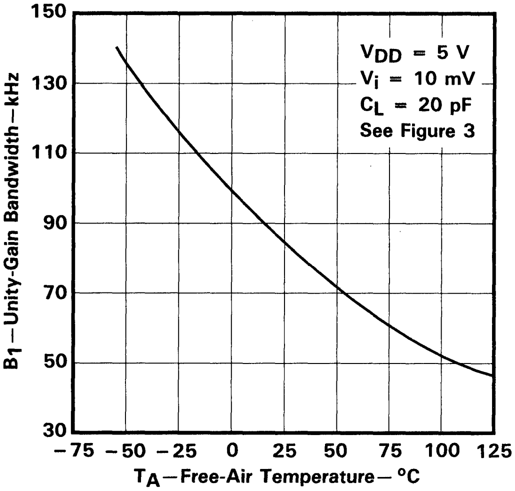


FIGURE 30

UNITY-GAIN BANDWIDTH
vs
SUPPLY VOLTAGE

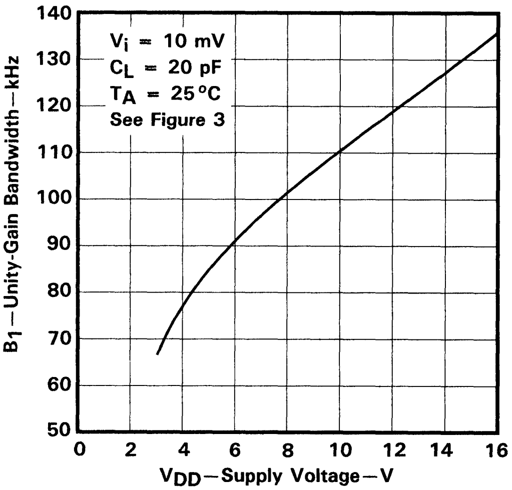


FIGURE 31

LARGE-SIGNAL DIFFERENTIAL VOLTAGE
AMPLIFICATION AND PHASE SHIFT
vs
FREQUENCY

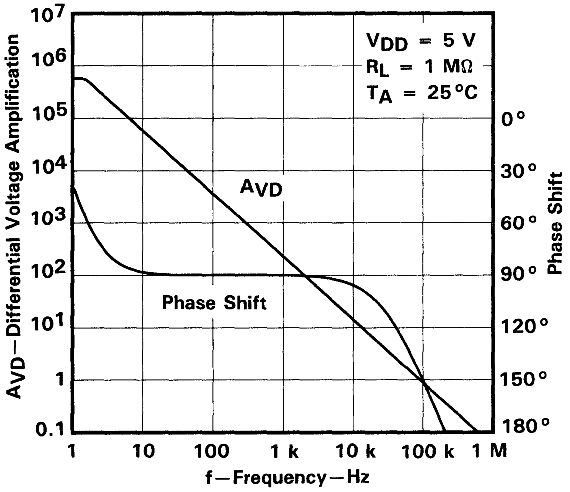


FIGURE 32

LARGE-SIGNAL DIFFERENTIAL VOLTAGE
AMPLIFICATION AND PHASE SHIFT
vs
FREQUENCY

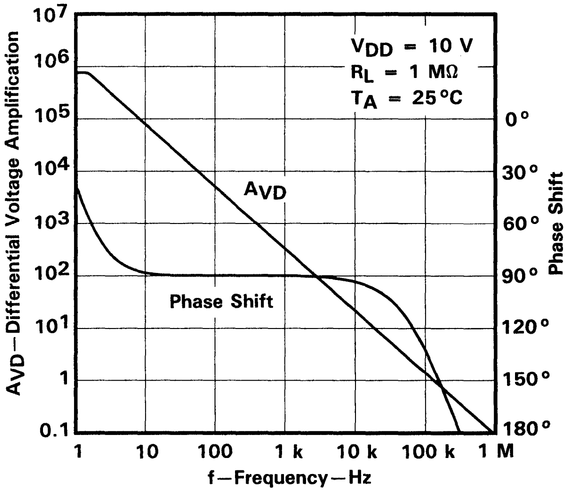


FIGURE 33

---

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

PHASE MARGIN
vs
SUPPLY VOLTAGE

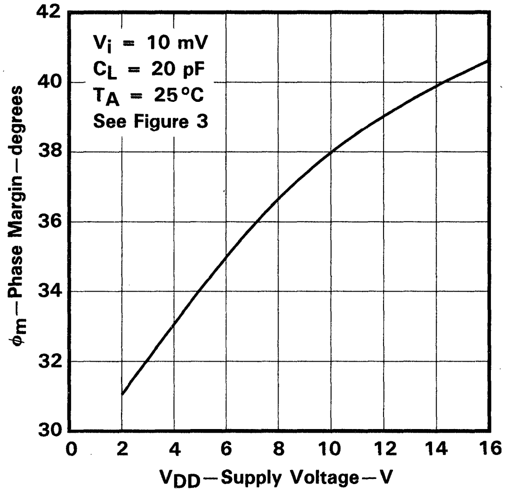


FIGURE 34

PHASE MARGIN
vs
FREE-AIR TEMPERATURE

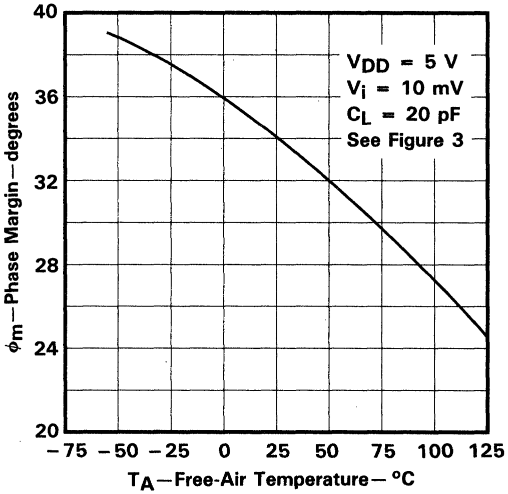


FIGURE 35

PHASE MARGIN
vs
CAPACITIVE LOAD

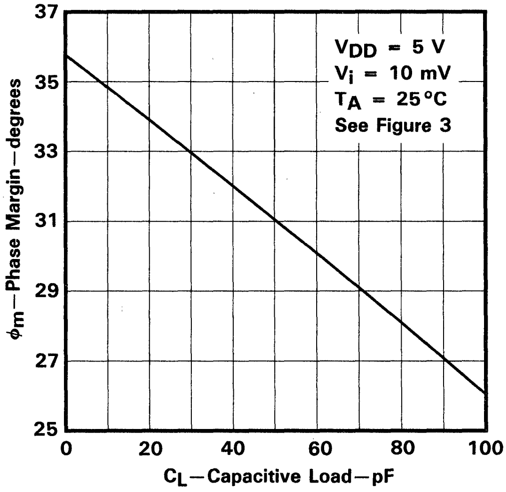


FIGURE 36

EQUIVALENT INPUT NOISE VOLTAGE
vs
FREQUENCY

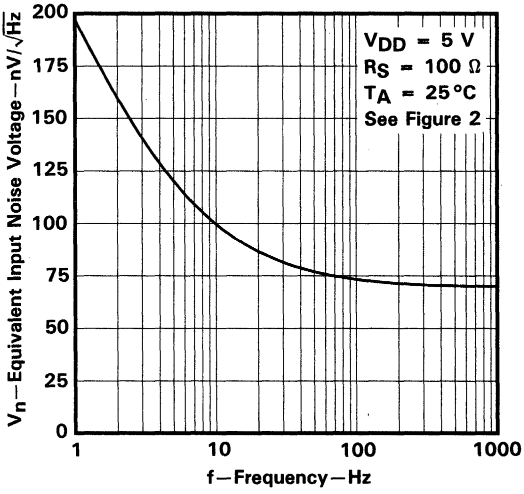


FIGURE 37

---

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL APPLICATION DATA

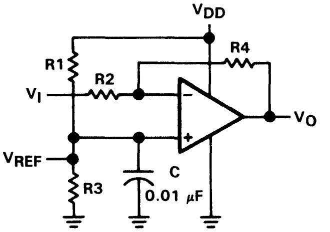
single-supply operation

While the TLC27L2 and TLC27L7 perform well using dual power supplies (also called balanced or split supplies), the design is optimized for single-supply operation. This design includes an input common-mode voltage range that encompasses ground as well as an output voltage range that pulls down to ground. The supply voltage range extends down to 3 V (C-suffix types), thus allowing operation with supply levels commonly available for TTL and HCMOS; however, for maximum dynamic range, 16-V single-supply operation is recommended.

Many single-supply applications require that a voltage be applied to one input to establish a reference level that is above ground. A resistive voltage divider is usually sufficient to establish this reference level (see Figure 38). The low input bias current of the TLC27L2 and TLC27L7 permits the use of very large resistive values to implement the voltage divider, thus minimizing power consumption.

The TLC27L2 and TLC27L7 work well in conjunction with digital logic; however, when powering both linear devices and digital logic from the same power supply, the following precautions are recommended:

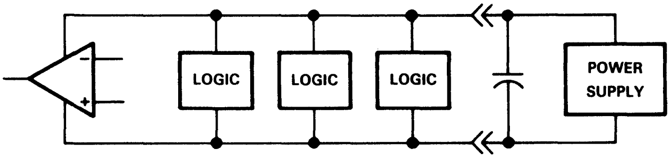
1. Power the linear devices from separate bypassed supply lines (see Figure 39); otherwise the linear device supply rails can fluctuate due to voltage drops caused by high switching currents in the digital logic.
2. Use proper bypass techniques to reduce the probability of noise-induced errors. Single capacitive decoupling is often adequate; however, high-frequency applications may require RC decoupling.



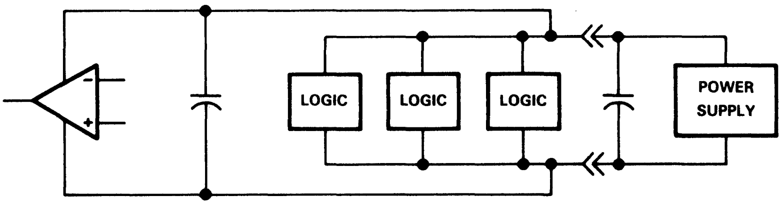
$$V_{REF} = V_{DD}\frac{R3}{R1 + R3}$$

$$V_O = \left(V_{REF} - V_I\right)\frac{R4}{R2} + V_{REF}$$

FIGURE 38. INVERTING AMPLIFIER WITH VOLTAGE REFERENCE



(a) Common Supply Rails



(b) Separate Bypassed Supply Rails (preferred)

FIGURE 39. COMMON VS SEPARATE SUPPLY RAILS

TYPICAL APPLICATION DATA

input characteristics

The TLC27L2 and TLC27L7 are specified with a minimum and a maximum input voltage that, if exceeded at either input, could cause the device to malfunction. Exceeding this specified range is a common problem, especially in single-supply operation. Note that the lower range limit includes the negative rail, while the upper range limit is specified at $V_{DD} - 1$ V at $T_A = 25\,°C$ and at $V_{DD} - 1.5$ V at all other temperatures.

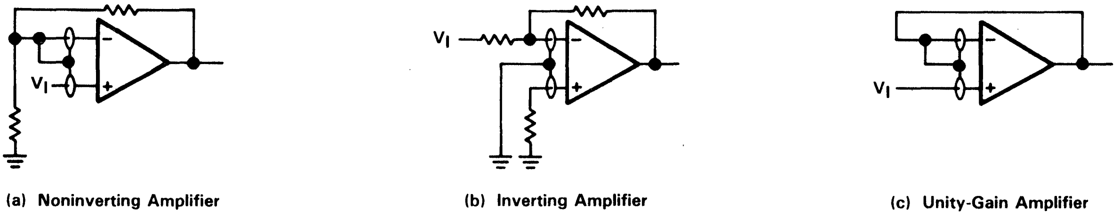
The use of the polysilicon-gate process and the careful input circuit design gives the TLC27L2 and TLC27L7 very good input offset voltage drift characteristics relative to conventional metal-gate processes. Offset voltage drift in CMOS devices is highly influenced by threshold voltage shifts caused by polarization of the phosphorus dopant implanted in the oxide. Placing the phosphorus dopant in a conductor (such as a polysilicon gate) alleviates the polarization problem, thus reducing threshold voltage shifts by more than an order of magnitude. The offset voltage drift with time has been calculated to be typically 0.1 μV/month, including the first month of operation.

Because of the extremely high input impedance and resulting low bias current requirements, the TLC27L2 and TLC27L7 are well suited for low-level signal processing; however, leakage currents on printed circuit boards and sockets can easily exceed bias current requirements and cause a degradation in device performance. It is good practice to include guard rings around inputs (similar to those of Figure 4 in the Parameter Measurement Information section). These guards should be driven from a low-impedance source at the same voltage level as the common-mode input (see Figure 40).

The inputs of any unused amplifiers should be tied to ground to avoid possible oscillation.

noise performance

The noise specifications in op amp circuits are greatly dependent on the current in the first-stage differential amplifier. The low input bias current requirements of the TLC27L2 and TLC27L7 result in a very low noise current, which is insignificant in most applications. This feature makes the devices especially favorable over bipolar devices when using values of circuit impedance greater than 50 kΩ, since bipolar devices exhibit greater noise currents.



(a) Noninverting Amplifier (b) Inverting Amplifier (c) Unity-Gain Amplifier

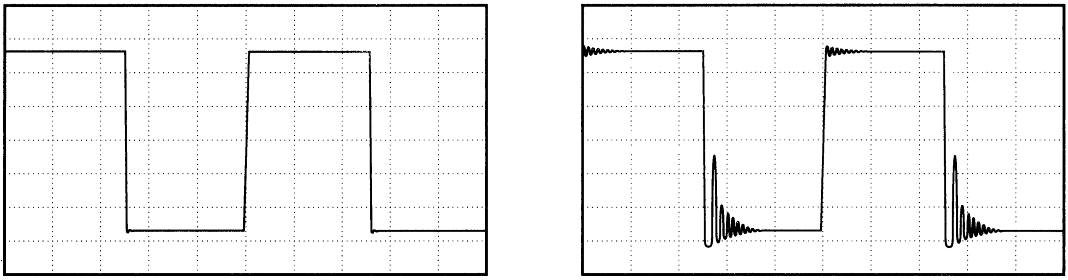
FIGURE 40. GUARD-RING SCHEMES

output characteristics

The output stage of the TLC27L2 and TLC27L7 is designed to sink and source relatively high amounts of current (see typical characteristics). If the output is subjected to a short-circuit condition, this high current capability can cause device damage under certain conditions. Output current capability increases with supply voltage.

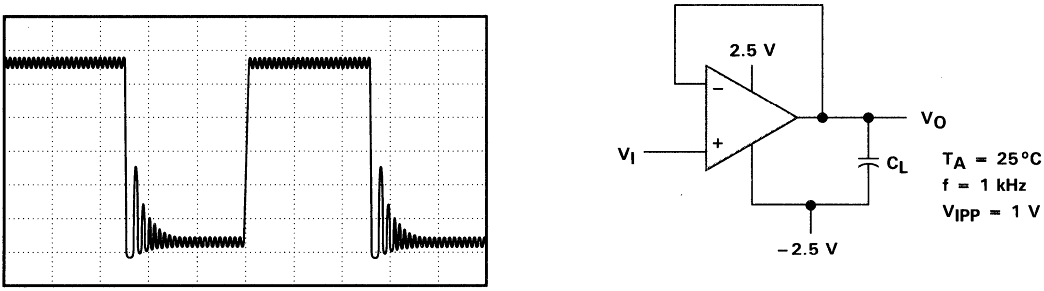
All operating characteristics of the TLC27L2 and TLC27L7 were measured using a 20-pF load. The devices will drive higher capacitive loads; however, as output load capacitance increases, the resulting response pole occurs at lower frequencies, thereby causing ringing, peaking, or even oscillation (see Figure 41). In many cases, adding a small amount of resistance in series with the load capacitance will alleviate the problem.

TYPICAL APPLICATION DATA



(a) C_L = 20 pF, R_L = No load

(b) C_L = 260 pF, R_L = No load



(c) C_L = 310 pF, R_L = No load

(d) Test Circuit

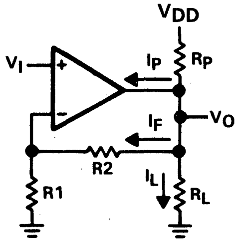
FIGURE 41. EFFECT OF CAPACITIVE LOADS AND TEST CIRCUIT

Although the TLC27L2 and TLC27L7 possess excellent high-level output voltage and current capability, methods for boosting this capability are available, if needed. The simplest method involves the use of a pullup resistor (R_P) connected from the output to the positive supply rail (see Figure 42). There are two disadvantages to the use of this circuit. First, the NMOS pulldown transistor N4 (see equivalent schematic) must sink a comparatively large amount of current. In this circuit, N4 behaves like a linear resistor with an on-resistance between approximately 60 Ω and 180 Ω, depending on how hard the op amp input is driven. With very low values of R_P, a voltage offset from 0 V at the output will occur. Second, pullup resistor R_P acts as a drain load to N4 and the gain of the op amp is reduced at output voltage levels where N5 is not supplying the output current.

feedback

Op amp circuits nearly always employ feedback, and since feedback is the first prerequisite for oscillation, some caution is appropriate. Most oscillation problems result from driving capacitive loads (discussed previously) and ignoring stray input capacitance. A small-value capacitor connected in parallel with the feedback resistor is an effective remedy (see Figure 43). The value of this capacitor is optimized empirically.

TYPICAL APPLICATION DATA



$$R_P = \frac{V_{DD} - V_O}{I_F + I_L + I_P}$$

I_P = Pullup current required by the op amp (typically 500 μA)

FIGURE 42. RESISTIVE PULLUP TO INCREASE V_{OH}

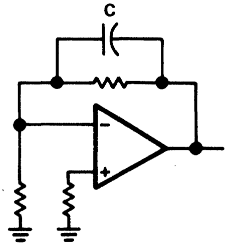


FIGURE 43. COMPENSATION FOR INPUT CAPACITANCE

electrostatic discharge protection

The TLC27L2 and TLC27L7 incorporate an internal electrostatic discharge (ESD) protection circuit that prevents functional failures at voltages up to 2000 V as tested under MIL-STD-883C, Method 3015.2. Care should be exercised, however, when handling these devices, as exposure to ESD may result in the degradation of the device parametric performance. The protection circuit also causes the input bias currents to be temperature-dependent and have the characteristics of a reverse-biased diode.

latch-up

Because CMOS devices are susceptible to latch-up due to their inherent parasitic thyristors, the TLC27L2 and TLC27L7 inputs and outputs were designed to withstand − 100-mA surge currents without sustaining latch-up; however, techniques should be used to reduce the chance of latch-up whenever possible. Internal protection diodes should not, by design, be forward biased. Applied input and output voltage should not exceed the supply voltage by more than 300 mV. Care should be exercised when using capacitive coupling on pulse generators. Supply transients should be shunted by the use of decoupling capacitors (0.1 μF typical) located across the supply rails as close to the device as possible.

The current path established if latch-up occurs is usually between the positive supply rail and ground and can be triggered by surges on the supply lines and/or voltages on either the output or inputs that exceed the supply voltage. Once latch-up occurs, the current flow is limited only by the impedance of the power supply and the forward resistance of the parasitic thyristor and usually results in the destruction of the device. The chance of latch-up occurring increases with increasing temperature and supply voltages.

TYPICAL APPLICATION DATA

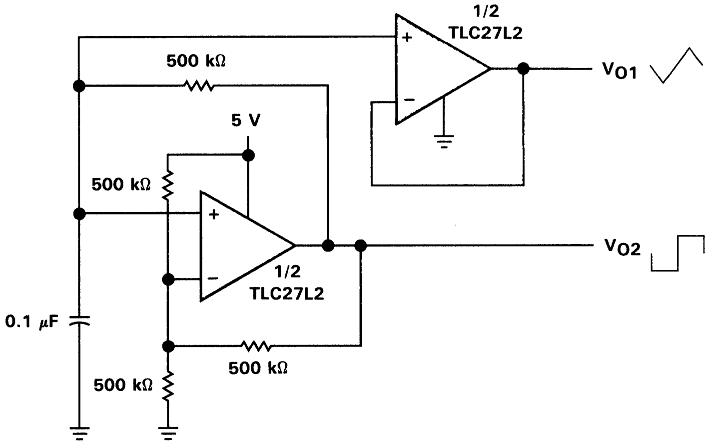
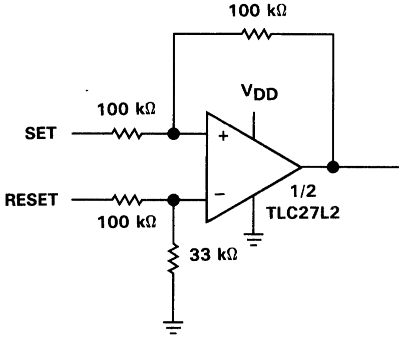


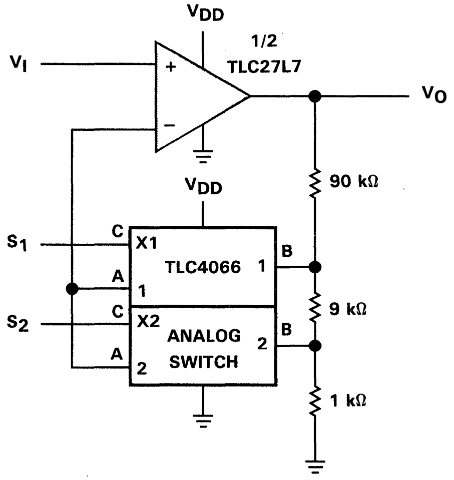
FIGURE 44. MULTIVIBRATOR



NOTE: V_{DD} = 5 V to 16 V

FIGURE 45. SET/RESET FLIP-FLOP

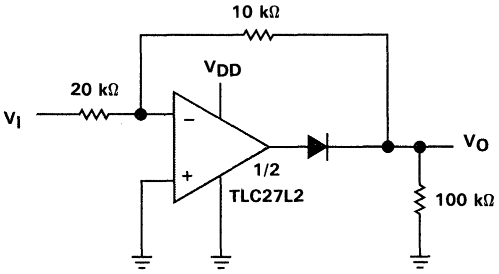
TYPICAL APPLICATION DATA



SELECT:	S_1	S_2
A_V	10	100

NOTE: V_{DD} = 5 V to 12 V

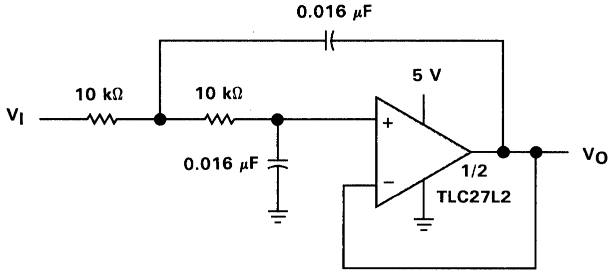
FIGURE 46. AMPLIFIER WITH DIGITAL GAIN SELECTION



NOTE: V_{DD} = 5 V to 16 V

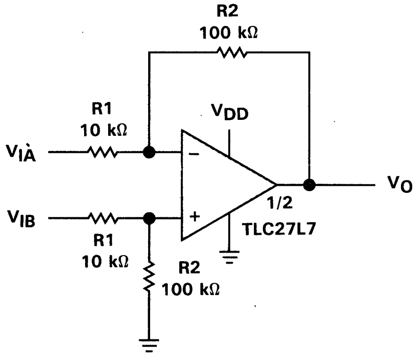
FIGURE 47. FULL-WAVE RECTIFIER

TYPICAL APPLICATION DATA



NOTE: Normalized to F_C = 1 kHz and R_L = 10 kΩ

FIGURE 48. TWO-POLE LOW-PASS BUTTERWORTH FILTER



NOTES: V_{DD} = 5 V to 16 V

$$V_O = \frac{R2}{R1}(V_{IB} - V_{IA})$$

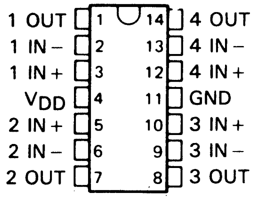
FIGURE 49. DIFFERENCE AMPLIFIER

TLC27L4, TLC27L4A, TLC27L4B, TLC27L9
LinCMOS™ PRECISION QUAD OPERATIONAL AMPLIFIERS

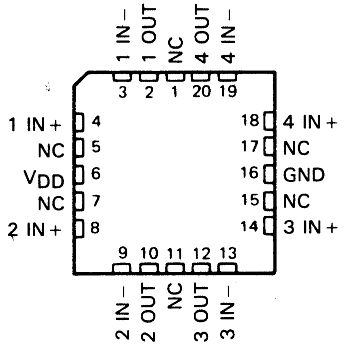
D3142, OCTOBER 1987—REVISED OCTOBER 1990

- **Trimmed Offset Voltage:**
  TLC27L9 . . . 900 μV Max at 25°C, V_{DD} = 5 V
- **Input Offset Voltage Drift . . . Typically 0.1 μV/Month, Including the First 30 Days**
- **Wide Range of Supply Voltages Over Specified Temperature Range:**
  0°C to 70°C . . . 3 V to 16 V
  −40°C to 85°C . . . 4 V to 16 V
  −55°C to 125°C . . . 4 V to 16 V
- **Single-Supply Operation**
- **Common-Mode Input Voltage Range Extends Below the Negative Rail (C-Suffix, I-Suffix types)**
- **Ultra-Low Power . . . Typically 195 μW at 25°C, V_{DD} = 5 V**
- **Output Voltage Range Includes Negative Rail**
- **High Input Impedance . . . 10^{12} Ω Typical**
- **ESD-Protection Circuitry**
- **Small-Outline Package Option Also Available in Tape and Reel**
- **Designed-In Latch-Up Immunity**

D, J, OR N PACKAGE
(TOP VIEW)



FK PACKAGE
(TOP VIEW)



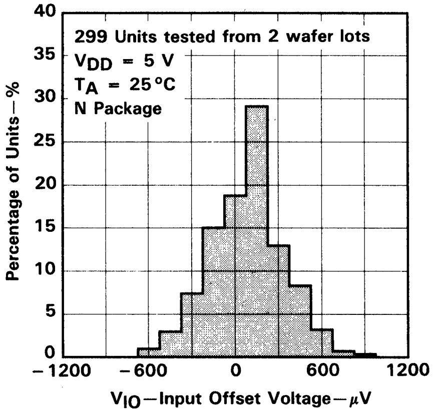
NC—No internal connection

AVAILABLE OPTIONS

T_A	V_{IO}max at 25°C	PACKAGE			
		SMALL OUTLINE (D)	CHIP CARRIER (FK)	CERAMIC DIP (J)	PLASTIC DIP (N)
0°C to 70°C	900 μV	TLC27L9CD	—	—	TLC27L9CN
	2 mV	TLC27L4BCD	—	—	TLC27L4BCN
	5 mV	TLC27L4ACD	—	—	TLC27L4ACN
	10 mV	TLC27L4CD	—	—	TLC27L4CN
−40°C to 85°C	900 μV	TLC27L9ID	—	—	TLC27L9IN
	2 mV	TLC27L4BID	—	—	TLC27L4BIN
	5 mV	TLC27L4AID	—	—	TLC27L4AIN
	10 mV	TLC27L4ID	—	—	TLC27L4IN
−55°C to 125°C	900 μV	TLC27L9MD	TLC27L9MFK	TLC27L9MJ	TLC27L9MN
	10 mV	TLC27L4MD	TLC27L4MFK	TLC27L4MJ	TLC27L4MN

The D package is available in tape and reel. Add R suffix to the device type, (e.g., TLC27L9CDR).

DISTRIBUTION OF TLC27L9
INPUT OFFSET VOLTAGE



LinCMOS is a trademark of Texas Instruments Incorporated

TEXAS INSTRUMENTS
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

description

The TLC27L4 and TLC27L9 quad operational amplifiers combine a wide range of input offset voltage grades with low offset voltage drift, high input impedance, extremely low power, and high gain.

These devices use Texas Instruments silicon-gate LinCMOS™ technology, which provides offset voltage stability far exceeding the stability available with conventional metal-gate processes.

The extremely high input impedance, low bias currents, and low power consumption make these cost-effective devices ideal for high gain, low frequency, low power applications. Four offset voltage grades are available (C-suffix and I-suffix types), ranging from the low-cost TLC27L4 (10 mV) to the high-precision TLC27L9 (900 μV). These advantages, in combination with good common-mode rejection and supply voltage rejection, make these devices a good choice for new state-of-the-art designs as well as for upgrading existing designs.

In general, many features associated with bipolar technology are available on LinCMOS™ operational amplifiers, without the power penalties of bipolar technology. General applications such as transducer interfacing, analog calculations, amplifier blocks, active filters, and signal buffering are easily designed with the TLC27L4 and TLC27L9. The devices also exhibit low voltage single-supply operation and ultra-low power comsumption, making them ideally suited for remote and inaccessible battery-powered applications. The common-mode input voltage range includes the negative rail.

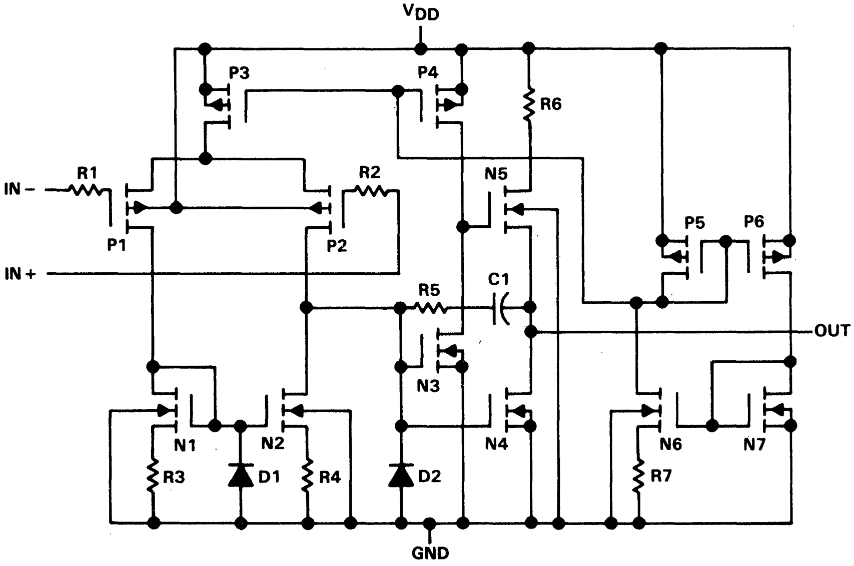
A wide range of packaging options is available, including small-outline and chip carrier versions for high-density system applications.

The device inputs and outputs are designed to withstand −100-mA surge currents without sustaining latch-up.

The TLC27L4 and TLC27L9 incorporate internal ESD-protection circuits that prevent functional failures at voltages up to 2000 V as tested under MIL-STD-883C, Method 3015.2; however, care should be exercised in handling these devices, as exposure to ESD may result in the degradation of the device parametric performance.

C-suffix devices are characterized for operation from 0°C to 70°C. I-suffix devices are characterized for operation from −40°C to 85°C. M-suffix devices are characterized for operation from −55°C to 125°C.

equivalent schematic (each amplifier)



absolute maximum ratings over operating free-air temperature (unless otherwise noted)

Supply voltage, V_{DD} (see Note 1)		18 V
Differential input voltage (see Note 2)		$\pm V_{DD}$
Input voltage range, V_I (any input)		-0.3 V to V_{DD}
Input current, I_I		±5 mA
Output current, I_O (each output)		±30 mA
Total current into V_{DD} terminal		45 mA
Total current out of ground terminal		45 mA
Duration of short-circuit current at (or below) 25°C (see Note 3)		Unlimited
Continuous total dissipation		See Dissipation Rating Table
Operating free-air temperature, T_A:	C-suffix	0°C to 70°C
	I-suffix	−40°C to 85°C
	M-suffix	−55°C to 125°C
Storage temperature range		−65°C to 150°C
Case temperature for 60 seconds: FK package		260°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D and N package		260°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: J package		300°C

NOTES:
1. All voltage values, except differential voltages, are with respect to network ground.
2. Differential voltages are at the noninverting input with respect to the inverting input.
3. The output may be shorted to either supply. Temperature and/or supply voltages must be limited to ensure that the maximum dissipation rating is not exceeded (see application section).

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING	$T_A = 125°C$ POWER RATING
D	950 mW	7.6 mW/°C	608 mW	494 mW	
FK	1375 mW	11 mW/°C	880 mW	715 mW	275 mW
J	1375 mW	11 mW/°C	880 mW	715 mW	275 mW
N	1575 mW	12.6 mW/°C	1008 mW	819 mW	

recommended operating conditions

		C-SUFFIX			I-SUFFIX			M-SUFFIX			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{DD}		3		16	4		16	4		16	V
Common-mode input voltage, V_{IC}	$V_{DD} = 5$ V	−0.2		3.5	−0.2		3.5	0		3.5	V
	$V_{DD} = 10$ V	−0.2		8.5	−0.2		8.5	0		8.5	
Operating free-air temperature, T_A		0		70	−40		85	−55		125	°C

electrical characteristics at specified free-air temperature, V_{DD} = 5 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS	T_A†	MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	TLC27L4C	V_O = 1.4 V, V_{IC} = 0, R_S = 50 Ω, R_L = 1 MΩ	25°C		1.1	10	mV
				Full range			12	
		TLC27L4AC	V_O = 1.4 V, V_{IC} = 0, R_S = 50 Ω, R_L = 1 MΩ	25°C		0.9	5	
				Full range			6.5	
		TLC27L4BC	V_O = 1.4 V, V_{IC} = 0, R_S = 50 Ω, R_L = 1 MΩ	25°C		240	2000	μV
				Full range			3000	
		TLC27L9C	V_O = 1.4 V, V_{IC} = 0, R_S = 50 Ω, R_L = 1 MΩ	25°C		200	900	
				Full range			1500	
α_{VIO}	Average temperature coefficient of input offset voltage			25°C to 70°C		1.1		μV/°C
I_{IO}	Input offset current (see Note 4)		V_O = 2.5 V, V_{IC} = 2.5 V	25°C		0.1		pA
				70°C		7	300	
I_{IB}	Input bias current (see Note 4)		V_O = 2.5 V, V_{IC} = 2.5 V	25°C		0.6		pA
				70°C		40	600	
V_{ICR}	Common-mode input voltage range (see Note 5)			25°C	−0.2 to 4	−0.3 to 4.2		V
				Full range	−0.2 to 3.5			V
V_{OH}	High-level output voltage		V_{ID} = 100 mV, R_L = 1 MΩ	25°C	3.2	4.1		V
				0°C	3	4.1		
				70°C	3	4.2		
V_{OL}	Low-level output voltage		V_{ID} = −100 mV, I_{OL} = 0	25°C		0	50	mV
				0°C		0	50	
				70°C		0	50	
A_{VD}	Large-signal differential voltage amplification		V_O = 0.25 V to 2 V, R_L = 1 MΩ	25°C	50	520		V/mV
				0°C	50	680		
				70°C	50	380		
CMRR	Common-mode rejection ratio		V_{IC} = V_{ICR} min	25°C	65	94		dB
				0°C	60	95		
				70°C	60	95		
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)		V_{DD} = 5 V to 10 V, V_O = 1.4 V	25°C	70	97		dB
				0°C	60	97		
				70°C	60	98		
I_{DD}	Supply current (four amplifiers)		V_O = 2.5 V, V_{IC} = 2.5 V, No load	25°C		40	68	μA
				0°C		48	84	
				70°C		31	56	

†Full range is 0°C to 70°C.

NOTES: 4. The typical values of input bias current and input offset current below 5 pA were determined mathematically.
5. This range also applies to each input individually.

electrical characteristics at specified free-air temperature, V_{DD} = 10 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS		T_A†	MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	TLC27L4C	V_O = 1.4 V,	V_{IC} = 0,	25°C		1.1	10	mV
			R_S = 50 Ω,	R_L = 1 MΩ	Full range			12	
		TLC27L4AC	V_O = 1.4 V,	V_{IC} = 0,	25°C		0.9	5	
			R_S = 50 Ω,	R_L = 1 MΩ	Full range			6.5	
		TLC27L4BC	V_O = 1.4 V,	V_{IC} = 0,	25°C		260	2000	µV
			R_S = 50 Ω,	R_L = 1 MΩ	Full range			3000	
		TLC27L9C	V_O = 1.4 V,	V_{IC} = 0,	25°C		210	1200	
			R_S = 50 Ω,	R_L = 1 MΩ	Full range			1900	
α_{VIO}	Average temperature coefficient of input offset voltage				25°C to 70°C		1		µV/°C
I_{IO}	Input offset current (see Note 4)		V_O = 5 V,	V_{IC} = 5 V	25°C		0.1		pA
					70°C		7	300	
I_{IB}	Input bias current (see Note 4)		V_O = 5 V,	V_{IC} = 5 V	25°C		0.7		pA
					70°C		50	600	
V_{ICR}	Common-mode input voltage range (see Note 5)				25°C	−0.2 to 9	−0.3 to 9.2		V
					Full range	−0.2 to 8.5			V
V_{OH}	High-level output voltage		V_{ID} = 100 mV,	R_L = 1 MΩ	25°C	8	8.9		V
					0°C	7.8	8.9		
					70°C	7.8	8.9		
V_{OL}	Low-level output voltage		V_{ID} = −100 mV,	I_{OL} = 0	25°C		0	50	mV
					0°C		0	50	
					70°C		0	50	
A_{VD}	Large-signal differential voltage amplification		V_O = 1 V to 6 V,	R_L = 1 MΩ	25°C	50	870		V/mV
					0°C	50	1020		
					70°C	50	660		
CMRR	Common-mode rejection ratio		V_{IC} = V_{ICR} min		25°C	65	97		dB
					0°C	60	97		
					70°C	60	97		
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)		V_{DD} = 5 V to 10 V,	V_O = 1.4 V	25°C	70	97		dB
					0°C	60	97		
					70°C	60	98		
I_{DD}	Supply current (four amplifiers)		V_O = 5 V, No load	V_{IC} = 5 V,	25°C		57	92	µA
					0°C		72	132	
					70°C		44	80	

†Full range is 0°C to 70°C.

NOTES: 4. The typical values of input bias current and input offset current below 5 pA were determined mathematically.
5. This range also applies to each input individually.

electrical characteristics at specified free-air temperature, V_{DD} = 5 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS	T_A†	MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	TLC27L4I	V_O = 1.4 V, V_{IC} = 0, R_S = 50 Ω, R_L = 1 MΩ	25°C		1.1	10	mV
				Full range			13	
		TLC27L4AI	V_O = 1.4 V, V_{IC} = 0, R_S = 50 Ω, R_L = 1 MΩ	25°C		0.9	5	
				Full range			7	
		TLC27L4BI	V_O = 1.4 V, V_{IC} = 0, R_S = 50 Ω, R_L = 1 MΩ	25°C		240	2000	µV
				Full range			3500	
		TLC27L9I	V_O = 1.4 V, V_{IC} = 0, R_S = 50 Ω, R_L = 1 MΩ	25°C		200	900	
				Full range			2000	
α_{VIO}	Average temperature coefficient of input offset voltage			25°C to 85°C		1.1		µV/°C
I_{IO}	Input offset current (see Note 4)		V_O = 2.5 V, V_{IC} = 2.5 V	25°C		0.1		pA
				85°C		24	1000	
I_{IB}	Input bias current (see Note 4)		V_O = 2.5 V, V_{IC} = 2.5 V	25°C		0.6		pA
				85°C		200	2000	
V_{ICR}	Common-mode input voltage range (see Note 5)			25°C	−0.2 to 4	−0.3 to 4.2		V
				Full range	−0.2 to 3.5			V
V_{OH}	High-level output voltage		V_{ID} = 100 mV, R_L = 1 MΩ	25°C	3.2	4.1		V
				−40°C	3	4.1		
				85°C	3	4.2		
V_{OL}	Low-level output voltage		V_{ID} = −100 mV, I_{OL} = 0	25°C		0	50	mV
				−40°C		0	50	
				85°C		0	50	
A_{VD}	Large-signal differential voltage amplification		V_O = 0.25 V to 2 V, R_L = 1 MΩ	25°C	50	480		V/mV
				−40°C	50	900		
				85°C	50	330		
CMRR	Common-mode rejection ratio		V_{IC} = V_{ICR} min	25°C	65	94		dB
				−40°C	60	95		
				85°C	60	95		
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)		V_{DD} = 5 V to 10 V, V_O = 1.4 V	25°C	70	97		dB
				−40°C	60	97		
				85°C	60	98		
I_{DD}	Supply current (four amplifiers)		V_O = 2.5 V, V_{IC} = 2.5 V, No load	25°C		39	68	µA
				−40°C		62	108	
				85°C		29	52	

†Full range is −40°C to 85°C.

NOTES: 4. The typical values of input bias current and input offset current below 5 pA were determined mathematically.
5. This range also applies to each input individually.

electrical characteristics at specified free-air temperature, V_{DD} = 10 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS	T_A†	MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	TLC27L4I	V_O = 1.4 V, V_{IC} = 0, R_S = 50 Ω, R_L = 1 MΩ	25°C		1.1	10	mV
				Full range			13	
		TLC27L4AI	V_O = 1.4 V, V_{IC} = 0, R_S = 50 Ω, R_L = 1 MΩ	25°C		0.9	5	
				Full range			7	
		TLC27L4BI	V_O = 1.4 V, V_{IC} = 0, R_S = 50 Ω, R_L = 1 MΩ	25°C		260	2000	μV
				Full range			3500	
		TLC27L9I	V_O = 1.4 V, V_{IC} = 0, R_S = 50 Ω, R_L = 1 MΩ	25°C		210	1200	
				Full range			2900	
α_{VIO}	Average temperature coefficient of input offset voltage			25°C to 85°C		1		μV/°C
I_{IO}	Input offset current (see Note 4)		V_O = 5 V, V_{IC} = 5 V	25°C		0.1		pA
				85°C		26	1000	
I_{IB}	Input bias current (see Note 4)		V_O = 5 V, V_{IC} = 5 V	25°C		0.7		pA
				85°C		220	2000	
V_{ICR}	Common-mode input voltage range (see Note 5)			25°C	−0.2 to 9	−0.3 to 9.2		V
				Full range	−0.2 to 8.5			V
V_{OH}	High-level output voltage		V_{ID} = 100 mV, R_L = 1 MΩ	25°C	8	8.9		V
				−40°C	7.8	8.9		
				85°C	7.8	8.9		
V_{OL}	Low-level output voltage		V_{ID} = −100 mV, I_{OL} = 0	25°C		0	50	mV
				−40°C		0	50	
				85°C		0	50	
A_{VD}	Large-signal differential voltage amplification		V_O = 1 V to 6 V, R_L = 1 MΩ	25°C	50	800		V/mV
				−40°C	50	1550		
				85°C	50	585		
CMRR	Common-mode rejection ratio		V_{IC} = V_{ICR} min	25°C	65	97		dB
				−40°C	60	97		
				85°C	60	98		
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)		V_{DD} = 5 V to 10 V, V_O = 1.4 V	25°C	70	97		dB
				−40°C	60	97		
				85°C	60	98		
I_{DD}	Supply current (four amplifiers)		V_O = 5 V, V_{IC} = 5 V, No load	25°C		57	92	μA
				−40°C		98	172	
				85°C		40	72	

†Full range is −40°C to 85°C.

NOTES: 4. The typical values of input bias current and input offset current below 5 pA were determined mathematically.
5. This range also applies to each input individually.

electrical characteristics at specified free-air temperature, V_{DD} = 5 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS	T_A†	MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	TLC27L4M	V_O = 1.4 V, V_{IC} = 0, R_S = 50 Ω, R_L = 1 MΩ	25°C		1.1	10	mV
				Full range			12	
		TLC27L9M	V_O = 1.4 V, V_{IC} = 0, R_S = 50 Ω, R_L = 1 MΩ	25°C		200	900	µV
				Full range			3750	
α_{VIO}	Average temperature coefficient of input offset voltage			25°C to 125°C		1.4		µV/°C
I_{IO}	Input offset current (see Note 4)		V_O = 2.5 V, V_{IC} = 2.5 V	25°C		0.1		pA
				125°C		1.4	15	nA
I_{IB}	Input bias current (see Note 4)		V_O = 2.5 V, V_{IC} = 2.5 V	25°C		0.6		pA
				125°C		9	35	nA
V_{ICR}	Common-mode input voltage range (see Note 5)			25°C	0 to 4	−0.3 to 4.2		V
				Full range	0 to 3.5			V
V_{OH}	High-level output voltage		V_{ID} = 100 mV, R_L = 1 MΩ	25°C	3.2	4.1		V
				−55°C	3	4.1		
				125°C	3	4.2		
V_{OL}	Low-level output voltage		V_{ID} = −100 mV, I_{OL} = 0	25°C		0	50	mV
				−55°C		0	50	
				125°C		0	50	
A_{VD}	Large-signal differential voltage amplification		V_O = 0.25 V to 2 V, R_L = 1 MΩ	25°C	50	480		V/mV
				−55°C	25	950		
				125°C	25	200		
CMRR	Common-mode rejection ratio		V_{IC} = V_{ICR} min	25°C	65	94		dB
				−55°C	60	95		
				125°C	60	85		
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)		V_{DD} = 5 V to 10 V, V_O = 1.4 V	25°C	70	97		dB
				−55°C	60	97		
				125°C	60	98		
I_{DD}	Supply current (four amplifiers)		V_O = 2.5 V, V_{IC} = 2.5 V, No load	25°C		39	68	µA
				−55°C		69	120	
				125°C		27	48	

†Full range is −55°C to 125°C.

NOTES: 4. The typical values of input bias current and input offset current below 5 pA were determined mathematically.

5. This range also applies to each input individually.

electrical characteristics at specified free-air temperature, V_{DD} = 10 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS		T_A†	MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	TLC27L4M	V_O = 1.4 V, R_S = 50 Ω,	V_{IC} = 0, R_L = 1 MΩ	25°C		1.1	10	mV
					Full range			12	
		TLC27L9M	V_O = 1.4 V, R_S = 50 Ω,	V_{IC} = 0, R_L = 1 MΩ	25°C		210	1200	µV
					Full range			4300	
α_{VIO}	Average temperature coefficient of input offset voltage				25°C to 125°C		1.4		µV/°C
I_{IO}	Input offset current (see Note 4)		V_O = 5 V,	V_{IC} = 5 V	25°C		0.1		pA
					125°C		1.8	15	nA
I_{IB}	Input bias current (see Note 4)		V_O = 5 V,	V_{IC} = 5 V	25°C		0.7		pA
					125°C		10	35	nA
V_{ICR}	Common-mode input voltage range (see Note 5)				25°C	0 to 9	−0.3 to 9.2		V
					Full range	0 to 8.5			V
V_{OH}	High-level output voltage		V_{ID} = 100 mV,	R_L = 1 MΩ	25°C	8	8.9		V
					−55°C	7.8	8.8		
					125°C	7.8	9		
V_{OL}	Low-level output voltage		V_{ID} = −100 mV,	I_{OL} = 0	25°C		0	50	mV
					−55°C		0	50	
					125°C		0	50	
A_{VD}	Large-signal differential voltage amplification		V_O = 1 V to 6 V,	R_L = 1 MΩ	25°C	50	800		V/mV
					−55°C	25	1750		
					125°C	25	380		
CMRR	Common-mode rejection ratio		V_{IC} = V_{ICR} min		25°C	65	97		dB
					−55°C	60	97		
					125°C	60	91		
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)		V_{DD} = 5 V to 10 V,	V_O = 1.4 V	25°C	70	97		dB
					−55°C	60	97		
					125°C	60	98		
I_{DD}	Supply current (four amplifiers)		V_O = 5 V, No load	V_{IC} = 5 V,	25°C		57	92	µA
					−55°C		111	192	
					125°C		35	60	

†Full range is −55°C to 125°C.

NOTES: 4. The typical values of input bias current and input offset current below 5 pA were determined mathematically.
5. This range also applies to each input individually.

operating characteristics, V_{DD} = 5 V

PARAMETER		TEST CONDITIONS		T_A	MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain	R_L = 1 MΩ, C_L = 20 pF, See Figure 1	V_{IPP} = 1 V	25°C		0.03		V/μs
				0°C		0.04		
				70°C		0.03		
			V_{IPP} = 2.5 V	25°C		0.03		
				0°C		0.03		
				70°C		0.02		
V_n	Equivalent input noise voltage	f = 1 kHz, See Figure 2	R_S = 100 Ω,	25°C		70		nV/√Hz
B_{OM}	Maximum output swing bandwidth	V_O = V_{OH}, R_L = 1 MΩ,	C_L = 20 pF, See Figure 1	25°C		5		kHz
				0°C		6		
				70°C		4.5		
B_1	Unity-gain bandwidth	V_i = 10 mV, See Figure 3	C_L = 20 pF,	25°C		85		kHz
				0°C		100		
				70°C		65		
ϕ_m	Phase margin	V_i = 10 mV, C_L = 20 pF,	f = B_1, See Figure 3	25°C		34°		
				0°C		36°		
				70°C		30°		

operating characteristics, V_{DD} = 10 V

PARAMETER		TEST CONDITIONS		T_A	MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain	R_L = 1 MΩ, C_L = 20 pF, See Figure 1	V_{IPP} = 1 V	25°C		0.05		V/μs
				0°C		0.05		
				70°C		0.04		
			V_{IPP} = 5.5 V	25°C		0.04		
				0°C		0.05		
				70°C		0.04		
V_n	Equivalent input noise voltage	f = 1 kHz, See Figure 2	R_S = 100 Ω,	25°C		70		nV/√Hz
B_{OM}	Maximum output swing bandwidth	V_O = V_{OH}, R_L = 1 MΩ,	C_L = 20 pF, See Figure 1	25°C		1		kHz
				0°C		1.3		
				70°C		0.9		
B_1	Unity-gain bandwidth	V_i = 10 mV, See Figure 3	C_L = 20 pF,	25°C		110		kHz
				0°C		125		
				70°C		90		
ϕ_m	Phase margin	V_i = 10 mV, C_L = 20 pF,	f = B_1, See Figure 3	25°C		38°		
				0°C		40°		
				70°C		34°		

operating characteristics, V_{DD} = 5 V

PARAMETER		TEST CONDITIONS		T_A	MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain	R_L = 1 MΩ, C_L = 20 pF, See Figure 1	V_{IPP} = 1 V	25°C		0.03		V/μs
				−40°C		0.04		
				85°C		0.03		
			V_{IPP} = 2.5 V	25°C		0.03		
				−40°C		0.04		
				85°C		0.02		
V_n	Equivalent input noise voltage	f = 1 kHz, See Figure 2	R_S = 100 Ω,	25°C		70		nV/√Hz
B_{OM}	Maximum output swing bandwidth	V_O = V_{OH}, R_L = 1 MΩ,	C_L = 20 pF, See Figure 1	25°C		5		kHz
				−40°C		7		
				85°C		4		
B_1	Unity-gain bandwidth	V_i = 10 mV, See Figure 3	C_L = 20 pF,	25°C		85		kHz
				−40°C		130		
				85°C		55		
ϕ_m	Phase margin	V_i = 10 mV, C_L = 20 pF,	f = B_1, See Figure 3	25°C		34°		
				−40°C		38°		
				85°C		28°		

operating characteristics, V_{DD} = 10 V

PARAMETER		TEST CONDITIONS		T_A	MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain	R_L = 1 MΩ, C_L = 20 pF, See Figure 1	V_{IPP} = 1 V	25°C		0.05		V/μs
				−40°C		0.06		
				85°C		0.03		
			V_{IPP} = 5.5 V	25°C		0.04		
				−40°C		0.05		
				85°C		0.03		
V_n	Equivalent input noise voltage	f = 1 kHz, See Figure 2	R_S = 100 Ω,	25°C		70		nV/√Hz
B_{OM}	Maximum output swing bandwidth	V_O = V_{OH}, R_L = 1 MΩ,	C_L = 20 pF, See Figure 1	25°C		1		kHz
				−40°C		1.4		
				85°C		0.8		
B_1	Unity-gain bandwidth	V_i = 10 mV, See Figure 3	C_L = 20 pF,	25°C		110		kHz
				−40°C		155		
				85°C		80		
ϕ_m	Phase margin	V_i = 10 mV, C_L = 20 pF,	f = B_1, See Figure 3	25°C		38°		
				−40°C		42°		
				85°C		32°		

operating characteristics, V_{DD} = 5 V

PARAMETER		TEST CONDITIONS		T_A	MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain	R_L = 1 MΩ, C_L = 20 pF, See Figure 1	V_{IPP} = 1 V	25°C		0.03		V/μs
				−55°C		0.04		
				125°C		0.02		
			V_{IPP} = 2.5 V	25°C		0.03		
				−55°C		0.04		
				125°C		0.02		
V_n	Equivalent input noise voltage	f = 1 kHz, See Figure 2	R_S = 100 Ω,	25°C		70		nV/$\sqrt{\text{Hz}}$
B_{OM}	Maximum output swing bandwidth	V_O = V_{OH}, R_L = 1 MΩ,	C_L = 20 pF, See Figure 1	25°C		5		kHz
				−55°C		8		
				125°C		3		
B_1	Unity-gain bandwidth	V_i = 10 mV, See Figure 3	C_L = 20 pF,	25°C		85		kHz
				−55°C		140		
				125°C		45		
ϕ_m	Phase margin	V_i = 10 mV, C_L = 20 pF,	f = B_1, See Figure 3	25°C		34°		
				−55°C		39°		
				125°C		25°		

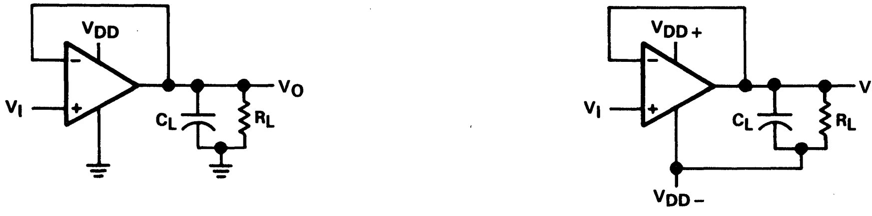
operating characteristics, V_{DD} = 10 V

PARAMETER		TEST CONDITIONS		T_A	MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain	R_L = 1 MΩ, C_L = 20 pF, See Figure 1	V_{IPP} = 1 V	25°C		0.05		V/μs
				−55°C		0.06		
				125°C		0.03		
			V_{IPP} = 5.5 V	25°C		0.04		
				−55°C		0.06		
				125°C		0.03		
V_n	Equivalent input noise voltage	f = 1 kHz, See Figure 2	R_S = 100 Ω,	25°C		70		nV/$\sqrt{\text{Hz}}$
B_{OM}	Maximum output swing bandwidth	V_O = V_{OH}, R_L = 1 MΩ,	C_L = 20 pF, See Figure 1	25°C		1		kHz
				−55°C		1.5		
				125°C		0.7		
B_1	Unity-gain bandwidth	V_i = 10 mV, See Figure 3	C_L = 20 pF,	25°C		110		kHz
				−55°C		165		
				125°C		70		
ϕ_m	Phase margin	V_i = 10 mV, C_L = 20 pF,	f = B_1, See Figure 3	25°C		38°		
				−55°C		43°		
				125°C		29°		

PARAMETER MEASUREMENT INFORMATION

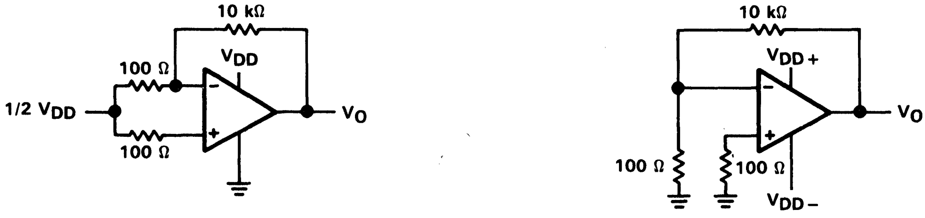
single-supply versus split-supply test circuits

Because the TLC27L4 and TLC27L9 are optimized for single-supply operation, circuit configurations used for the various tests often present some inconvenience since the input signal, in many cases, must be offset from ground. This inconvenience can be avoided by testing the device with split supplies and the output load tied to the negative rail. A comparison of single-supply versus split-supply test circuits is shown below. The use of either circuit will give the same result.



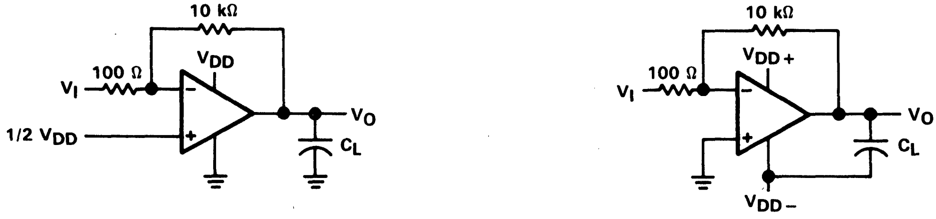
(a) SINGLE-SUPPLY (b) SPLIT-SUPPLY

FIGURE 1. UNITY-GAIN AMPLIFIER



(a) SINGLE-SUPPLY (b) SPLIT-SUPPLY

FIGURE 2. NOISE TEST CIRCUIT



(a) SINGLE-SUPPLY (b) SPLIT-SUPPLY

FIGURE 3. GAIN-OF-100 INVERTING AMPLIFIER

PARAMETER MEASUREMENT INFORMATION

input bias current

Because of the high input impedance of the TLC27L4 and TLC27L9 op amps, attempts to measure the input bias current can result in erroneous readings. The bias current at normal room ambient temperature is typically less than 1 pA, a value that is easily exceeded by leakages on the test socket. Two suggestions are offered to avoid erroneous measurements:

1. Isolate the device from other potential leakage sources. Use a grounded shield around and between the device inputs (see Figure 4). Leakages that would otherwise flow to the inputs will be shunted away.
2. Compensate for the leakage of the test socket by actually performing an input bias current test (using a picoammeter) with no device in the test socket. The actual input bias current can then be calculated by subtracting the "open-socket" leakage readings from the readings obtained with a device in the test socket.

One word of caution . . . many automatic testers as well as some bench-top op amp testers use the servo-loop technique with a resistor in series with the device input to measure the input bias current (the voltage drop across the series resistor is measured and the bias current is calculated). This method requires that a device be inserted into the test socket to obtain a correct reading; therefore, an "open-socket" reading is not feasible using this method.

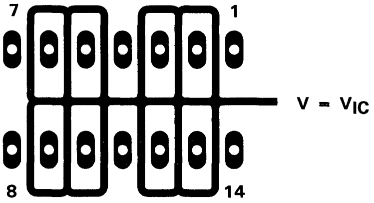


FIGURE 4. ISOLATION METAL AROUND DEVICE INPUTS
(J AND N DUAL-IN-LINE-PACKAGE)

low-level output voltage

To obtain low-supply-voltage operation, some compromise was necessary in the input stage. This compromise results in the device low-level output being dependent on both the common-mode input voltage level as well as the differential input voltage level. When attempting to correlate low-level output readings with those quoted in the electrical specifications, these two conditions should be observed. If conditions other than these are to be used, please refer to Figures 14 through 19 in the Typical Characteristics of this data sheet.

input offset voltage temperature coefficient

Erroneous readings often result from attempts to measure temperature coefficient of input offset voltage. This parameter is actually a calculation using input offset voltage measurements obtained at two different temperatures. When one (or both) of the temperatures is below freezing, moisture can collect on both the device and the test socket. This moisture will result in leakage and contact resistance, which can cause erroneous input offset voltage readings. The isolation techniques previously mentioned have no effect on the leakage since the moisture also covers the isolation metal itself, thereby rendering it useless. It is suggested that these measurements be performed at temperatures above freezing to minimize error.

PARAMETER MEASUREMENT INFORMATION

full-power response

Full-power response, the frequency above which the op amp slew rate limits the output voltage swing, is often specified two ways . . . full-linear response and full-peak response. The full-linear response is generally measured by monitoring the distortion level of the output while increasing the frequency of a sinusoidal input signal until the maximum frequency is found above which the output contains significant distortion. The full-peak response is defined as the maximum output frequency, without regard to distortion, above which full peak-to-peak output swing cannot be maintained.

Because there is no industry-wide accepted value for "significant" distortion, the full-peak response is specified in this data sheet and is measured using the circuit of Figure 1. The initial setup involves the use of a sinusoidal input to determine the maximum peak-to-peak output of the device (the amplitude of the sinusoidal wave is increased until clipping occurs). The sinusoidal wave is then replaced with a square wave of the same amplitude. The frequency is then increased until the maximum peak-to-peak output can no longer be maintained (Figure 5). A square wave is used to allow a more accurate determination of the point at which the maximum peak-to-peak output is reached.

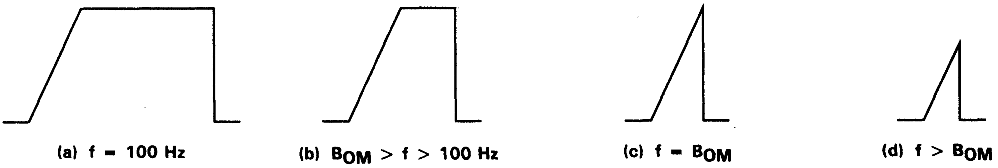


FIGURE 5. FULL-POWER-RESPONSE OUTPUT SIGNAL

test time

Inadequate test time is a frequent problem, especially when testing CMOS devices in a high-volume, short-test-time environment. Internal capacitances are inherently higher in CMOS than in bipolar and BiFET devices and require longer test times than their bipolar and BiFET counterparts. The problem becomes more pronounced with reduced supply levels and lower temperatures.

TYPICAL CHARACTERISTICS

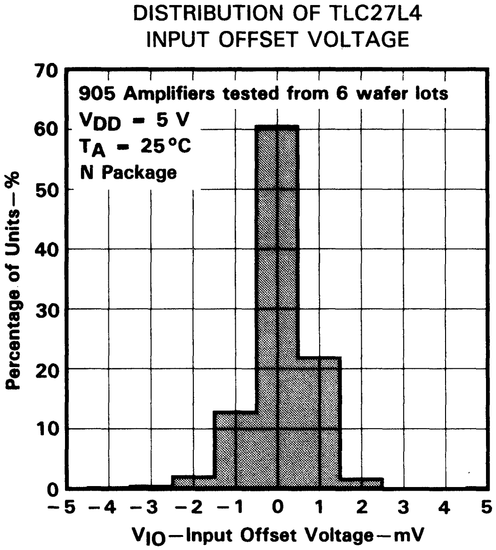

DISTRIBUTION OF TLC27L4
INPUT OFFSET VOLTAGE

FIGURE 6

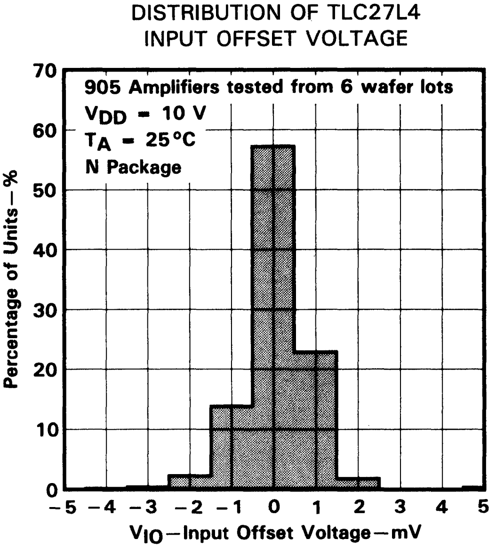

DISTRIBUTION OF TLC27L4
INPUT OFFSET VOLTAGE

FIGURE 7

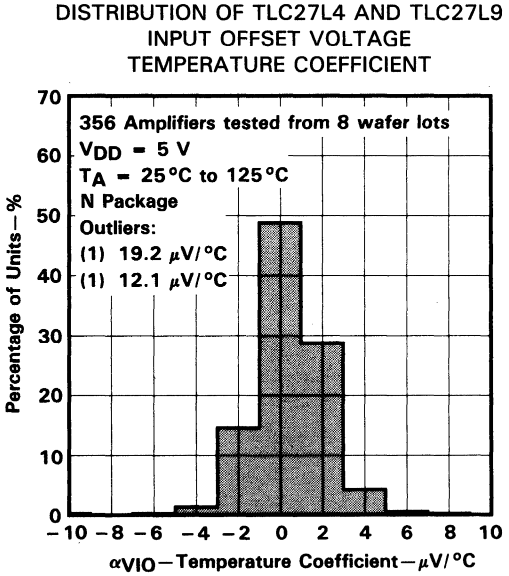

DISTRIBUTION OF TLC27L4 AND TLC27L9
INPUT OFFSET VOLTAGE
TEMPERATURE COEFFICIENT

FIGURE 8

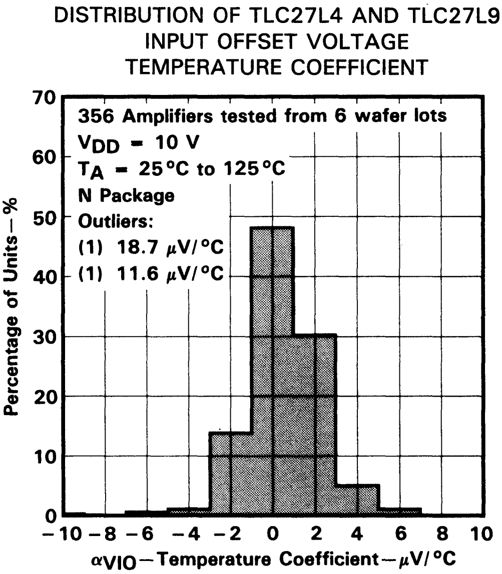

DISTRIBUTION OF TLC27L4 AND TLC27L9
INPUT OFFSET VOLTAGE
TEMPERATURE COEFFICIENT

FIGURE 9

TYPICAL CHARACTERISTICS[†]

HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

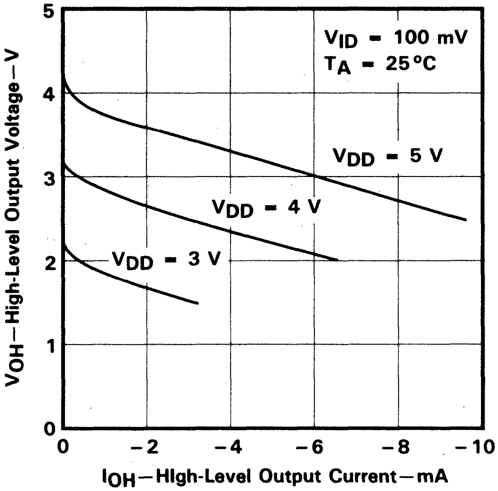


FIGURE 10

HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

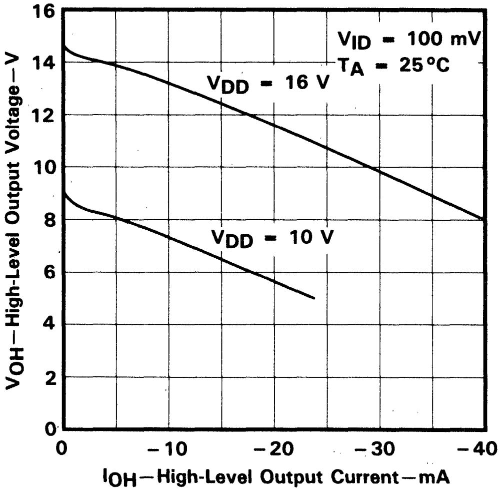


FIGURE 11

HIGH-LEVEL OUTPUT VOLTAGE
vs
SUPPLY VOLTAGE

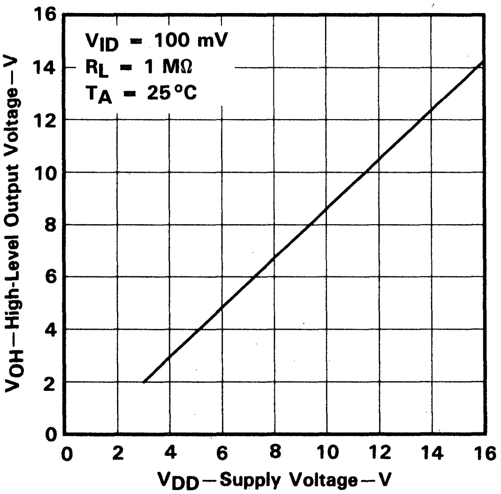


FIGURE 12

HIGH-LEVEL OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

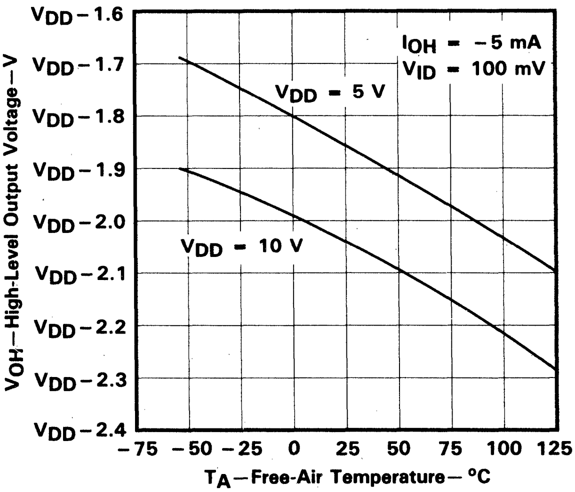


FIGURE 13

[†] Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

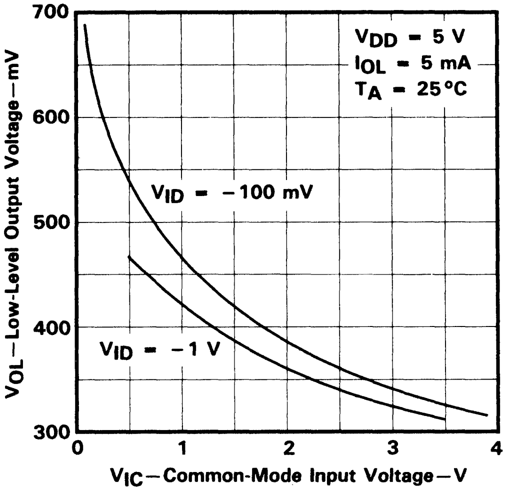

LOW-LEVEL OUTPUT VOLTAGE
vs
COMMON-MODE INPUT VOLTAGE

FIGURE 14

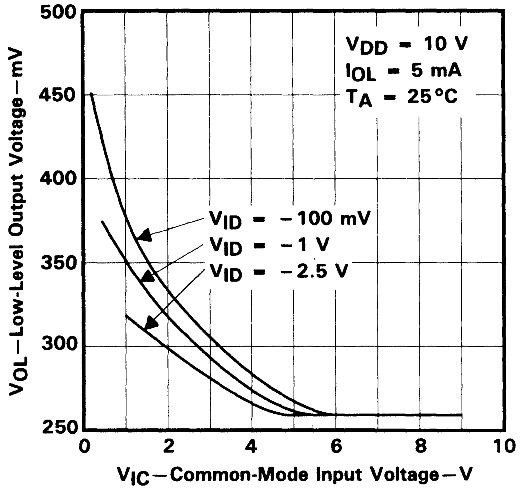

LOW-LEVEL OUTPUT VOLTAGE
vs
COMMON-MODE INPUT VOLTAGE

FIGURE 15

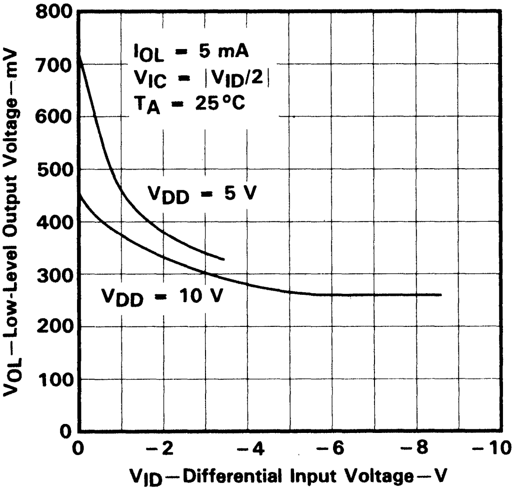

LOW-LEVEL OUTPUT VOLTAGE
vs
DIFFERENTIAL INPUT VOLTAGE

FIGURE 16

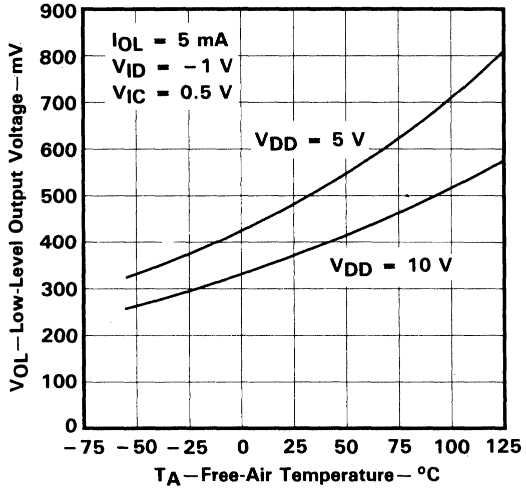

LOW-LEVEL OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

FIGURE 17

---

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS[†]

LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

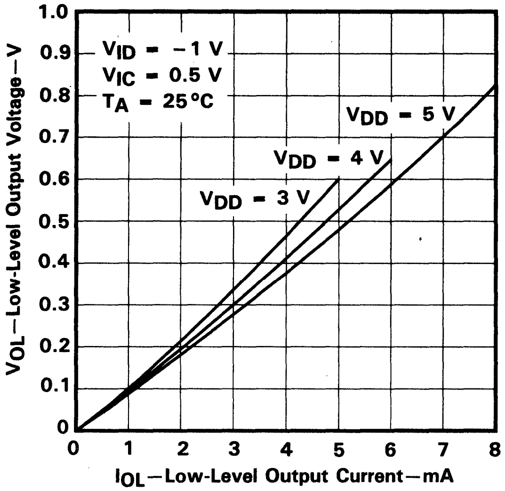


FIGURE 18

LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

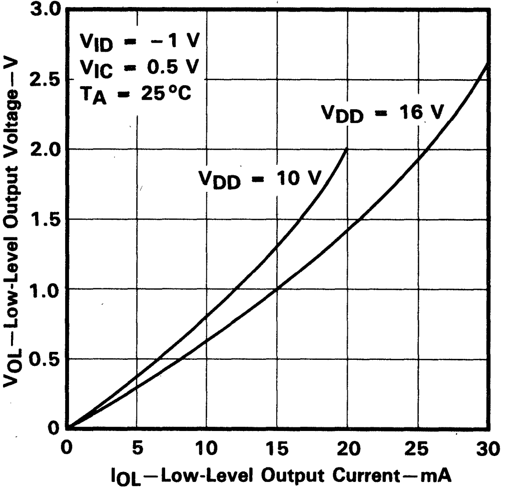


FIGURE 19

LARGE-SIGNAL
DIFFERENTIAL VOLTAGE AMPLIFICATION
vs
SUPPLY VOLTAGE

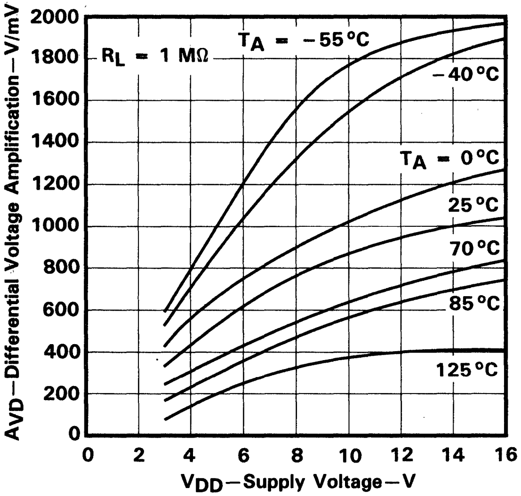


FIGURE 20

LARGE-SIGNAL
DIFFERENTIAL VOLTAGE AMPLIFICATION
vs
FREE-AIR TEMPERATURE

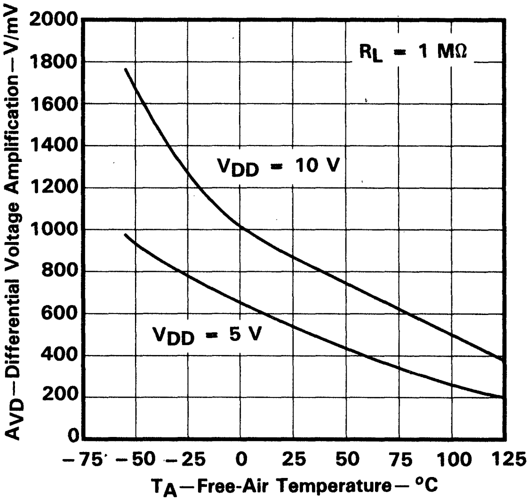


FIGURE 21

[†] Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

INPUT BIAS CURRENT AND INPUT OFFSET CURRENT
vs
FREE-AIR TEMPERATURE

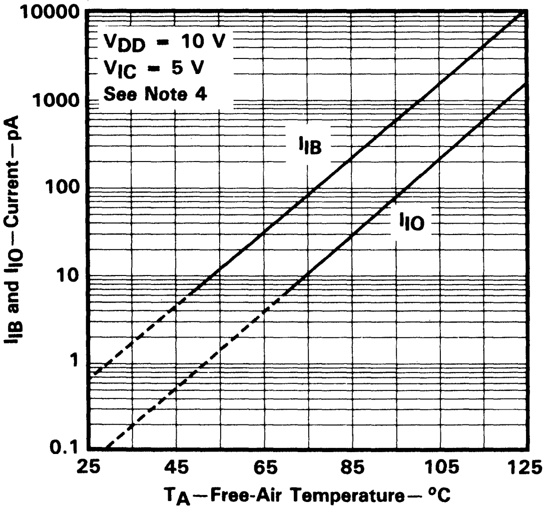


FIGURE 22

COMMON-MODE
INPUT VOLTAGE POSITIVE LIMIT
vs
SUPPLY VOLTAGE

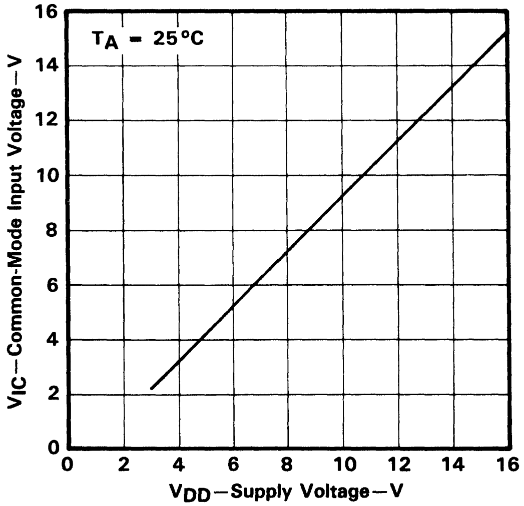


FIGURE 23

SUPPLY CURRENT
vs
SUPPLY VOLTAGE

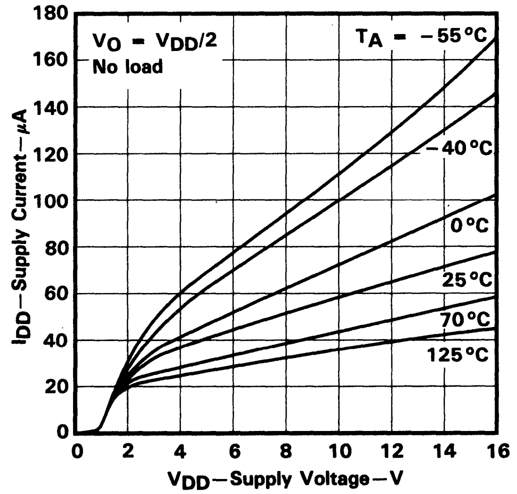


FIGURE 24

SUPPLY CURRENT
vs
FREE-AIR TEMPERATURE

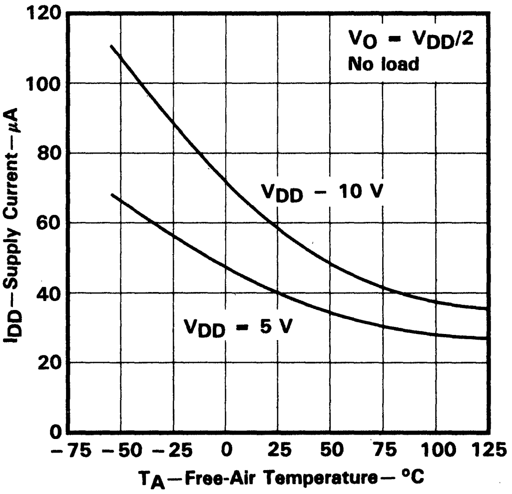


FIGURE 25

---

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.
NOTE 4: The typical values of input bias current and input offset current below 5 pA were determined mathematically.

TYPICAL CHARACTERISTICS†

SLEW RATE
vs
SUPPLY VOLTAGE

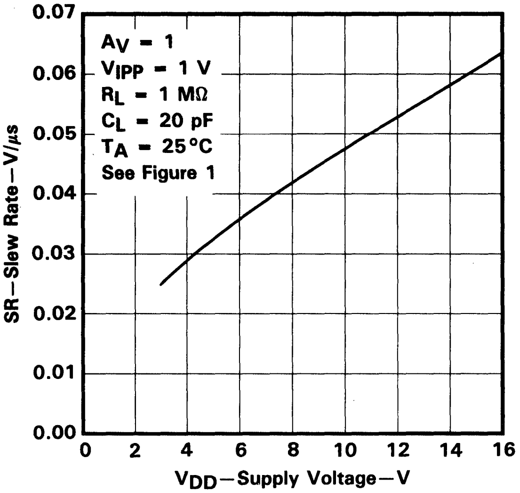


FIGURE 26

SLEW RATE
vs
FREE-AIR TEMPERATURE

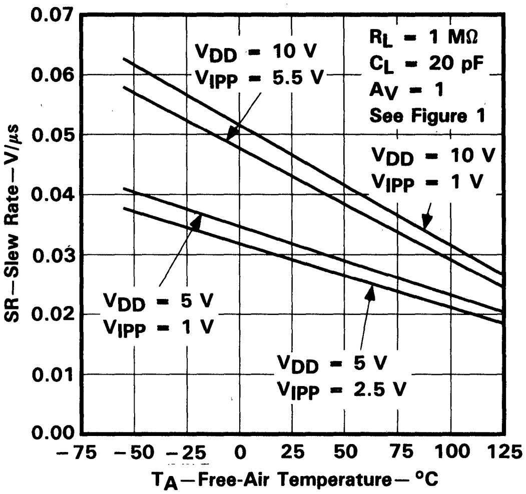


FIGURE 27

NORMALIZED SLEW RATE
vs
FREE-AIR TEMPERATURE

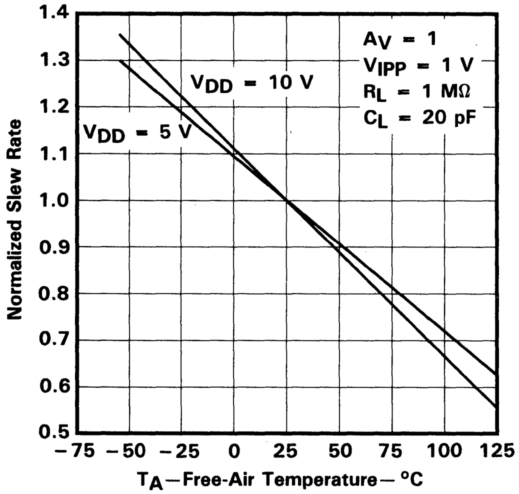


FIGURE 28

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE
vs
FREQUENCY

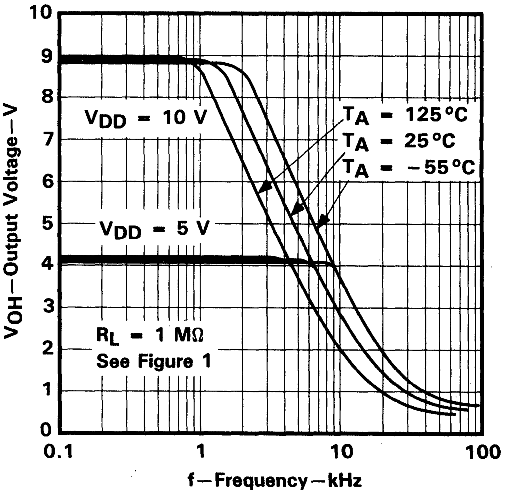


FIGURE 29

---

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

UNITY-GAIN BANDWIDTH
vs
FREE-AIR TEMPERATURE

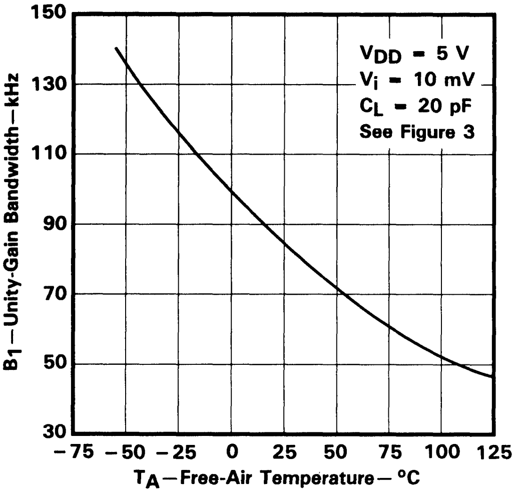


FIGURE 30

UNITY-GAIN BANDWIDTH
vs
SUPPLY VOLTAGE

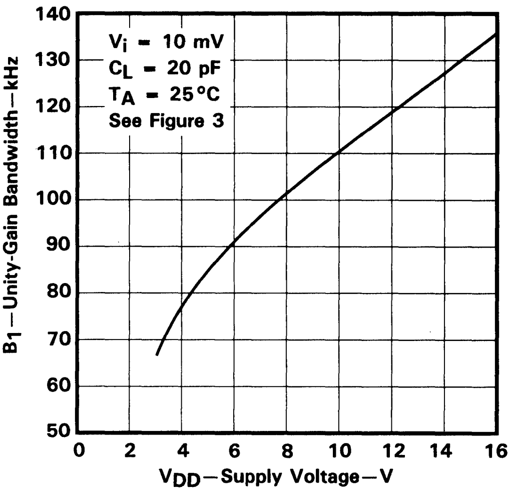


FIGURE 31

LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION AND PHASE SHIFT
vs
FREQUENCY

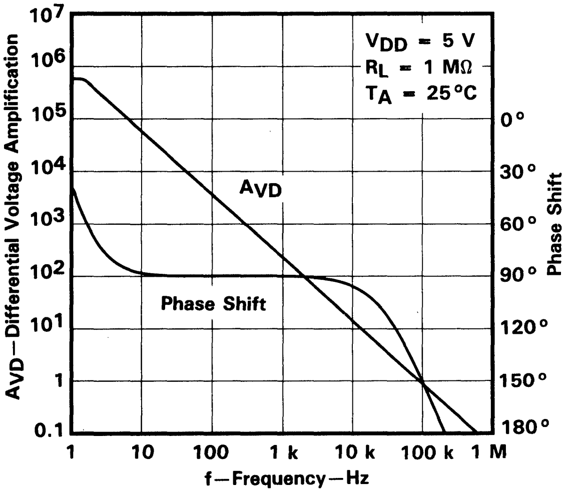


FIGURE 32

LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION AND PHASE SHIFT
vs
FREQUENCY

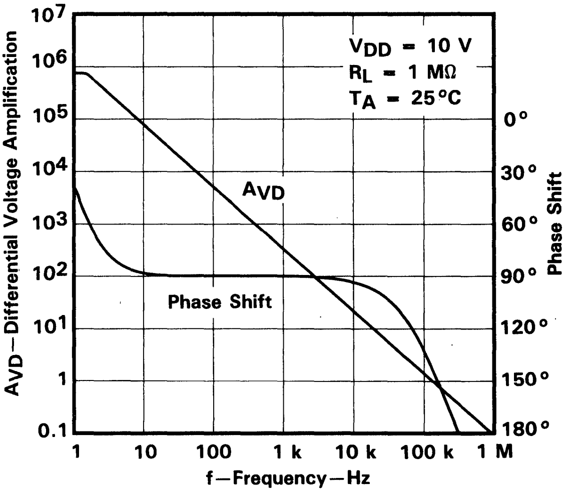


FIGURE 33

---

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

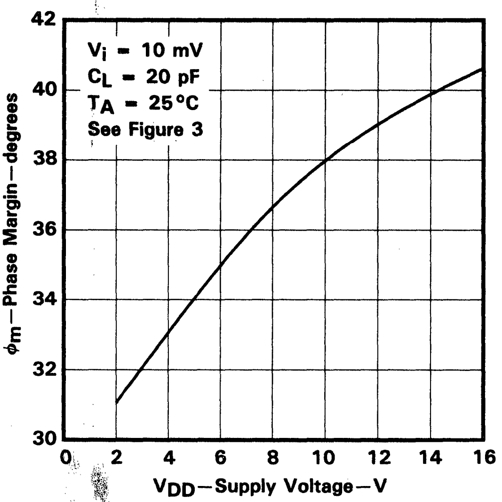

PHASE MARGIN
vs
SUPPLY VOLTAGE

FIGURE 34

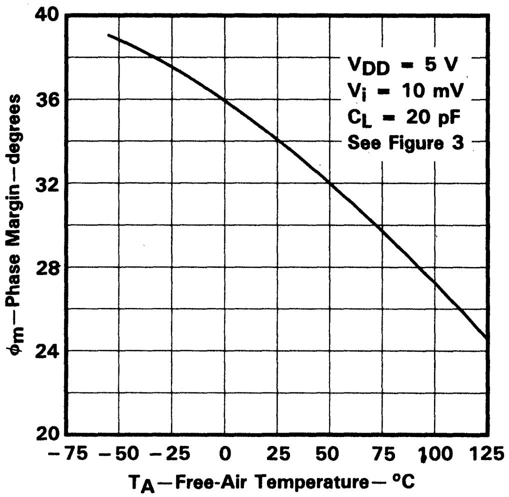

PHASE MARGIN
vs
FREE-AIR TEMPERATURE

FIGURE 35

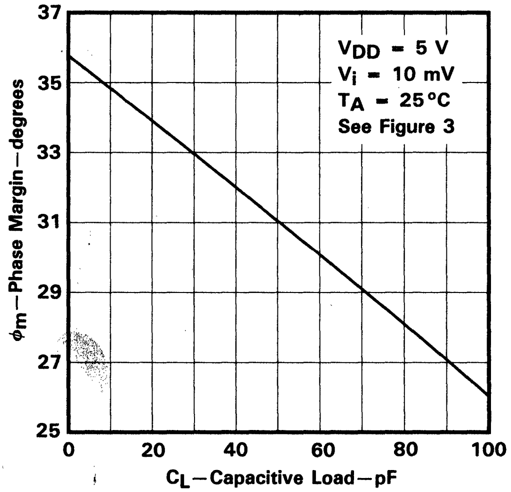

PHASE MARGIN
vs
CAPACITIVE LOAD

FIGURE 36

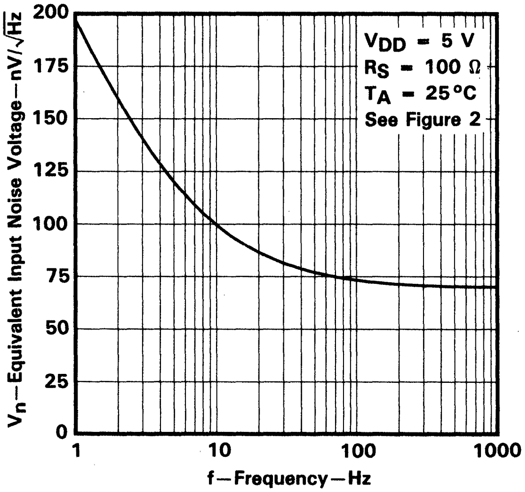

EQUIVALENT INPUT NOISE VOLTAGE
vs
FREQUENCY

FIGURE 37

---

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

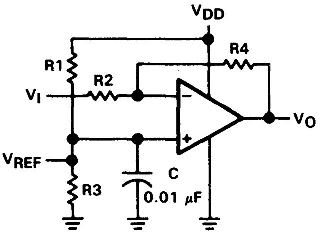
single-supply operation

While the TLC27L4 and TLC27L9 perform well using dual power supplies (also called balanced or split supplies), the design is optimized for single-supply operation. This design includes an input common-mode voltage range that encompasses ground as well as an output voltage range that pulls down to ground. The supply voltage range extends down to 3 V (C-suffix types), thus allowing operation with supply levels commonly available for TTL and HCMOS; however, for maximum dynamic range, 16-V single-supply operation is recommended.

Many single-supply applications require that a voltage be applied to one input to establish a reference level that is above ground. A resistive voltage divider is usually sufficient to establish this reference level (see Figure 38). The low input bias current of the TLC27L4 and TLC27L9 permits the use of very large resistive values to implement the voltage divider, thus minimizing power consumption.

The TLC27L4 and TLC27L9 work well in conjunction with digital logic; however, when powering both linear devices and digital logic from the same power supply, the following precautions are recommended:

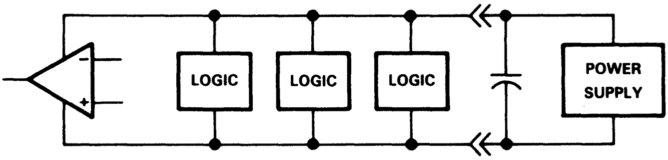
1. Power the linear devices from separate bypassed supply lines (see Figure 39); otherwise the linear device supply rails can fluctuate due to voltage drops caused by high switching currents in the digital logic.
2. Use proper bypass techniques to reduce the probability of noise-induced errors. Single capacitive decoupling is often adequate; however, high-frequency applications may require RC decoupling.



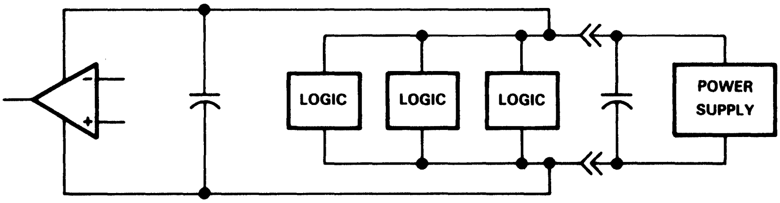
$$V_{REF} = V_{DD} \frac{R3}{R1 + R3}$$

$$V_O = \left(V_{REF} - V_I\right) \frac{R4}{R2} + V_{REF}$$

FIGURE 38. INVERTING AMPLIFIER WITH VOLTAGE REFERENCE



(a) COMMON SUPPLY RAILS



(b) SEPARATE BYPASSED SUPPLY RAILS (PREFERRED)

FIGURE 39. COMMON VS SEPARATE SUPPLY RAILS

TYPICAL APPLICATION DATA

input characteristics

The TLC27L4 and TLC27L9 are specified with a minimum and a maximum input voltage that, if exceeded at either input, could cause the device to malfunction. Exceeding this specified range is a common problem, especially in single-supply operation. Note that the lower range limit includes the negative rail, while the upper range limit is specified at $V_{DD} - 1$ V at $T_A = 25\,°C$ and at $V_{DD} - 1.5$ V at all other temperatures.

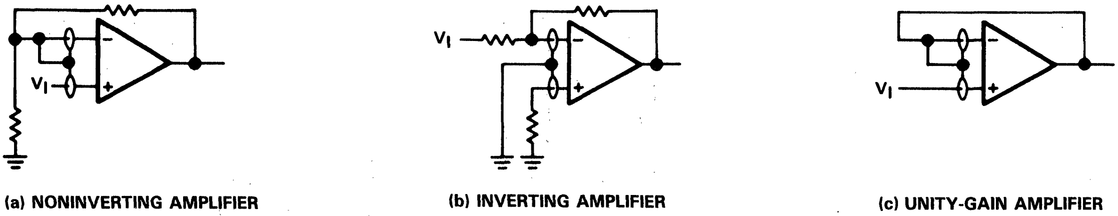
The use of the polysilicon-gate process and the careful input circuit design gives the TLC27L4 and TLC27L9 very good input offset voltage drift characteristics relative to conventional metal-gate processes. Offset voltage drift in CMOS devices is highly influenced by threshold voltage shifts caused by polarization of the phosphorus dopant implanted in the oxide. Placing the phosphorus dopant in a conductor (such as a polysilicon gate) alleviates the polarization problem, thus reducing threshold voltage shifts by more than an order of magnitude. The offset voltage drift with time has been calculated to be typically 0.1 μV/month, including the first month of operation.

Because of the extremely high input impedance and resulting low bias current requirements, the TLC27L4 and TLC27L9 are well suited for low-level signal processing; however, leakage currents on printed circuit boards and sockets can easily exceed bias current requirements and cause a degradation in device performance. It is good practice to include guard rings around inputs (similar to those of Figure 4 in the Parameter Measurement Information section). These guards should be driven from a low-impedance source at the same voltage level as the common-mode input (see Figure 40).

The inputs of any unused amplifiers should be tied to ground to avoid possible oscillation.

noise performance

The noise specifications in op amp circuits are greatly dependent on the current in the first-stage differential amplifier. The low input bias current requirements of the TLC27L4 and TLC27L9 result in a very low noise current, which is insignificant in most applications. This feature makes the devices especially favorable over bipolar devices when using values of circuit impedance greater than 50 kΩ, since bipolar devices exhibit greater noise currents.



(a) NONINVERTING AMPLIFIER (b) INVERTING AMPLIFIER (c) UNITY-GAIN AMPLIFIER

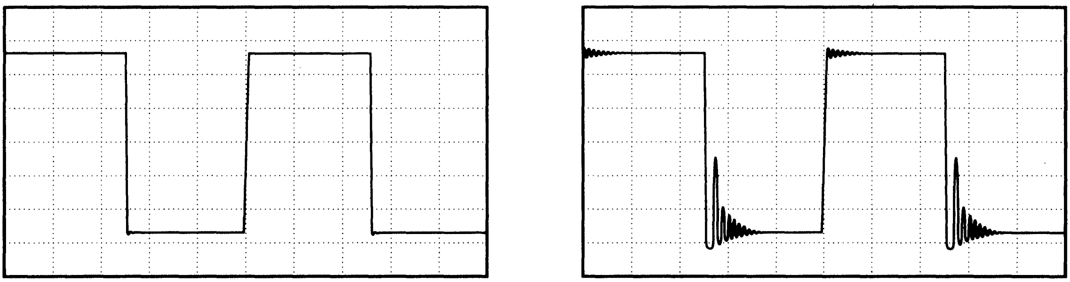
FIGURE 40. GUARD-RING SCHEMES

output characteristics

The output stage of the TLC27L4 and TLC27L9 is designed to sink and source relatively high amounts of current (see typical characteristics). If the output is subjected to a short-circuit condition, this high current capability can cause device damage under certain conditions. Output current capability increases with supply voltage.

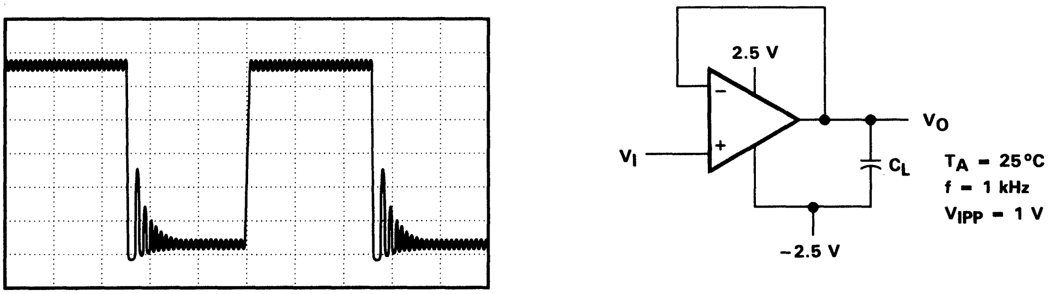
All operating characteristics of the TLC27L4 and TLC27L9 were measured using a 20-pF load. The devices will drive higher capacitive loads; however, as output load capacitance increases, the resulting response pole occurs at lower frequencies, thereby causing ringing, peaking, or even oscillation (see Figure 41). In many cases, adding a small amount of resistance in series with the load capacitance will alleviate the problem.

TYPICAL APPLICATION DATA



(a) C_L = 20 pF, R_L = NO LOAD

(b) C_L = 260 pF, R_L = NO LOAD



(c) C_L = 310 pF, R_L = NO LOAD

(d) TEST CIRCUIT

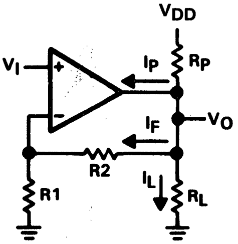
FIGURE 41. EFFECT OF CAPACITIVE LOADS AND TEST CIRCUIT

Although the TLC27L4 and TLC27L9 possess excellent high-level output voltage and current capability, methods for boosting this capability are available, if needed. The simplest method involves the use of a pullup resistor (R_P) connected from the output to the positive supply rail (see Figure 42). There are two disadvantages to the use of this circuit. First, the NMOS pulldown transistor N4 (see equivalent schematic) must sink a comparatively large amount of current. In this circuit, N4 behaves like a linear resistor with an on-resistance between approximately 60 Ω and 180 Ω, depending on how hard the op amp input is driven. With very low values of R_P, a voltage offset from 0 V at the output will occur. Second, pullup resistor R_P acts as a drain load to N4 and the gain of the op amp is reduced at output voltage levels where N5 is not supplying the output current.

feedback

Op amp circuits nearly always employ feedback, and since feedback is the first prerequisite for oscillation, some caution is appropriate. Most oscillation problems result from driving capacitive loads (discussed previously) and ignoring stray input capacitance. A small-value capacitor connected in parallel with the feedback resistor is an effective remedy (see Figure 43). The value of this capacitor is optimized empirically.

TYPICAL APPLICATION DATA



$$R_P = \frac{V_{DD} - V_O}{I_F + I_L + I_P}$$

I_P = Pullup current required by the op amp (typically 500 μA)

FIGURE 42. RESISTIVE PULLUP TO INCREASE V_{OH}

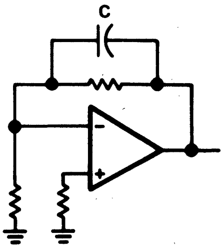


FIGURE 43. COMPENSATION FOR INPUT CAPACITANCE

electrostatic discharge protection

The TLC27L4 and TLC27L9 incorporate an internal electrostatic discharge (ESD) protection circuit that prevents functional failures at voltages up to 2000 V as tested under MIL-STD-883C, Method 3015.2. Care should be exercised, however, when handling these devices, as exposure to ESD may result in the degradation of the device parametric performance. The protection circuit also causes the input bias currents to be temperature dependent and have the characteristics of a reverse-biased diode.

latch-up

Because CMOS devices are susceptible to latch-up due to their inherent parasitic thyristors, the TLC27L4 and TLC27L9 inputs and outputs were designed to withstand −100-mA surge currents without sustaining latch-up; however, techniques should be used to reduce the chance of latch-up whenever possible. Internal protection diodes should not, by design, be forward biased. Applied input and output voltage should not exceed the supply voltage by more than 300 mV. Care should be exercised when using capacitive coupling on pulse generators. Supply transients should be shunted by the use of decoupling capacitors (0.1 μF typical) located across the supply rails as close to the device as possible.

The current path established if latch-up occurs is usually between the positive supply rail and ground and can be triggered by surges on the supply lines and/or voltages on either the output or inputs that exceed the supply voltage. Once latch-up occurs, the current flow is limited only by the impedance of the power supply and the forward resistance of the parasitic thyristor and usually results in the destruction of the device. The chance of latch-up occurring increases with increasing temperature and supply voltages.

TYPICAL APPLICATION DATA

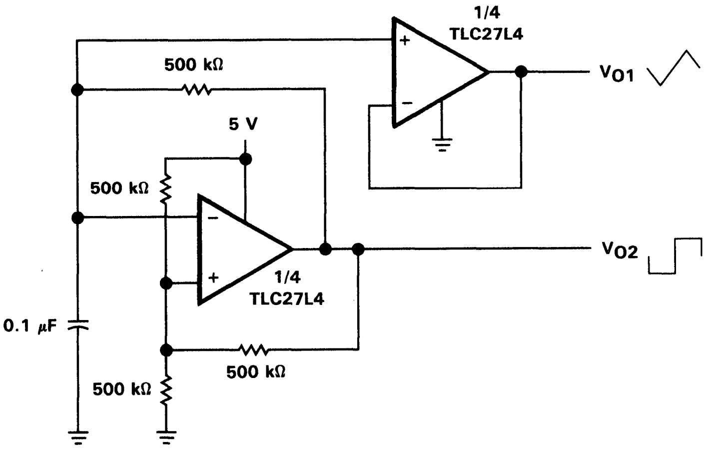
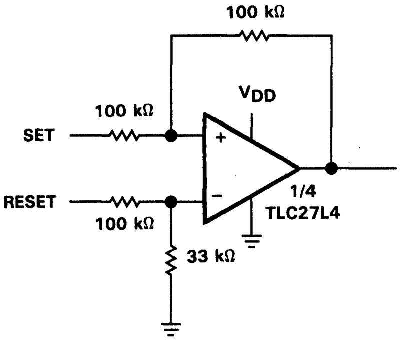


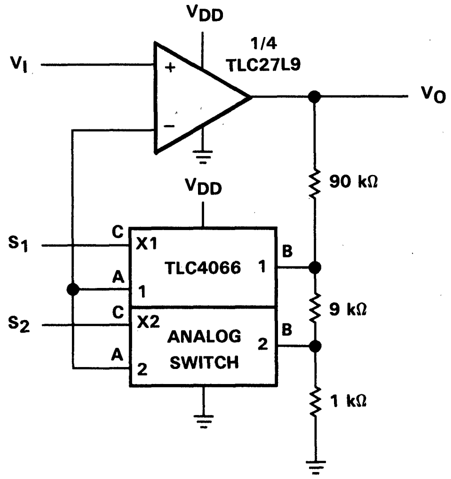
FIGURE 44. MULTIVIBRATOR



NOTE: V_{DD} = 5 V to 16 V

FIGURE 45. SET/RESET FLIP-FLOP

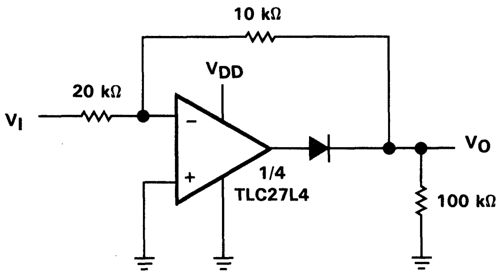
TYPICAL APPLICATION DATA



SELECT:	S_1	S_2
A_V	10	100

NOTE: V_{DD} = 5 V to 12 V

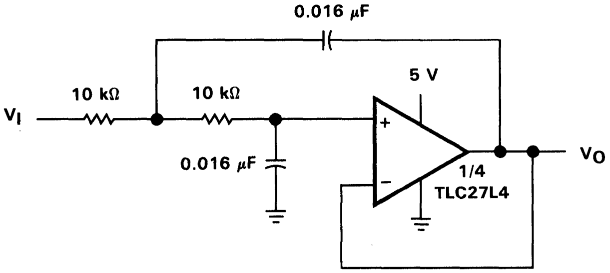
FIGURE 46. AMPLIFIER WITH DIGITAL GAIN SELECTION



NOTE: V_{DD} = 5 V to 16 V

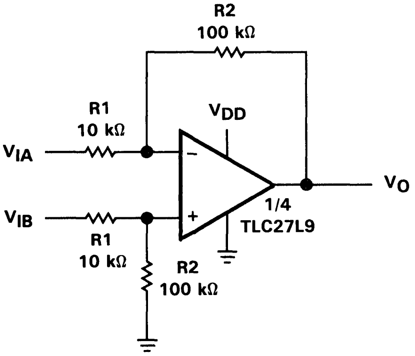
FIGURE 47. FULL-WAVE RECTIFIER

TYPICAL APPLICATION DATA



NOTE: Normalized to F_C = 1 kHz and R_L = 10 kΩ

FIGURE 48. TWO-POLE LOW-PASS BUTTERWORTH FILTER



NOTES: V_{DD} = 5 V to 16 V

$$V_O = \frac{R2}{R1}(V_{IB} - V_{IA})$$

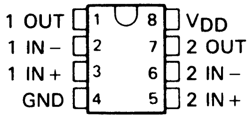
FIGURE 49. DIFFERENCE AMPLIFIER

TLC27M2, TLC27M2A, TLC27M2B, TLC27M7
LinCMOS™ PRECISION DUAL OPERATIONAL AMPLIFIERS

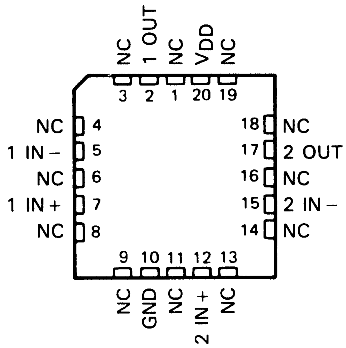
D3140, OCTOBER 1987—REVISED OCTOBER 1990

- **Trimmed Offset Voltage:**
  TLC27M7 . . . 500 μV Max at 25°C,
  V_{DD} = 5 V
- **Input Offset Voltage Drift . . . Typically 0.1 μV/Month, Including the First 30 Days**
- **Wide Range of Supply Voltages over Specified Temperature Range:**
  0°C to 70°C . . . 3 V to 16 V
  −40°C to 85°C . . . 4 V to 16 V
  −55°C to 125°C . . . 4 V to 16 V
- **Single-Supply Operation**
- **Common-Mode Input Voltage Range Extends Below the Negative Rail (C-Suffix, I-Suffix types)**
- **Low Noise . . . Typically 32 $\text{nV}/\sqrt{\text{Hz}}$ at f = 1 kHz**
- **Low Power . . . Typically 2.1 mW at 25°C, V_{DD} = 5 V**
- **Output Voltage Range Includes Negative Rail**
- **High Input Impedance . . . 10^{12} Ω Typical**
- **ESD-Protection Circuitry**
- **Small-Outline Package Option Also Available in Tape and Reel**
- **Designed-In Latch-Up Immunity**

D, JG, OR P PACKAGE
(TOP VIEW)



FK PACKAGE
(TOP VIEW)



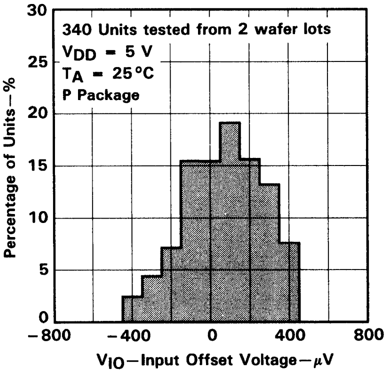
NC—No internal connection

AVAILABLE OPTIONS

T_A	V_{IO}max at 25°C	PACKAGE			
		SMALL OUTLINE (D)	CHIP CARRIER (FK)	CERAMIC DIP (JG)	PLASTIC DIP (P)
0°C to 70°C	500 μV	TLC27M7CD	—	—	TLC27M7CP
	2 mV	TLC27M2BCD	—	—	TLC27M2BCP
	5 mV	TLC27M2ACD	—	—	TLC27M2ACP
	10 mV	TLC27M2CD	—	—	TLC27M2CP
−40°C to 85°C	500 μV	TLC27M7ID	—	—	TLC27M7IP
	2 mV	TLC27M2BID	—	—	TLC27M2BIP
	5 mV	TLC27M2AID	—	—	TLC27M2AIP
	10 mV	TLC27M2ID	—	—	TLC27M2IP
−55°C to 125°C	500 μV	TLC27M7MD	TLC27M7MFK	TLC27M7MJG	TLC27M7MP
	10 mV	TLC27M2MD	TLC27M2MFK	TLC27M2MJG	TLC27M2MP

The D package is available in tape and reel. Add R suffix to the device type, (e.g., TLC27M7CDR).

DISTRIBUTION OF TLC27M7
INPUT OFFSET VOLTAGE



LinCMOS is a trademark of Texas Instruments Incorporated

description

The TLC27M2 and TLC27M7 dual operational amplifiers combine a wide range of input offset voltage grades with low offset voltage drift, high input impedance, low noise, and speeds comparable to that of general-purpose bipolar devices. These devices use Texas Instruments silicon-gate LinCMOS™ technology, which provides offset voltage stability far exceeding the stability available with conventional metal-gate processes.

The extremely high input impedance and low bias currents make these cost-effective devices ideal for applications that have previously been reserved for general-purpose bipolar products, but with only a fraction of the power consumption. Four offset voltage grades are available (C-suffix and I-suffix types), ranging from the low-cost TLC27M2 (10 mV) to the high-precision TLC27M7 (500 μV). These advantages, in combination with good common-mode rejection and supply voltage rejection, make these devices a good choice for new state-of-the-art designs as well as for upgrading existing designs.

In general, many features associated with bipolar technology are available on LinCMOS™ operational amplifiers, without the power penalties of bipolar technology. General applications such as transducer interfacing, analog calculations, amplifier blocks, active filters, and signal buffering are easily designed with the TLC27M2 and TLC27M7. The devices also exhibit low voltage single-supply operation and low power consumption, making them ideally suited for remote and inaccessible battery-powered applications. The common-mode input voltage range includes the negative rail.

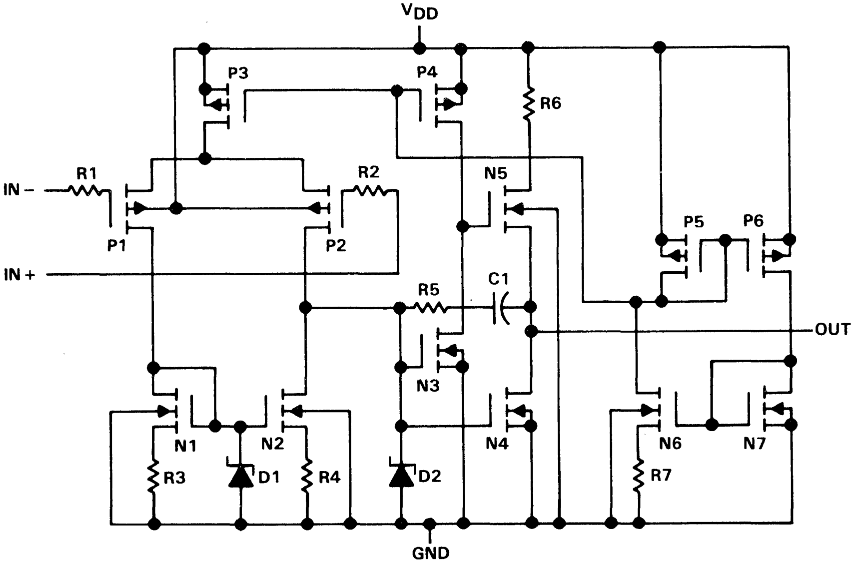
A wide range of packaging options is available, including small-outline and chip carrier versions for high-density system applications.

The device inputs and outputs are designed to withstand −100-mA surge currents without sustaining latch-up.

The TLC27M2 and TLC27M7 incorporate internal ESD-protection circuits that prevent functional failures at voltages up to 2000 V as tested under MIL-STD-883C, Method 3015.2; however, care should be exercised in handling these devices as exposure to ESD may result in the degradation of the device parametric performance.

C-suffix devices are characterized for operation from 0°C to 70°C. I-suffix devices are characterized for operation from −40°C to 85°C. M-suffix devices are characterized for operation over the full military temperature range of −55°C to 125°C.

equivalent schematic (each amplifier)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{DD} (see Note 1)	18 V
Differential input voltage (see Note 2)	$\pm V_{DD}$
Input voltage range, V_I (any input)	-0.3 V to V_{DD}
Input current, I_I	±5 mA
Output current, I_O (each output)	±30 mA
Total current into V_{DD} terminal	45 mA
Total current out of ground terminal	45 mA
Duration of short-circuit current at (or below) 25°C (see Note 3)	unlimited
Continuous total dissipation	See Dissipation Rating Table
Operating free-air temperature, T_A: C-suffix	0°C to 70°C
I-suffix	−40°C to 85°C
M-suffix	−55°C to 125°C
Storage temperature range	−65°C to 150°C
Case temperature for 60 seconds: FK package	260°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D and P package	260°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: JG package	300°C

NOTES: 1. All voltage values, except differential voltages, are with respect to network ground.
2. Differential voltages are at the noninverting input with respect to the inverting input.
3. The output may be shorted to either supply. Temperature and/or supply voltages must be limited to ensure that the maximum dissipation rating is not exceeded (see application section).

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING	$T_A = 125°C$ POWER RATING
D	725 mW	5.8 mW/°C	464 mW	377 mW	
FK	1375 mW	11 mW/°C	880 mW	715 mW	275 mW
JG	1050 mW	8.4 mW/°C	672 mW	546 mW	210 mW
P	1000 mW	8.0 mW/°C	640 mW	520 mW	

recommended operating conditions

		C-SUFFIX			I-SUFFIX			M-SUFFIX			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{DD}		3		16	4		16	4		16	V
Common-mode input voltage, V_{IC}	V_{DD} = 5 V	−0.2		3.5	−0.2		3.5	0		3.5	V
	V_{DD} = 10 V	−0.2		8.5	−0.2		8.5	0		8.5	
Operating free-air temperature, T_A		0		70	−40		85	−55		125	°C

electrical characteristics at specified free-air temperature, V_{DD} = 5 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS	T_A†	MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	TLC27M2C	V_O = 1.4 V, V_{IC} = 0, R_S = 50 Ω, R_L = 100 kΩ	25°C		1.1	10	mV
				Full range			12	
		TLC27M2AC	V_O = 1.4 V, V_{IC} = 0, R_S = 50 Ω, R_L = 100 kΩ	25°C		0.9	5	
				Full range			6.5	
		TLC27M2BC	V_O = 1.4 V, V_{IC} = 0, R_S = 50 Ω, R_L = 100 kΩ	25°C		220	2000	μV
				Full range			3000	
		TLC27M7C	V_O = 1.4 V, V_{IC} = 0, R_S = 50 Ω, R_L = 100 kΩ	25°C		185	500	
				Full range			1500	
α_{VIO}	Average temperature coefficient of input offset voltage			25°C to 70°C		1.7		μV/°C
I_{IO}	Input offset current (see Note 4)		V_O = 2.5 V, V_{IC} = 2.5 V	25°C		0.1		pA
				70°C		7	300	
I_{IB}	Input bias current (see Note 4)		V_O = 2.5 V, V_{IC} = 2.5 V	25°C		0.6		pA
				70°C		40	600	
V_{ICR}	Common-mode input voltage range (see Note 5)			25°C	−0.2 to 4	−0.3 to 4.2		V
				Full range	−0.2 to 3.5			V
V_{OH}	High-level output voltage		V_{ID} = 100 mV, R_L = 100 kΩ	25°C	3.2	3.9		V
				0°C	3	3.9		
				70°C	3	4		
V_{OL}	Low-level output voltage		V_{ID} = −100 mV, I_{OL} = 0	25°C		0	50	mV
				0°C		0	50	
				70°C		0	50	
A_{VD}	Large-signal differential voltage amplification		V_O = 0.25 V to 2 V, R_L = 100 kΩ	25°C	25	170		V/mV
				0°C	15	200		
				70°C	15	140		
CMRR	Common-mode rejection ratio		V_{IC} = V_{ICR} min	25°C	65	91		dB
				0°C	60	91		
				70°C	60	92		
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)		V_{DD} = 5 V to 10 V, V_O = 1.4 V	25°C	70	93		dB
				0°C	60	92		
				70°C	60	94		
I_{DD}	Supply current (two amplifiers)		V_O = 2.5 V, V_{IC} = 2.5 V, No load	25°C		210	560	μA
				0°C		250	640	
				70°C		170	440	

† Full range is 0°C to 70°C.

NOTES: 4. The typical values of input bias current and input offset current below 5 pA were determined mathematically.

5. This range also applies to each input individually.

electrical characteristics at specified free-air temperature, V_{DD} = 10 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS	T_A†	MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	TLC27M2C	V_O = 1.4 V, V_{IC} = 0, R_S = 50 Ω, R_L = 100 kΩ	25°C		1.1	10	mV
				Full range			12	
		TLC27M2AC	V_O = 1.4 V, V_{IC} = 0, R_S = 50 Ω, R_L = 100 kΩ	25°C		0.9	5	
				Full range			6.5	
		TLC27M2BC	V_O = 1.4 V, V_{IC} = 0, R_S = 50 Ω, R_L = 100 kΩ	25°C		224	2000	µV
				Full range			3000	
		TLC27M7C	V_O = 1.4 V, V_{IC} = 0, R_S = 50 Ω, R_L = 100 kΩ	25°C		190	800	
				Full range			1900	
α_{VIO}	Average temperature coefficient of input offset voltage			25°C to 70°C		2.1		µV/°C
I_{IO}	Input offset current (see Note 4)		V_O = 5 V, V_{IC} = 5 V	25°C		0.1		pA
				70°C		7	300	
I_{IB}	Input bias current (see Note 4)		V_O = 5 V, V_{IC} = 5 V	25°C		0.7		pA
				70°C		50	600	
V_{ICR}	Common-mode input voltage range (see Note 5)			25°C	−0.2 to 9	−0.3 to 9.2		V
				Full range	−0.2 to 8.5			V
V_{OH}	High-level output voltage		V_{ID} = 100 mV, R_L = 100 kΩ	25°C	8	8.7		V
				0°C	7.8	8.7		
				70°C	7.8	8.7		
V_{OL}	Low-level output voltage		V_{ID} = −100 mV, I_{OL} = 0	25°C		0	50	mV
				0°C		0	50	
				70°C		0	50	
A_{VD}	Large-signal differential voltage amplification		V_O = 1 V to 6 V, R_L = 100 kΩ	25°C	25	275		V/mV
				0°C	15	320		
				70°C	15	230		
CMRR	Common-mode rejection ratio		V_{IC} = V_{ICR} min	25°C	65	94		dB
				0°C	60	94		
				70°C	60	94		
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)		V_{DD} = 5 V to 10 V, V_O = 1.4 V	25°C	70	93		dB
				0°C	60	92		
				70°C	60	94		
I_{DD}	Supply current (two amplifiers)		V_O = 5 V, V_{IC} = 5 V, No load	25°C		285	600	µA
				0°C		345	800	
				70°C		220	560	

† Full range is 0°C to 70°C.

NOTES: 4. The typical values of input bias current and input offset current below 5 pA were determined mathematically.
5. This range also applies to each input individually.

electrical characteristics at specified free-air temperature, V_{DD} = 5 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS	T_A†	MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	TLC27M2I	V_O = 1.4 V, V_{IC} = 0, R_S = 50 Ω, R_L = 100 kΩ	25°C		1.1	10	mV
				Full range			13	
		TLC27M2AI	V_O = 1.4 V, V_{IC} = 0, R_S = 50 Ω, R_L = 100 kΩ	25°C		0.9	5	
				Full range			7	
		TLC27M2BI	V_O = 1.4 V, V_{IC} = 0, R_S = 50 Ω, R_L = 100 kΩ	25°C		220	2000	µV
				Full range			3500	
		TLC27M7I	V_O = 1.4 V, V_{IC} = 0, R_S = 50 Ω, R_L = 100 kΩ	25°C		185	500	
				Full range			2000	
α_{VIO}	Average temperature coefficient of input offset voltage			25°C to 85°C		1.7		µV/°C
I_{IO}	Input offset current (see Note 4)		V_O = 2.5 V, V_{IC} = 2.5 V	25°C		0.1		pA
				85°C		24	1000	
I_{IB}	Input bias current (see Note 4)		V_O = 2.5 V, V_{IC} = 2.5 V	25°C		0.6		pA
				85°C		200	2000	
V_{ICR}	Common-mode input voltage range (see Note 5)			25°C	−0.2 to 4	−0.3 to 4.2		V
				Full range	−0.2 to 3.5			V
V_{OH}	High-level output voltage		V_{ID} = 100 mV, R_L = 100 kΩ	25°C	3.2	3.9		V
				−40°C	3	3.9		
				85°C	3	4		
V_{OL}	Low-level output voltage		V_{ID} = −100 mV, I_{OL} = 0	25°C		0	50	mV
				−40°C		0	50	
				85°C		0	50	
A_{VD}	Large-signal differential voltage amplification		V_O = 0.25 V to 2 V, R_L = 100 kΩ	25°C	25	170		V/mV
				−40°C	15	270		
				85°C	15	130		
CMRR	Common-mode rejection ratio		V_{IC} = V_{ICR} min	25°C	65	91		dB
				−40°C	60	90		
				85°C	60	90		
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)		V_{DD} = 5 V to 10 V, V_O = 1.4 V	25°C	70	93		dB
				−40°C	60	91		
				85°C	60	94		
I_{DD}	Supply current (two amplifiers)		V_O = 2.5 V, V_{IC} = 2.5 V, No load	25°C		210	560	µA
				−40°C		315	800	
				85°C		160	400	

† Full range is −40°C to 85°C.

NOTES: 4. The typical values of input bias current and input offset current below 5 pA were determined mathematically.
5. This range also applies to each input individually.

electrical characteristics at specified free-air temperature, V_{DD} = 10 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS		T_A†	MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	TLC27M2I	V_O = 1.4 V, R_S = 50 Ω,	V_{IC} = 0, R_L = 100 kΩ	25°C		1.1	10	mV
					Full range			13	
		TLC27M2AI	V_O = 1.4 V, R_S = 50 Ω,	V_{IC} = 0, R_L = 100 kΩ	25°C		0.9	5	
					Full range			7	
		TLC27M2BI	V_O = 1.4 V, R_S = 50 Ω,	V_{IC} = 0, R_L = 100 kΩ	25°C		224	2000	μV
					Full range			3500	
		TLC27M7I	V_O = 1.4 V, R_S = 50 Ω,	V_{IC} = 0, R_L = 100 kΩ	25°C		190	800	
					Full range			2900	
α_{VIO}	Average temperature coefficient of input offset voltage				25°C to 85°C		2.1		μV/°C
I_{IO}	Input offset current (see Note 4)		V_O = 5 V,	V_{IC} = 5 V	25°C		0.1		pA
					85°C		26	1000	
I_{IB}	Input bias current (see Note 4)		V_O = 5 V,	V_{IC} = 5 V	25°C		0.7		pA
					85°C		220	2000	
V_{ICR}	Common-mode input voltage range (see Note 5)				25°C	−0.2 to 9	−0.3 to 9.2		V
					Full range	−0.2 to 8.5			V
V_{OH}	High-level output voltage		V_{ID} = 100 mV,	R_L = 100 kΩ	25°C	8	8.7		V
					−40°C	7.8	8.7		
					85°C	7.8	8.7		
V_{OL}	Low-level output voltage		V_{ID} = −100 mV,	I_{OL} = 0	25°C		0	50	mV
					−40°C		0	50	
					85°C		0	50	
A_{VD}	Large-signal differential voltage amplification		V_O = 1 V to 6 V,	R_L = 100 kΩ	25°C	25	275		V/mV
					−40°C	15	390		
					85°C	15	220		
CMRR	Common-mode rejection ratio		V_{IC} = V_{ICR} min		25°C	65	94		dB
					−40°C	60	93		
					85°C	60	94		
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)		V_{DD} = 5 V to 10 V,	V_O = 1.4 V	25°C	70	93		dB
					−40°C	60	91		
					85°C	60	94		
I_{DD}	Supply current (two amplifiers)		V_O = 5 V, No load	V_{IC} = 5 V,	25°C		285	600	μA
					−40°C		450	900	
					85°C		205	520	

† Full range is −40°C to 85°C.

NOTES: 4. The typical values of input bias current and input offset current below 5 pA were determined mathematically.
5. This range also applies to each input individually.

electrical characteristics at specified free-air temperature, V_{DD} = 5 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS	T_A†	MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	TLC27M2M	V_O = 1.4 V, V_{IC} = 0, R_S = 50 Ω, R_L = 100 kΩ	25°C		1.1	10	mV
				Full range			12	
		TLC27M7M	V_O = 1.4 V, V_{IC} = 0, R_S = 50 Ω, R_L = 100 kΩ	25°C		185	500	μV
				Full range			3750	
α_{VIO}	Average temperature coefficient of input offset voltage			25°C to 125°C		1.7		μV/°C
I_{IO}	Input offset current (see Note 4)		V_O = 2.5 V, V_{IC} = 2.5 V	25°C		0.1		pA
				125°C		1.4	15	nA
I_{IB}	Input bias current (see Note 4)		V_O = 2.5 V, V_{IC} = 2.5 V	25°C		0.6		pA
				125°C		9	35	nA
V_{ICR}	Common-mode input voltage range (see Note 5)			25°C	0 to 4	−0.3 to 4.2		V
				Full range	0 to 3.5			V
V_{OH}	High-level output voltage		V_{ID} = 100 mV, R_L = 100 kΩ	25°C	3.2	3.9		V
				−55°C	3	3.9		
				125°C	3	4		
V_{OL}	Low-level output voltage		V_{ID} = −100 mV, I_{OL} = 0	25°C		0	50	mV
				−55°C		0	50	
				125°C		0	50	
A_{VD}	Large-signal differential voltage amplification		V_O = 0.25 V to 2 V, R_L = 100 kΩ	25°C	25	170		V/mV
				−55°C	15	290		
				125°C	15	120		
CMRR	Common-mode rejection ratio		V_{IC} = V_{ICR} min	25°C	65	91		dB
				−55°C	60	89		
				125°C	60	91		
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)		V_{DD} = 5 V to 10 V, V_O = 1.4 V	25°C	70	93		dB
				−55°C	60	91		
				125°C	60	94		
I_{DD}	Supply current (two amplifiers)		V_O = 2.5 V, V_{IC} = 2.5 V, No load	25°C		210	560	μA
				−55°C		340	880	
				125°C		140	360	

† Full range is −55°C to 125°C.

NOTES: 4. The typical values of input bias current and input offset current below 5 pA were determined mathematically.

5. This range also applies to each input individually.

electrical characteristics at specified free-air temperature, V_{DD} = 10 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS		T_A†	MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	TLC27M2M	V_O = 1.4 V, R_S = 50 Ω,	V_{IC} = 0, R_L = 100 kΩ	25°C		1.1	10	mV
					Full range			12	
		TLC27M7M	V_O = 1.4 V, R_S = 50 Ω,	V_{IC} = 0, R_L = 100 kΩ	25°C		190	800	µV
					Full range			4300	
α_{VIO}	Average temperature coefficient of input offset voltage				25°C to 125°C		2.1		µV/°C
I_{IO}	Input offset current (see Note 4)		V_O = 5 V,	V_{IC} = 5 V	25°C		0.1		pA
					125°C		1.8	15	nA
I_{IB}	Input bias current (see Note 4)		V_O = 5 V,	V_{IC} = 5 V	25°C		0.7		pA
					125°C		10	35	nA
V_{ICR}	Common-mode input voltage range (see Note 5)				25°C	0 to 9	−0.3 to 9.2		V
					Full range	0 to 8.5			V
V_{OH}	High-level output voltage		V_{ID} = 100 mV,	R_L = 100 kΩ	25°C	8	8.7		V
					−55°C	7.8	8.6		
					125°C	7.8	8.8		
V_{OL}	Low-level output voltage		V_{ID} = −100 mV,	I_{OL} = 0	25°C		0	50	mV
					−55°C		0	50	
					125°C		0	50	
A_{VD}	Large-signal differential voltage amplification		V_O = 1 V to 6 V,	R_L = 100 kΩ	25°C	25	275		V/mV
					−55°C	15	420		
					125°C	15	190		
CMRR	Common-mode rejection ratio		V_{IC} = V_{ICR} min		25°C	65	94		dB
					−55°C	60	93		
					125°C	60	93		
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)		V_{DD} = 5 V to 10 V,	V_O = 1.4 V	25°C	70	93		dB
					−55°C	60	91		
					125°C	60	94		
I_{DD}	Supply current (two amplifiers)		V_O = 5 V, No load	V_{IC} = 5 V,	25°C		285	600	µA
					−55°C		490	1000	
					125°C		180	480	

† Full range is −55°C to 125°C.

NOTES: 4. The typical values of input bias current and input offset current below 5 pA were determined mathematically.
5. This range also applies to each input individually.

operating characteristics, V_{DD} = 5 V

PARAMETER		TEST CONDITIONS		T_A	MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain	R_L = 100 kΩ, C_L = 20 pF, See Figure 1	V_{IPP} = 1 V	25°C		0.43		V/μs
				0°C		0.46		
				70°C		0.36		
			V_{IPP} = 2.5 V	25°C		0.40		
				0°C		0.43		
				70°C		0.34		
V_n	Equivalent input noise voltage	f = 1 kHz, See Figure 2	R_S = 100 Ω,	25°C		32		nV/√Hz
B_{OM}	Maximum output swing bandwidth	V_O = V_{OH}, R_L = 100 kΩ,	C_L = 20 pF, See Figure 1	25°C		55		kHz
				0°C		60		
				70°C		50		
B_1	Unity-gain bandwidth	V_i = 10 mV, See Figure 3	C_L = 20 pF,	25°C		525		kHz
				0°C		600		
				70°C		400		
ϕ_m	Phase margin	V_i = 10 mV, C_L = 20 pF,	f = B_1, See Figure 3	25°C		40°		
				0°C		41°		
				70°C		39°		

operating characteristics, V_{DD} = 10 V

PARAMETER		TEST CONDITIONS		T_A	MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain	R_L = 100 kΩ, C_L = 20 pF, See Figure 1	V_{IPP} = 1 V	25°C		0.62		V/μs
				0°C		0.67		
				70°C		0.51		
			V_{IPP} = 5.5 V	25°C		0.56		
				0°C		0.61		
				70°C		0.46		
V_n	Equivalent input noise voltage	f = 1 kHz, See Figure 2	R_S = 100 Ω,	25°C		32		nV/√Hz
B_{OM}	Maximum output swing bandwidth	V_O = V_{OH}, R_L = 100 kΩ,	C_L = 20 pF, See Figure 1	25°C		35		kHz
				0°C		40		
				70°C		30		
B_1	Unity-gain bandwidth	V_i = 10 mV, See Figure 3	C_L = 20 pF,	25°C		635		kHz
				0°C		710		
				70°C		510		
ϕ_m	Phase margin	V_i = 10 mV, C_L = 20 pF,	f = B_1, See Figure 3	25°C		43°		
				0°C		44°		
				70°C		42°		

operating characteristics, V_{DD} = 5 V

PARAMETER		TEST CONDITIONS		T_A	MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain	R_L = 100 kΩ, C_L = 20 pF, See Figure 1	V_{IPP} = 1 V	25°C		0.43		V/µs
				−40°C		0.51		
				85°C		0.35		
			V_{IPP} = 2.5 V	25°C		0.40		
				−40°C		0.48		
				85°C		0.32		
V_n	Equivalent input noise voltage	f = 1 kHz, See Figure 2	R_S = 100 Ω,	25°C		32		nV/√Hz
B_{OM}	Maximum output swing bandwidth	V_O = V_{OH}, R_L = 100 kΩ,	C_L = 20 pF, See Figure 1	25°C		55		kHz
				−40°C		75		
				85°C		45		
B_1	Unity-gain bandwidth	V_i = 10 mV, See Figure 3	C_L = 20 pF,	25°C		525		kHz
				−40°C		770		
				85°C		370		
ϕ_m	Phase margin	V_i = 10 mV, C_L = 20 pF,	f = B_1, See Figure 3	25°C		40°		
				−40°C		43°		
				85°C		38°		

operating characteristics, V_{DD} = 10 V

PARAMETER		TEST CONDITIONS		T_A	MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain	R_L = 100 kΩ, C_L = 20 pF, See Figure 1	V_{IPP} = 1 V	25°C		0.62		V/µs
				−40°C		0.77		
				85°C		0.47		
			V_{IPP} = 5.5 V	25°C		0.56		
				−40°C		0.70		
				85°C		0.44		
V_n	Equivalent input noise voltage	f = 1 kHz, See Figure 2	R_S = 100 Ω,	25°C		32		nV/√Hz
B_{OM}	Maximum output swing bandwidth	V_O = V_{OH}, R_L = 100 kΩ,	C_L = 20 pF, See Figure 1	25°C		35		kHz
				−40°C		45		
				85°C		25		
B_1	Unity-gain bandwidth	V_i = 10 mV, See Figure 3	C_L = 20 pF,	25°C		635		kHz
				−40°C		880		
				85°C		480		
ϕ_m	Phase margin	V_i = 10 mV, C_L = 20 pF,	f = B_1, See Figure 3	25°C		43°		
				−40°C		46°		
				85°C		41°		

operating characteristics, V_{DD} = 5 V

PARAMETER		TEST CONDITIONS		T_A	MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain	R_L = 100 kΩ, C_L = 20 pF, See Figure 1	V_{IPP} = 1 V	25°C		0.43		V/μs
				−55°C		0.54		
				125°C		0.29		
			V_{IPP} = 2.5 V	25°C		0.40		
				−55°C		0.49		
				125°C		0.28		
V_n	Equivalent input noise voltage	f = 1 kHz, See Figure 2	R_S = 100 Ω,	25°C		32		nV/$\sqrt{Hz}$
B_{OM}	Maximum output swing bandwidth	V_O = V_{OH}, R_L = 100 kΩ,	C_L = 20 pF, See Figure 1	25°C		55		kHz
				−55°C		80		
				125°C		40		
B_1	Unity-gain bandwidth	V_i = 10 mV, See Figure 3	C_L = 20 pF,	25°C		525		kHz
				−55°C		850		
				125°C		330		
ϕ_m	Phase margin	V_i = 10 mV, C_L = 20 pF,	f = B_1, See Figure 3	25°C		40°		
				−55°C		44°		
				125°C		36°		

operating characteristics, V_{DD} = 10 V

PARAMETER		TEST CONDITIONS		T_A	MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain	R_L = 100 kΩ, C_L = 20 pF, See Figure 1	V_{IPP} = 1 V	25°C		0.62		V/μs
				−55°C		0.81		
				125°C		0.38		
			V_{IPP} = 5.5 V	25°C		0.56		
				−55°C		0.73		
				125°C		0.35		
V_n	Equivalent input noise voltage	f = 1 kHz, See Figure 2	R_S = 100 Ω,	25°C		32		nV/$\sqrt{Hz}$
B_{OM}	Maximum output swing bandwidth	V_O = V_{OH}, R_L = 100 kΩ,	C_L = 20 pF, See Figure 1	25°C		35		kHz
				−55°C		50		
				125°C		20		
B_1	Unity-gain bandwidth	V_i = 10 mV, See Figure 3	C_L = 20 pF,	25°C		635		kHz
				−55°C		960		
				125°C		440		
ϕ_m	Phase margin	V_i = 10 mV, C_L = 20 pF,	f = B_1, See Figure 3	25°C		43°		
				−55°C		47°		
				125°C		39°		

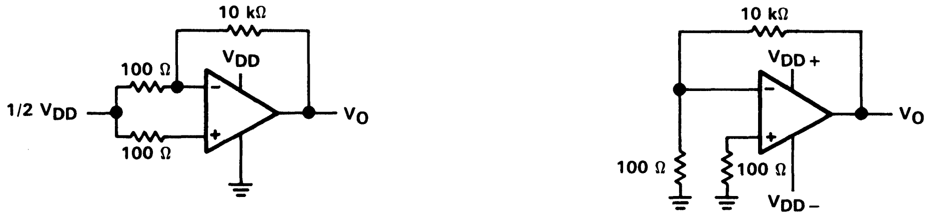
PARAMETER MEASUREMENT INFORMATION

single-supply versus split-supply test circuits

Because the TLC27M2 and TLC27M7 are optimized for single-supply operation, circuit configurations used for the various tests often present some inconvenience since the input signal, in many cases, must be offset from ground. This inconvenience can be avoided by testing the device with split supplies and the output load tied to the negative rail. A comparison of single-supply versus split-supply test circuits is shown below. The use of either circuit will give the same result.

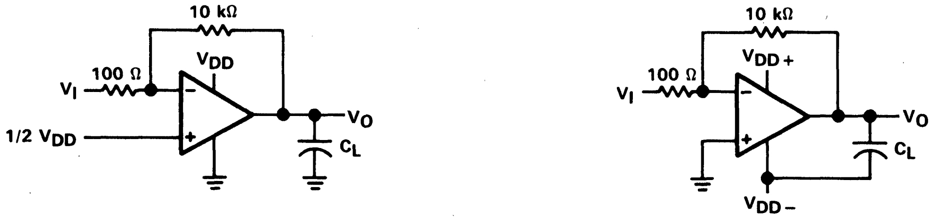
(a) Single-Supply (b) Split-Supply

FIGURE 1. UNITY-GAIN AMPLIFIER



(a) Single-Supply (b) Split-Supply

FIGURE 2. NOISE TEST CIRCUIT



(a) Single-Supply (b) Split-Supply

FIGURE 3. GAIN-OF-100 INVERTING AMPLIFIER

PARAMETER MEASUREMENT INFORMATION

input bias current

Because of the high input impedance of the TLC27M2 and TLC27M7 op amps, attempts to measure the input bias current can result in erroneous readings. The bias current at normal room ambient temperature is typically less than 1 pA, a value that is easily exceeded by leakages on the test socket. Two suggestions are offered to avoid erroneous measurements:

1. Isolate the device from other potential leakage sources. Use a grounded shield around and between the device inputs (see Figure 4). Leakages that would otherwise flow to the inputs will be shunted away.
2. Compensate for the leakage of the test socket by actually performing an input bias current test (using a picoammeter) with no device in the test socket. The actual input bias current can then be calculated by subtracting the "open-socket" leakage readings from the readings obtained with a device in the test socket.

One word of caution . . . many automatic testers as well as some bench-top op amp testers use the servo-loop technique with a resistor in series with the device input to measure the input bias current (the voltage drop across the series resistor is measured and the bias current is calculated). This method requires that a device be inserted into the test socket to obtain a correct reading; therefore, an "open-socket" reading is not feasible using this method.

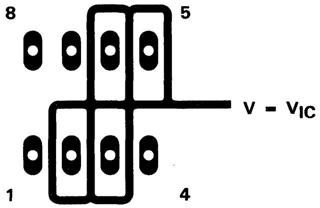


FIGURE 4. ISOLATION METAL AROUND DEVICE INPUTS
(JG AND P DUAL-IN-LINE-PACKAGE)

low-level output voltage

To obtain low-supply-voltage operation, some compromise was necessary in the input stage. This compromise results in the device low-level output being dependent on both the common-mode input voltage level as well as the differential input voltage level. When attempting to correlate low-level output readings with those quoted in the electrical specifications, these two conditions should be observed. If conditions other than these are to be used, please refer to Figures 14 through 19 in the Typical Characteristics of this data sheet.

PARAMETER MEASUREMENT INFORMATION

input offset voltage temperature coefficient

Erroneous readings often result from attempts to measure temperature coefficient of input offset voltage. This parameter is actually a calculation using input offset voltage measurements obtained at two different temperatures. When one (or both) of the temperatures is below freezing, moisture can collect on both the device and the test socket. This moisture will result in leakage and contact resistance, which can cause erroneous input offset voltage readings. The isolation techniques previously mentioned have no effect on the leakage since the moisture also covers the isolation metal itself, thereby rendering it useless. It is suggested that these measurements be performed at temperatures above freezing to minimize error.

full-power response

Full-power response, the frequency above which the op amp slew rate limits the output voltage swing, is often specified two ways . . . full-linear response and full-peak response. The full-linear response is generally measured by monitoring the distortion level of the output while increasing the frequency of a sinusoidal input signal until the maximum frequency is found above which the output contains significant distortion. The full-peak response is defined as the maximum output frequency, without regard to distortion, above which full peak-to-peak output swing cannot be maintained.

Because there is no industry-wide accepted value for "significant" distortion, the full-peak response is specified in this data sheet and is measured using the circuit of Figure 1. The initial setup involves the use of a sinusoidal input to determine the maximum peak-to-peak output of the device (the amplitude of the sinusoidal wave is increased until clipping occurs). The sinusoidal wave is then replaced with a square wave of the same amplitude. The frequency is then increased until the maximum peak-to-peak output can no longer be maintained (Figure 5). A square wave is used to allow a more accurate determination of the point at which the maximum peak-to-peak output is reached.

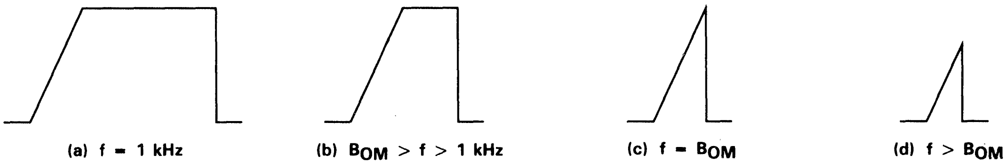

(a) $f = 1$ kHz (b) $B_{OM} > f > 1$ kHz (c) $f = B_{OM}$ (d) $f > B_{OM}$

FIGURE 5. FULL-POWER-RESPONSE OUTPUT SIGNAL

test time

Inadequate test time is a frequent problem, especially when testing CMOS devices in a high-volume, short-test-time environment. Internal capacitances are inherently higher in CMOS than in bipolar and BiFET devices and require longer test times than their bipolar and BiFET counterparts. The problem becomes more pronounced with reduced supply levels and lower temperatures.

TYPICAL CHARACTERISTICS

DISTRIBUTION OF TLC27M2
INPUT OFFSET VOLTAGE

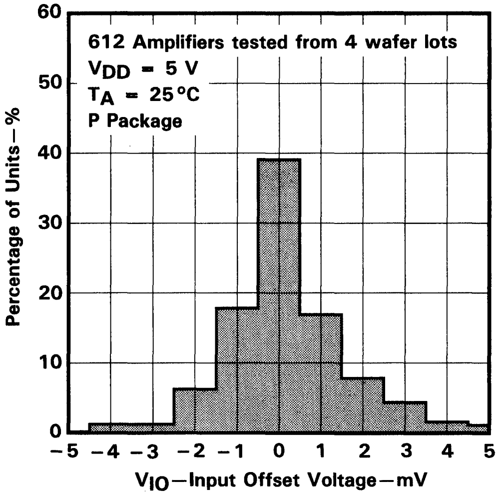


FIGURE 6

DISTRIBUTION OF TLC27M2
INPUT OFFSET VOLTAGE

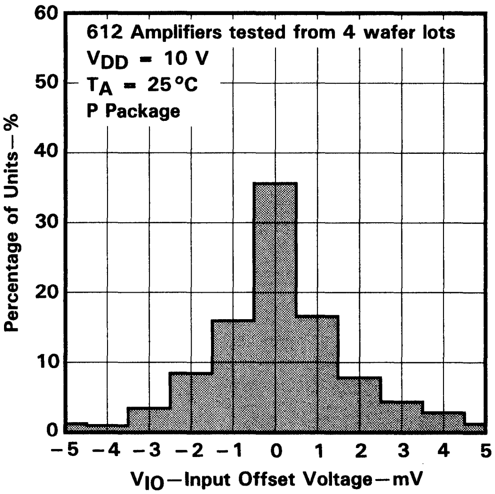


FIGURE 7

DISTRIBUTION OF TLC27M2 AND TLC27M7
INPUT OFFSET VOLTAGE
TEMPERATURE COEFFICIENT

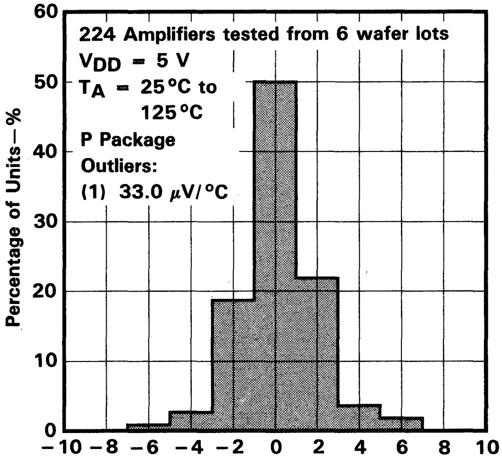


FIGURE 8

DISTRIBUTION OF TLC27M2 AND TLC27M7
INPUT OFFSET VOLTAGE
TEMPERATURE COEFFICIENT

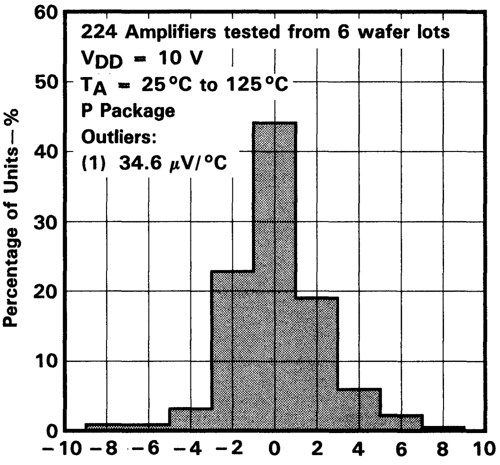


FIGURE 9

TYPICAL CHARACTERISTICS†

HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

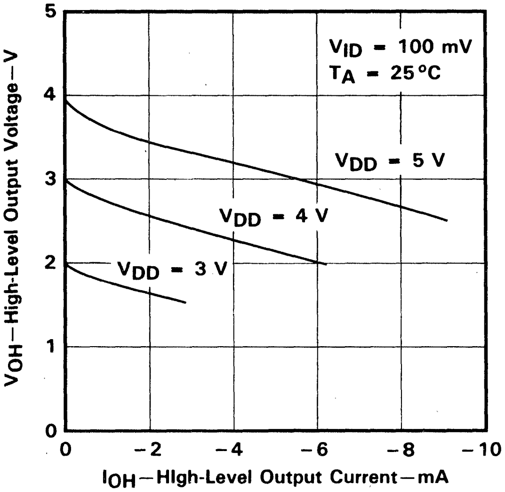


FIGURE 10

HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

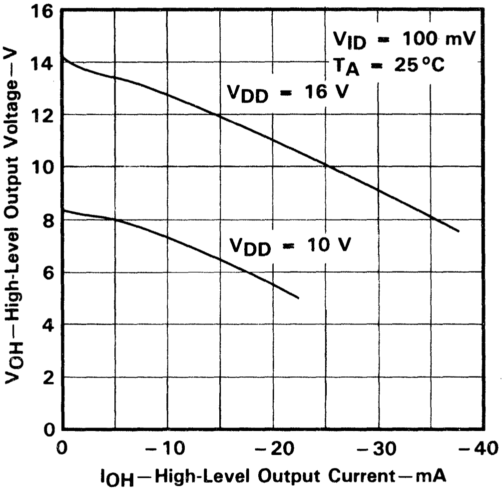


FIGURE 11

HIGH-LEVEL OUTPUT VOLTAGE
vs
SUPPLY VOLTAGE

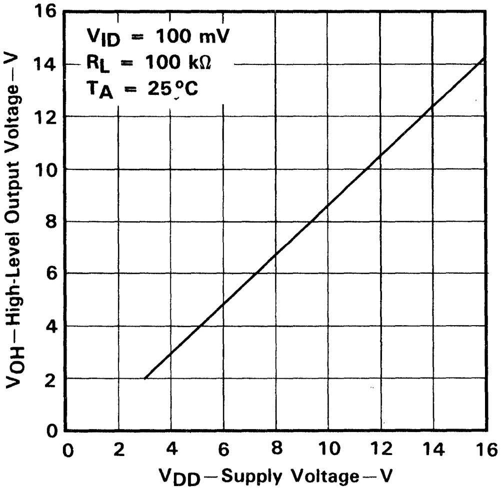


FIGURE 12

HIGH-LEVEL OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

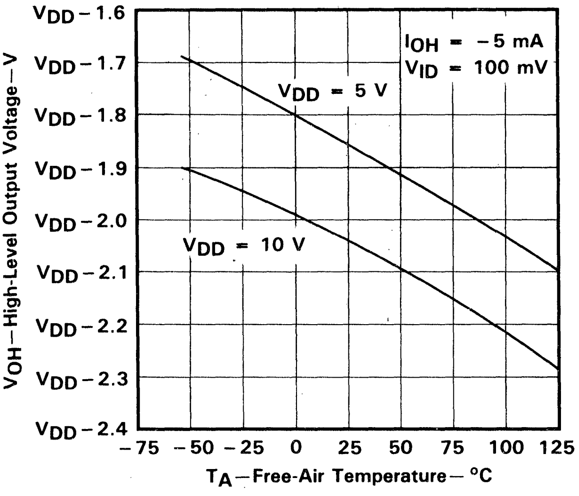


FIGURE 13

---

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

LOW-LEVEL OUTPUT VOLTAGE
vs
COMMON-MODE INPUT VOLTAGE

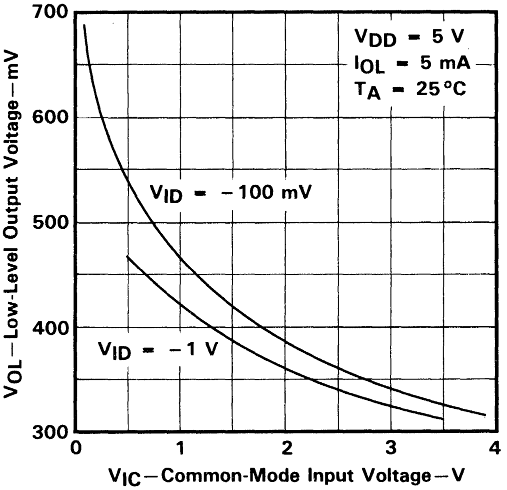


FIGURE 14

LOW-LEVEL OUTPUT VOLTAGE
vs
COMMON-MODE INPUT VOLTAGE

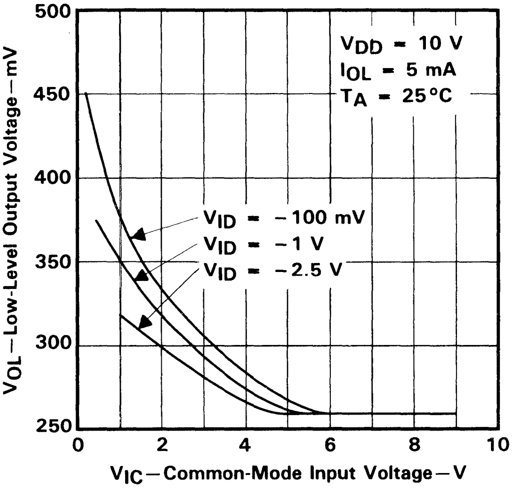


FIGURE 15

LOW-LEVEL OUTPUT VOLTAGE
vs
DIFFERENTIAL INPUT VOLTAGE

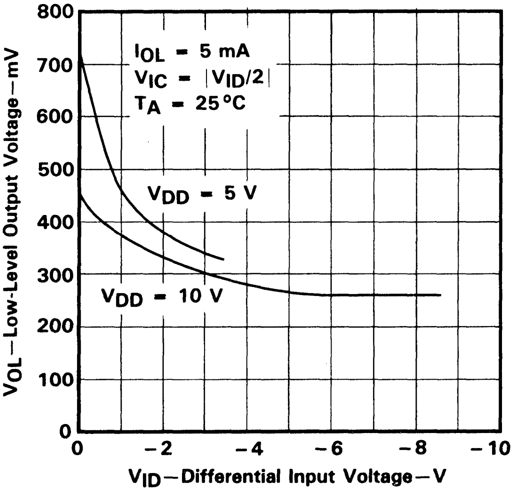


FIGURE 16

LOW-LEVEL OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

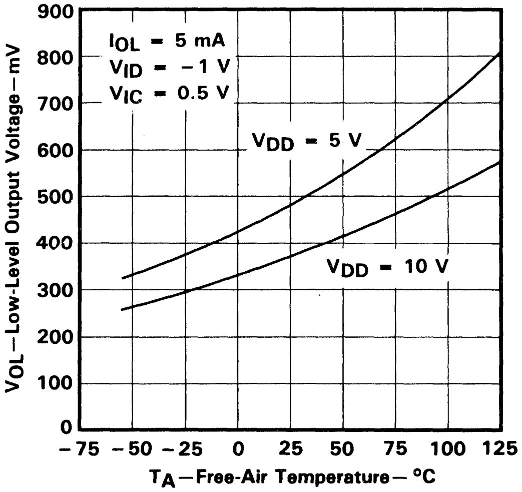


FIGURE 17

---

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

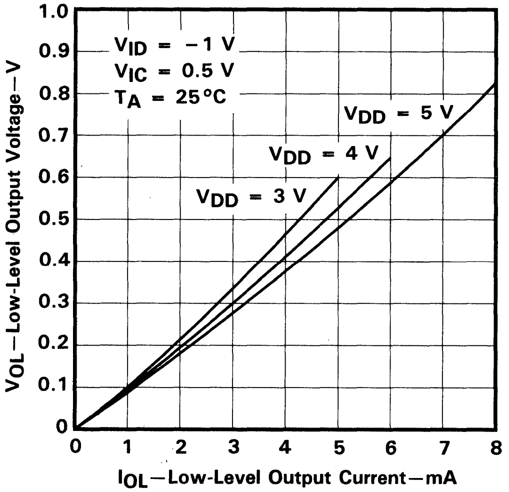


FIGURE 18

LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

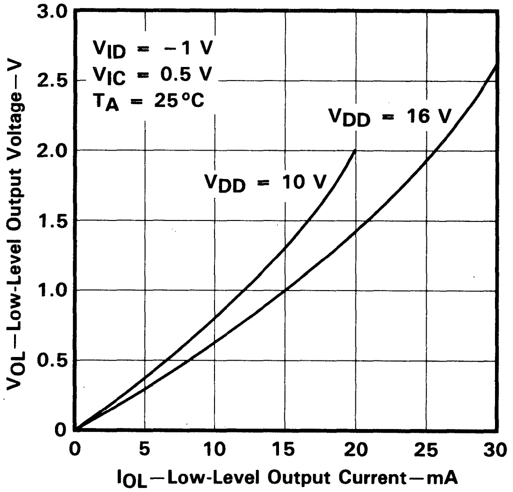


FIGURE 19

LARGE-SIGNAL
DIFFERENTIAL VOLTAGE AMPLIFICATION
vs
SUPPLY VOLTAGE

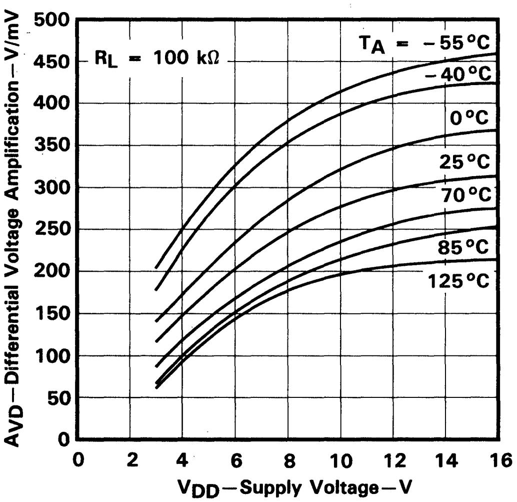


FIGURE 20

LARGE-SIGNAL
DIFFERENTIAL VOLTAGE AMPLIFICATION
vs
FREE-AIR TEMPERATURE

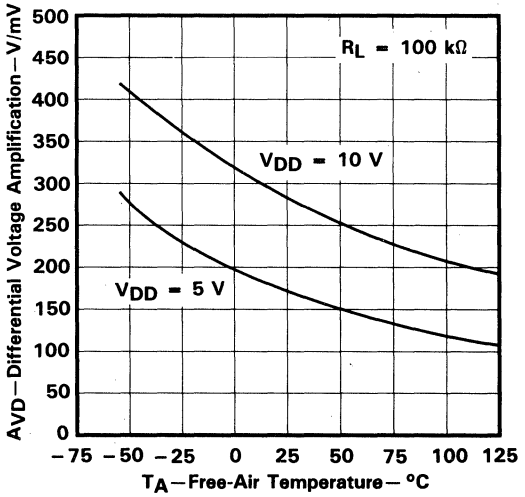


FIGURE 21

---

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS[†]

INPUT BIAS CURRENT AND INPUT OFFSET CURRENT
vs
FREE-AIR TEMPERATURE

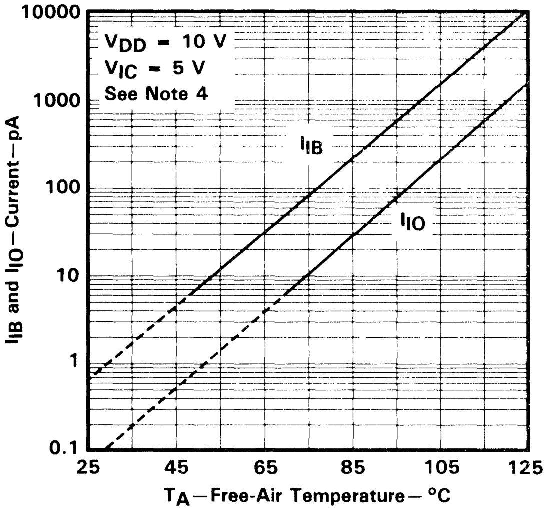


FIGURE 22

COMMON-MODE
INPUT VOLTAGE POSITIVE LIMIT
vs
SUPPLY VOLTAGE

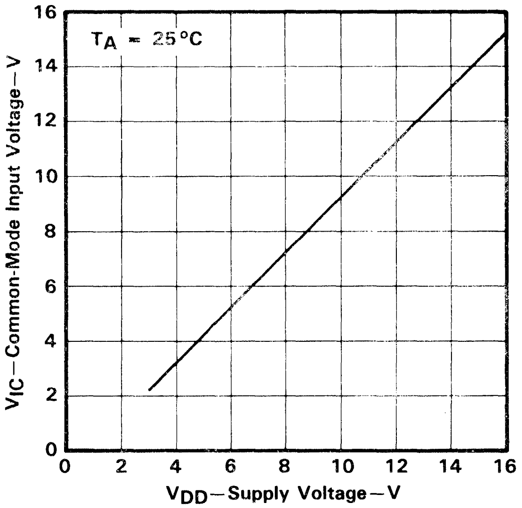


FIGURE 23

SUPPLY CURRENT
vs
SUPPLY VOLTAGE

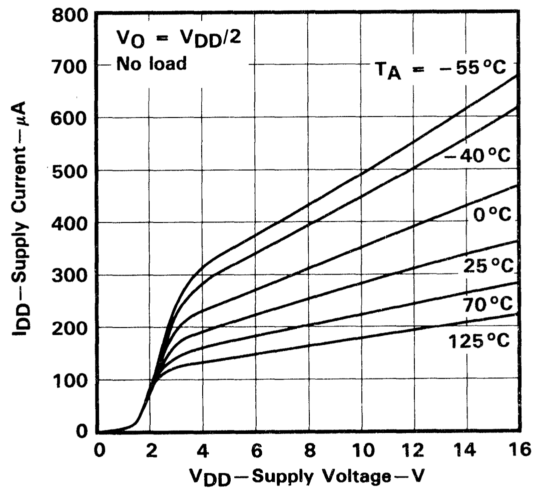


FIGURE 24

SUPPLY CURRENT
vs
FREE-AIR TEMPERATURE

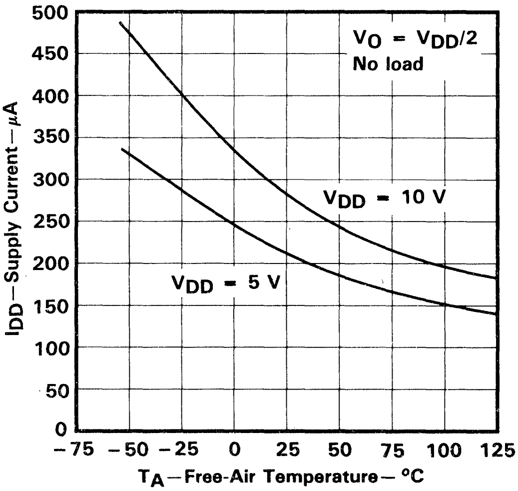


FIGURE 25

[†] Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.
NOTE 4: The typical values of input bias current and input offset current below 5 pA were determined mathematically.

TYPICAL CHARACTERISTICS†

SLEW RATE
vs
SUPPLY VOLTAGE

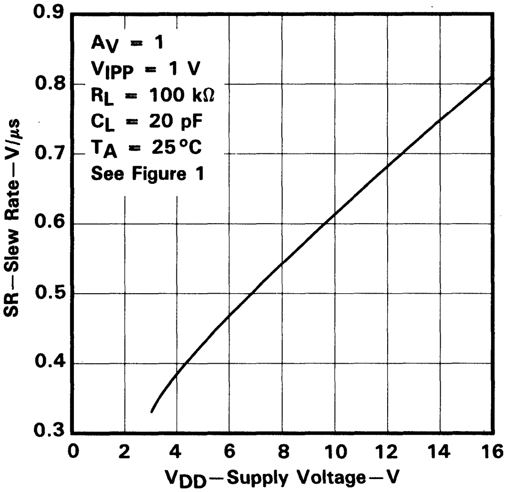


FIGURE 26

SLEW RATE
vs
FREE-AIR TEMPERATURE

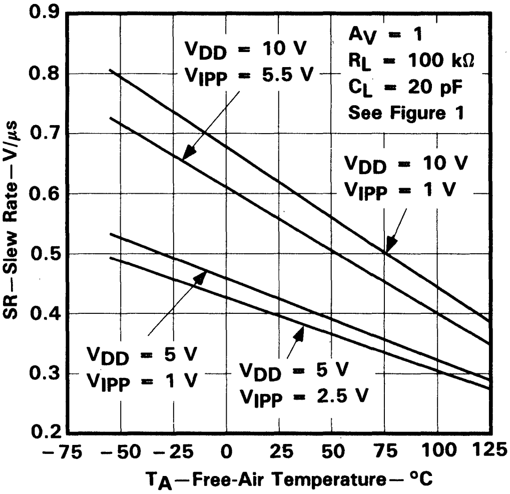


FIGURE 27

NORMALIZED SLEW RATE
vs
FREE-AIR TEMPERATURE

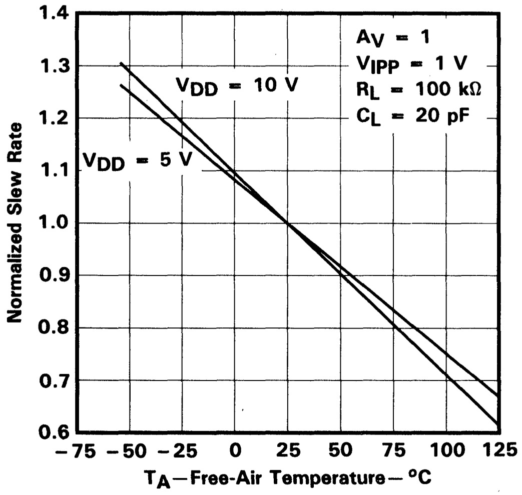


FIGURE 28

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE
vs
FREQUENCY

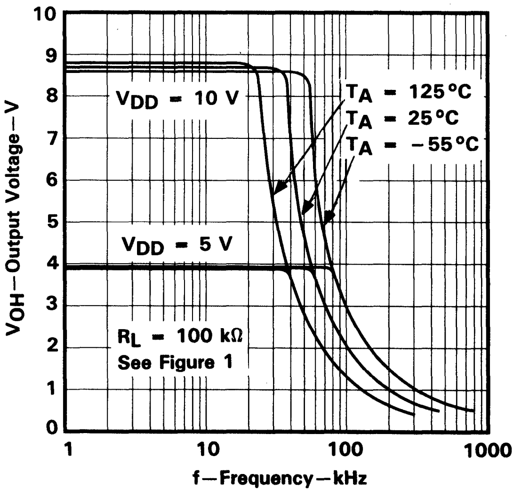


FIGURE 29

---

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS[†]

UNITY-GAIN BANDWIDTH
vs
FREE-AIR TEMPERATURE

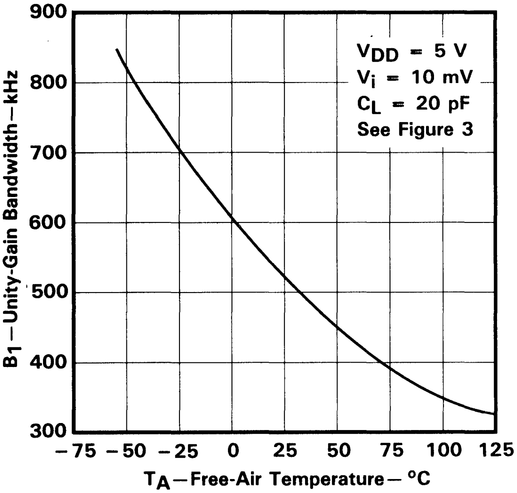


FIGURE 30

UNITY-GAIN BANDWIDTH
vs
SUPPLY VOLTAGE

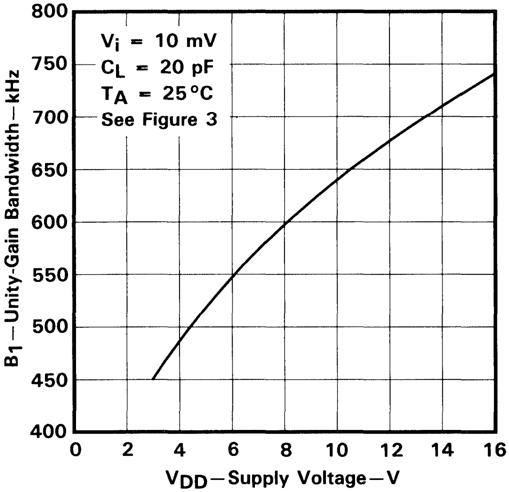


FIGURE 31

LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION AND PHASE SHIFT
vs
FREQUENCY

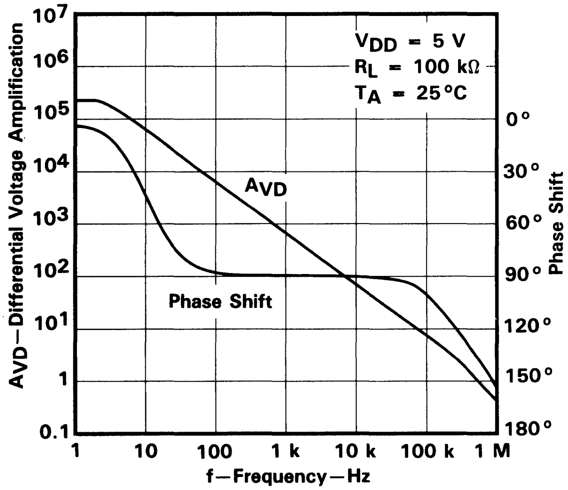


FIGURE 32

LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION AND PHASE SHIFT
vs
FREQUENCY

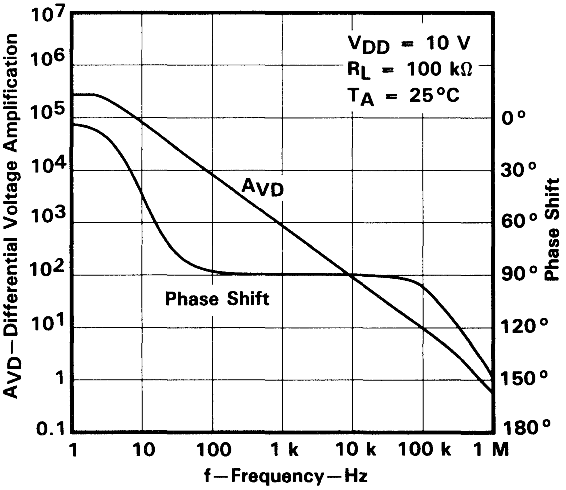


FIGURE 33

[†] Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

PHASE MARGIN
vs
SUPPLY VOLTAGE

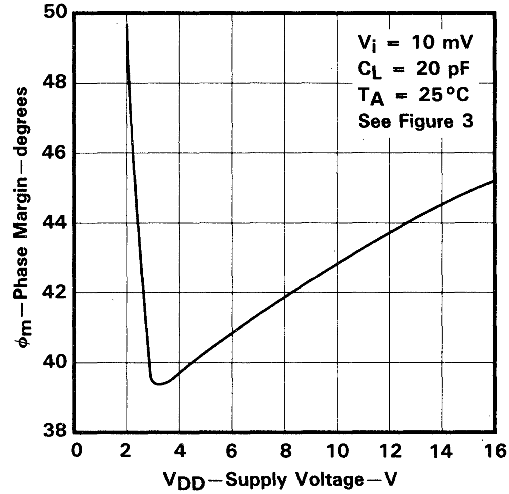


FIGURE 34

PHASE MARGIN
vs
FREE-AIR TEMPERATURE

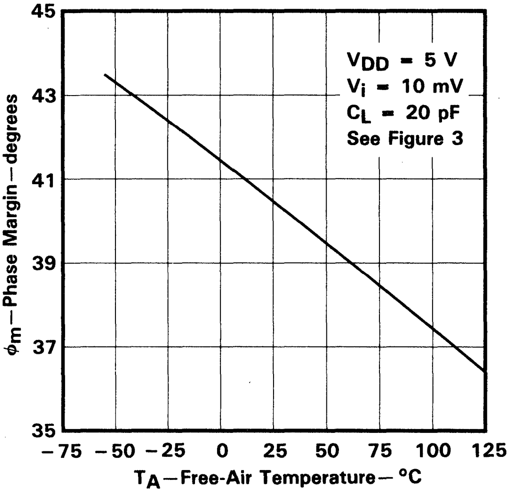


FIGURE 35

PHASE MARGIN
vs
CAPACITIVE LOAD

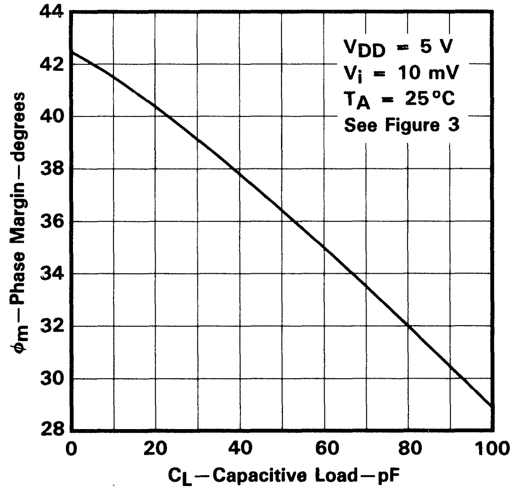


FIGURE 36

EQUIVALENT INPUT NOISE VOLTAGE
vs
FREQUENCY

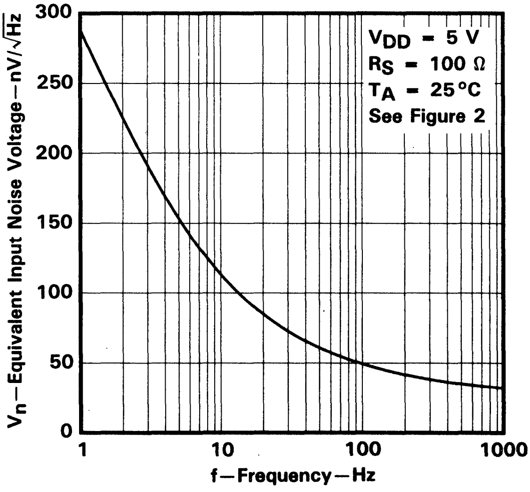


FIGURE 37

---

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL APPLICATION DATA

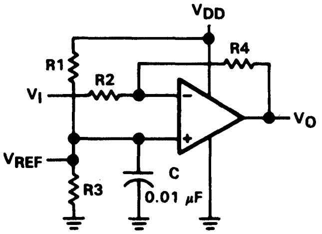
single-supply operation

While the TLC27M2 and TLC27M7 perform well using dual power supplies (also called balanced or split supplies), the design is optimized for single-supply operation. This design includes an input common-mode voltage range that encompasses ground as well as an output voltage range that pulls down to ground. The supply voltage range extends down to 3 V (C-suffix types), thus allowing operation with supply levels commonly available for TTL and HCMOS; however, for maximum dynamic range, 16-V single-supply operation is recommended.

Many single-supply applications require that a voltage be applied to one input to establish a reference level that is above ground. A resistive voltage divider is usually sufficient to establish this reference level (see Figure 38). The low input bias current of the TLC27M2 and TLC27M7 permits the use of very large resistive values to implement the voltage divider, thus minimizing power consumption.

The TLC27M2 and TLC27M7 work well in conjunction with digital logic; however, when powering both linear devices and digital logic from the same power supply, the following precautions are recommended:

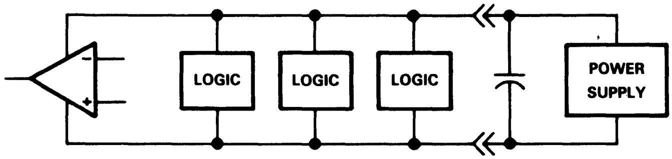
1. Power the linear devices from separate bypassed supply lines (see Figure 39); otherwise the linear device supply rails can fluctuate due to voltage drops caused by high switching currents in the digital logic.
2. Use proper bypass techniques to reduce the probability of noise-induced errors. Single capacitive decoupling is often adequate; however, high-frequency applications may require RC decoupling.



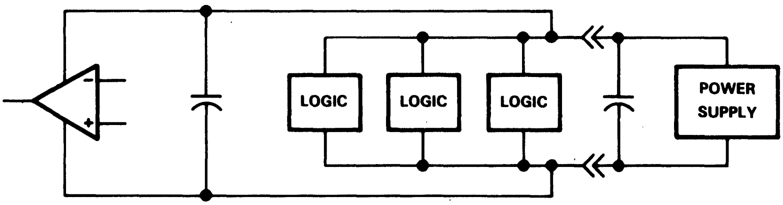
$$V_{REF} = V_{DD} \frac{R3}{R1 + R3}$$

$$V_O = \left(V_{REF} - V_I\right) \frac{R4}{R2} + V_{REF}$$

FIGURE 38. INVERTING AMPLIFIER WITH VOLTAGE REFERENCE



(a) Common Supply Rails



(b) Separate Bypassed Supply Rails (preferred)

FIGURE 39. COMMON VS SEPARATE SUPPLY RAILS

TYPICAL APPLICATION DATA

input characteristics

The TLC27M2 and TLC27M7 are specified with a minimum and a maximum input voltage that, if exceeded at either input, could cause the device to malfunction. Exceeding this specified range is a common problem, especially in single-supply operation. Note that the lower range limit includes the negative rail, while the upper range limit is specified at $V_{DD} - 1$ V at $T_A = 25°C$ and at $V_{DD} - 1.5$ V at all other temperatures.

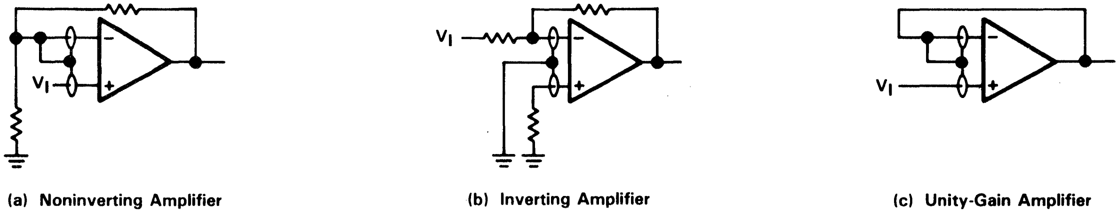
The use of the polysilicon-gate process and the careful input circuit design gives the TLC27M2 and TLC27M7 very good input offset voltage drift characteristics relative to conventional metal-gate processes. Offset voltage drift in CMOS devices is highly influenced by threshold voltage shifts caused by polarization of the phosphorus dopant implanted in the oxide. Placing the phosphorus dopant in a conductor (such as a polysilicon gate) alleviates the polarization problem, thus reducing threshold voltage shifts by more than an order of magnitude. The offset voltage drift with time has been calculated to be typically 0.1 μV/month, including the first month of operation.

Because of the extremely high input impedance and resulting low bias current requirements, the TLC27M2 and TLC27M7 are well suited for low-level signal processing; however, leakage currents on printed circuit boards and sockets can easily exceed bias current requirements and cause a degradation in device performance. It is good practice to include guard rings around inputs (similar to those of Figure 4 in the Parameter Measurement Information section). These guards should be driven from a low-impedance source at the same voltage level as the common-mode input (see Figure 40).

The inputs of any unused amplifiers should be tied to ground to avoid possible oscillation.

noise performance

The noise specifications in op amp circuits are greatly dependent on the current in the first-stage differential amplifier. The low input bias current requirements of the TLC27M2 and TLC27M7 result in a very low noise current, which is insignificant in most applications. This feature makes the devices especially favorable over bipolar devices when using values of circuit impedance greater than 50 kΩ, since bipolar devices exhibit greater noise currents.



(a) Noninverting Amplifier (b) Inverting Amplifier (c) Unity-Gain Amplifier

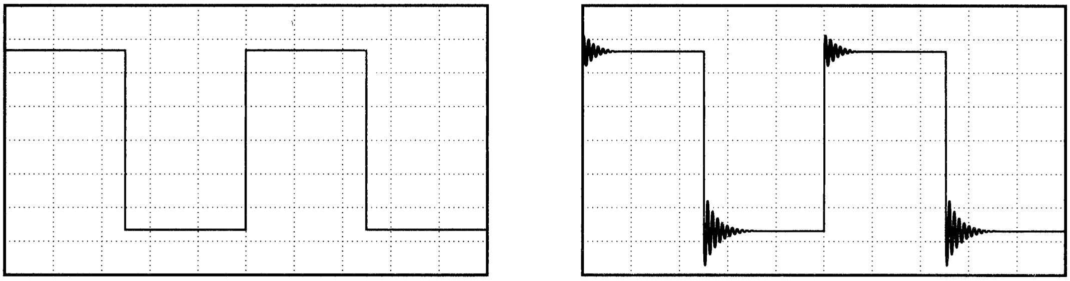
FIGURE 40. GUARD-RING SCHEMES

output characteristics

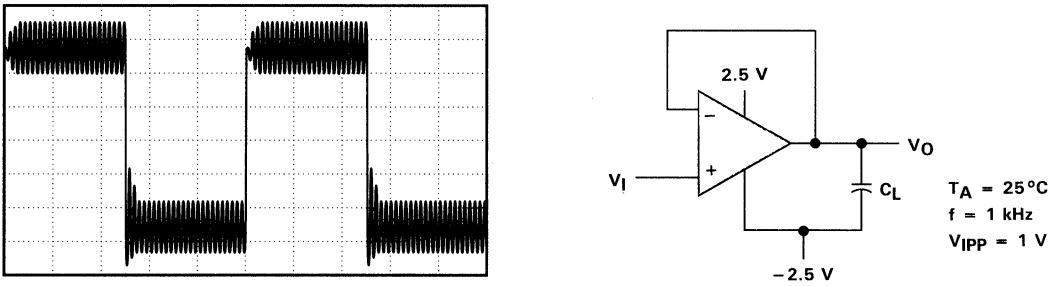
The output stage of the TLC27M2 and TLC27M7 is designed to sink and source relatively high amounts of current (see typical characteristics). If the output is subjected to a short-circuit condition, this high current capability can cause device damage under certain conditions. Output current capability increases with supply voltage.

All operating characteristics of the TLC27M2 and TLC27M7 were measured using a 20-pF load. The devices will drive higher capacitive loads; however, as output load capacitance increases, the resulting response pole occurs at lower frequencies, thereby causing ringing, peaking, or even oscillation (see Figure 41). In many cases, adding a small amount of resistance in series with the load capacitance will alleviate the problem.

TYPICAL APPLICATION DATA



(a) C_L = 20 pF, R_L = no load (b) C_L = 170 pF, R_L = no load



(c) C_L = 190 pF, R_L = no load (d) Test Circuit

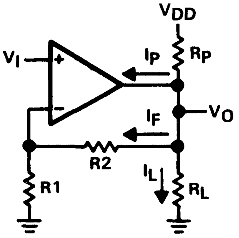
FIGURE 41. EFFECT OF CAPACITIVE LOADS AND TEST CIRCUIT

Although the TLC27M2 and TLC27M7 possess excellent high-level output voltage and current capability, methods for boosting this capability are available, if needed. The simplest method involves the use of a pullup resistor (R_P) connected from the output to the positive supply rail (see Figure 42). There are two disadvantages to the use of this circuit. First, the NMOS pulldown transistor N4 (see equivalent schematic) must sink a comparatively large amount of current. In this circuit, N4 behaves like a linear resistor with an on-resistance between approximately 60 Ω and 180 Ω, depending on how hard the op amp input is driven. With very low values of R_P, a voltage offset from 0 V at the output will occur. Second, pullup resistor R_P acts as a drain load to N4 and the gain of the op amp is reduced at output voltage levels where N5 is not supplying the output current.

feedback

Op amp circuits nearly always employ feedback, and since feedback is the first prerequisite for oscillation, some caution is appropriate. Most oscillation problems result from driving capacitive loads (discussed previously) and ignoring stray input capacitance. A small-value capacitor connected in parallel with the feedback resistor is an effective remedy (see Figure 43). The value of this capacitor is optimized empirically.

TYPICAL APPLICATION DATA



$$R_P = \frac{V_{DD} - V_O}{I_F + I_L + I_P}$$

I_P = Pullup current required by the op amp (typically 500 μA)

FIGURE 42. RESISTIVE PULLUP TO INCREASE V_{OH}

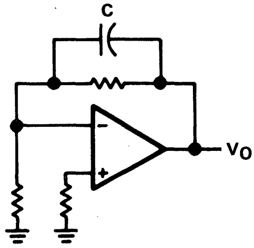


FIGURE 43. COMPENSATION FOR INPUT CAPACITANCE

electrostatic discharge protection

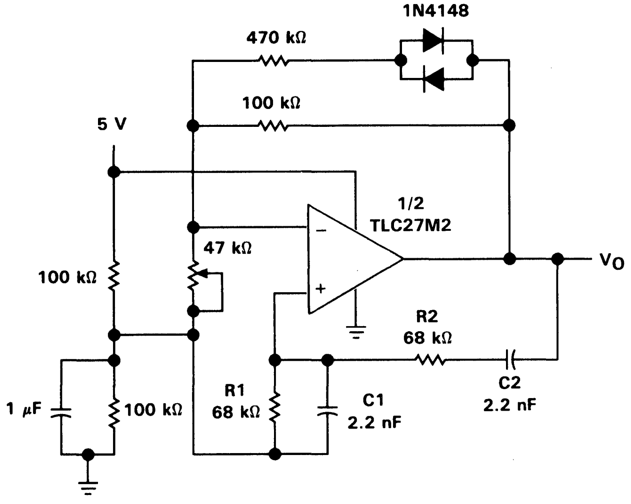
The TLC27M2 and TLC27M7 incorporate an internal electrostatic discharge (ESD) protection circuit that prevents functional failures at voltages up to 2000 V as tested under MIL-STD-883C, Method 3015.2. Care should be exercised, however, when handling these devices, as exposure to ESD may result in the degradation of the device parametric performance. The protection circuit also causes the input bias currents to be temperature-dependent and have the characteristics of a reverse-biased diode.

latch-up

Because CMOS devices are susceptible to latch-up due to their inherent parasitic thyristors, the TLC27M2 and TLC27M7 inputs and outputs were designed to withstand − 100-mA surge currents without sustaining latch-up; however, techniques should be used to reduce the chance of latch-up whenever possible. Internal protection diodes should not, by design, be forward biased. Applied input and output voltage should not exceed the supply voltage by more than 300 mV. Care should be exercised when using capacitive coupling on pulse generators. Supply transients should be shunted by the use of decoupling capacitors (0.1 μF typical) located across the supply rails as close to the device as possible.

The current path established if latch-up occurs is usually between the positive supply rail and ground and can be triggered by surges on the supply lines and/or voltages on either the output or inputs that exceed the supply voltage. Once latch-up occurs, the current flow is limited only by the impedance of the power supply and the forward resistance of the parasitic thyristor and usually results in the destruction of the device. The chance of latch-up occurring increases with increasing temperature and supply voltages.

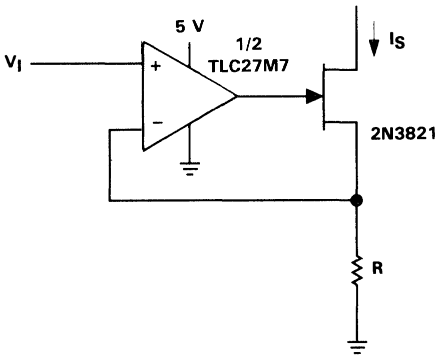
TYPICAL APPLICATION DATA



NOTES: $V_{OPP} \approx 2$ V

$$f_O = \frac{1}{2\pi\sqrt{R1R2C1C2}}$$

FIGURE 44. WIEN OSCILLATOR

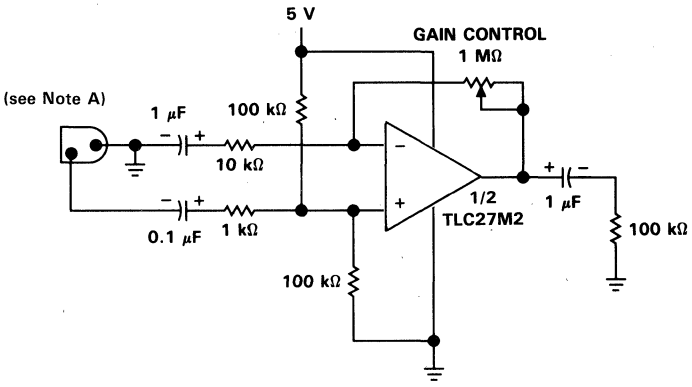


NOTES: $V_I = 0$ V to 3 V

$$I_S = \frac{V_I}{R}$$

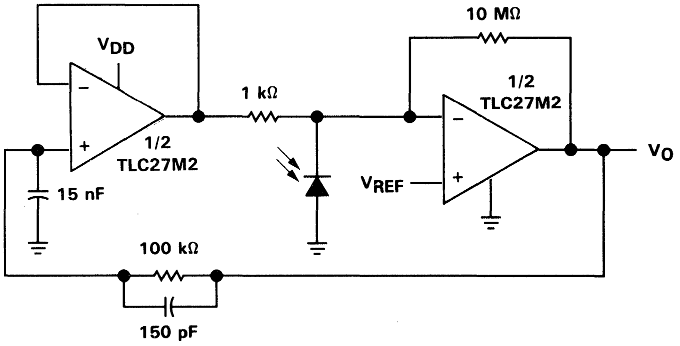
FIGURE 45. PRECISION LOW-CURRENT SINK

TYPICAL APPLICATION DATA



NOTE A.: Low to medium impedance dynamic mike

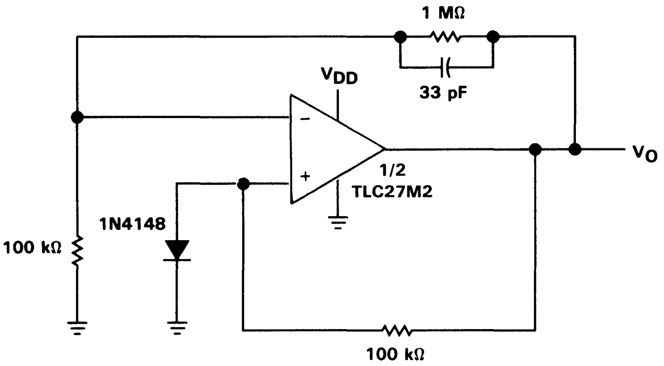
FIGURE 46. MICROPHONE PREAMPLIFIER



NOTES: V_{DD} = 4 V to 15 V
V_{REF} = 0 V to $V_{DD} - 2$ V

FIGURE 47. PHOTO DIODE AMPLIFIER WITH AMBIENT LIGHT REJECTION

TYPICAL APPLICATION DATA



NOTES: V_{DD} = 8 V to 16 V
V_O = 5 V, 10 mA

FIGURE 48. 5-V LOW-POWER VOLTAGE REGULATOR

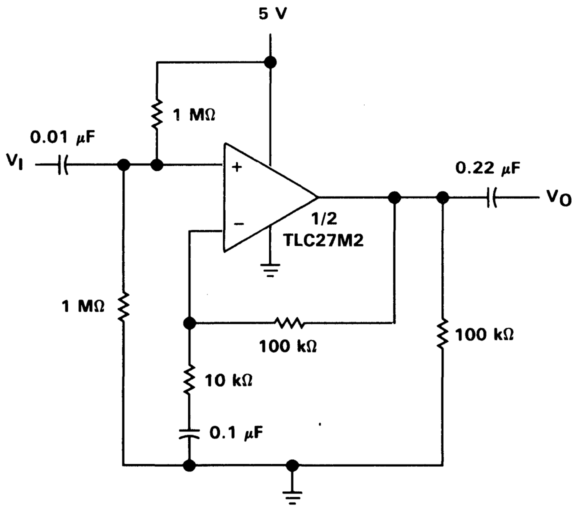


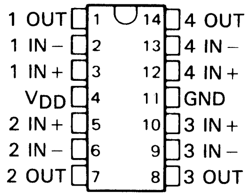
FIGURE 49. SINGLE-RAIL AC AMPLIFIER

TLC27M4, TLC27M4A, TLC27M4B, TLC27M9
LinCMOS™ PRECISION QUAD OPERATIONAL AMPLIFIERS

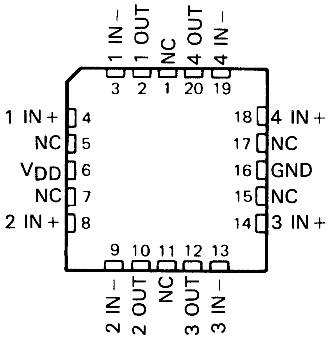
D3143, OCTOBER 1987—REVISED OCTOBER 1990

- **Trimmed Offset Voltage:**
  TLC27M9 . . . 900 μV Max at 25 °C, V_{DD} = 5 V
- **Input Offset Voltage Drift . . . Typically 0.1 μV/Month, Including the First 30 Days**
- **Wide Range of Supply Voltages over Specified Temperature Range:**
  0 °C to 70 °C . . . 3 V to 16 V
  −40 °C to 85 °C . . . 4 V to 16 V
  −55 °C to 125 °C . . . 4 V to 16 V
- **Single-Supply Operation**
- **Common-Mode Input Voltage Range Extends Below the Negative Rail (C-Suffix, I-Suffix Types)**
- **Low Noise . . . Typically 32 nV/$\sqrt{Hz}$ at f = 1 kHz**
- **Low Power . . . Typically 2.1 mW at 25 °C, V_{DD} = 5 V**
- **Output Voltage Range Includes Negative Rail**
- **High Input Impedance . . . 10^{12} Ω Typical**
- **ESD-Protection Circuitry**
- **Small-Outline Package Option Also Available in Tape and Reel**
- **Designed-In Latch-Up Immunity**

D, J, OR N PACKAGE
(TOP VIEW)



FK PACKAGE
(TOP VIEW)



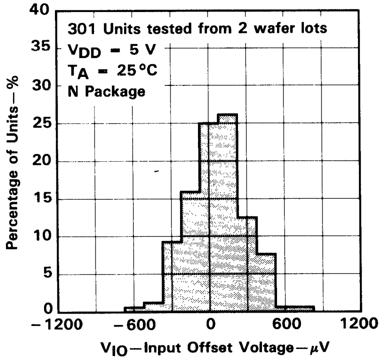
NC—No internal connection

AVAILABLE OPTIONS

T_A	V_{IO}max at 25 °C	PACKAGE			
		SMALL OUTLINE (D)	CHIP CARRIER (FK)	CERAMIC DIP (J)	PLASTIC DIP (N)
0 °C to 70 °C	900 μV	TLC27M9CD	—	—	TLC27M9CN
	2 mV	TLC27M4BCD	—	—	TLC27M4BCN
	5 mV	TLC27M4ACD	—	—	TLC27M4ACN
	10 mV	TLC27M4CD	—	—	TLC27M4CN
−40 °C to 85 °C	900 μV	TLC27M9ID	—	—	TLC27M9IN
	2 mV	TLC27M4BID	—	—	TLC27M4BIN
	5 mV	TLC27M4AID	—	—	TLC27M4AIN
	10 mV	TLC27M4ID	—	—	TLC27M4IN
−55 °C to 125 °C	900 μV	TLC27M9MD	TLC27M9MFK	TLC27M9MJ	TLC27M9MN
	10 mV	TLC27M4MD	TLC27M4MFK	TLC27M4MJ	TLC27M4MN

The D package is available in tape and reel. Add R suffix to the device type, (e.g., TLC27M9CDR).

DISTRIBUTION OF TLC27M9
INPUT OFFSET VOLTAGE



description

The TLC27M4 and TLC27M9 quad operational amplifiers combine a wide range of input offset voltage grades with low offset voltage drift, high input impedance, low noise, and speeds comparable to that of general-purpose bipolar devices. These devices use Texas Instruments silicon-gate LinCMOS™ technology, which provides offset voltage stability far exceeding the stability available with conventional metal-gate processes.

The extremely high input impedance and low bias currents make these cost-effective devices ideal for applications that have previously been reserved for general-purpose bipolar products, but with only a fraction of the power consumption. Four offset voltage grades are available (C-suffix and I-suffix types), ranging from the low-cost TLC27M4 (10 mV) to the high-precision TLC27M9 (900 μV). These advantages, in combination with good common-mode rejection and supply voltage rejection, make these devices a good choice for new state-of-the-art designs as well as for upgrading existing designs.

In general, many features associated with bipolar technology are available on LinCMOS™ operational amplifiers, without the power penalties of bipolar technology. General applications such as transducer interfacing, analog calculations, amplifier blocks, active filters, and signal buffering are easily designed with the TLC27M4 and TLC27M9. The devices also exhibit low voltage single-supply operation and low power consumption, making them ideally suited for remote and inaccessible battery-powered applications. The common-mode input voltage range includes the negative rail.

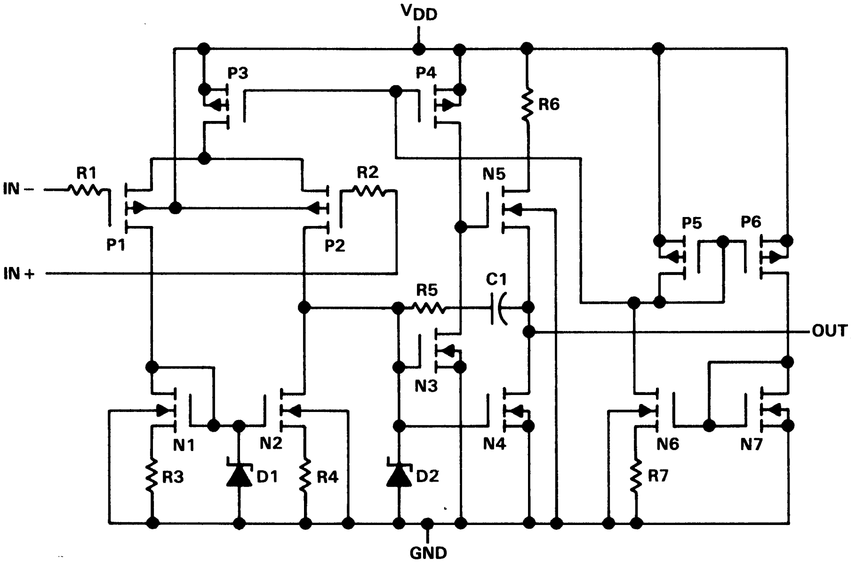
A wide range of packaging options is available, including small-outline and chip carrier versions for high-density system applications.

The device inputs and outputs are designed to withstand −100-mA surge currents without sustaining latch-up.

The TLC27M4 and TLC27M9 incorporate internal ESD-protection circuits that prevent functional failures at voltages up to 2000 V as tested under MIL-STD-883C, Method 3015; however, care should be exercised in handling these devices as exposure to ESD may result in the degradation of the device parametric performance.

The C-suffix devices are characterized for operation from 0°C to 70°C. The I-suffix devices are characterized for operation from −40°C to 85°C. The M-suffix devices are characterized for operation over the full military temperature range of −55°C to 125°C.

equivalent schematic (each amplifier)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{DD} (see Note 1)	18 V
Differential input voltage (see Note 2)	$\pm V_{DD}$
Input voltage range, V_I (any input)	-0.3 V to V_{DD}
Input current, I_I	±5 mA
Output current, I_O (each output)	±30 mA
Total current into V_{DD} terminal	45 mA
Total current out of ground terminal	45 mA
Duration of short-circuit current at (or below) 25°C (see Note 3)	unlimited
Continuous total dissipation	See Dissipation Rating Table
Operating free-air temperature, T_A: C-suffix	0°C to 70°C
I-suffix	−40°C to 85°C
M-suffix	−55°C to 125°C
Storage temperature range	−65°C to 150°C
Case temperature for 60 seconds: FK package	260°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D and N package	260°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: J package	300°C

NOTES: 1. All voltage values, except differential voltages, are with respect to network ground.
2. Differential voltages are at the noninverting input with respect to the inverting input.
3. The output may be shorted to either supply. Temperature and/or supply voltages must be limited to ensure that the maximum dissipation rating is not exceeded (see application section).

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING	$T_A = 125°C$ POWER RATING
D	950 mW	7.6 mW/°C	608 mW	494 mW	
FK	1375 mW	11 mW/°C	880 mW	715 mW	275 mW
J	1375 mW	11 mW/°C	880 mW	715 mW	275 mW
N	1575 mW	12.6 mW/°C	1008 mW	819 mW	

recommended operating conditions

		C-SUFFIX			I-SUFFIX			M-SUFFIX			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{DD}		3		16	4		16	4		16	V
Common-mode input voltage, V_{IC}	$V_{DD} = 5$ V	−0.2		3.5	−0.2		3.5	0		3.5	V
	$V_{DD} = 10$ V	−0.2		8.5	−0.2		8.5	0		8.5	
Operating free-air temperature, T_A		0		70	−40		85	−55		125	°C

electrical characteristics at specified free-air temperature, V_{DD} = 5 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS		T_A†	MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	TLC27M4C	V_O = 1.4 V,	V_{IC} = 0,	25°C		1.1	10	mV
			R_S = 50 Ω,	R_L = 100 kΩ	Full range			12	
		TLC27M4AC	V_O = 1.4 V,	V_{IC} = 0,	25°C		0.9	5	
			R_S = 50 Ω,	R_L = 100 kΩ	Full range			6.5	
		TLC27M4BC	V_O = 1.4 V,	V_{IC} = 0,	25°C		250	2000	µV
			R_S = 50 Ω,	R_L = 100 kΩ	Full range			3000	
		TLC27M9C	V_O = 1.4 V,	V_{IC} = 0,	25°C		210	900	
			R_S = 50 Ω,	R_L = 100 kΩ	Full range			1500	
α_{VIO}	Average temperature coefficient of input offset voltage				25°C to 70°C		1.7		µV/°C
I_{IO}	Input offset current (see Note 4)		V_O = 2.5 V,	V_{IC} = 2.5 V	25°C		0.1		pA
					70°C		7	300	
I_{IB}	Input bias current (see Note 4)		V_O = 2.5 V,	V_{IC} = 2.5 V	25°C		0.6		pA
					70°C		40	600	
V_{ICR}	Common-mode input voltage range (see Note 5)				25°C	−0.2 to 4	−0.3 to 4.2		V
					Full range	−0.2 to 3.5			V
V_{OH}	High-level output voltage		V_{ID} = 100 mV,	R_L = 100 kΩ	25°C	3.2	3.9		V
					0°C	3	3.9		
					70°C	3	4		
V_{OL}	Low-level output voltage		V_{ID} = −100 mV,	I_{OL} = 0	25°C		0	50	mV
					0°C		0	50	
					70°C		0	50	
A_{VD}	Large-signal differential voltage amplification		V_O = 0.25 V to 2 V,	R_L = 100 kΩ	25°C	25	170		V/mV
					0°C	15	200		
					70°C	15	140		
CMRR	Common-mode rejection ratio		V_{IC} = V_{ICR} min		25°C	65	91		dB
					0°C	60	91		
					70°C	60	92		
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)		V_{DD} = 5 V to 10 V,	V_O = 1.4 V	25°C	70	93		dB
					0°C	60	92		
					70°C	60	94		
I_{DD}	Supply current (four amplifiers)		V_O = 2.5 V, No load	V_{IC} = 2.5 V,	25°C		420	1120	µA
					0°C		500	1280	
					70°C		340	880	

† Full range is 0°C to 70°C.

NOTES: 4. The typical values of input bias current and input offset current below 5 pA were determined mathematically.
5. This range also applies to each input individually.

electrical characteristics at specified free-air temperature, V_{DD} = 10 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS	T_A†	MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	TLC27M4C	V_O = 1.4 V, V_{IC} = 0, R_S = 50 Ω, R_L = 100 kΩ	25°C		1.1	10	mV
				Full range			12	
		TLC27M4AC	V_O = 1.4 V, V_{IC} = 0, R_S = 50 Ω, R_L = 100 kΩ	25°C		0.9	5	
				Full range			6.5	
		TLC27M4BC	V_O = 1.4 V, V_{IC} = 0, R_S = 50 Ω, R_L = 100 kΩ	25°C		260	2000	µV
				Full range			3000	
		TLC27M9C	V_O = 1.4 V, V_{IC} = 0, R_S = 50 Ω, R_L = 100 kΩ	25°C		220	1200	
				Full range			1900	
α_{VIO}	Average temperature coefficient of input offset voltage			25°C to 70°C		2.1		µV/°C
I_{IO}	Input offset current (see Note 4)		V_O = 5 V, V_{IC} = 5 V	25°C		0.1		pA
				70°C		7	300	
I_{IB}	Input bias current (see Note 4)		V_O = 5 V, V_{IC} = 5 V	25°C		0.7		pA
				70°C		50	600	
V_{ICR}	Common-mode input voltage range (see Note 5)			25°C	−0.2 to 9	−0.3 to 9.2		V
				Full range	−0.2 to 8.5			V
V_{OH}	High-level output voltage		V_{ID} = 100 mV, R_L = 100 kΩ	25°C	8	8.7		V
				0°C	7.8	8.7		
				70°C	7.8	8.7		
V_{OL}	Low-level output voltage		V_{ID} = −100 mV, I_{OL} = 0	25°C		0	50	mV
				0°C		0	50	
				70°C		0	50	
A_{VD}	Large-signal differential voltage amplification		V_O = 1 V to 6 V, R_L = 100 kΩ	25°C	25	275		V/mV
				0°C	15	320		
				70°C	15	230		
CMRR	Common-mode rejection ratio		V_{IC} = V_{ICR} min	25°C	65	94		dB
				0°C	60	94		
				70°C	60	94		
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)		V_{DD} = 5 V to 10 V, V_O = 1.4 V	25°C	70	93		dB
				0°C	60	92		
				70°C	60	94		
I_{DD}	Supply current (four amplifiers)		V_O = 5 V, V_{IC} = 5 V, No load	25°C		570	1200	µA
				0°C		690	1600	
				70°C		440	1120	

† Full range is 0°C to 70°C.

NOTES: 4. The typical values of input bias current and input offset current below 5 pA were determined mathematically.
5. This range also applies to each input individually.

electrical characteristics at specified free-air temperature, V_{DD} = 5 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS	T_A†	MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	TLC27M4I	V_O = 1.4 V, V_{IC} = 0, R_S = 50 Ω, R_L = 100 kΩ	25°C		1.1	10	mV
				Full range			13	
		TLC27M4AI	V_O = 1.4 V, V_{IC} = 0, R_S = 50 Ω, R_L = 100 kΩ	25°C		0.9	5	
				Full range			7	
		TLC27M4BI	V_O = 1.4 V, V_{IC} = 0, R_S = 50 Ω, R_L = 100 kΩ	25°C		250	2000	µV
				Full range			3500	
		TLC27M9I	V_O = 1.4 V, V_{IC} = 0, R_S = 50 Ω, R_L = 100 kΩ	25°C		210	900	
				Full range			2000	
α_{VIO}	Average temperature coefficient of input offset voltage			25°C to 85°C		1.7		µV/°C
I_{IO}	Input offset current (see Note 4)		V_O = 2.5 V, V_{IC} = 2.5 V	25°C		0.1		pA
				85°C		24	1000	
I_{IB}	Input bias current (see Note 4)		V_O = 2.5 V, V_{IC} = 2.5 V	25°C		0.6		pA
				85°C		200	2000	
V_{ICR}	Common-mode input voltage range (see Note 5)			25°C	−0.2 to 4	−0.3 to 4.2		V
				Full range	−0.2 to 3.5			V
V_{OH}	High-level output voltage		V_{ID} = 100 mV, R_L = 100 kΩ	25°C	3.2	3.9		V
				−40°C	3	3.9		
				85°C	3	4		
V_{OL}	Low-level output voltage		V_{ID} = −100 mV, I_{OL} = 0	25°C		0	50	mV
				−40°C		0	50	
				85°C		0	50	
A_{VD}	Large-signal differential voltage amplification		V_O = 0.25 V to 2 V, R_L = 100 kΩ	25°C	25	170		V/mV
				−40°C	15	270		
				85°C	15	130		
CMRR	Common-mode rejection ratio		V_{IC} = V_{ICR}min	25°C	65	91		dB
				−40°C	60	90		
				85°C	60	90		
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)		V_{DD} = 5 V to 10 V, V_O = 1.4 V	25°C	70	93		dB
				−40°C	60	91		
				85°C	60	94		
I_{DD}	Supply current (four amplifiers)		V_O = 2.5 V, V_{IC} = 2.5 V, No load	25°C		420	1120	µA
				−40°C		630	1600	
				85°C		320	800	

† Full range is −40°C to 85°C.

NOTES: 4. The typical values of input bias current and input offset current below 5 pA were determined mathematically.
5. This range also applies to each input individually.

electrical characteristics at specified free-air temperature, V_{DD} = 10 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS		T_A[†]	MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	TLC27M4I	V_O = 1.4 V, R_S = 50 Ω,	V_{IC} = 0, R_L = 100 kΩ	25°C		1.1	10	mV
					Full range			13	
		TLC27M4AI	V_O = 1.4 V, R_S = 50 Ω,	V_{IC} = 0, R_L = 100 kΩ	25°C		0.9	5	
					Full range			7	
		TLC27M4BI	V_O = 1.4 V, R_S = 50 Ω,	V_{IC} = 0, R_L = 100 kΩ	25°C		260	2000	µV
					Full range			3500	
		TLC27M9I	V_O = 1.4 V, R_S = 50 Ω,	V_{IC} = 0, R_L = 100 kΩ	25°C		220	1200	
					Full range			2900	
α_{VIO}	Average temperature coefficient of input offset voltage				25°C to 85°C		2.1		µV/°C
I_{IO}	Input offset current (see Note 4)		V_O = 5 V,	V_{IC} = 5 V	25°C		0.1		pA
					85°C		26	1000	
I_{IB}	Input bias current (see Note 4)		V_O = 5 V,	V_{IC} = 5 V	25°C		0.7		pA
					85°C		220	2000	
V_{ICR}	Common-mode input voltage range (see Note 5)				25°C	−0.2 to 9	−0.3 to 9.2		V
					Full range	−0.2 to 8.5			V
V_{OH}	High-level output voltage		V_{ID} = 100 mV,	R_L = 100 kΩ	25°C	8	8.7		V
					−40°C	7.8	8.7		
					85°C	7.8	8.7		
V_{OL}	Low-level output voltage		V_{ID} = −100 mV,	I_{OL} = 0	25°C		0	50	mV
					−40°C		0	50	
					85°C		0	50	
A_{VD}	Large-signal differential voltage amplification		V_O = 1 V to 6 V,	R_L = 100 kΩ	25°C	25	275		V/mV
					−40°C	15	390		
					85°C	15	220		
CMRR	Common-mode rejection ratio		V_{IC} = V_{ICR} min		25°C	65	94		dB
					−40°C	60	93		
					85°C	60	94		
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)		V_{DD} = 5 V to 10 V,	V_O = 1.4 V	25°C	70	93		dB
					−40°C	60	91		
					85°C	60	94		
I_{DD}	Supply current (four amplifiers)		V_O = 5 V, No load	V_{IC} = 5 V,	25°C		570	1200	µA
					−40°C		900	1800	
					85°C		410	1040	

[†] Full range is −40°C to 85°C.

NOTES: 4. The typical values of input bias current and input offset current below 5 pA were determined mathematically.
5. This range also applies to each input individually.

electrical characteristics at specified free-air temperature, V_{DD} = 5 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS	T_A†	MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	TLC27M4M	V_O = 1.4 V, V_{IC} = 0, R_S = 50 Ω, R_L = 100 kΩ	25°C		1.1	10	mV
				Full range			12	
		TLC27M9M	V_O = 1.4 V, V_{IC} = 0, R_S = 50 Ω, R_L = 100 kΩ	25°C		210	900	µV
				Full range			3750	
α_{VIO}	Average temperature coefficient of input offset voltage			25°C to 125°C		1.7		µV/°C
I_{IO}	Input offset current (see Note 4)		V_O = 2.5 V, V_{IC} = 2.5 V	25°C		0.1		pA
				125°C		1.4	15	nA
I_{IB}	Input bias current (see Note 4)		V_O = 2.5 V, V_{IC} = 2.5 V	25°C		0.6		pA
				125°C		9	35	nA
V_{ICR}	Common-mode input voltage range (see Note 5)			25°C	0 to 4	−0.3 to 4.2		V
				Full range	0 to 3.5			V
V_{OH}	High-level output voltage		V_{ID} = 100 mV, R_L = 100 kΩ	25°C	3.2	3.9		V
				−55°C	3	3.9		
				125°C	3	4		
V_{OL}	Low-level output voltage		V_{ID} = −100 mV, I_{OL} = 0	25°C		0	50	mV
				−55°C		0	50	
				125°C		0	50	
A_{VD}	Large-signal differential voltage amplification		V_O = 0.25 V to 2 V, R_L = 100 kΩ	25°C	25	170		V/mV
				−55°C	15	290		
				125°C	15	120		
CMRR	Common-mode rejection ratio		V_{IC} = V_{ICR} min	25°C	65	91		dB
				−55°C	60	89		
				125°C	60	91		
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)		V_{DD} = 5 V to 10 V, V_O = 1.4 V	25°C	70	93		dB
				−55°C	60	91		
				125°C	60	94		
I_{DD}	Supply current (four amplifiers)		V_O = 2.5 V, V_{IC} = 2.5 V, No load	25°C		420	1120	µA
				−55°C		680	1760	
				125°C		280	720	

† Full range is −55°C to 125°C.

NOTES: 4. The typical values of input bias current and input offset current below 5 pA were determined mathematically.
5. This range also applies to each input individually.

electrical characteristics at specified free-air temperature, V_{DD} = 10 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS	T_A†	MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	TLC27M4M	V_O = 1.4 V, V_{IC} = 0, R_S = 50 Ω, R_L = 100 kΩ	25°C		1.1	10	mV
				Full range			12	
		TLC27M9M	V_O = 1.4 V, V_{IC} = 0, R_S = 50 Ω, R_L = 100 kΩ	25°C		220	1200	μV
				Full range			4300	
α_{VIO}	Average temperature coefficient of input offset voltage			25°C to 125°C		2.1		μV/°C
I_{IO}	Input offset current (see Note 4)		V_O = 5 V, V_{IC} = 5 V	25°C		0.1		pA
				125°C		1.8	15	nA
I_{IB}	Input bias current (see Note 4)		V_O = 5 V, V_{IC} = 5 V	25°C		0.7		pA
				125°C		10	35	nA
V_{ICR}	Common-mode input voltage range (see Note 5)			25°C	0 to 9	−0.3 to 9.2		V
				Full range	0 to 8.5			V
V_{OH}	High-level output voltage		V_{ID} = 100 mV, R_L = 100 kΩ	25°C	8	8.7		V
				−55°C	7.8	8.6		
				125°C	7.8	8.8		
V_{OL}	Low-level output voltage		V_{ID} = −100 mV, I_{OL} = 0	25°C		0	50	mV
				−55°C		0	50	
				125°C		0	50	
A_{VD}	Large-signal differential voltage amplification		V_O = 1 V to 6 V, R_L = 100 kΩ	25°C	25	275		V/mV
				−55°C	15	420		
				125°C	15	190		
CMRR	Common-mode rejection ratio		V_{IC} = V_{ICR} min	25°C	65	94		dB
				−55°C	60	93		
				125°C	60	93		
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)		V_{DD} = 5 V to 10 V, V_O = 1.4 V	25°C	70	93		dB
				−55°C	60	91		
				125°C	60	94		
I_{DD}	Supply current (four amplifiers)		V_O = 5 V, V_{IC} = 5 V, No load	25°C		570	1200	μA
				−55°C		980	2000	
				125°C		360	960	

† Full range is −55°C to 125°C.

NOTES: 4. The typical values of input bias current and input offset current below 5 pA were determined mathematically.
5. This range also applies to each input individually.

operating characteristics, V_{DD} = 5 V

PARAMETER		TEST CONDITIONS		T_A	MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain	R_L = 100 kΩ, C_L = 20 pF, See Figure 1	V_{IPP} = 1 V	25°C		0.43		V/μs
				0°C		0.46		
				70°C		0.36		
			V_{IPP} = 2.5 V	25°C		0.40		
				0°C		0.43		
				70°C		0.34		
V_n	Equivalent input noise voltage	f = 1 kHz, See Figure 2	R_S = 100 Ω,	25°C		32		$\mathrm{nV}/\sqrt{\mathrm{Hz}}$
B_{OM}	Maximum output swing bandwidth	V_O = V_{OH}, R_L = 100 kΩ,	C_L = 20 pF, See Figure 1	25°C		55		kHz
				0°C		60		
				70°C		50		
B_1	Unity-gain bandwidth	V_i = 10 mV, See Figure 3	C_L = 20 pF,	25°C		525		kHz
				0°C		610		
				70°C		400		
ϕ_m	Phase margin	V_i = 10 mV, C_L = 20 pF,	f = B_1, See Figure 3	25°C		40°		
				0°C		41°		
				70°C		39°		

operating characteristics, V_{DD} = 10 V

PARAMETER		TEST CONDITIONS		T_A	MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain	R_L = 100 kΩ, C_L = 20 pF, See Figure 1	V_{IPP} = 1 V	25°C		0.62		V/μs
				0°C		0.67		
				70°C		0.51		
			V_{IPP} = 5.5 V	25°C		0.56		
				0°C		0.61		
				70°C		0.46		
V_n	Equivalent input noise voltage	f = 1 kHz, See Figure 2	R_S = 100 Ω,	25°C		32		$\mathrm{nV}/\sqrt{\mathrm{Hz}}$
B_{OM}	Maximum output swing bandwidth	V_O = V_{OH}, R_L = 100 kΩ,	C_L = 20 pF, See Figure 1	25°C		35		kHz
				0°C		40		
				70°C		30		
B_1	Unity-gain bandwidth	V_i = 10 mV, See Figure 3	C_L = 20 pF,	25°C		635		kHz
				0°C		710		
				70°C		510		
ϕ_m	Phase margin	V_i = 10 mV, C_L = 20 pF,	f = B_1, See Figure 3	25°C		43°		
				0°C		44°		
				70°C		42°		

operating characteristics, V_{DD} = 5 V

PARAMETER		TEST CONDITIONS		T_A	MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain	R_L = 100 kΩ, C_L = 20 pF, See Figure 1	V_{IPP} = 1 V	25°C		0.43		V/μs
				−40°C		0.51		
				85°C		0.35		
			V_{IPP} = 2.5 V	25°C		0.40		
				−40°C		0.48		
				85°C		0.32		
V_n	Equivalent input noise voltage	f = 1 kHz, See Figure 2	R_S = 100 Ω,	25°C		32		nV/√Hz
B_{OM}	Maximum output swing bandwidth	V_O = V_{OH}, R_L = 100 kΩ,	C_L = 20 pF, See Figure 1	25°C		55		kHz
				−40°C		75		
				85°C		45		
B_1	Unity-gain bandwidth	V_i = 10 mV, See Figure 3	C_L = 20 pF,	25°C		525		kHz
				−40°C		770		
				85°C		370		
ϕ_m	Phase margin	V_i = 10 mV, C_L = 20 pF,	f = B_1, See Figure 3	25°C		40°		
				−40°C		43°		
				85°C		38°		

operating characteristics, V_{DD} = 10 V

PARAMETER		TEST CONDITIONS		T_A	MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain	R_L = 100 kΩ, C_L = 20 pF, See Figure 1	V_{IPP} = 1 V	25°C		0.62		V/μs
				−40°C		0.77		
				85°C		0.47		
			V_{IPP} = 5.5 V	25°C		0.56		
				−40°C		0.70		
				85°C		0.44		
V_n	Equivalent input noise voltage	f = 1 kHz, See Figure 2	R_S = 100 Ω,	25°C		32		nV/√Hz
B_{OM}	Maximum output swing bandwidth	V_O = V_{OH}, R_L = 100 kΩ,	C_L = 20 pF, See Figure 1	25°C		35		kHz
				−40°C		45		
				85°C		25		
B_1	Unity-gain bandwidth	V_i = 10 mV, See Figure 3	C_L = 20 pF,	25°C		635		kHz
				−40°C		880		
				85°C		480		
ϕ_m	Phase margin	V_i = 10 mV, C_L = 20 pF,	f = B_1, See Figure 3	25°C		43°		
				−40°C		46°		
				85°C		41°		

operating characteristics, V_{DD} = 5 V

PARAMETER		TEST CONDITIONS		T_A	MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain	R_L = 100 kΩ, C_L = 20 pF, See Figure 1	V_{IPP} = 1 V	25°C		0.43		V/μs
				−55°C		0.54		
				125°C		0.29		
			V_{IPP} = 2.5 V	25°C		0.40		
				−55°C		0.50		
				125°C		0.28		
V_n	Equivalent input noise voltage	f = 1 kHz, See Figure 2	R_S = 100 Ω,	25°C		32		nV/√Hz
B_{OM}	Maximum output swing bandwidth	V_O = V_{OH}, R_L = 100 kΩ,	C_L = 20 pF, See Figure 1	25°C		55		kHz
				−55°C		80		
				125°C		40		
B_1	Unity-gain bandwidth	V_i = 10 mV, See Figure 3	C_L = 20 pF,	25°C		525		kHz
				−55°C		850		
				125°C		330		
ϕ_m	Phase margin	V_i = 10 mV, C_L = 20 pF,	f = B_1, See Figure 3	25°C		40°		
				−55°C		44°		
				125°C		36°		

operating characteristics, V_{DD} = 10 V

PARAMETER		TEST CONDITIONS		T_A	MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain	R_L = 100 kΩ, C_L = 20 pF, See Figure 1	V_{IPP} = 1 V	25°C		0.62		V/μs
				−55°C		0.81		
				125°C		0.38		
			V_{IPP} = 5.5 V	25°C		0.56		
				−55°C		0.73		
				125°C		0.35		
V_n	Equivalent input noise voltage	f = 1 kHz, See Figure 2	R_S = 100 Ω,	25°C		32		nV/√Hz
B_{OM}	Maximum output swing bandwidth	V_O = V_{OH}, R_L = 100 kΩ,	C_L = 20 pF, See Figure 1	25°C		35		kHz
				−55°C		50		
				125°C		20		
B_1	Unity-gain bandwidth	V_i = 10 mV, See Figure 3	C_L = 20 pF,	25°C		635		kHz
				−55°C		960		
				125°C		440		
ϕ_m	Phase margin	V_i = 10 mV, C_L = 20 pF,	f = B_1, See Figure 3	25°C		43°		
				−55°C		47°		
				125°C		39°		

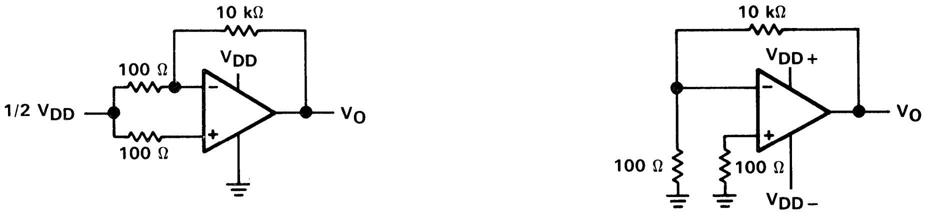
PARAMETER MEASUREMENT INFORMATION

single-supply versus split-supply test circuits

Because the TLC27M4 and TLC27M9 are optimized for single-supply operation, circuit configurations used for the various tests often present some inconvenience since the input signal, in many cases, must be offset from ground. This inconvenience can be avoided by testing the device with split supplies and the output load tied to the negative rail. A comparison of single-supply versus split-supply test circuits is shown below. The use of either circuit will give the same result.

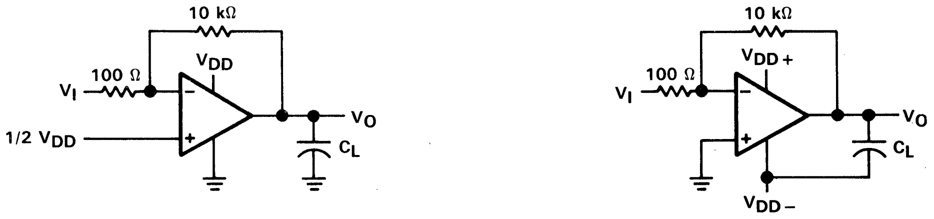
(a) Single-Supply (b) Split-Supply

FIGURE 1. UNITY-GAIN AMPLIFIER



(a) Single-Supply (b) Split-Supply

FIGURE 2. NOISE TEST CIRCUIT



(a) Single-Supply (b) Split-Supply

FIGURE 3. GAIN-OF-100 INVERTING AMPLIFIER

PARAMETER MEASUREMENT INFORMATION

input bias current

Because of the high input impedance of the TLC27M4 and TLC27M9 op amps, attempts to measure the input bias current can result in erroneous readings. The bias current at normal room ambient temperature is typically less than 1 pA, a value that is easily exceeded by leakages on the test socket. Two suggestions are offered to avoid erroneous measurements:

1. Isolate the device from other potential leakage sources. Use a grounded shield around and between the device inputs (see Figure 4). Leakages that would otherwise flow to the inputs will be shunted away.
2. Compensate for the leakage of the test socket by actually performing an input bias current test (using a picoammeter) with no device in the test socket. The actual input bias current can then be calculated by subtracting the "open-socket" leakage readings from the readings obtained with a device in the test socket.

One word of caution . . . many automatic testers as well as some bench-top op amp testers use the servo-loop technique with a resistor in series with the device input to measure the input bias current (the voltage drop across the series resistor is measured and the bias current is calculated). This method requires that a device be inserted into the test socket to obtain a correct reading; therefore, an "open-socket" reading is not feasible using this method.

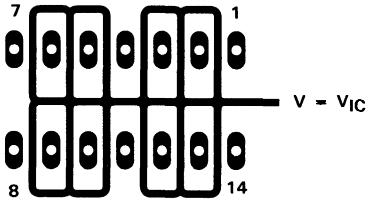


FIGURE 4. ISOLATION METAL AROUND DEVICE INPUTS
(J AND N DUAL-IN-LINE-PACKAGE)

low-level output voltage

To obtain low-supply-voltage operation, some compromise was necessary in the input stage. This compromise results in the device low-level output being dependent on both the common-mode input voltage level as well as the differential input voltage level. When attempting to correlate low-level output readings with those quoted in the electrical specifications, these two conditions should be observed. If conditions other than these are to be used, please refer to Figures 14 through 19 in the Typical Characteristics of this data sheet.

PARAMETER MEASUREMENT INFORMATION

input offset voltage temperature coefficient

Erroneous readings often result from attempts to measure temperature coefficient of input offset voltage. This parameter is actually a calculation using input offset voltage measurements obtained at two different temperatures. When one (or both) of the temperatures is below freezing, moisture can collect on both the device and the test socket. This moisture will result in leakage and contact resistance, which can cause erroneous input offset voltage readings. The isolation techniques previously mentioned have no effect on the leakage since the moisture also covers the isolation metal itself, thereby rendering it useless. It is suggested that these measurements be performed at temperatures above freezing to minimize error.

full-power response

Full-power response, the frequency above which the op amp slew rate limits the output voltage swing, is often specified two ways . . . full-linear response and full-peak response. The full-linear response is generally measured by monitoring the distortion level of the output while increasing the frequency of a sinusoidal input signal until the maximum frequency is found above which the output contains significant distortion. The full-peak response is defined as the maximum output frequency, without regard to distortion, above which full peak-to-peak output swing cannot be maintained.

Because there is no industry-wide accepted value for ''significant'' distortion, the full-peak response is specified in this data sheet and is measured using the circuit of Figure 1. The initial setup involves the use of a sinusoidal input to determine the maximum peak-to-peak output of the device (the amplitude of the sinusoidal wave is increased until clipping occurs). The sinusoidal wave is then replaced with a square wave of the same amplitude. The frequency is then increased until the maximum peak-to-peak output can no longer be maintained (Figure 5). A square wave is used to allow a more accurate determination of the point at which the maximum peak-to-peak output is reached.

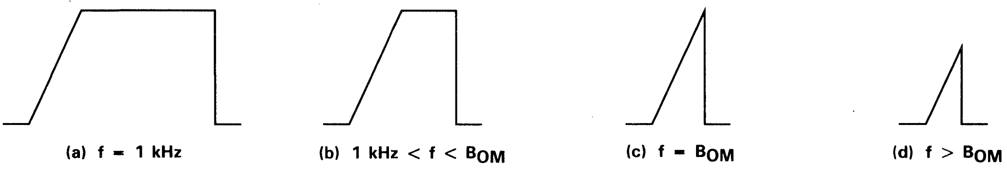

(a) f = 1 kHz (b) 1 kHz < f < B_{OM} (c) f = B_{OM} (d) f > B_{OM}

FIGURE 5. FULL-POWER-RESPONSE OUTPUT SIGNAL

test time

Inadequate test time is a frequent problem, especially when testing CMOS devices in a high-volume, short-test-time environment. Internal capacitances are inherently higher in CMOS than in bipolar and BiFET devices and require longer test times than their bipolar and BiFET counterparts. The problem becomes more pronounced with reduced supply levels and lower temperatures.

TYPICAL CHARACTERISTICS

DISTRIBUTION OF TLC27M4
INPUT OFFSET VOLTAGE

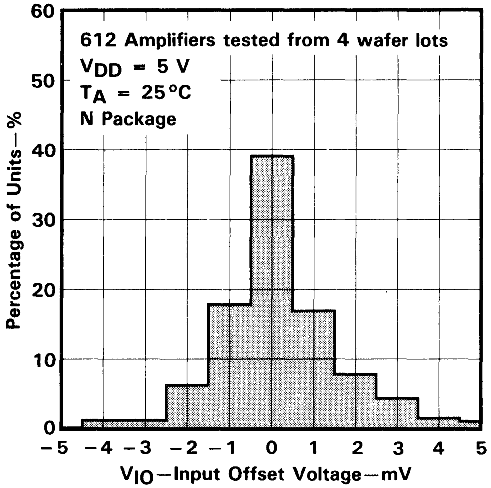


FIGURE 6

DISTRIBUTION OF TLC27M4
INPUT OFFSET VOLTAGE

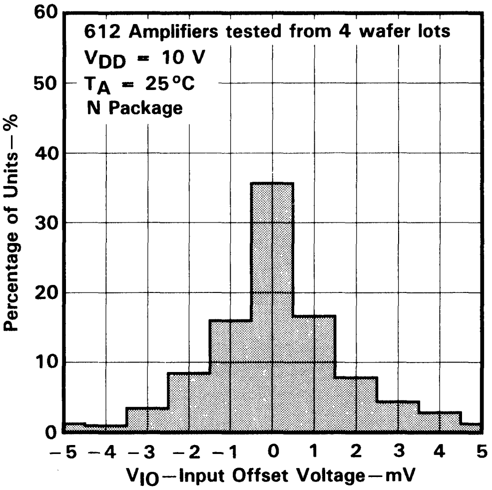


FIGURE 7

DISTRIBUTION OF TLC27M4 AND TLC27M9
INPUT OFFSET VOLTAGE
TEMPERATURE COEFFICIENT

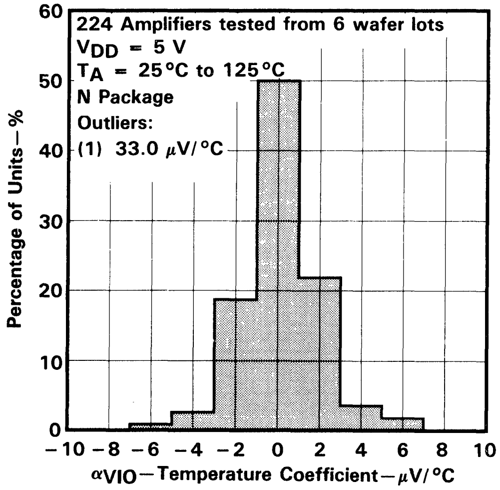


FIGURE 8

DISTRIBUTION OF TLC27M4 AND TLC27M9
INPUT OFFSET VOLTAGE
TEMPERATURE COEFFICIENT

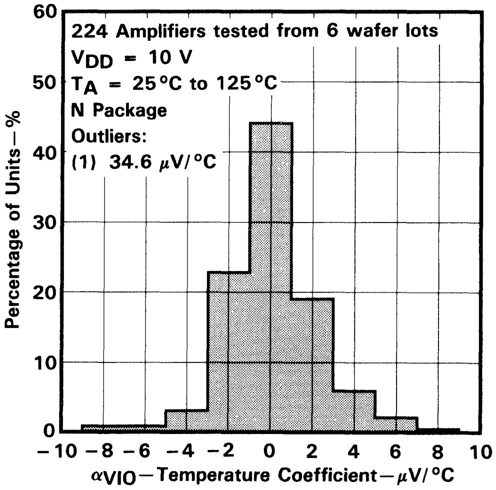


FIGURE 9

TYPICAL CHARACTERISTICS†

HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

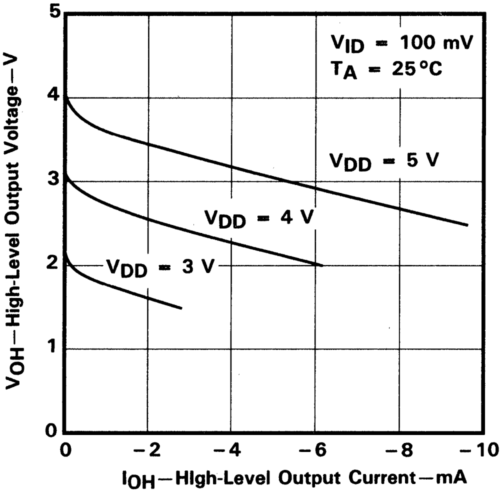


FIGURE 10

HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

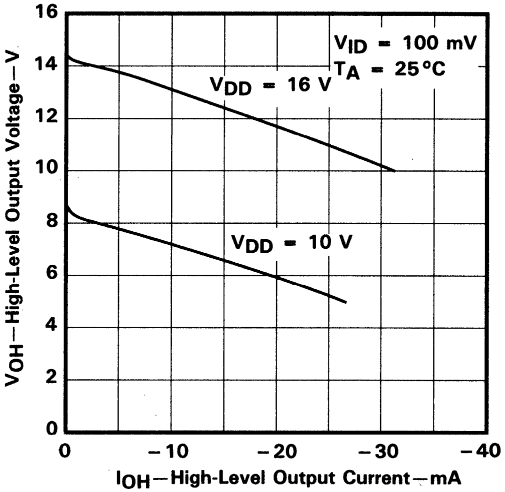


FIGURE 11

HIGH-LEVEL OUTPUT VOLTAGE
vs
SUPPLY VOLTAGE

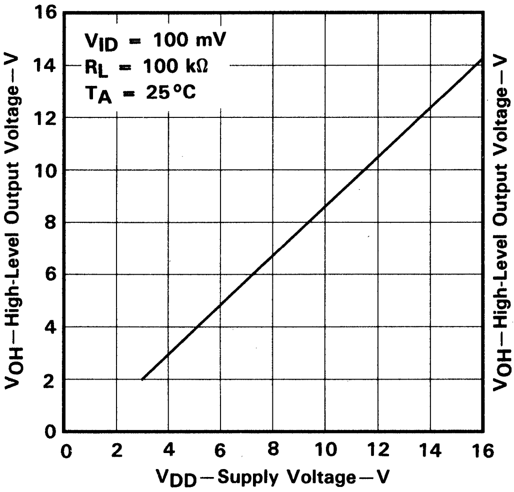


FIGURE 12

HIGH-LEVEL OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

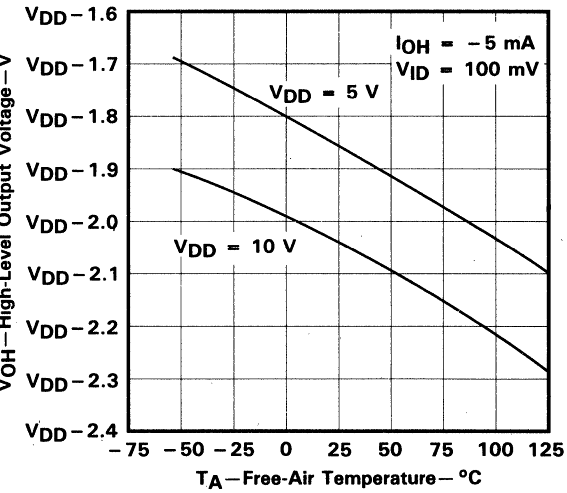


FIGURE 13

---

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

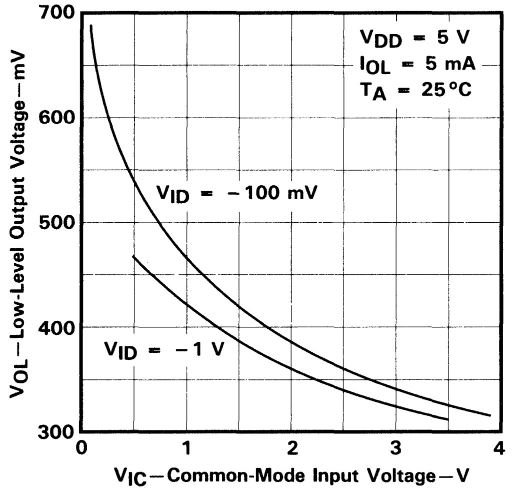

LOW-LEVEL OUTPUT VOLTAGE
vs
COMMON-MODE INPUT VOLTAGE

FIGURE 14

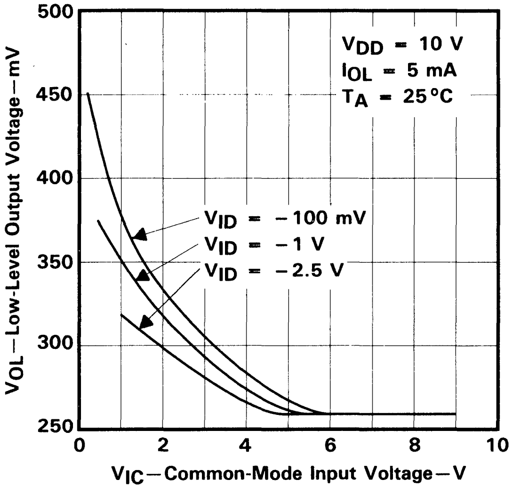

LOW-LEVEL OUTPUT VOLTAGE
vs
COMMON-MODE INPUT VOLTAGE

FIGURE 15

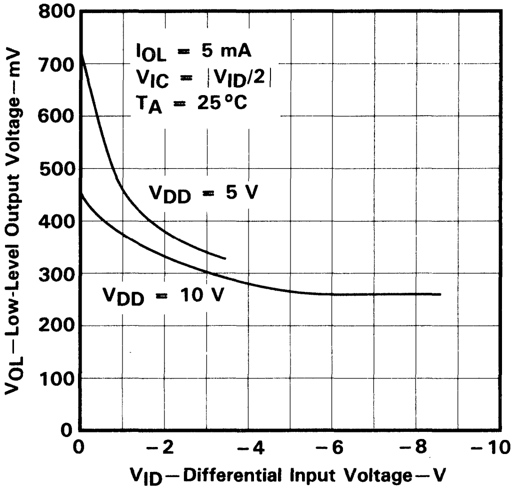

LOW-LEVEL OUTPUT VOLTAGE
vs
DIFFERENTIAL INPUT VOLTAGE

FIGURE 16

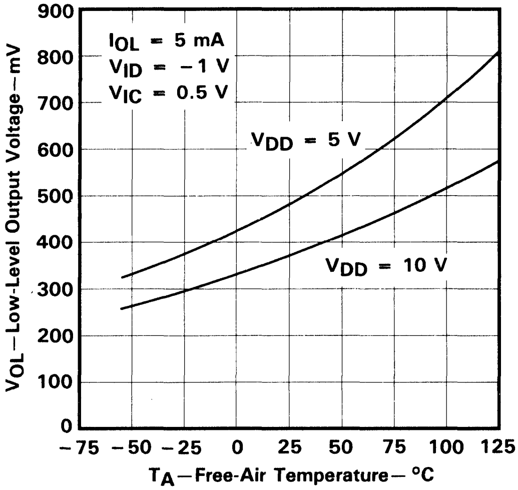

LOW-LEVEL OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

FIGURE 17

---

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

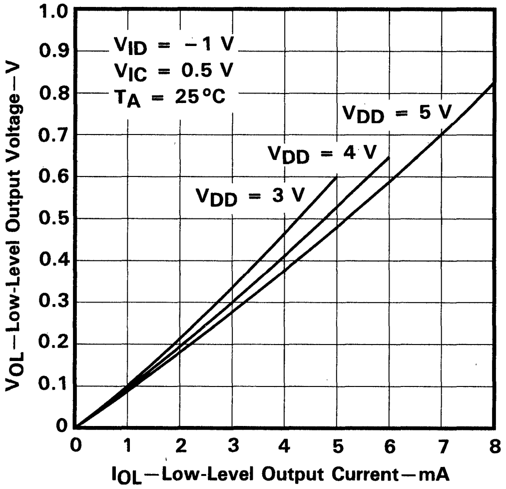


FIGURE 18

LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

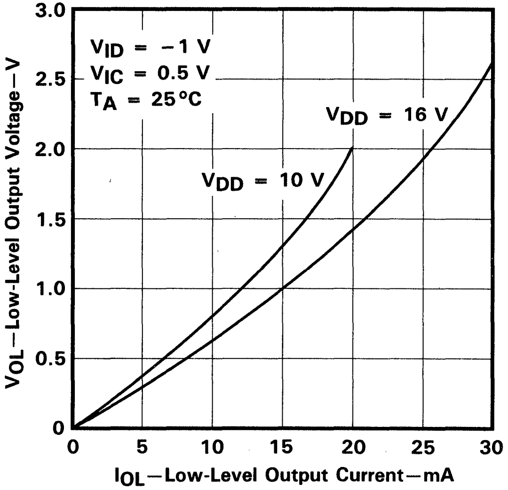


FIGURE 19

LARGE-SIGNAL
DIFFERENTIAL VOLTAGE AMPLIFICATION
vs
SUPPLY VOLTAGE

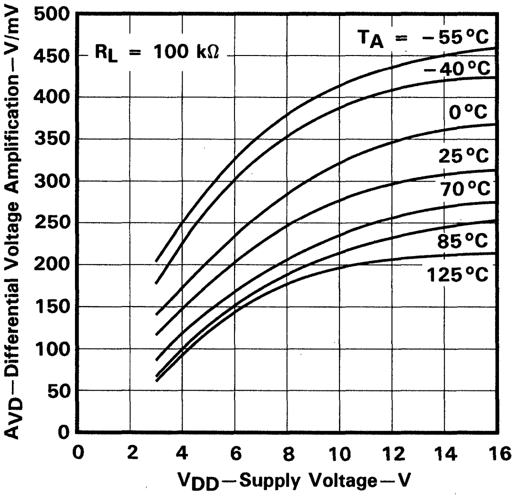


FIGURE 20

LARGE-SIGNAL
DIFFERENTIAL VOLTAGE AMPLIFICATION
vs
FREE-AIR TEMPERATURE

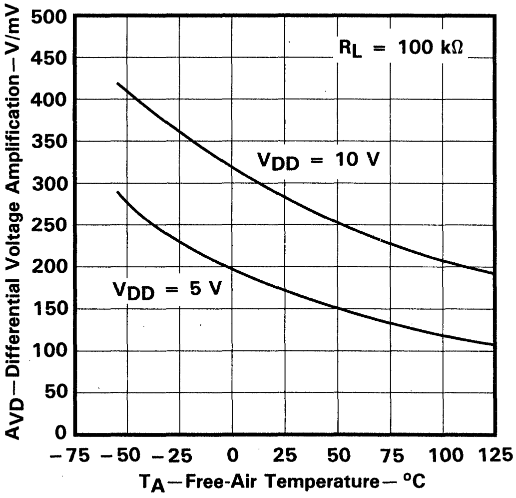


FIGURE 21

---

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

INPUT BIAS CURRENT AND INPUT OFFSET CURRENT
vs
FREE-AIR TEMPERATURE

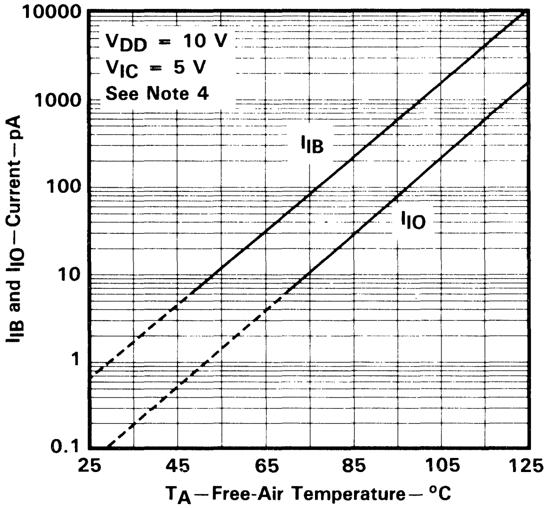


FIGURE 22

COMMON-MODE
INPUT VOLTAGE POSITIVE LIMIT
vs
SUPPLY VOLTAGE

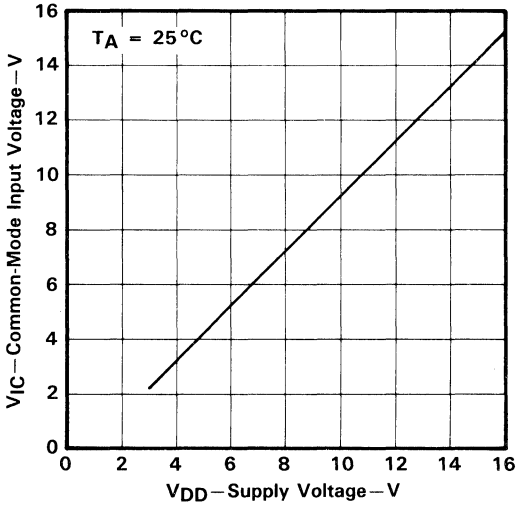


FIGURE 23

SUPPLY CURRENT
vs
SUPPLY VOLTAGE

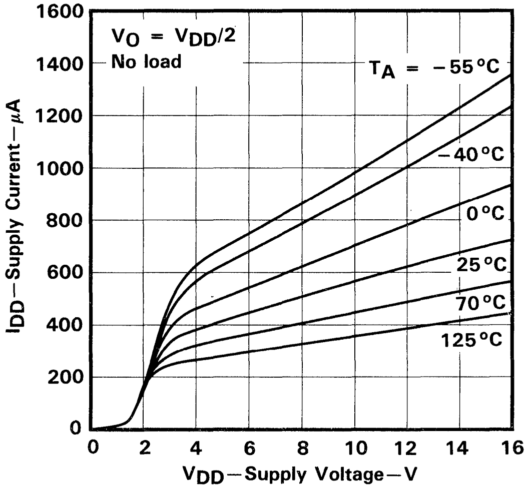


FIGURE 24

SUPPLY CURRENT
vs
FREE-AIR TEMPERATURE

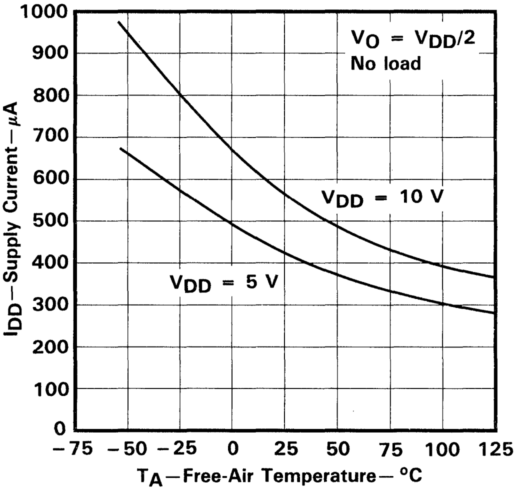


FIGURE 25

---

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

NOTE 4: The typical values of input bias current and input offset current below 5 pA were determined mathematically.

TYPICAL CHARACTERISTICS†

SLEW RATE
vs
SUPPLY VOLTAGE

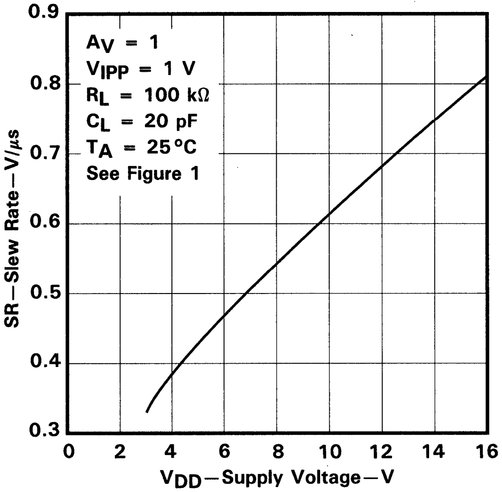


FIGURE 26

SLEW RATE
vs
FREE-AIR TEMPERATURE

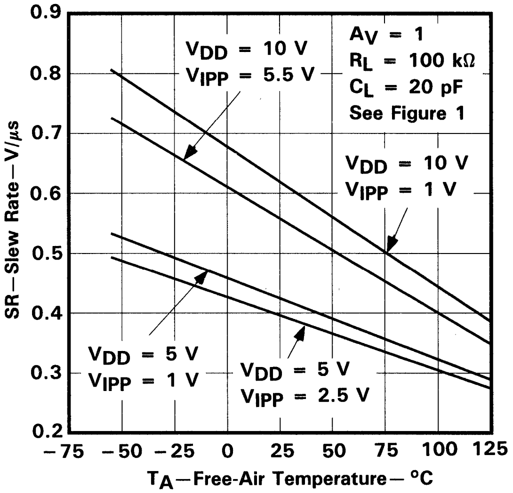


FIGURE 27

NORMALIZED SLEW RATE
vs
FREE-AIR TEMPERATURE

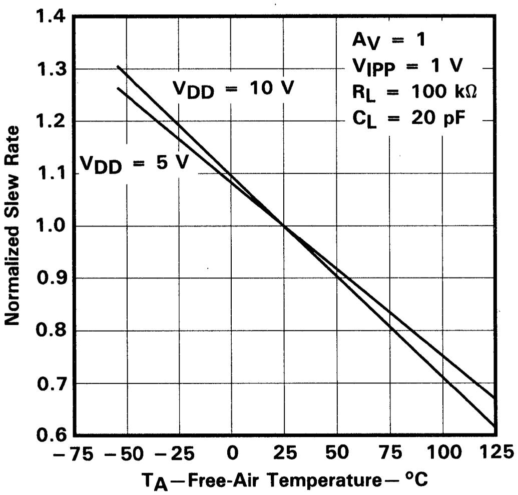


FIGURE 28

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE
vs
FREQUENCY

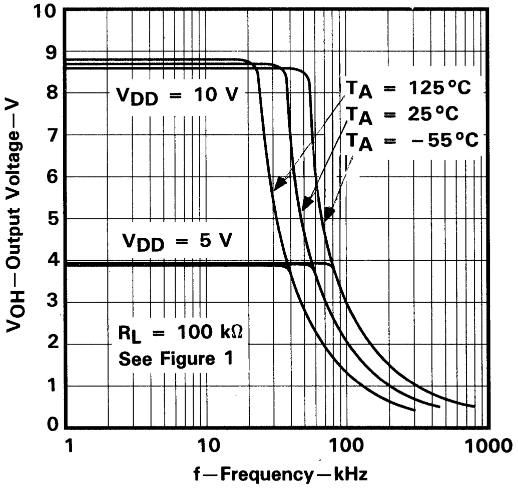


FIGURE 29

---

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

UNITY-GAIN BANDWIDTH
vs
FREE-AIR TEMPERATURE

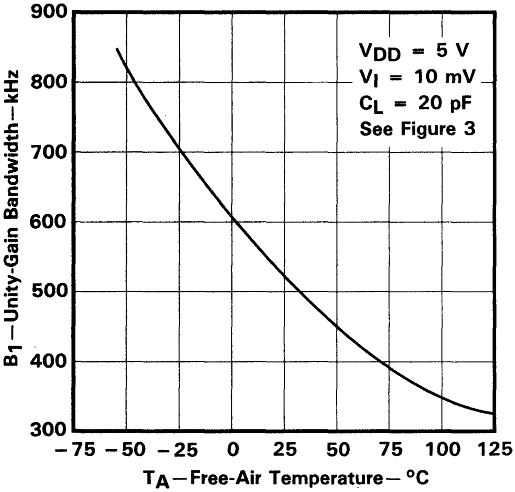


FIGURE 30

UNITY-GAIN BANDWIDTH
vs
SUPPLY VOLTAGE

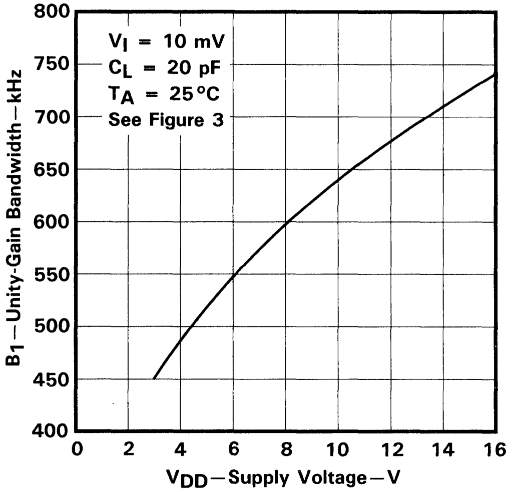


FIGURE 31

LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION AND PHASE SHIFT
vs
FREQUENCY

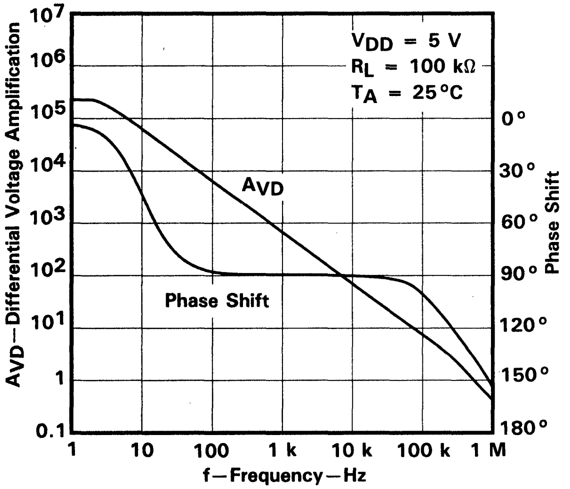


FIGURE 32

LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION AND PHASE SHIFT
vs
FREQUENCY

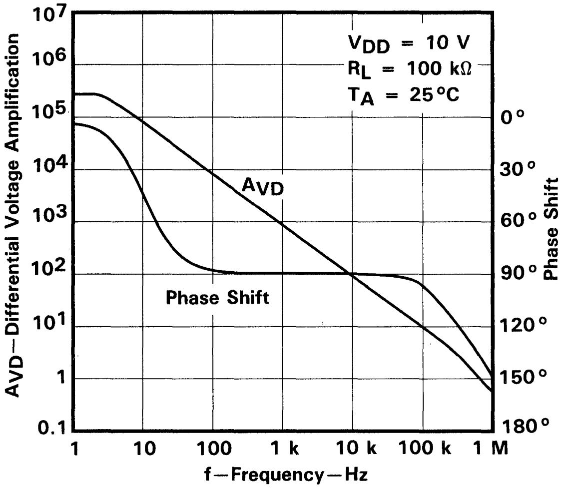


FIGURE 33

---

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

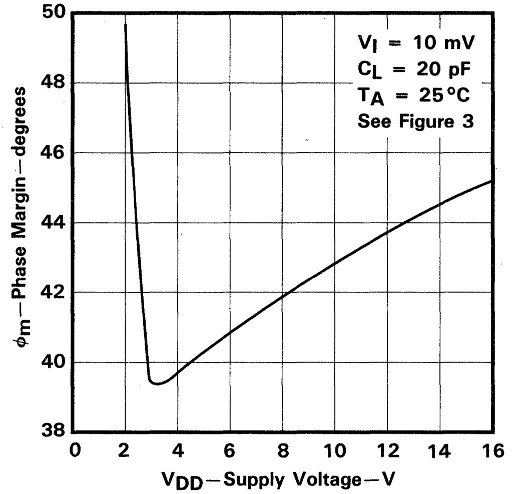

PHASE MARGIN
vs
SUPPLY VOLTAGE

FIGURE 34

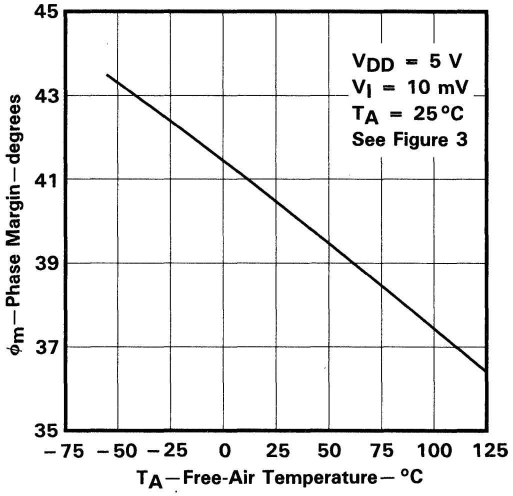

PHASE MARGIN
vs
FREE-AIR TEMPERATURE

FIGURE 35

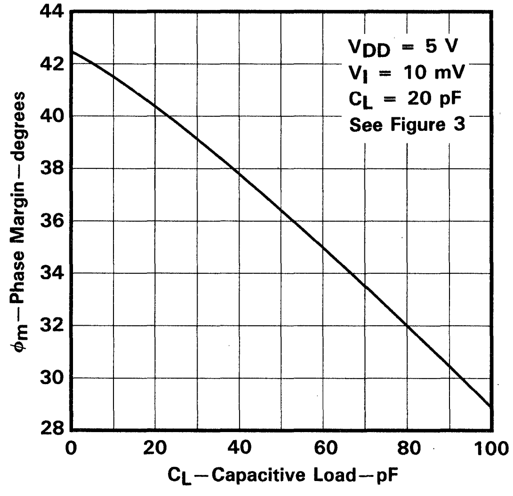

PHASE MARGIN
vs
CAPACITIVE LOAD

FIGURE 36

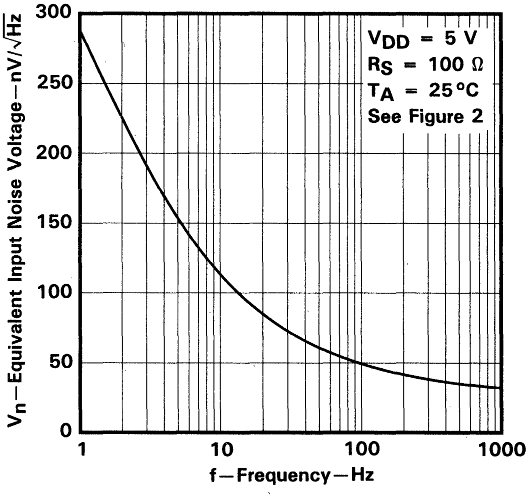

EQUIVALENT INPUT NOISE VOLTAGE
vs
FREQUENCY

FIGURE 37

---

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL APPLICATION DATA

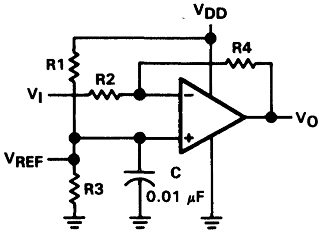
single-supply operation

While the TLC27M4 and TLC27M9 perform well using dual power supplies (also called balanced or split supplies), the design is optimized for single-supply operation. This design includes an input common-mode voltage range that encompasses ground as well as an output voltage range that pulls down to ground. The supply voltage range extends down to 3 V (C-suffix types), thus allowing operation with supply levels commonly available for TTL and HCMOS; however, for maximum dynamic range, 16-V single-supply operation is recommended.

Many single-supply applications require that a voltage be applied to one input to establish a reference level that is above ground. A resistive voltage divider is usually sufficient to establish this reference level (see Figure 38). The low input bias current of the TLC27M4 and TLC27M9 permits the use of very large resistive values to implement the voltage divider, thus minimizing power consumption.

The TLC27M4 and TLC27M9 work well in conjunction with digital logic; however, when powering both linear devices and digital logic from the same power supply, the following precautions are recommended:

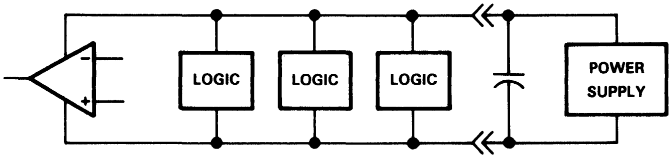
1. Power the linear devices from separate bypassed supply lines (see Figure 39); otherwise the linear device supply rails can fluctuate due to voltage drops caused by high switching currents in the digital logic.
2. Use proper bypass techniques to reduce the probability of noise-induced errors. Single capacitive decoupling is often adequate; however, high-frequency applications may require RC decoupling.



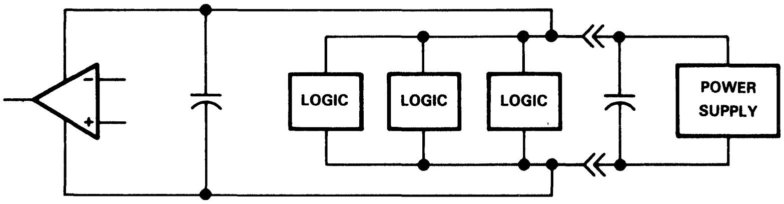
$$V_{REF} = V_{DD} \frac{R3}{R1 + R3}$$

$$V_O = \left(V_{REF} - V_I\right) \frac{R4}{R2} + V_{REF}$$

FIGURE 38. INVERTING AMPLIFIER WITH VOLTAGE REFERENCE



(a) Common Supply Rails



(b) Separate Bypassed Supply Rails (preferred)

FIGURE 39. COMMON VS SEPARATE SUPPLY RAILS

TYPICAL APPLICATION DATA

input characteristics

The TLC27M4 and TLC27M9 are specified with a minimum and a maximum input voltage that, if exceeded at either input, could cause the device to malfunction. Exceeding this specified range is a common problem, especially in single-supply operation. Note that the lower range limit includes the negative rail, while the upper range limit is specified at $V_{DD} - 1$ V at $T_A = 25°C$ and at $V_{DD} - 1.5$ V at all other temperatures.

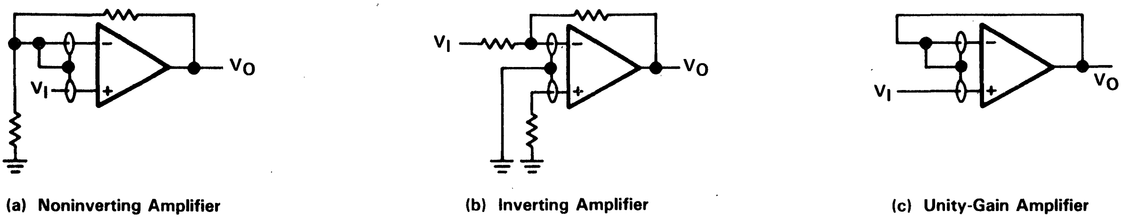
The use of the polysilicon-gate process and the careful input circuit design gives the TLC27M4 and TLC27M9 very good input offset voltage drift characteristics relative to conventional metal-gate processes. Offset voltage drift in CMOS devices is highly influenced by threshold voltage shifts caused by polarization of the phosphorus dopant implanted in the oxide. Placing the phosphorus dopant in a conductor (such as a polysilicon gate) alleviates the polarization problem, thus reducing threshold voltage shifts by more than an order of magnitude. The offset voltage drift with time has been calculated to be typically 0.1 μV/month, including the first month of operation.

Because of the extremely high input impedance and resulting low bias current requirements, the TLC27M4 and TLC27M9 are well suited for low-level signal processing; however, leakage currents on printed circuit boards and sockets can easily exceed bias current requirements and cause a degradation in device performance. It is good practice to include guard rings around inputs (similar to those of Figure 4 in the Parameter Measurement Information section). These guards should be driven from a low-impedance source at the same voltage level as the common-mode input (see Figure 40).

The inputs of any unused amplifiers should be tied to ground to avoid possible oscillation.

noise performance

The noise specifications in op amp circuits are greatly dependent on the current in the first-stage differential amplifier. The low input bias current requirements of the TLC27M4 and TLC27M9 result in a very low noise current, which is insignificant in most applications. This feature makes the devices especially favorable over bipolar devices when using values of circuit impedance greater than 50 kΩ, since bipolar devices exhibit greater noise currents.



(a) Noninverting Amplifier (b) Inverting Amplifier (c) Unity-Gain Amplifier

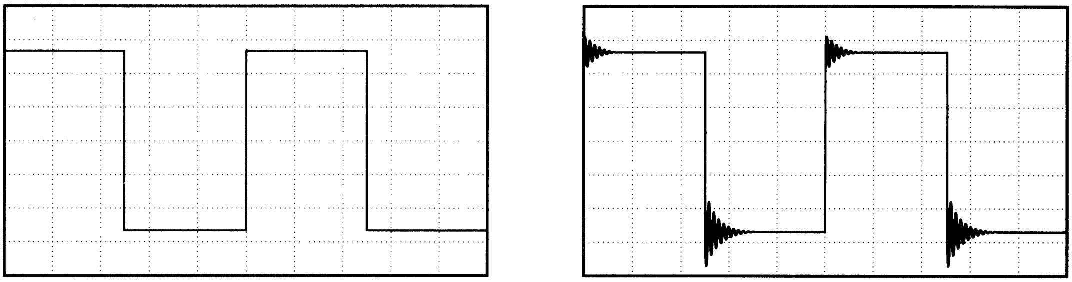
FIGURE 40. GUARD-RING SCHEMES

output characteristics

The output stage of the TLC27M4 and TLC27M9 is designed to sink and source relatively high amounts of current (see typical characteristics). If the output is subjected to a short-circuit condition, this high current capability can cause device damage under certain conditions. Output current capability increases with supply voltage.

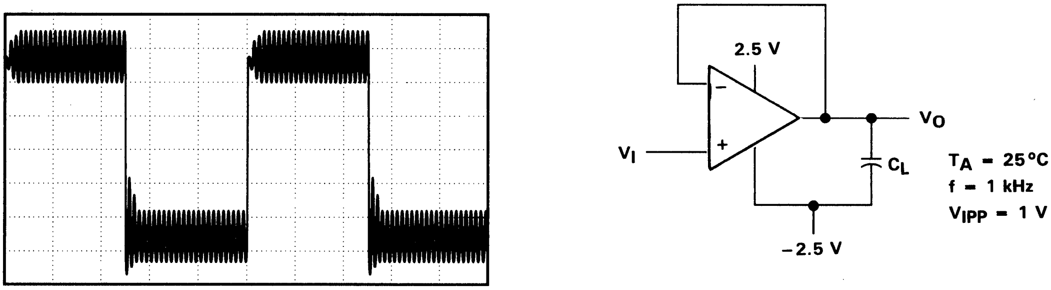
All operating characteristics of the TLC27M4 and TLC27M9 were measured using a 20-pF load. The devices will drive higher capacitive loads; however, as output load capacitance increases, the resulting response pole occurs at lower frequencies, thereby causing ringing, peaking, or even oscillation (see Figure 41). In many cases, adding a small amount of resistance in series with the load capacitance will alleviate the problem.

TYPICAL APPLICATION DATA



(a) C_L = 20 pF, R_L = No load

(b) C_L = 170 pF, R_L = No load



(c) C_L = 190 pF, R_L = No load

(d) Test Circuit

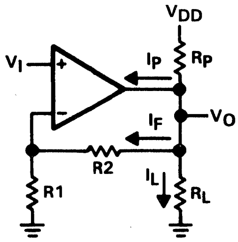
FIGURE 41. EFFECT OF CAPACITIVE LOADS AND TEST CIRCUIT

Although the TLC27M4 and TLC27M9 possess excellent high-level output voltage and current capability, methods for boosting this capability are available, if needed. The simplest method involves the use of a pullup resistor (R_P) connected from the output to the positive supply rail (see Figure 42). There are two disadvantages to the use of this circuit. First, the NMOS pulldown transistor N4 (see equivalent schematic) must sink a comparatively large amount of current. In this circuit, N4 behaves like a linear resistor with an on-resistance between approximately 60 Ω and 180 Ω, depending on how hard the op amp input is driven. With very low values of R_P, a voltage offset from 0 V at the output will occur. Second, pullup resistor R_P acts as a drain load to N4 and the gain of the op amp is reduced at output voltage levels where N5 is not supplying the output current.

feedback

Op amp circuits nearly always employ feedback, and since feedback is the first prerequisite for oscillation, some caution is appropriate. Most oscillation problems result from driving capacitive loads (discussed previously) and ignoring stray input capacitance. A small-value capacitor connected in parallel with the feedback resistor is an effective remedy (see Figure 43). The value of this capacitor is optimized empirically.

TYPICAL APPLICATION DATA



$$R_R = \frac{V_{DD} - V_O}{I_F + I_L + I_P}$$

I_P = Pullup current required by the op amp (typically 500 μA)

FIGURE 42. RESISTIVE PULLUP TO INCREASE V_{OH}

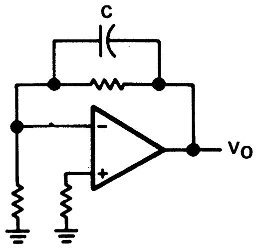


FIGURE 43. COMPENSATION FOR INPUT CAPACITANCE

electrostatic discharge protection

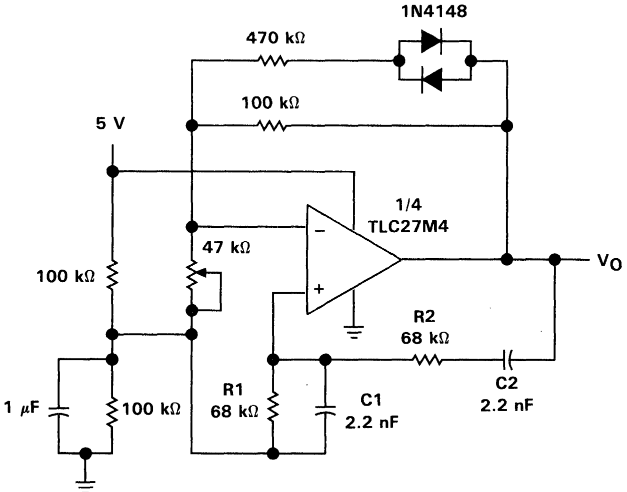
The TLC27M4 and TLC27M9 incorporate an internal electrostatic discharge (ESD) protection circuit that prevents functional failures at voltages up to 2000 V as tested under MIL-STD-883C, Method 3015.2. Care should be exercised, however, when handling these devices as exposure to ESD may result in the degradation of the device parametric performance. The protection circuit also causes the input bias currents to be temperature dependent and have the characteristics of a reverse-biased diode.

latch-up

Because CMOS devices are susceptible to latch-up due to their inherent parasitic thyristors, the TLC27M4 and TLC27M9 inputs and outputs were designed to withstand −100-mA surge currents without sustaining latch-up; however, techniques should be used to reduce the chance of latch-up whenever possible. Internal protection diodes should not, by design, be forward biased. Applied input and output voltage should not exceed the supply voltage by more than 300 mV. Care should be exercised when using capacitive coupling on pulse generators. Supply transients should be shunted by the use of decoupling capacitors (0.1 μF typical) located across the supply rails as close to the device as possible.

The current path established if latch-up occurs is usually between the positive supply rail and ground and can be triggered by surges on the supply lines and/or voltages on either the output or inputs that exceed the supply voltage. Once latch-up occurs, the current flow is limited only by the impedance of the power supply and the forward resistance of the parasitic thyristor and usually results in the destruction of the device. The chance of latch-up occurring increases with increasing temperature and supply voltages.

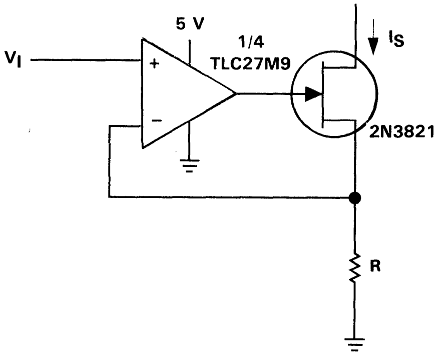
TYPICAL APPLICATION DATA



NOTES: $V_{OPP} \approx 2$ V

$$f_O = \frac{1}{2\pi\sqrt{R1R2C1C2}}$$

FIGURE 44. WIEN OSCILLATOR

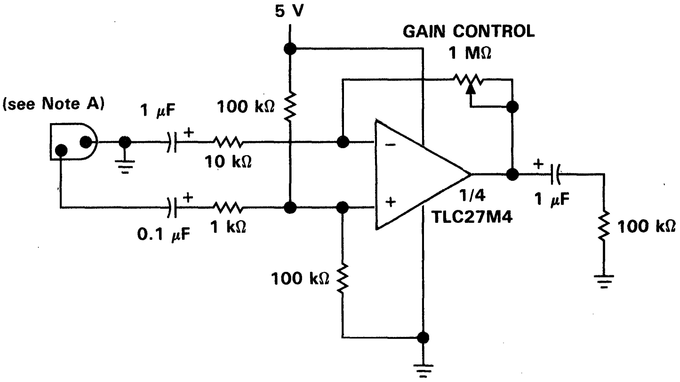


NOTES: V_I = 0 V to 3 V

$$I_S = \frac{V_I}{R}$$

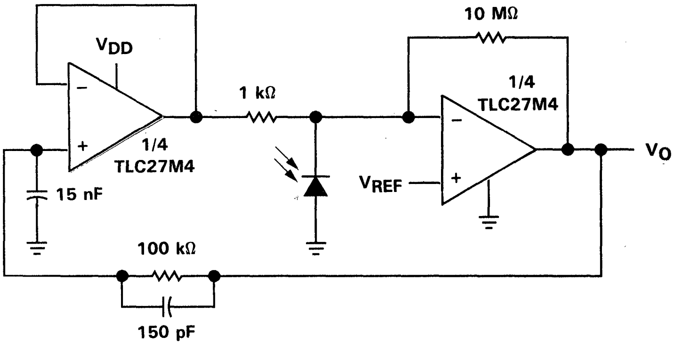
FIGURE 45. PRECISION LOW-CURRENT SINK

TYPICAL APPLICATION DATA



NOTE A: Low to medium impedance dynamic mike.

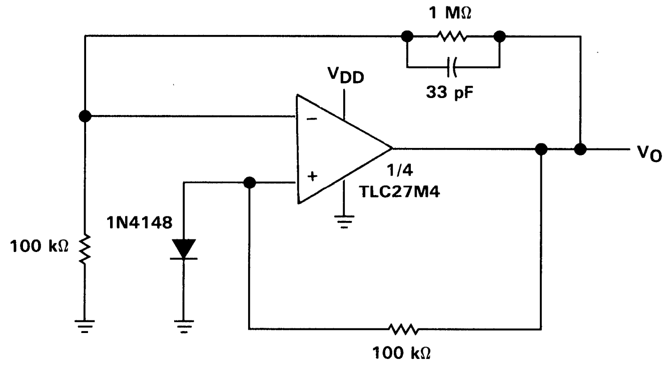
FIGURE 46. MICROPHONE PREAMPLIFIER



NOTES: V_{DD} = 4 V to 15 V
V_{REF} = 0 V to $V_{DD}-2$ V

FIGURE 47. PHOTO DIODE AMPLIFIER WITH AMBIENT LIGHT REJECTION

TYPICAL APPLICATION DATA



NOTES: V_{DD} = 8 V to 16 V
V_O = 5 V, 10 mA

FIGURE 48. 5-V LOW-POWER VOLTAGE REGULATOR

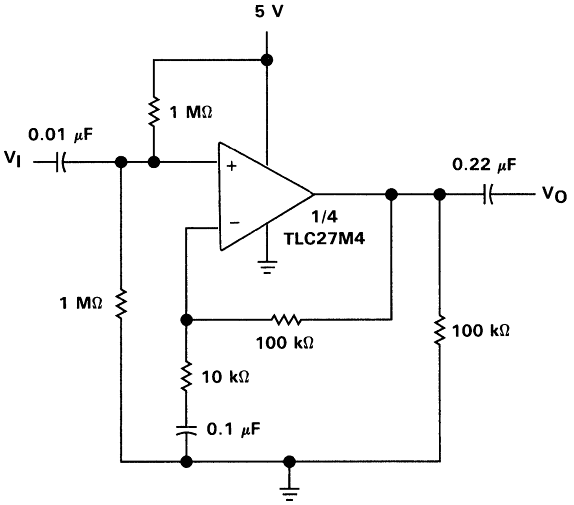


FIGURE 49. SINGLE-RAIL AC AMPLIFIER

TLC1078
LinCMOS™ μPOWER PRECISION DUAL OPERATIONAL AMPLIFIER

D3146, AUGUST 1988–REVISED JANUARY 1991

- **Power Dissipation as Low as 10 μW Typ per Amplifier**
- **Operates on a Single Silver-Oxide Watch Battery, $V_{DD} = 1.4$ V Min**
- **V_{IO} . . . 450 μV Max in DIP and Small-Outline Package**
- **Input Offset Voltage Drift . . . 0.1 μV/Month Typ, Including the First 30 Days**
- **High-Impedance LinCMOS™ Inputs $I_{IB} = 0.6$ pA Typ**
- **High Open-Loop Gain . . . 800,000 Typ**
- **Output Drive Capability > 20 mA**
- **Slew Rate . . . 47 V/ms Typ**
- **Common-Mode Input Voltage Range Extends Below the Negative Rail**
- **Output Voltage Range Includes Negative Rail**
- **On-Chip ESD-Protection Circuitry**
- **Small-Outline Package Option Also Available in Tape and Reel**

description

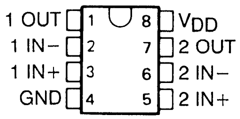
The TLC1078 operational amplifier offers ultra-low offset voltage, high gain, 110-kHz bandwidth, 47-V/ms slew rate, and just 150-μW power dissipation per amplifier.

With a supply voltage of 1.4 V, common-mode input to the negative rail, and output swing to the negative rail, the TLC1078C is an ideal solution for low-voltage battery-operated systems. The 20-mA output drive capability means that the TLC1078 can easily drive small resistive and large capacitive loads when needed, while maintaining ultra-low standby power dissipation.

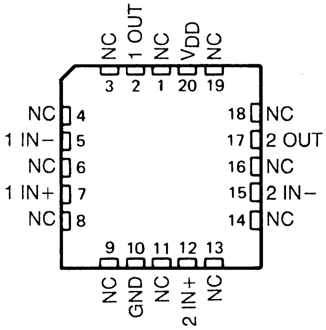
Since this device is functionally compatible as well as pin compatible with the TLC27L2 and TLC27L7, the TLC1078 easily upgrades existing designs that can benefit from its improved performance.

The TLC1078 incorporates internal ESD-protection circuits that will prevent functional failures at voltages up to 2000 V as tested under MIL-STD-883C, Method 3015.2; however, care

D, JG, OR P PACKAGE
(TOP VIEW)

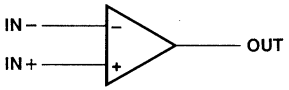


FK PACKAGE
(TOP VIEW)

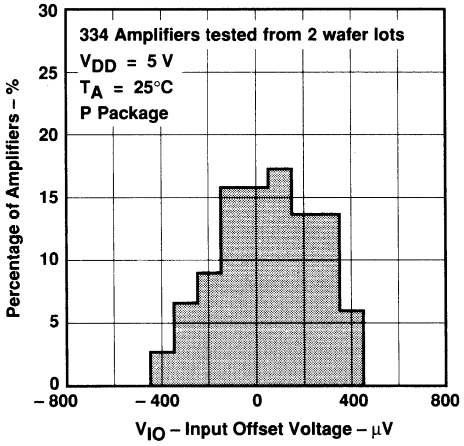


NC—No internal connection

symbol (each amplifier)



DISTRIBUTION OF TLC1078
INPUT OFFSET VOLTAGE



LinCMOS is a trademark of Texas Instruments Incorporated.

description (continued)

should be exercised when handling these devices as exposure to ESD may result in degradation of the device parametric performance. The TLC1078 design also inhibits latchup of the device inputs and outputs even with surge currents as large as 100 mA.

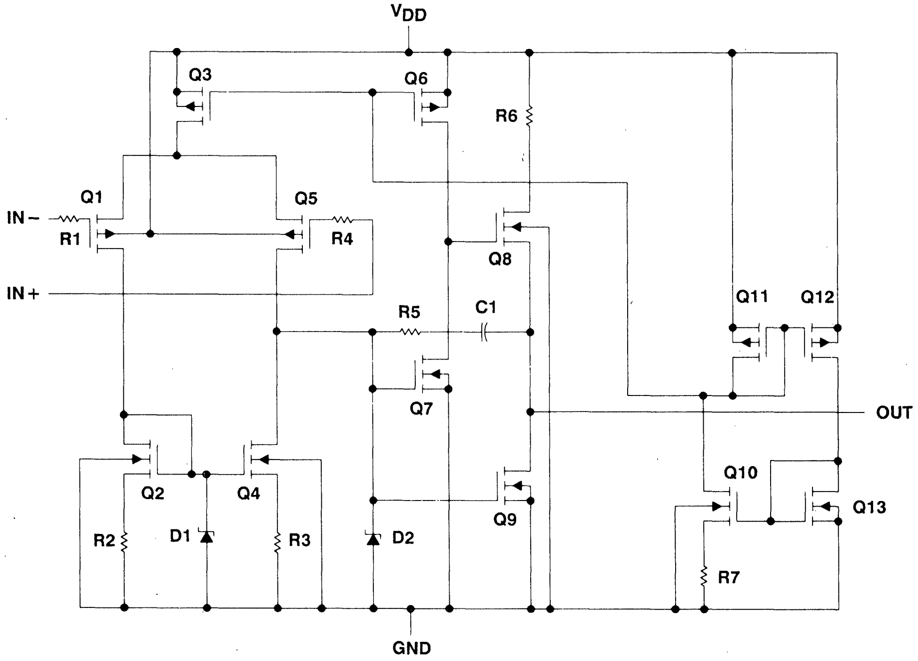
The C- suffix devices are characterized for operation from 0°C to 70°C. The I- suffix devices are characterized for operation from − 40°C to 85°C. The M- suffix devices are characterized for operation over the full military temperature range of − 55°C to 125°C. The wide range of packaging options includes small-outline and chip-carrier versions for high-density system applications.

AVAILABLE OPTIONS

T_A	PACKAGE			
	SMALL OUTLINE (D)	CHIP CARRIER (FK)	CERAMIC DIP (JG)	PLASTIC DIP (P)
0°C to 70°C	TLC1078CD	—	—	TLC1078CP
−40°C to 85°C	TLC1078ID	—	—	TLC1078IP
−55°C to 125°C	TLC1078MD	TLC1078MFK	TLC1078MJG	TLC1078MP

The D package is available taped and reeled. Add the suffix R to the device type (e.g., TLC1078CDR).

equivalent schematic (each amplifier)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{DD} (see Note 1)	18 V
Differential input voltage (see Note 2)	$\pm V_{DD}$
Input voltage range, V_I (any input)	-0.3 V to V_{DD}
Input current, I_I (each input)	± 5 mA
Output current, I_O (each output)	± 30 mA
Total current into V_{DD} terminal (see Note 3)	45 mA
Duration of short-circuit at (or below) 25°C (see Note 3)	Unlimited
Continuous total dissipation	see Dissipation Rating Table
Operating free-air temperature range, T_A: C-suffix	0°C to 70°C
I-suffix	− 40°C to 85°C
M-suffix	− 55°C to 125°C
Storage temperature range	− 65°C to 150°C
Case temperature for 60 seconds: FK package	260°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D or P package	260°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: JG package	300°C

NOTES: 1. All voltage values, except differential voltages, are with respect to network ground.
2. Differential voltages are at the noninverting input with respect to the inverting input.
3. The output may be shorted to either supply. Temperature and/or supply voltages must be limited to ensure that the maximum dissipation ratings are not exceeded.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING	$T_A = 125°C$ POWER RATING
D	725 mW	5.8 mW/°C	464 mW	377 mW	145 mW
FK	1375 mW	11 mW/°C	880 mW	715 mW	275 mW
JG	1050 mW	8.4 mW/°C	672 mW	546 mW	210 mW
P	1000 mW	8.0 mW/°C	640 mW	520 mW	200 mW

recommended operating conditions

		C-SUFFIX			I-SUFFIX			M-SUFFIX			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{DD}		1.4		16	3		16	4		16	V
Common-mode input voltage, V_{IC}	$V_{DD} = 5$ V	− 0.2		4	− 0.2		4	0		4	V
	$V_{DD} = 10$ V	− 0.2		9	− 0.2		9	0		9	
Operating free-air temperature, T_A		0		70	− 40		85	− 55		125	°C

electrical characteristics over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		V_{DD} = 5 V			V_{DD} = 10 V			UNIT
			T_A	MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_O = 1.4 V, V_{IC} = 0, R_S = 50 Ω, R_I = 1 MΩ	25°C		160	450		180	600	μV
			Full range			800			950	
α_{VIO}	Temperature coefficient of input offset voltage		25°C to 70°C		1.1			1		μV/°C
I_{IO}	Input offset current (see Note 4)	V_O = V_{DD}/ 2, V_{IC} = V_{DD}/ 2	25°C		0.1			0.1		pA
			70°C		7	300		7	300	
I_{IB}	Input bias current (see Note 4)		25°C		0.6			0.7		pA
			70°C		40	600		50	600	
V_{ICR}	Common-mode input voltage range (see Note 5)		25°C	−0.2 to 4	−0.3 to 4.2		−0.2 to 9	−0.3 to 9.2		V
			Full range	−0.2 to 3.5			−0.2 to 8.5			V
V_{OH}	High-level output voltage	V_{ID} = 100 mV, R_L = 1 MΩ	25°C	3.2	4.1		8.2	8.9		V
			0°C	3.2	4.1		8.2	8.9		
			70°C	3.2	4.2		8.2	8.9		
V_{OL}	Low-level output voltage	V_{ID} = −100 mV, I_{OL} = 0	25°C		0	25		0	25	mV
			0°C		0	25		0	25	
			70°C		0	25		0	25	
A_{VD}	Large-signal differential voltage amplification	R_L = 1 MΩ, See Note 6	25°C	250	525		500	850		V/mV
			0°C	250	680		500	1010		
			70°C	200	380		350	660		
CMRR	Common-mode rejection ratio	V_{IC} = V_{ICR} min	25°C	70	95		75	97		dB
			0°C	70	95		75	97		
			70°C	70	95		75	97		
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)	V_{DD} = 5 V to 10 V, V_O = 1.4 V	25°C	75	98		75	98		dB
			0°C	75	98		75	98		
			70°C	75	98		75	98		
I_{DD}	Supply current (two amplifiers)	V_O = V_{DD}/ 2, V_{IC} = V_{DD}/ 2, No load	25°C		20	34		29	46	μA
			0°C		24	42		36	66	
			70°C		16	28		22	40	

NOTES: 4. The typical values of input bias current and input offset current below 5 pA were determined mathematically.
5. This range also applies to each input individually.
6. At V_{DD} = 5 V, V_O = 0.25 V to 2 V; at V_{DD} = 10 V, V_O = 1 V to 6 V.

operating characteristics

PARAMETER		TEST CONDITIONS		V_{DD} = 5 V			V_{DD} = 10 V			UNIT
			T_A	MIN	TYP	MAX	MIN	TYP	MAX	
SR	Slew rate at unity gain	R_L = 1 MΩ, C_L = 20 pF, V_{IPP} = 1 V, See Figure 1	25°C		32			47		V/ms
			0°C		35			51		
			70°C		27			38		
V_n	Equivalent input noise voltage	f = 1 kHz, R_S = 100 Ω	25°C		68			68		nv/√Hz
B_1	Unity-gain bandwidth	C_L = 20 pF, See Figure 2	25°C		85			110		kHz
			0°C		100			125		
			70°C		65			90		
ϕ_m	Phase margin at unity gain	C_L = 20 pF, See Figure 2	25°C		34°			38°		
			0°C		36°			40°		
			70°C		30°			34°		

electrical characteristics over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		V_{DD} = 5 V			V_{DD} = 10 V			UNIT
			T_A	MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_O = 1.4 V, V_{IC} = 0, R_S = 50 Ω, R_I = 1 MΩ	25°C		160	450		180	600	μV
			Full range			950			1100	
α_{VIO}	Temperature coefficient of input offset voltage		25°C to 85°C		1.1			1		μV/°C
I_{IO}	Input offset current (see Note 4)	V_O = V_{DD}/ 2, V_{IC} = V_{DD}/ 2	25°C		0.1			0.1		pA
			85°C		24	1000		26	1000	
I_{IB}	Input bias current (see Note 4)		25°C		0.6			0.7		pA
			85°C		200	2000		220	2000	
V_{ICR}	Common-mode input voltage range (see Note 5)		25°C	−0.2 to 4	−0.3 to 4.2		−0.2 to 9	−0.3 to 9.2		V
			Full range	−0.2 to 3.5			−0.2 to 8.5			V
V_{OH}	High-level output voltage	V_{ID} = 100 mV, R_L = 1 MΩ	25°C	3.2	4.1		8.2	8.9		V
			−40°C	3.2	4.1		8.2	8.9		
			85°C	3.2	4.2		8.2	8.9		
V_{OL}	Low-level output voltage	V_{ID} = −100 mV, I_{OL} = 0	25°C		0	25		0	25	mV
			−40°C		0	25		0	25	
			85°C		0	25		0	25	
A_{VD}	Large-signal differential voltage amplification	R_L = 1 MΩ, See Note 6	25°C	250	525		500	850		V/mV
			−40°C	250	900		500	1550		
			85°C	150	300		250	585		
CMRR	Common-mode rejection ratio	V_{IC} = V_{ICR} min	25°C	70	95		75	97		dB
			−40°C	70	95		75	97		
			85°C	70	95		75	97		
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)	V_{DD} = 5 V to 10 V, V_O = 1.4 V	25°C	75	98		75	98		dB
			−40°C	75	98		75	98		
			85°C	75	98		75	98		
I_{DD}	Supply current (two amplifiers)	V_O = V_{DD}/ 2, V_{IC} = V_{DD}/ 2, No load	25°C		20	34		29	46	μA
			−40°C		31	54		50	86	
			85°C		15	26		20	36	

NOTES: 4. The typical values of input bias current and input offset current below 5 pA were determined mathematically.
5. This range also applies to each input individually.
6. At V_{DD} = 5 V, V_O = 0.25 V to 2 V; at V_{DD} = 10 V, V_O = 1 V to 6 V.

operating characteristics

PARAMETER		TEST CONDITIONS		V_{DD} = 5 V			V_{DD} = 10 V			UNIT
			T_A	MIN	TYP	MAX	MIN	TYP	MAX	
SR	Slew rate at unity gain	R_L = 1 MΩ, C_L = 20 pF, V_{IPP} = 1 V, See Figure 1	25°C		32			47		V/ms
			−40°C		39			59		
			85°C		25			34		
V_n	Equivalent input noise voltage	f = 1 kHz, R_S = 100 Ω	25°C		68			68		nv/$\sqrt{Hz}$
B_1	Unity-gain bandwidth	C_L = 20 pF, See Figure 2	25°C		85			110		kHz
			−40°C		130			155		
			85°C		55			80		
ϕ_m	Phase margin at unity gain	C_L = 20 pF, See Figure 2	25°C		34°			38°		
			−40°C		38°			42°		
			85°C		28°			32°		

electrical characteristics over operating free-air temperature range (unless otherwise noted)

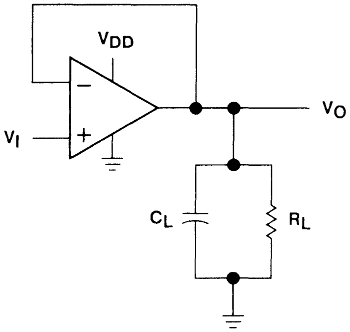
PARAMETER		TEST CONDITIONS		V_{DD} = 5 V			V_{DD} = 10 V			UNIT
			T_A	MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	$V_O = 1.4$ V, $V_{IC} = 0$, $R_S = 50\ \Omega$, $R_I = 1\ \text{M}\Omega$	25°C		160	450		180	600	µV
			Full range			1250			1400	
α_{VIO}	Temperature coefficient of input offset voltage		25°C to 125°C		1.4			1.4		µV/°C
I_{IO}	Input offset current (see Note 4)	$V_O = V_{DD}/2$, $V_{IC} = V_{DD}/2$	25°C		0.1			0.1		pA
			125°C		1.4	15		1.8	15	nA
I_{IB}	Input bias current (see Note 4)		25°C		0.6			0.7		pA
			125°C		9	35		10	35	nA
V_{ICR}	Common-mode input voltage range (see Note 5)		25°C	0 to 4	−0.3 to 4.2		0 to 9	−0.3 to 9.2		V
			Full range	0 to 3.5			0 to 8.5			V
V_{OH}	High-level output voltage	$V_{ID} = 100$ mV, $R_L = 1\ \text{M}\Omega$	25°C	3.2	4.1		8.2	8.9		V
			−55°C	3.2	4.1		8.2	8.8		
			125°C	3.2	4.2		8.2	9		
V_{OL}	Low-level output voltage	$V_{ID} = -100$ mV, $I_{OL} = 0$	25°C		0	25		0	25	mV
			−55°C		0	25		0	25	
			125°C		0	25		0	25	
A_{VD}	Large-signal differential voltage amplification	$R_L = 1\ \text{M}\Omega$, See Note 6	25°C	250	525		500	850		V/mV
			−55°C	250	950		500	1750		
			125°C	75	200		150	380		
CMRR	Common-mode rejection ratio	$V_{IC} = V_{ICR}$ min	25°C	70	95		75	97		dB
			−55°C	70	95		75	97		
			125°C	70	85		75	91		
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)	$V_{DD} = 5$ V to 10 V, $V_O = 1.4$ V	25°C	75	98		75	98		dB
			−55°C	70	98		70	98		
			125°C	70	98		70	98		
I_{DD}	Supply current (two amplifiers)	$V_O = V_{DD}/2$, $V_{IC} = V_{DD}/2$, No load	25°C		20	34		29	46	µA
			−55°C		35	60		56	96	
			125°C		14	24		18	30	

NOTES: 4. The typical values of input bias current and input offset current below 5 pA were determined mathematically.
5. This range also applies to each input individually.
6. At $V_{DD} = 5$ V, $V_O = 0.25$ V to 2 V; at $V_{DD} = 10$ V, $V_O = 1$ V to 6 V.

operating characteristics

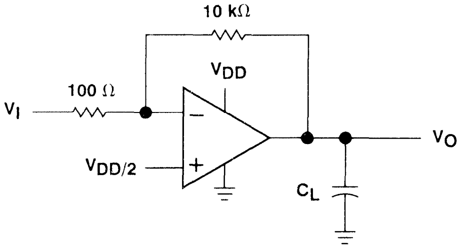
PARAMETER		TEST CONDITIONS		V_{DD} = 5 V			V_{DD} = 10 V			UNIT
			T_A	MIN	TYP	MAX	MIN	TYP	MAX	
SR	Slew rate at unity gain	$R_L = 1\ \text{M}\Omega$, $C_L = 20$ pF, $V_{IPP} = 1$ V, See Figure 1	25°C		32			47		V/ms
			−55°C		41			63		
			125°C		20			27		
V_n	Equivalent input noise voltage	f = 1 kHz, $R_S = 100\ \Omega$	25°C		68			68		nV/√Hz
B_1	Unity-gain bandwidth	$C_L = 20$ pF, See Figure 2	25°C		85			110		kHz
			−55°C		140			165		
			125°C		45			70		
ϕ_m	Phase margin at unity gain	$C_L = 20$ pF, See Figure 2	25°C		34°			38°		
			−55°C		39°			43°		
			125°C		25°			29°		

PARAMETER MEASUREMENT INFORMATION



CL includes fixture capacitance.

FIGURE 1. SLEW RATE TEST CIRCUIT



CL includes fixture capacitance.

FIGURE 2. UNITY-GAIN BANDWIDTH AND PHASE MARGIN TEST CIRCUIT

TYPICAL CHARACTERISTICS

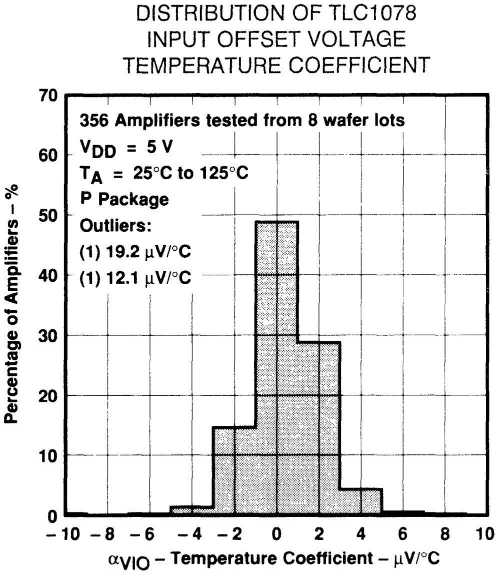


FIGURE 3

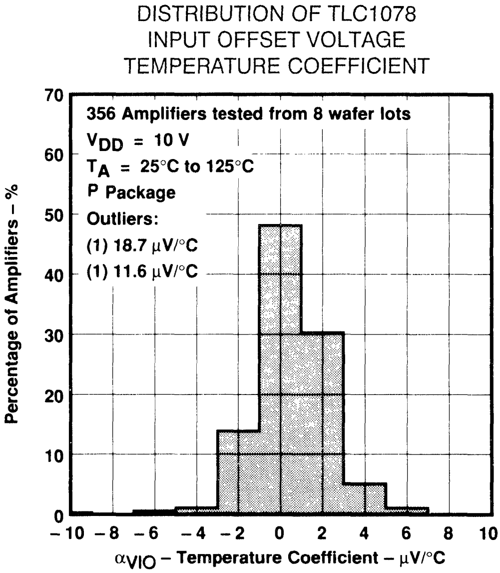
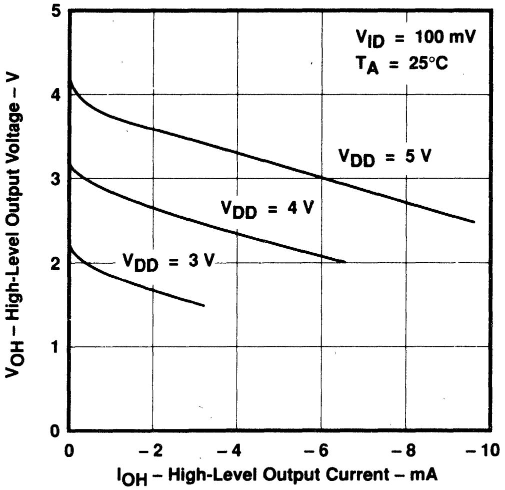


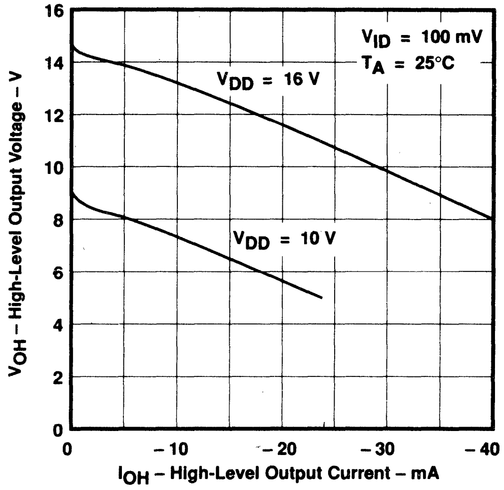
FIGURE 4

TYPICAL CHARACTERISTICS†



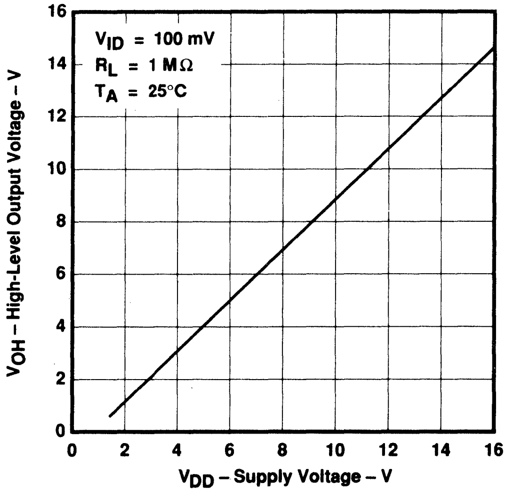
HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

FIGURE 5



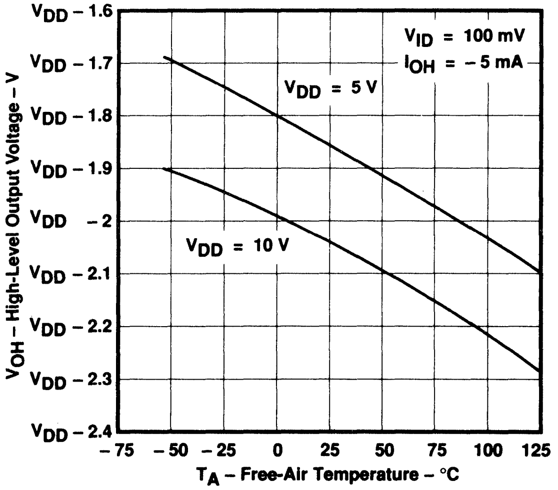
HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

FIGURE 6



HIGH-LEVEL OUTPUT VOLTAGE
vs
SUPPLY VOLTAGE

FIGURE 7



HIGH-LEVEL OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

FIGURE 8

---

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

LOW-LEVEL OUTPUT VOLTAGE
vs
COMMON-MODE INPUT VOLTAGE

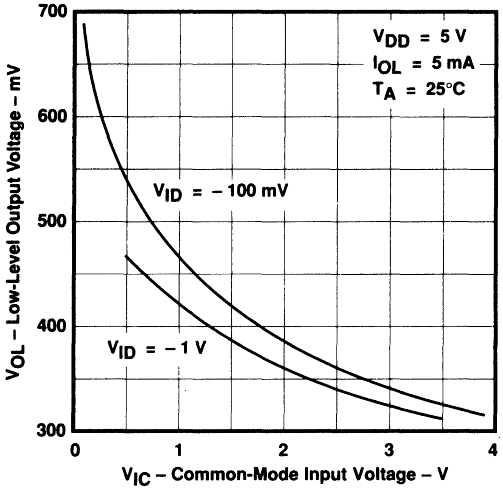


FIGURE 9

LOW-LEVEL OUTPUT VOLTAGE
vs
COMMON-MODE INPUT VOLTAGE

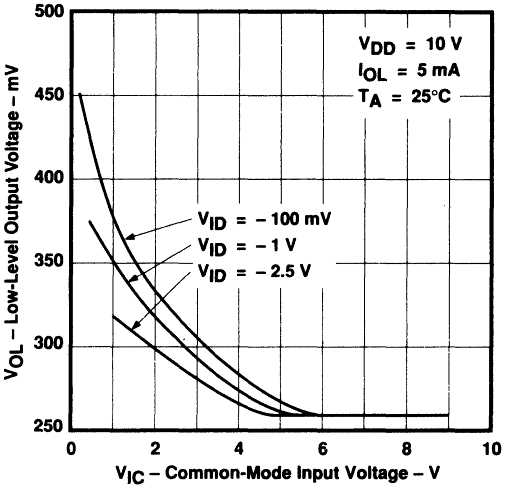


FIGURE 10

LOW-LEVEL OUTPUT VOLTAGE
vs
DIFFERENTIAL INPUT VOLTAGE

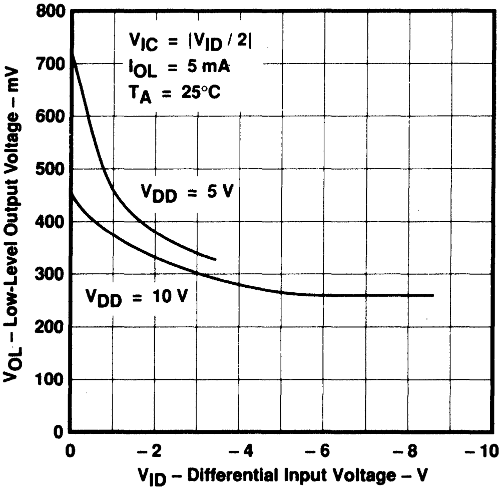


FIGURE 11

LOW-LEVEL OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

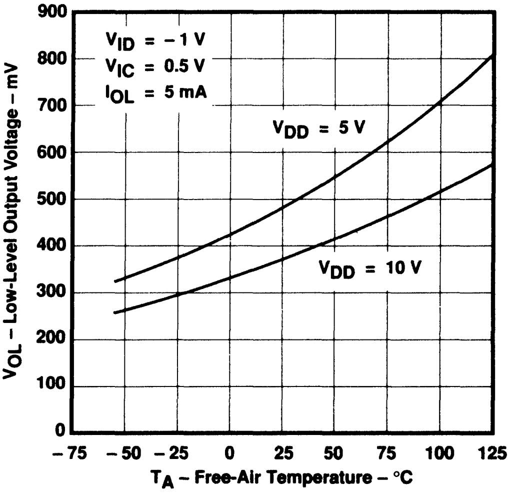


FIGURE 12

---

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

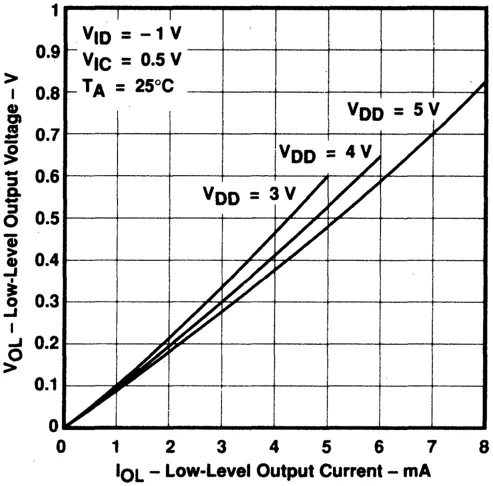


FIGURE 13

LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

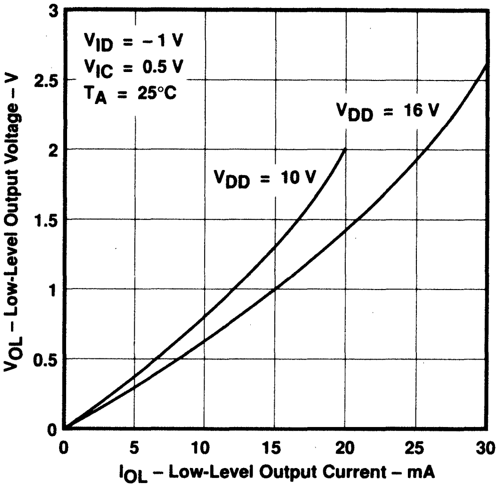


FIGURE 14

LARGE-SIGNAL
DIFFERENTIAL VOLTAGE AMPLIFICATION
vs
SUPPLY VOLTAGE

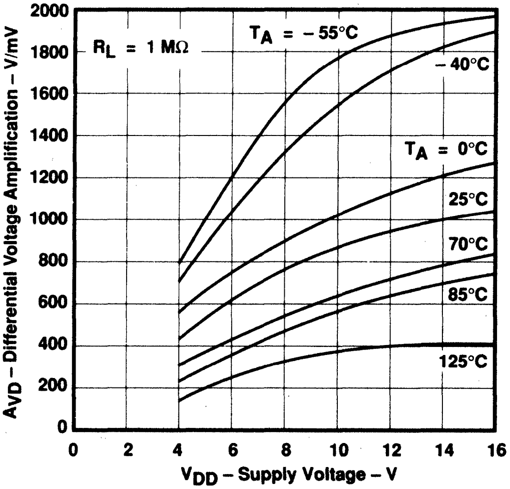


FIGURE 15

LARGE-SIGNAL
DIFFERENTIAL VOLTAGE AMPLIFICATION
vs
FREE-AIR TEMPERATURE

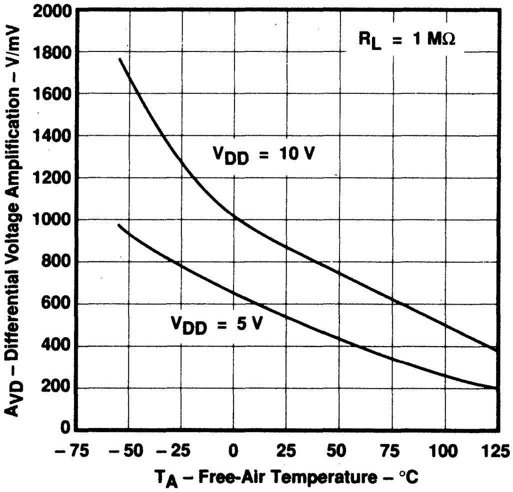


FIGURE 16

---

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

INPUT BIAS CURRENT AND INPUT OFFSET CURRENT
vs
FREE-AIR TEMPERATURE

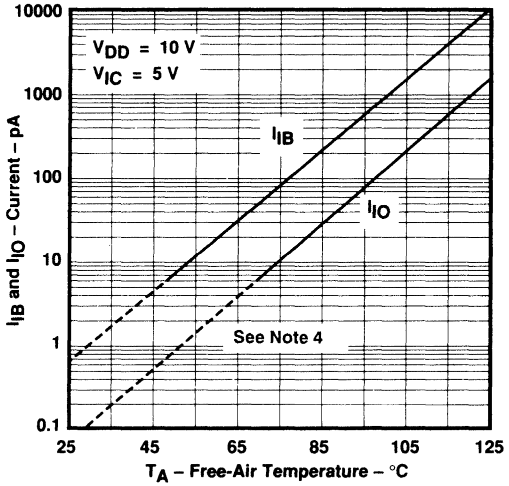


FIGURE 17

COMMON-MODE INPUT VOLTAGE POSITIVE LIMIT
vs
SUPPLY VOLTAGE

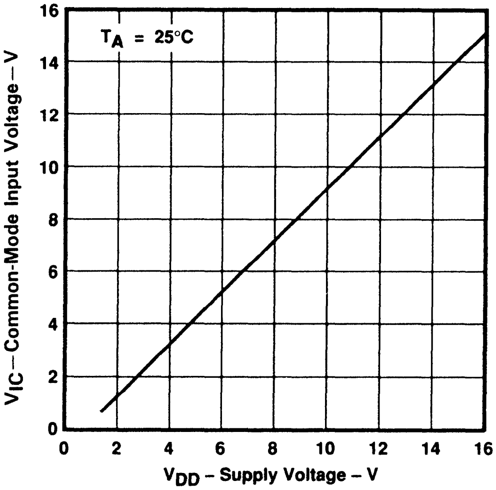


FIGURE 18

SUPPLY CURRENT
vs
SUPPLY VOLTAGE

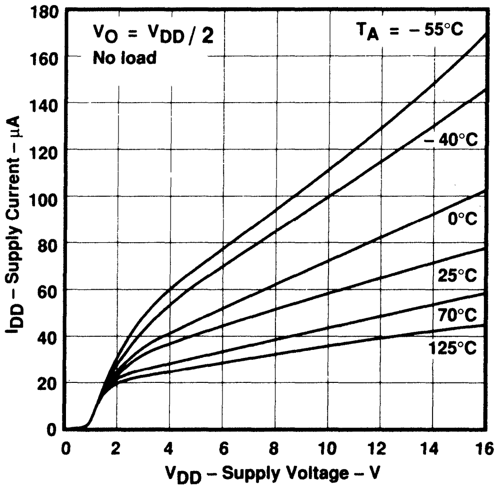


FIGURE 19

SUPPLY CURRENT
vs
FREE-AIR TEMPERATURE

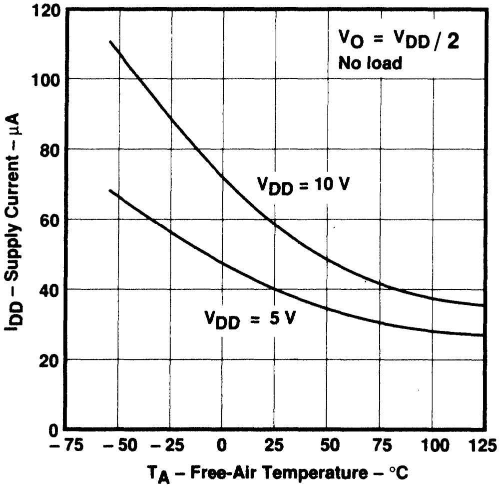


FIGURE 20

---

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

NOTE 4: The typical values of input bias current and input offset current below 5 pA were determined mathematically.

TYPICAL CHARACTERISTICS†

SLEW RATE
vs
SUPPLY VOLTAGE

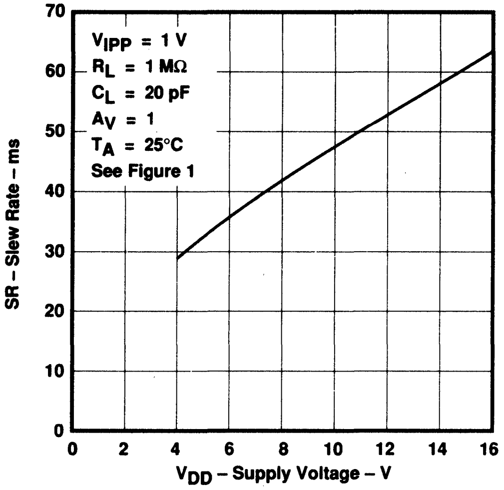


FIGURE 21

SLEW RATE
vs
FREE-AIR TEMPERATURE

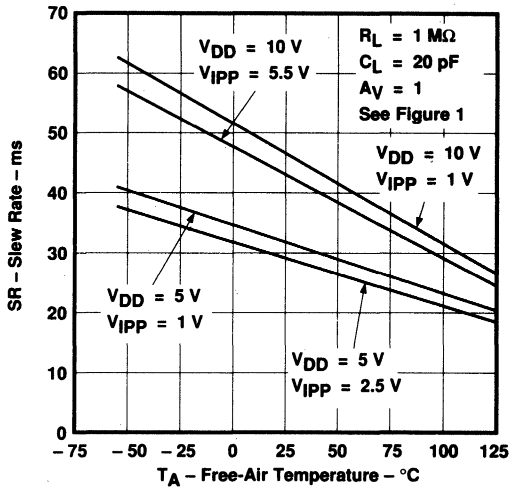


FIGURE 22

NORMALIZED SLEW RATE
vs
FREE-AIR TEMPERATURE

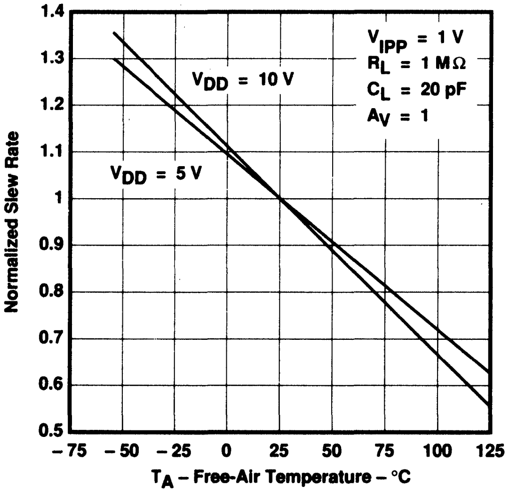


FIGURE 23

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE
vs
FREQUENCY

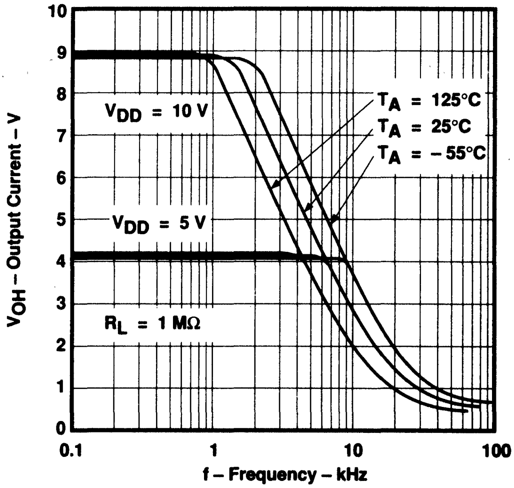


FIGURE 24

---

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

UNITY-GAIN BANDWIDTH
vs
FREE-AIR TEMPERATURE

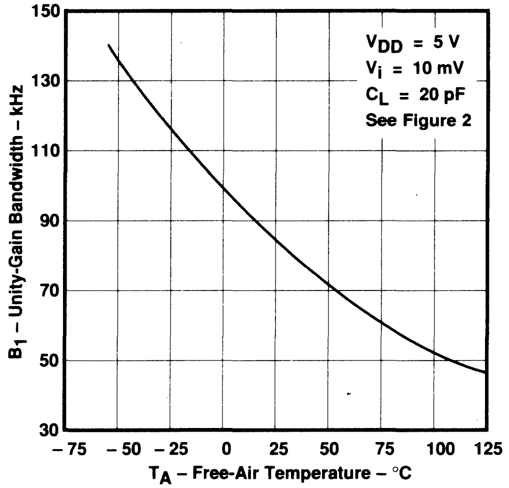


FIGURE 25

UNITY-GAIN BANDWIDTH
vs
SUPPLY VOLTAGE

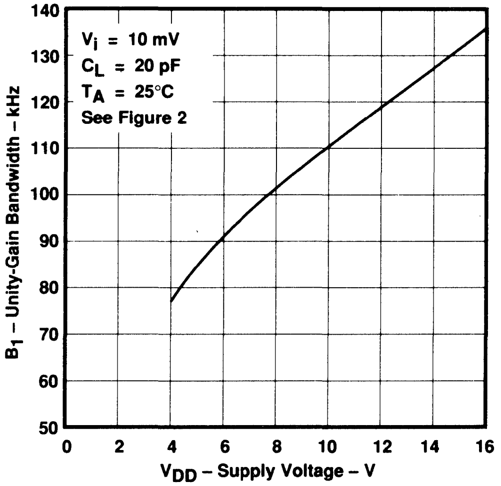


FIGURE 26

LARGE-SIGNAL DIFFERENTIAL VOLTAGE
AMPLIFICATION AND PHASE SHIFT
vs
FREQUENCY

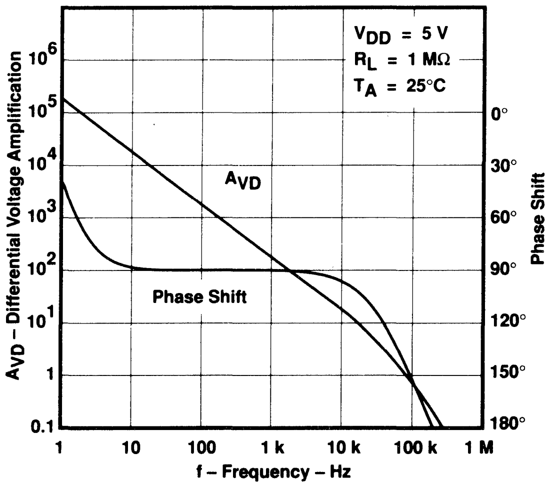


FIGURE 27

LARGE-SIGNAL DIFFERENTIAL VOLTAGE
AMPLIFICATION AND PHASE SHIFT
vs
FREQUENCY

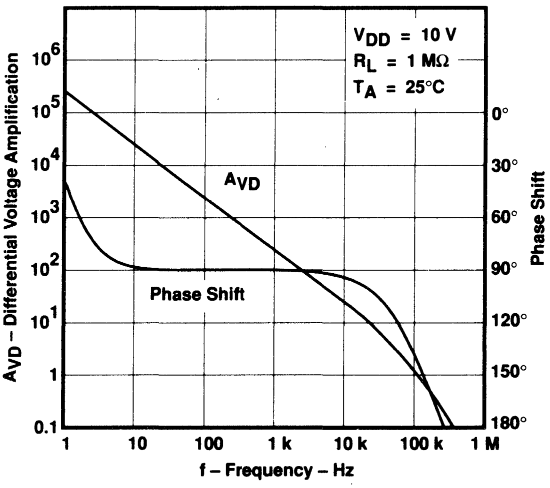


FIGURE 28

---

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

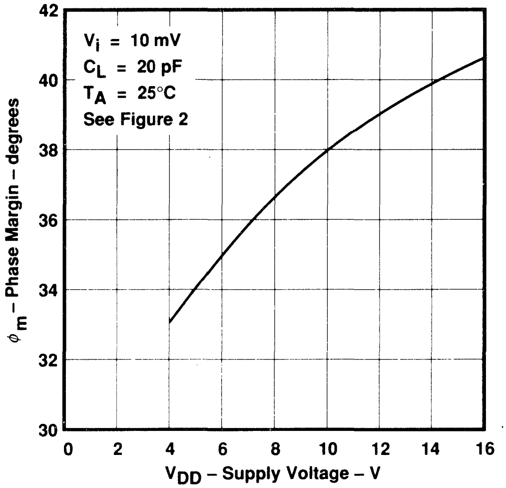

PHASE MARGIN
vs
SUPPLY VOLTAGE

FIGURE 29

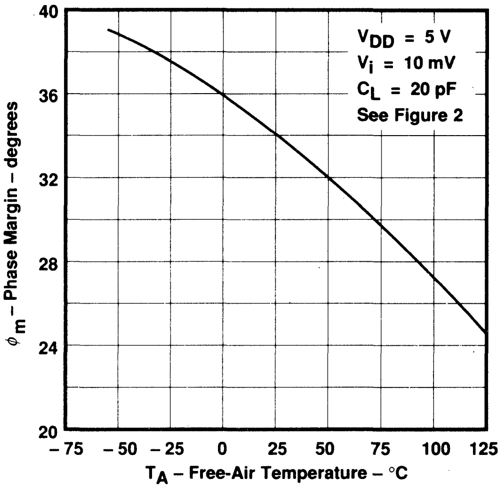

PHASE MARGIN
vs
FREE-AIR TEMPERATURE

FIGURE 30

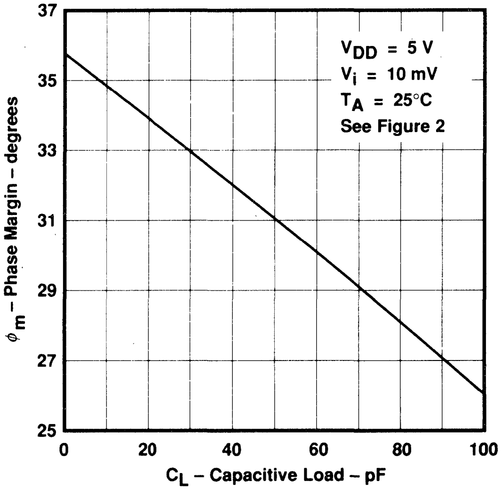

PHASE MARGIN
vs
CAPACITIVE LOAD

FIGURE 31

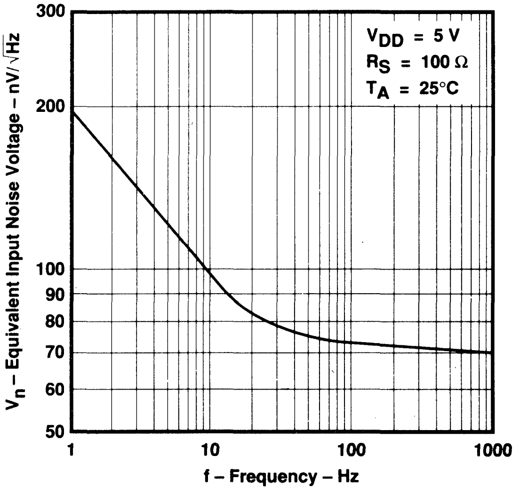

EQUIVALENT INPUT NOISE VOLTAGE
vs
FREQUENCY

FIGURE 32

---

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TLC1079
LinCMOS™ μPOWER PRECISION QUAD OPERATIONAL AMPLIFIER

D3147, AUGUST 1988–REVISED JANUARY 1991

- **Power Dissipation as Low as 10 μW Typ per Amplifier**
- **Operates on a Single Silver-Oxide Watch Battery, V_{DD} = 1.4 V Min**
- **V_{IO} . . . 850 μV Max in DIP and Small-Outline Package**
- **Input Offset Voltage Drift . . . 0.1 μV/Month Typ, Including the First 30 Days**
- **High-Impedance LinCMOS™ Inputs I_{IB} = 0.6 pA Typ**
- **High Open-Loop Gain . . . 800,000 Typ**
- **Output Drive Capability > 20 mA**
- **Slew Rate . . . 47 V/ms Typ**
- **Common-Mode Input Voltage Range Extends Below the Negative Rail**
- **Output Voltage Range Includes Negative Rail**
- **On-Chip ESD-Protection Circuitry**
- **14-Pin Small-Outline Package Option Also Available in Tape and Reel**

description

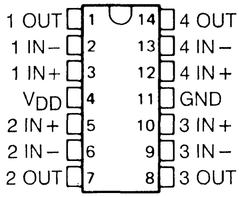
The TLC1079 operational amplifier offers ultra-low offset voltage, high gain, 110-kHz bandwidth, 47-V/ms slew rate, and just 150-μW power dissipation per amplifier.

With a supply voltage of 1.4 V, common-mode input to the negative rail, and output swing to the negative rail, the TLC1079 is an ideal solution for low-voltage, battery-operated systems. The 20-mA output drive capability means that the TLC1079 can easily drive small resistive and large capacitive loads when needed, while maintaining ultra-low standby power dissipation.

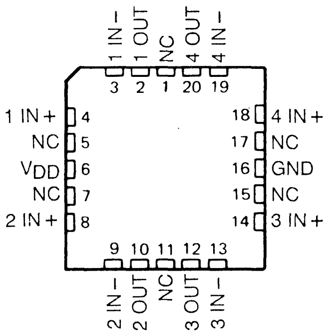
Since this device is functionally compatible as well as pin compatible with the TLC27L4 and TLC27L9, the TLC1079 easily upgrades existing designs that can benefit from its improved performance.

The TLC1079 incorporates internal ESD-protection circuits that prevent functional failures at voltages up to 2000 V as tested under MIL-STD-883C, Method 3015.2; however, care

D, J, OR N PACKAGE
(TOP VIEW)

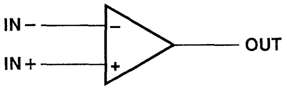


FK PACKAGE
(TOP VIEW)

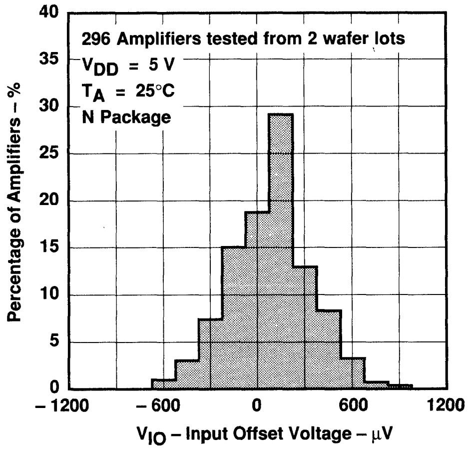


NC – No internal connection

symbol (each amplifier)



DISTRIBUTION OF TLC1079
INPUT OFFSET VOLTAGE



LinCMOS is a trademark of Texas Instruments Incorporated.

description (continued)

should be exercised when handling these devices as exposure to ESD may result in degradation of the device parametric performance. The TLC1079 design also inhibits latchup of the device inputs and outputs even with surge currents as large as 100 mA.

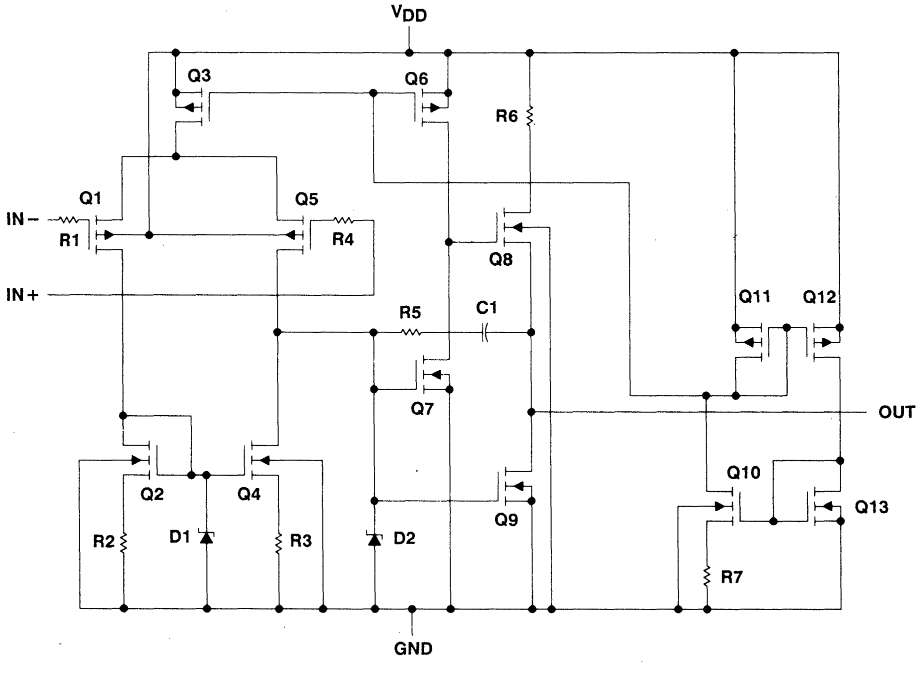
The C- suffix devices are characterized for operation from 0°C to 70°C. The I- suffix devices are characterized for operation from – 40°C to 85°C. The M- suffix devices are characterized for operation over the full military temperature range – 55°C to 125°C. The wide range of packaging options includes small-outline and chip-carrier versions for high-density system applications.

AVAILABLE OPTIONS

T_A	PACKAGE			
	SMALL OUTLINE (D)	CHIP CARRIER (FK)	CERAMIC DIP (J)	PLASTIC DIP (N)
0°C to 70°C	TLC1079CD	–	–	TLC1079CN
– 40°C to 85°C	TLC1079ID	–	–	TLC1079IN
– 55°C to 125°C	TLC1079MD	TLC1079MFK	TLC1079MJ	TLC1079MN

The D package is available taped and reeled. Add the suffix R to the device type (e.g., TLC1079CDR).

equivalent schematic (each amplifier)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{DD} (see Note 1)	18 V
Differential input voltage (see Note 2)	$\pm V_{DD}$
Input voltage range, V_I (any input)	-0.3 to V_{DD}
Input current, I_I (each input)	± 5 mA
Output current, I_O (each output)	± 30 mA
Total current into V_{DD} terminal (see Note 3)	45 mA
Duration of short-circuit current at (or below) 25°C (see Note 3)	Unlimited
Continuous total dissipation	See Dissipation Rating Table
Operating free-air temperature range, T_A: C-suffix	0°C to 70°C
I-suffix	− 40°C to 85°C
M-suffix	− 55°C to 125°C
Storage temperature range	− 65°C to 150°C
Case temperature for 60 seconds: FK package	260°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D or N package	260°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: J package	300°C

NOTES: 1. All voltage values, except differential voltages, are with respect to network ground.
2. Differential voltages are at the noninverting input with respect to the inverting input.
3. The output may be shorted to either supply. Temperature and/or supply voltages must be limited to ensure that the maximum dissipation ratings are not exceeded.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING	$T_A = 125°C$ POWER RATING
D	950 mW	7.6 mW/°C	608 mW	494 mW	190 mW
FK	1375 mW	11 mW/°C	880 mW	715 mW	275 mW
J	1375 mW	11 mW/°C	880 mW	715 mW	275 mW
N	1150 mW	9.2 mW/°C	736 mW	598 mW	230 mW

recommended operating conditions

		C-SUFFIX			I-SUFFIX			M-SUFFIX			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{DD}		1.4		16	3		16	4		16	V
Common-mode input voltage, V_{IC}	$V_{DD} = 5$ V	− 0.2		4	− 0.2		4	0		4	V
	$V_{DD} = 10$ V	− 0.2		9	− 0.2		9	0		9	
Operating free-air temperature, T_A		0		70	− 40		85	− 55		125	°C

electrical characteristics over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		V_{DD} = 5 V			V_{DD} = 10 V			UNIT
			T_A	MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_O = 1.4 V, V_{IC} = 0, R_S = 50 Ω, R_I = 1 MΩ	25°C		190	850		200	1150	μV
			Full range			1200			1500	
α_{VIO}	Temperature coefficient of input offset voltage		25°C to 70°C		1.1			1		μV/°C
I_{IO}	Input offset current (see Note 4)	V_O = V_{DD}/ 2, V_{IC} = V_{DD}/ 2	25°C		0.1			0.1		pA
			70°C		7	300		7	300	
I_{IB}	Input bias current (see Note 4)		25°C		0.6			0.7		pA
			70°C		40	600		50	600	
V_{ICR}	Common-mode input voltage range (see Note 5)		25°C	−0.2 to 4	−0.3 to 4.2		−0.2 to 9	−0.3 to 9.2		V
			Full range	−0.2 to 3.5			−0.2 to 8.5			V
V_{OH}	High-level output voltage	V_{ID} = 100 mV, R_L = 1 MΩ	25°C	3.2	4.1		8.2	8.9		V
			0°C	3.2	4.1		8.2	8.9		
			70°C	3.2	4.2		8.2	8.9		
V_{OL}	Low-level output voltage	V_{ID} = −100 mV, I_{OL} = 0	25°C		0	25		0	25	mV
			0°C		0	25		0	25	
			70°C		0	25		0	25	
A_{VD}	Large-signal differential voltage amplification	R_L = 1 MΩ, See Note 6	25°C	250	525		500	850		V/mV
			0°C	250	700		500	1010		
			70°C	200	380		350	660		
CMRR	Common-mode rejection ratio	V_{IC} = V_{ICR} min	25°C	70	95		75	97		dB
			0°C	70	95		75	97		
			70°C	70	95		75	97		
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)	V_{DD} = 5 V to 10 V, V_O = 1.4 V	25°C	75	98		75	98		dB
			0°C	75	98		75	98		
			70°C	75	98		75	98		
I_{DD}	Supply current (four amplifiers)	V_O = V_{DD}/ 2, V_{IC} = V_{DD}/ 2, No load	25°C		40	68		57	92	μA
			0°C		48	84		72	132	
			70°C		31	56		44	80	

NOTES: 4. The typical values of input bias current and input offset current below 5 pA were determined mathematically.
5. This range also applies to each input individually.
6. At V_{DD} = 5 V, V_O = 0.25 V to 2 V; at V_{DD} = 10 V, V_O = 1 V to 6 V.

operating characteristics

PARAMETER		TEST CONDITIONS		V_{DD} = 5 V			V_{DD} = 10 V			UNIT
			T_A	MIN	TYP	MAX	MIN	TYP	MAX	
SR	Slew rate at unity gain	R_L = 1 MΩ, C_L = 20 pF, V_{IPP} = 1 V, See Figure 1	25°C		32			47		V/ms
			0°C		35			51		
			70°C		27			38		
V_n	Equivalent input noise voltage	f = 1 kHz, R_S = 100 Ω	25°C		68			68		nv/$\sqrt{Hz}$
B_1	Unity-gain bandwidth	C_L = 20 pF, See Figure 2	25°C		85			110		kHz
			0°C		100			125		
			70°C		65			90		
ϕ_m	Phase margin at unity gain	C_L = 20 pF, See Figure 2	25°C		34°			38°		
			0°C		36°			40°		
			70°C		30°			34°		

electrical characteristics over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		V_{DD} = 5 V			V_{DD} = 10 V			UNIT
			T_A	MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_O = 1.4 V, V_{IC} = 0, R_S = 50 Ω, R_I = 1 MΩ	25°C		190	850		200	1150	µV
			Full range			1350			1650	
α_{VIO}	Temperature coefficient of input offset voltage		25°C to 85°C		1.1			1		µV/°C
I_{IO}	Input offset current (see Note 4)	V_O = V_{DD}/ 2, V_{IC} = V_{DD}/ 2	25°C		0.1			0.1		pA
			85°C		24	1000		26	1000	
I_{IB}	Input bias current (see Note 4)		25°C		0.6			0.7		pA
			85°C		200	2000		220	2000	
V_{ICR}	Common-mode input voltage range (see Note 5)		25°C	−0.2 to 4	−0.3 to 4.2		−0.2 to 9	−0.3 to 9.2		V
			Full range	−0.2 to 3.5			−0.2 to 8.5			V
V_{OH}	High-level output voltage	V_{ID} = 100 mV, R_L = 1 MΩ	25°C	3.2	4.1		8.2	8.9		V
			−40°C	3.2	4.1		8.2	8.9		
			85°C	3.2	4.2		8.2	8.9		
V_{OL}	Low-level output voltage	V_{ID} = −100 mV, I_{OL} = 0	25°C		0	25		0	25	mV
			−40°C		0	25		0	25	
			85°C		0	25		0	25	
A_{VD}	Large-signal differential voltage amplification	R_L = 1 MΩ, See Note 6	25°C	250	525		500	850		V/mV
			−40°C	250	900		500	1550		
			85°C	150	330		250	585		
CMRR	Common-mode rejection ratio	V_{IC} = V_{ICR} min	25°C	70	95		75	97		dB
			−40°C	70	95		75	97		
			85°C	70	95		75	97		
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)	V_{DD} = 5 V to 10 V, V_O = 1.4 V	25°C	75	98		75	98		dB
			−40°C	75	98		75	98		
			85°C	75	98		75	98		
I_{DD}	Supply current (four amplifiers)	V_O = V_{DD}/ 2, V_{IC} = V_{DD}/ 2, No load	25°C		40	68		57	92	µA
			−40°C		62	108		98	172	
			85°C		29	52		40	72	

NOTES: 4. The typical values of input bias current and input offset current below 5 pA were determined mathematically.
5. This range also applies to each input individually.
6. At V_{DD} = 5 V, V_O = 0.25 V to 2 V; at V_{DD} = 10 V, V_O = 1 V to 6 V.

operating characteristics

PARAMETER		TEST CONDITIONS		V_{DD} = 5 V			V_{DD} = 10 V			UNIT
			T_A	MIN	TYP	MAX	MIN	TYP	MAX	
SR	Slew rate at unity gain	R_L = 1 MΩ, C_L = 20 pF, V_{IPP} = 1 V, See Figure 1	25°C		32			47		V/ms
			−40°C		39			59		
			85°C		25			34		
V_n	Equivalent input noise voltage	f = 1 kHz, R_S = 100 Ω	25°C		68			68		nv/$\sqrt{Hz}$
B_1	Unity-gain bandwidth	C_L = 20 pF, See Figure 2	25°C		85			110		kHz
			−40°C		130			155		
			85°C		55			80		
ϕ_m	Phase margin at unity gain	C_L = 20 pF, See Figure 2	25°C		34°			38°		
			−40°C		38°			42°		
			85°C		28°			32°		

electrical characteristics over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		V_{DD} = 5 V			V_{DD} = 10 V			UNIT
			T_A	MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_O = 1.4 V, V_{IC} = 0, R_S = 50 Ω, R_I = 1 MΩ	25°C		190	850		200	1150	µV
			Full range			1600			1900	
α_{VIO}	Temperature coefficient of input offset voltage		25°C to 125°C		1.4			1.4		µV/°C
I_{IO}	Input offset current (see Note 4)	V_O = V_{DD}/ 2, V_{IC} = V_{DD}/ 2	25°C		0.1			0.1		pA
			125°C		1.4	15		1.8	15	nA
I_{IB}	Input bias current (see Note 4)		25°C		0.6			0.7		pA
			125°C		9	35		10	35	nA
V_{ICR}	Common-mode input voltage range (see Note 5)		25°C	0 to 4	−0.3 to 4.2		0 to 9	−0.3 to 9.2		V
			Full range	0 to 3.5			0 to 8.5			V
V_{OH}	High-level output voltage	V_{ID} = 100 mV, R_L = 1 MΩ	25°C	3.2	4.1		8.2	8.9		V
			−55°C	3.2	4.1		8.2	8.8		
			125°C	3.2	4.2		8.2	9		
V_{OL}	Low-level output voltage	V_{ID} = −100 mV, I_{OL} = 0	25°C		0	25		0	25	mV
			−55°C		0	25		0	25	
			125°C		0	25		0	25	
A_{VD}	Large-signal differential voltage amplification	R_L = 1 MΩ, See Note 6	25°C	250	525		500	850		V/mV
			−55°C	250	950		500	1750		
			125°C	75	200		150	380		
CMRR	Common-mode rejection ratio	V_{IC} = V_{ICR} min	25°C	70	95		75	97		dB
			−55°C	70	95		75	97		
			125°C	70	85		75	91		
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)	V_{DD} = 5 V to 10 V, V_O = 1.4 V	25°C	75	98		75	98		dB
			−55°C	70	98		70	98		
			125°C	70	98		70	98		
I_{DD}	Supply current (four amplifiers)	V_O = V_{DD}/ 2, V_{IC} = V_{DD}/ 2, No load	25°C		40	68		57	92	µA
			−55°C		69	120		111	192	
			125°C		27	48		35	60	

NOTES: 4. The typical values of input bias current and input offset current below 5 pA were determined mathematically.

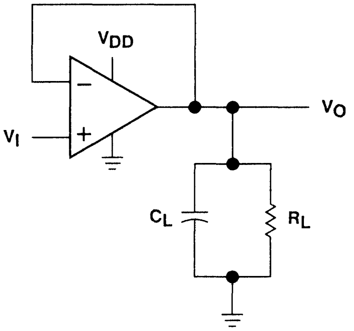
5. This range also applies to each input individually.

6. At V_{DD} = 5 V, V_O = 0.25 V to 2 V; at V_{DD} = 10 V, V_O = 1 V to 6 V.

operating characteristics

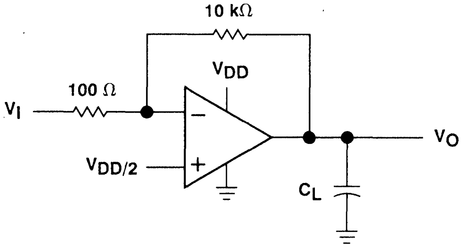
PARAMETER		TEST CONDITIONS		V_{DD} = 5 V			V_{DD} = 10 V			UNIT
			T_A	MIN	TYP	MAX	MIN	TYP	MAX	
SR	Slew rate at unity gain	R_L = 1 MΩ, C_L = 20 pF, V_{IPP} = 1 V, See Figure 1	25°C		32			47		V/ms
			−55°C		41			63		
			125°C		20			27		
V_n	Equivalent input noise voltage	f = 1 kHz, R_S = 100 Ω	25°C		68			68		nv/$\sqrt{\mathrm{Hz}}$
B_1	Unity-gain bandwidth	C_L = 20 pF, See Figure 2	25°C		85			110		kHz
			−55°C		140			165		
			125°C		45			70		
ϕ_m	Phase margin at unity gain	C_L = 20 pF, See Figure 2	25°C		34°			38°		
			−55°C		39°			43°		
			125°C		25°			29°		

PARAMETER MEASUREMENT INFORMATION



C_L includes fixture capacitance.

FIGURE 1. SLEW RATE TEST CIRCUIT



C_L includes fixture capacitance.

FIGURE 2. UNITY-GAIN BANDWIDTH AND PHASE MARGIN TEST CIRCUIT

TYPICAL CHARACTERISTICS

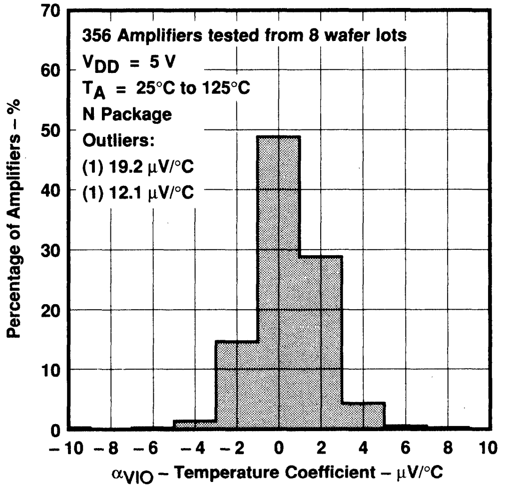

DISTRIBUTION OF TLC1079
INPUT OFFSET VOLTAGE
TEMPERATURE COEFFICIENT

FIGURE 3

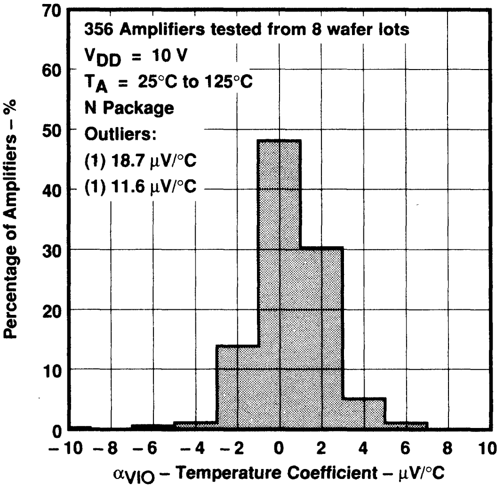

DISTRIBUTION OF TLC1079
INPUT OFFSET VOLTAGE
TEMPERATURE COEFFICIENT

FIGURE 4

TYPICAL CHARACTERISTICS†

HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

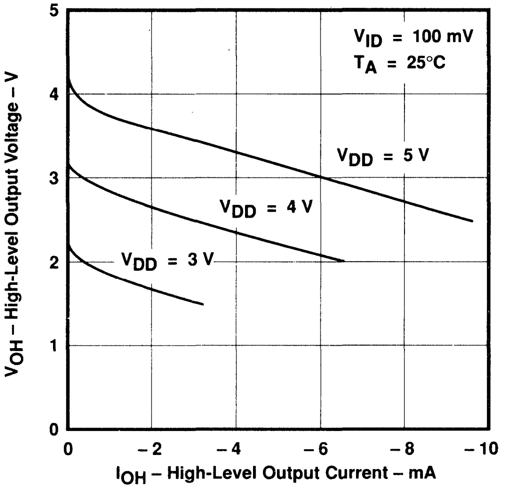


FIGURE 5

HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

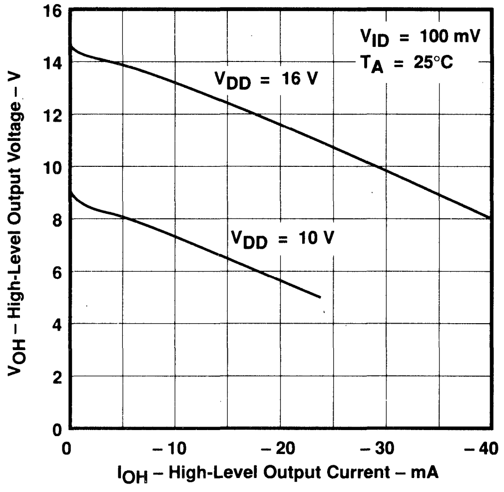


FIGURE 6

HIGH-LEVEL OUTPUT VOLTAGE
vs
SUPPLY VOLTAGE

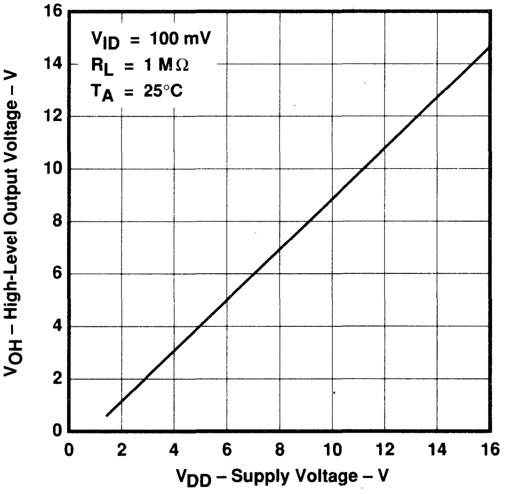


FIGURE 7

HIGH-LEVEL OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

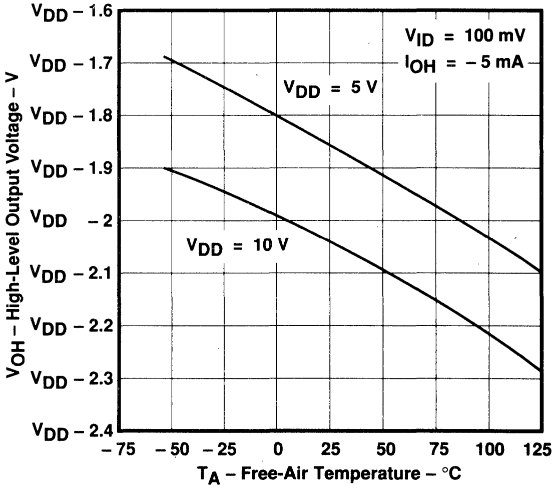


FIGURE 8

---

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

LOW-LEVEL OUTPUT VOLTAGE
vs
COMMON-MODE INPUT VOLTAGE

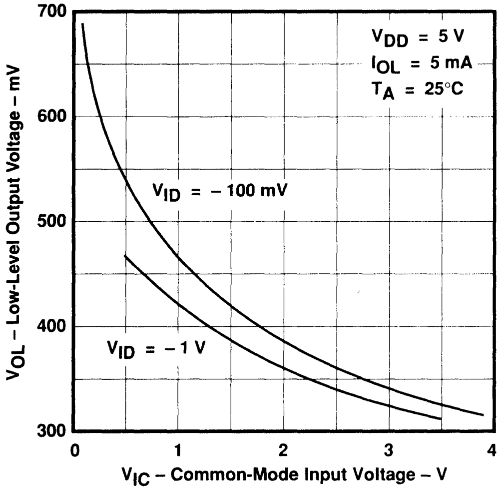


FIGURE 9

LOW-LEVEL OUTPUT VOLTAGE
vs
COMMON-MODE INPUT VOLTAGE

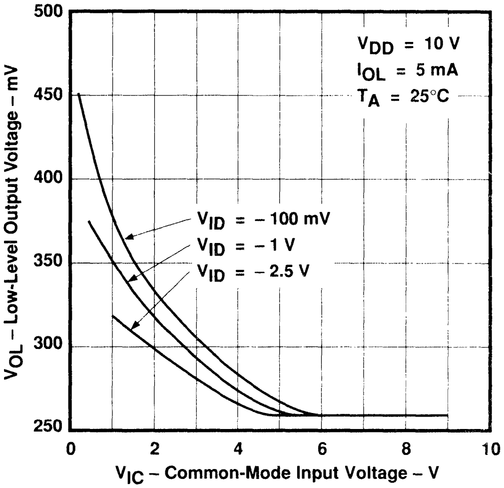


FIGURE 10

LOW-LEVEL OUTPUT VOLTAGE
vs
DIFFERENTIAL INPUT VOLTAGE

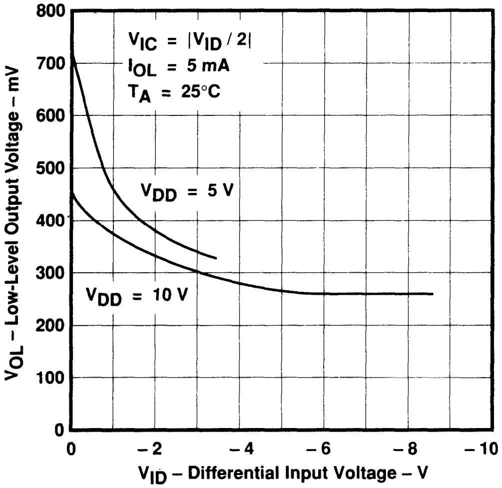


FIGURE 11

LOW-LEVEL OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

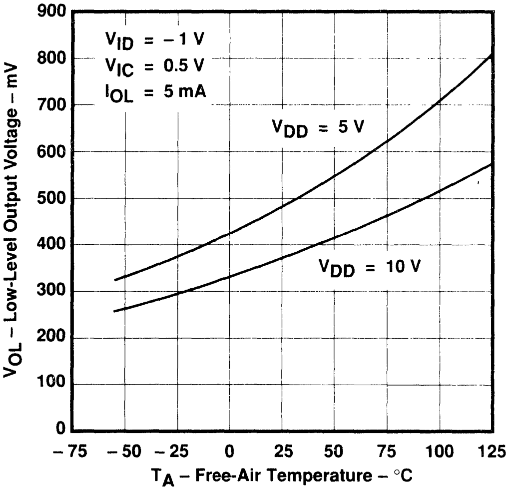


FIGURE 12

---

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

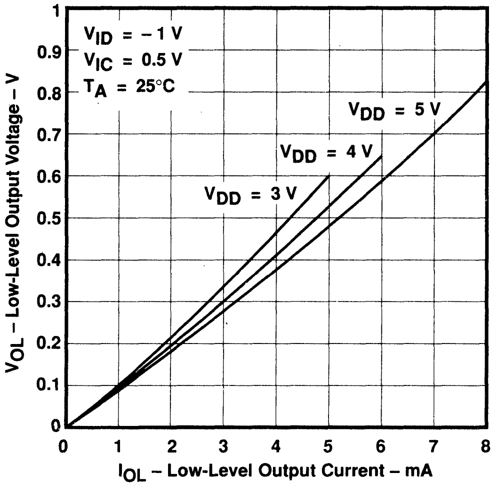


FIGURE 13

LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

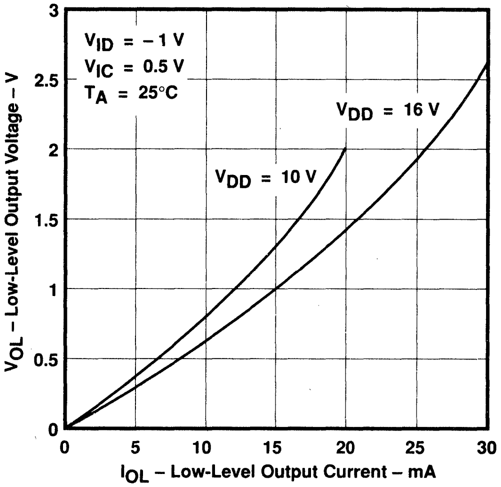


FIGURE 14

LARGE-SIGNAL
DIFFERENTIAL VOLTAGE AMPLIFICATION
vs
SUPPLY VOLTAGE

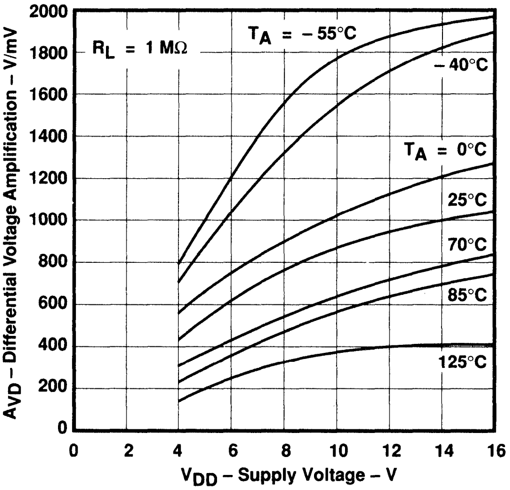


FIGURE 15

LARGE-SIGNAL
DIFFERENTIAL VOLTAGE AMPLIFICATION
vs
FREE-AIR TEMPERATURE

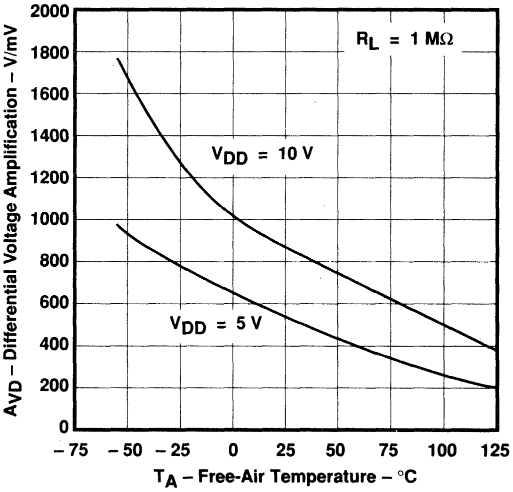


FIGURE 16

---

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

INPUT BIAS CURRENT AND OFFSET CURRENT
vs
FREE-AIR TEMPERATURE

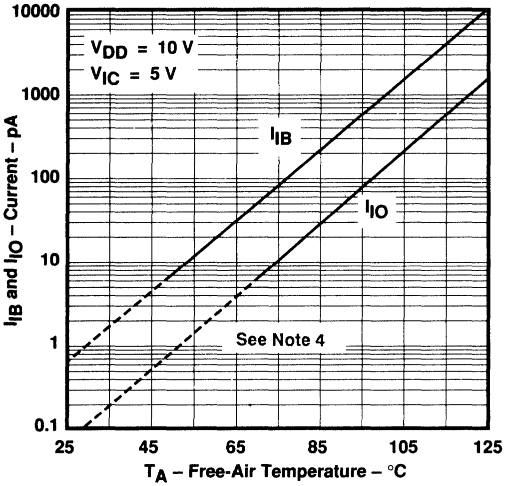


FIGURE 17

COMMON-MODE INPUT VOLTAGE POSITIVE LIMIT
vs
SUPPLY VOLTAGE

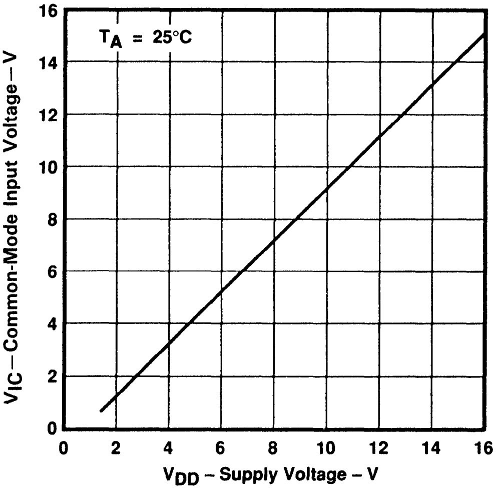


FIGURE 18

SUPPLY CURRENT
vs
SUPPLY VOLTAGE

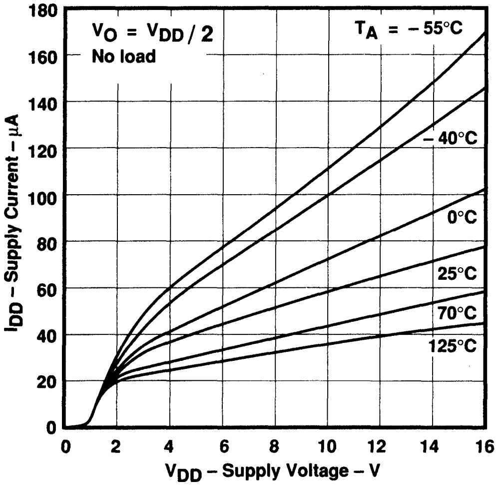


FIGURE 19

SUPPLY CURRENT
vs
FREE-AIR TEMPERATURE

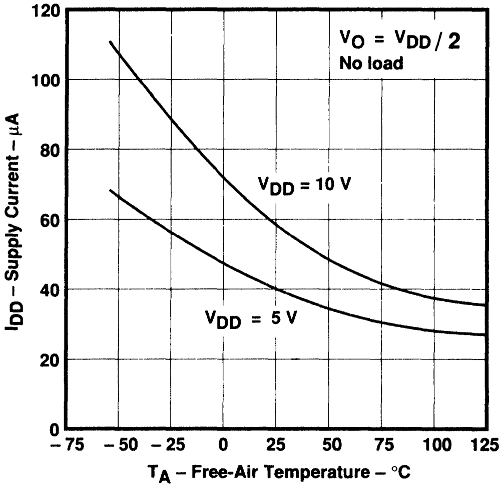


FIGURE 20

---

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

NOTE 4: The typical values of input bias current and input offset current below 5 pA were determined mathematically.

TYPICAL CHARACTERISTICS†

SLEW RATE
vs
SUPPLY VOLTAGE

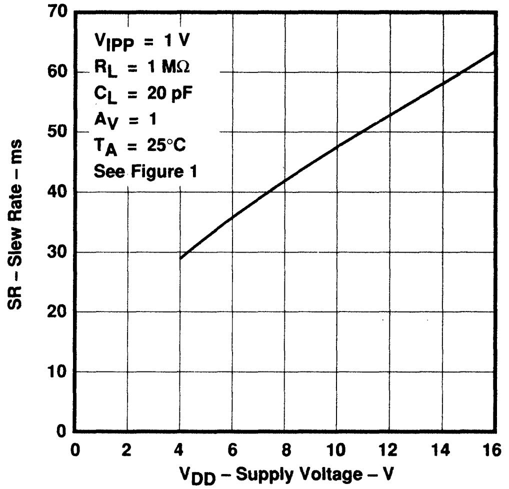


FIGURE 21

SLEW RATE
vs
FREE-AIR TEMPERATURE

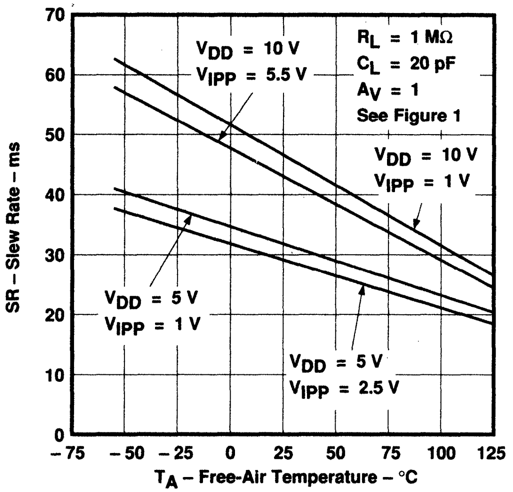


FIGURE 22

NORMALIZED SLEW RATE
vs
FREE-AIR TEMPERATURE

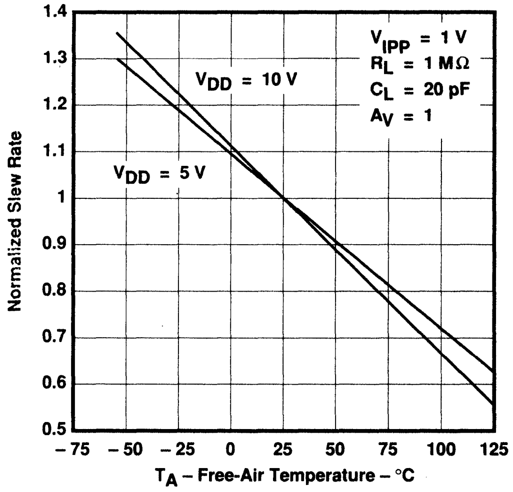


FIGURE 23

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE
vs
FREQUENCY

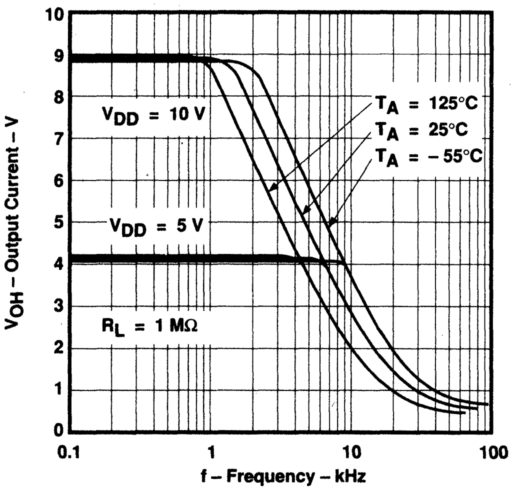


FIGURE 24

---

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

UNITY-GAIN BANDWIDTH
vs
FREE-AIR TEMPERATURE

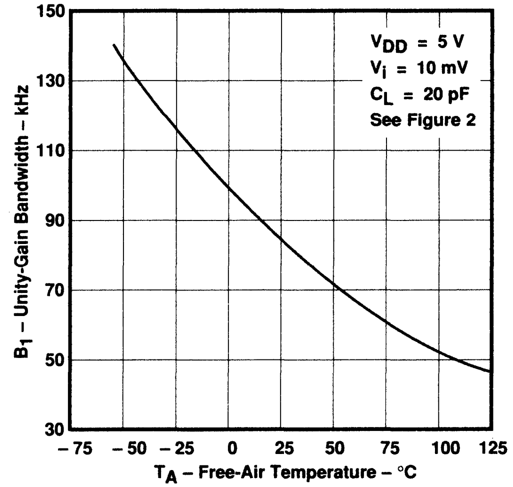


FIGURE 25

UNITY-GAIN BANDWIDTH
vs
SUPPLY VOLTAGE

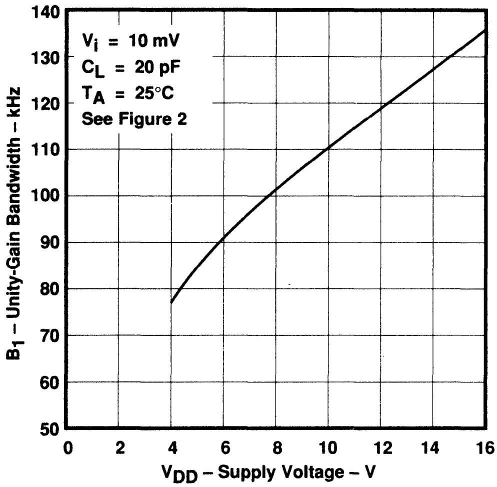


FIGURE 26

LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION AND PHASE SHIFT
vs
FREQUENCY

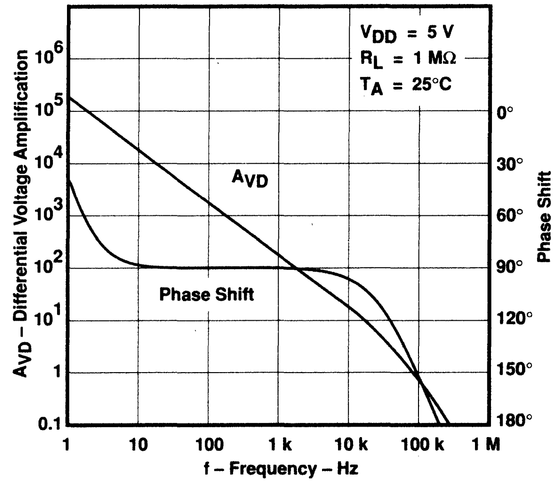


FIGURE 27

LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION AND PHASE SHIFT
vs
FREQUENCY

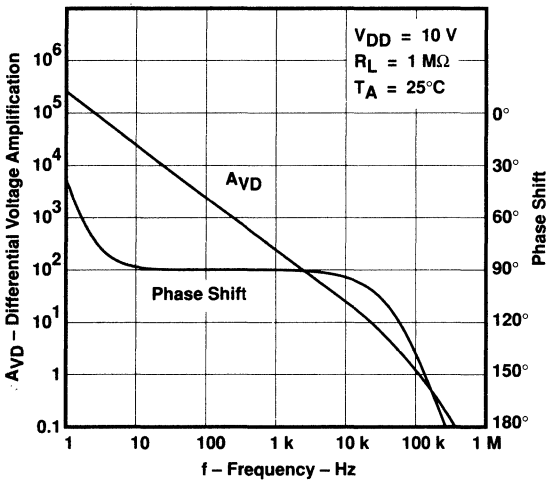


FIGURE 28

---

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

PHASE MARGIN
vs
SUPPLY VOLTAGE

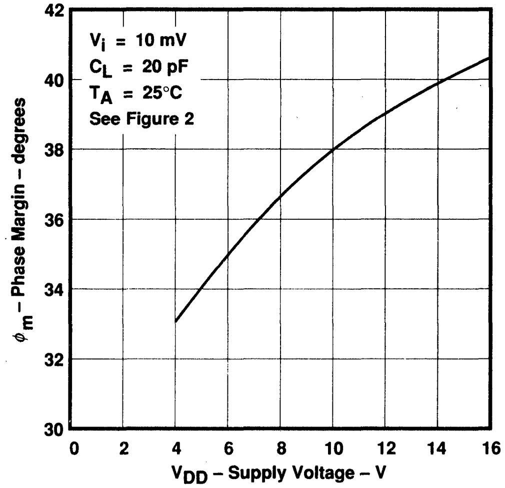


FIGURE 29

PHASE MARGIN
vs
FREE-AIR TEMPERATURE

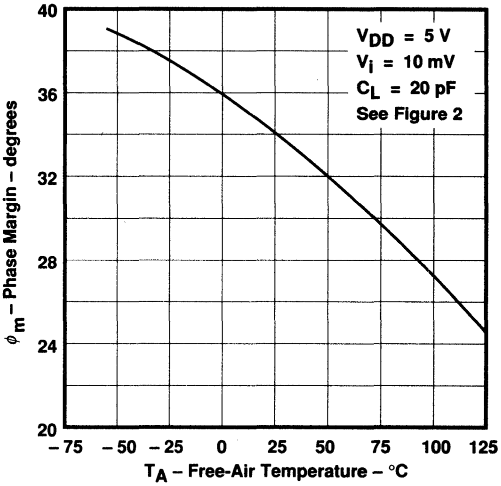


FIGURE 30

PHASE MARGIN
vs
CAPACITIVE LOAD

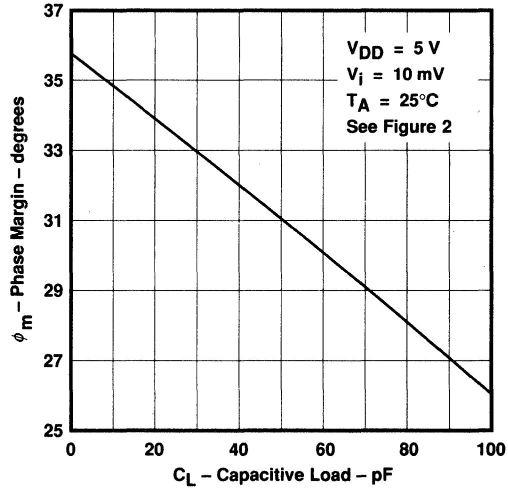


FIGURE 31

EQUIVALENT INPUT NOISE VOLTAGE
vs
FREQUENCY

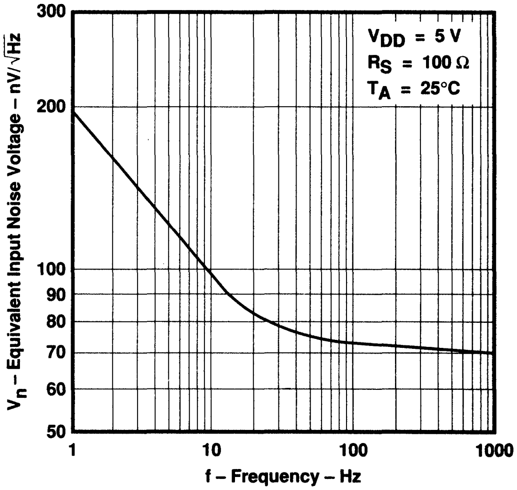


FIGURE 32

---

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TLC2201, TLC2201A, TLC2201B, TLC2201Y
Advanced LinCMOS™ LOW-NOISE PRECISION OPERATIONAL AMPLIFIERS

D3173, NOVEMBER 1988 – REVISED AUGUST 1991

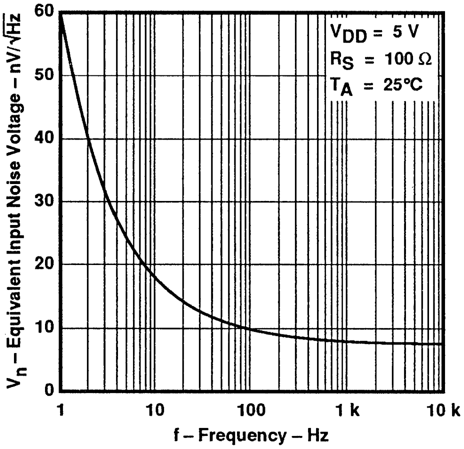
- **TLC2201B Is 100% Tested for Noise:**
  25 nV/$\sqrt{\text{Hz}}$ Max at f = 10 Hz
  12 nV/$\sqrt{\text{Hz}}$ Max at f = 1 kHz
- **Low Input Offset Voltage . . . 200 μV Max**
- **Excellent Offset Voltage Stability With Temperature . . . 0.5 μV/°C Typ**
- **Low Input Bias Current . . . 1 pA Typ at T_A = 25°C**
- **Fully Specified for Both Single-Supply and Split-Supply Operation**
- **Common-Mode Input Voltage Range Includes the Negative Rail**

description

The TLC2201, TLC2201A, TLC2201B, and TLC2201Y are precision, low-noise operational amplifiers using Texas Instruments Advanced LinCMOS™ process. These devices combine the noise performance of the lowest-noise JFET amplifiers with the dc precision available previously only in bipolar amplifiers. The Advanced LinCMOS™ process uses silicon-gate technology to obtain input offset voltage stability with temperature and time that far exceeds that obtainable using metal-gate technology. In addition, this technology makes possible input impedance levels that meet or exceed levels offered by top-gate JFET and expensive dielectric-isolated devices.

The combination of excellent dc and noise performance with a common-mode input voltage range that includes the negative rail makes these devices an ideal choice for high-impedance, low-level signal conditioning applications in either single-supply or split-supply configurations.

TYPICAL EQUIVALENT
INPUT NOISE VOLTAGE
vs
FREQUENCY



The device inputs and outputs are designed to withstand –100-mA surge currents without sustaining latch-up. In addition, internal ESD-protection circuits prevent functional failures at voltages up to 2000 V as tested under MIL-STD-883C, Method 3015.2; however, care should be exercised in handling these devices as exposure to ESD may result in degradation of the device parametric performance.

AVAILABLE OPTIONS

T_A	V_{IO} max AT 25°C	V_n max f = 10 Hz AT 25°C	V_n max f = 1 kHz AT 25°C	PACKAGE				CHIP FORM (Y)
				SMALL-OUTLINE (D)	PLASTIC DIP (P)	CERAMIC DIP (JG)	CHIP CARRIER (FK)	
0°C	200 μV	35 nV/$\sqrt{\text{Hz}}$	15 nV/$\sqrt{\text{Hz}}$	TLC2201ACD	TLC2201ACP		—	
to	200 μV	25 nV/$\sqrt{\text{Hz}}$	12 nV/$\sqrt{\text{Hz}}$	TLC2201BCD	TLC2201BCP		—	
70°C	500 μV	—	—	TLC2201CD	TLC2201CP		—	TLC2201Y
– 40°C	200 μV	35 nV/$\sqrt{\text{Hz}}$	15 nV/$\sqrt{\text{Hz}}$	TLC2201AID	TLC2201AIP		—	
to	200 μV	25 nV/$\sqrt{\text{Hz}}$	12 nV/$\sqrt{\text{Hz}}$	TLC2201BID	TLC2201BIP		—	
85°C	500 μV	—	—	TLC2201ID	TLC2201IP		—	
– 55°C	200 μV	35 nV/$\sqrt{\text{Hz}}$	15 nV/$\sqrt{\text{Hz}}$	TLC2201AMD	TLC2201AMP	TLC2201AMJG	TLC2201AMFK	
to	200 μV	25 nV/$\sqrt{\text{Hz}}$	12 nV/$\sqrt{\text{Hz}}$	TLC2201BMD	TLC2201BMP	TLC2201BMJG	TLC2201BMFK	
125°C	500 μV	—	—	TLC2201MD	TLC2201MP	TLC2201MJG	TLC2201MFK	

D packages are available taped-and-reeled. Add "R" suffix to device type (e.g., TLC2201BCDR). Chips are tested at 25°C.

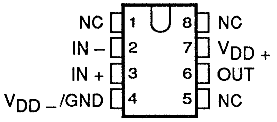
Advanced LinCMOS is a trademark of Texas Instruments Incorporated.

TEXAS INSTRUMENTS

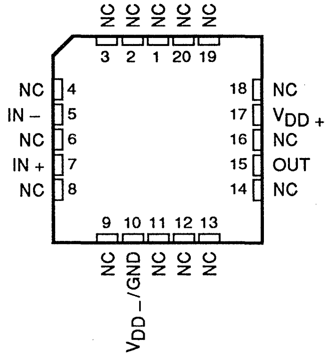
description (continued)

The C-suffix devices are characterized for operation from 0°C to 70°C. The I-suffix devices are characterized for operation from –40°C to 85°C. The M-suffix devices are characterized for operation over the full military temperature range of –55°C to 125°C.

D, JG, or P PACKAGE
(TOP VIEW)

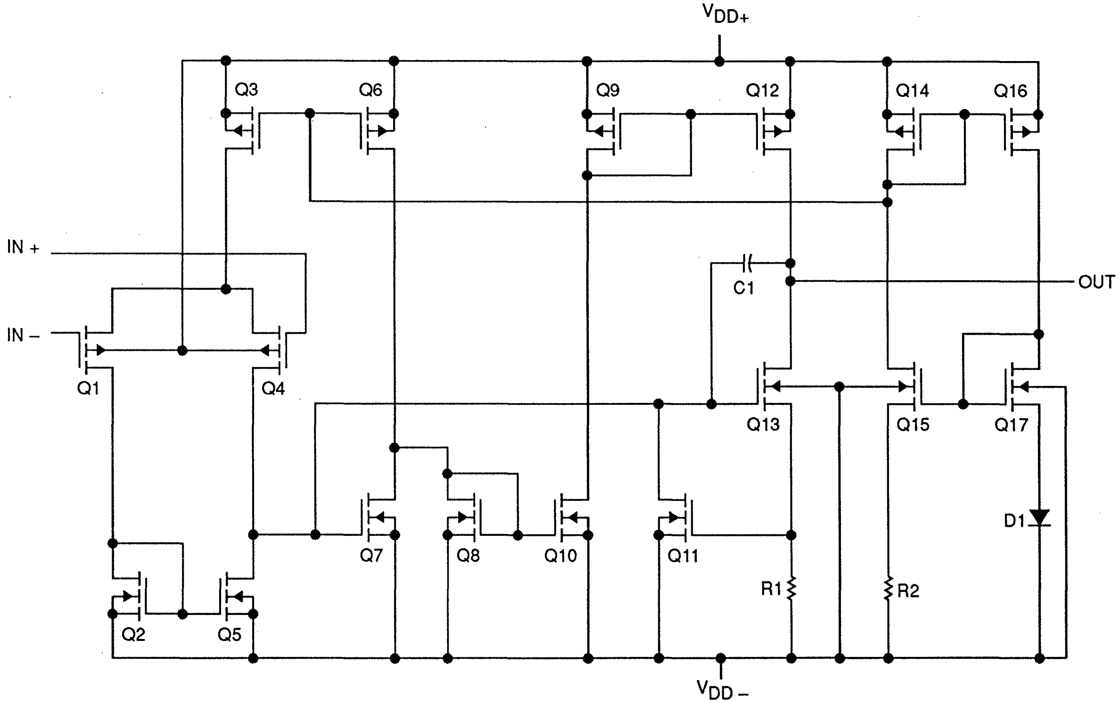


FK PACKAGE
(TOP VIEW)



NC – No internal connection

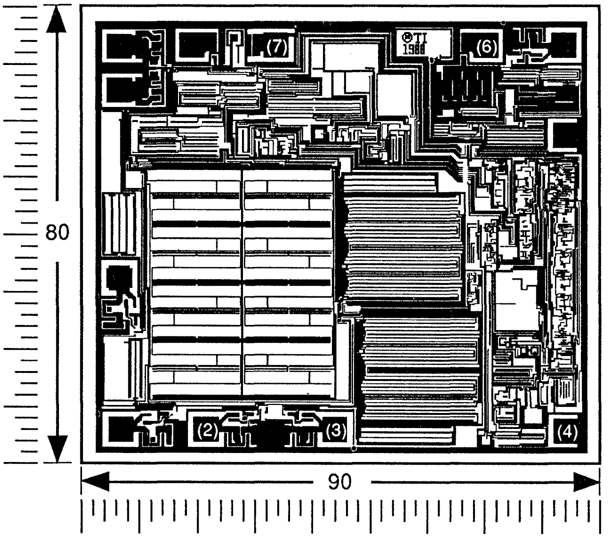
equivalent schematic (each amplifier)

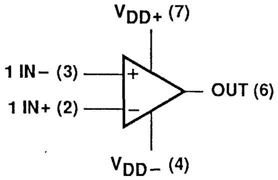


chip information

These chips, properly assembled, display characteristics similar to the TLC2201. Thermal compression or ultrasonic bonding may be used on the doped aluminum bonding pads. Chips may be mounted with conductive epoxy or a gold-silicon preform.

BONDING PAD ASSIGNMENTS





CHIP THICKNESS:
15 TYPICAL

BONDING PADS:
4 X 4 MINIMUM

T_J max = 150°C

TOLERANCES
ARE ±10%

ALL DIMENSIONS
ARE IN MILS

PIN (4) INTERNALLY
CONNECTED TO
BACKSIDE OF CHIP

absolute maximum ratings over operating free-air temperature (unless otherwise noted)

Supply voltage, V_{DD+} (see Note 1)	8 V
Supply voltage, V_{DD-} (see Note 1)	– 8 V
Differential input voltage (see Note 2)	± 16 V
Input voltage, V_I (any input, see Note 1)	± 8 V
Input current, I_I (each input)	± 5 mA
Output current, I_O	± 50 mA
Duration of short-circuit current at (or below) 25°C (see Note 3)	Unlimited
Continuous total dissipation	See Dissipation Rating Table
Operating free-air temperature, T_A: C-suffix	0°C to 70°C
I-suffix	– 40°C to 85°C
M-suffix	– 55°C to 125°C
Storage temperature range	– 65°C to 150°C
Case temperature for 60 seconds: FK package	260°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D or P package	260°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: JG package	300°C

NOTES: 1. All voltage values, except differential voltages, are with respect to the midpoint between V_{DD+} and V_{DD-}.
2. Differential voltages are at the noninverting input with respect to the inverting input.
3. The output may be shorted to either supply. Temperature and/or supply voltages must be limited to ensure that the maximum dissipation rating is not exceeded.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING	$T_A = 125°C$ POWER RATING
D	725 mW	5.8 mW/°C	464 mW	377 mW	145 mW
FK	1375 mW	11.0 mW/°C	880 mW	715 mW	275 mW
JG	1050 mW	8.4 mW/°C	672 mW	546 mW	210 mW
P	1000 mW	8.0 mW/°C	640 mW	520 mW	200 mW

recommended operating conditions

	C-SUFFIX		I-SUFFIX		M-SUFFIX		UNIT
	MIN	MAX	MIN	MAX	MIN	MAX	
Supply voltage, $V_{DD\pm}$	±2.3	±8	±2.3	±8	±2.3	±8	V
Common-mode input voltage, V_{IC}	V_{DD-}	$V_{DD+} - 2.3$	V_{DD-}	$V_{DD+} - 2.3$	V_{DD-}	$V_{DD+} - 2.3$	V
Operating free-air temperature, T_A	0	70	– 40	85	– 55	125	°C

electrical characteristics at specified free-air temperature, $V_{DD\pm} = \pm 5$ V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A†	MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	$V_{IC} = 0$, $R_S = 50\ \Omega$	25°C		100	500	µV
			Full range			600	
α_{VIO}	Temperature coefficient of input offset voltage		Full range		0.5		µV/°C
	Input offset voltage long-term drift (see Note 4)		25°C		0.001	0.005	µV/mo
I_{IO}	Input offset current		25°C		0.5		pA
			Full range			100	
I_{IB}	Input bias current		25°C		1		pA
			Full range			100	
V_{ICR}	Common-mode input voltage range	$R_S = 50\ \Omega$	Full range	−5 to 2.7			V
V_{OM+}	Maximum positive peak output voltage swing	$R_L = 10$ kΩ	25°C	4.7	4.8		V
			Full range	4.7			
V_{OM-}	Maximum negative peak output voltage swing		25°C	−4.7	−4.9		V
			Full range	−4.7			
A_{VD}	Large-signal differential voltage amplification	$V_O = \pm 4$ V, $R_L = 500$ kΩ,	25°C	400	560		V/mV
			Full range	300			
		$V_O = \pm 4$ V, $R_L = 10$ kΩ	25°C	90	100		
			Full range	70			
CMRR	Common-mode rejection ratio	$V_O = 0$, $V_{IC} = V_{ICR}$ min, $R_S = 50\ \Omega$	25°C	90	115		dB
			Full range	85			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD\pm} / \Delta V_{IO}$)	$V_{DD\pm} = \pm 2.3$ V to ± 8 V	25°C	90	110		dB
			Full range	85			
I_{DD}	Supply current	$V_O = 0$, No load	25°C		1.1	1.5	mA
			Full range			1.5	

operating characteristics at specified free-air temperature, $V_{DD\pm} = \pm 5$ V

PARAMETER		TEST CONDITIONS	T_A†	MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain	$V_O = \pm 2.3$ V, $R_L = 10$ kΩ, $C_L = 100$ pF	25°C	2	2.7		V/µs
			Full range	1.5			
V_n	Equivalent input noise voltage	f = 10 Hz	25°C		18		nV/√Hz
		f = 1 kHz	25°C		8		
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 to 1 Hz	25°C		0.5		µV
		f = 0.1 to 10 Hz	25°C		0.7		
I_n	Equivalent input noise current		25°C		0.6		fA/√Hz
	Gain-bandwidth product	f = 10 kHz, $R_L = 10$ kΩ, $C_L = 100$ pF	25°C		1.9		MHz
ϕ_m	Phase margin at unity gain	$R_L = 10$ kΩ, $C_L = 100$ pF	25°C		48°		

†Full range is 0°C to 70°C.

NOTE 4: Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at $T_A = 150°C$ extrapolated to $T_A = 25°C$ using the Arrhenius equation and assuming an activation energy of 0.96 eV.

electrical characteristics at specified free-air temperature, $V_{DD\pm} = \pm 5$ V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A†	TLC2201AC			TLC2201BC			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	$V_{IC} = 0$, $R_S = 50\ \Omega$	25°C		80	200		80	200	µV
			Full range			300			300	
α_{VIO}	Temperature coefficient of input offset voltage		Full range		0.5			0.5		µV/°C
	Input offset voltage long-term drift (see Note 4)		25°C		0.001	0.005		0.001	0.005	µV/mo
I_{IO}	Input offset current		25°C		0.5			0.5		pA
			Full range			100			100	
I_{IB}	Input bias current		25°C		1			1		pA
			Full range			100			100	
V_{ICR}	Common-mode input voltage range	$R_S = 50\ \Omega$	Full range	−5 to 2.7			−5 to 2.7			V
V_{OM+}	Maximum positive peak output voltage swing	$R_L = 10\ k\Omega$	25°C	4.7	4.8		4.7	4.8		V
			Full range	4.7			4.7			
V_{OM-}	Maximum negative peak output voltage swing		25°C	−4.7	−4.9		−4.7	−4.9		V
			Full range	−4.7			−4.7			
A_{VD}	Large-signal differential voltage amplification	$V_O = \pm 4$ V, $R_L = 500\ k\Omega$	25°C	400	560		400	560		V/mV
			Full range	300			300			
		$V_O = \pm 4$ V, $R_L = 10\ k\Omega$	25°C	90	100		90	100		
			Full range	70			70			
CMRR	Common-mode rejection ratio	$V_O = 0$, $V_{IC} = V_{ICR}$ min, $R_S = 50\ \Omega$	25°C	90	115		90	115		dB
			Full range	85			85			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD\pm} / \Delta V_{IO}$)	$V_{DD\pm} = \pm 2.3$ V to ± 8 V	25°C	90	110		90	110		dB
			Full range	85			85			
I_{DD}	Supply current	$V_O = 0$, No load	25°C		1.1	1.5		1.1	1.5	mA
			Full range			1.5			1.5	

operating characteristics at specified free-air temperature, $V_{DD\pm} = \pm 5$ V

PARAMETER		TEST CONDITIONS	T_A†	TLC2201AC			TLC2201BC			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
SR	Slew rate at unity gain	$V_O = \pm 2.3$ V, $R_L = 10\ k\Omega$, $C_L = 100$ pF	25°C	2	2.7		2	2.7		V/µs
			Full range	1.5			1.5			
V_n	Equivalent input noise voltage (see Note 5)	f = 10 Hz	25°C		18	35		18	25	nV/√Hz
		f = 1 kHz	25°C		8	15		8	12	
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 to 1 Hz	25°C		0.5			0.5		µV
		f = 0.1 to 10 Hz	25°C		0.7			0.7		
I_n	Equivalent input noise current		25°C		0.6			0.6		fA/√Hz
	Gain-bandwidth product	f = 10 kHz, $R_L = 10\ k\Omega$, $C_L = 100$ pF	25°C		1.9			1.9		MHz
ϕ_m	Phase margin at unity gain	$R_L = 10\ k\Omega$, $C_L = 100$ pF	25°C		48°			48°		

†Full range is 0°C to 70°C.

NOTES: 4. Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at $T_A = 150$°C extrapolated to $T_A = 25$°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

5. This parameter is tested on a sample basis for the TLC2201A and on all devices for the TLC2201B. For other test requirements, please contact the factory. This statement has no bearing on testing or nontesting of other parameters.

electrical characteristics at specified free-air temperature, V_{DD} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A†	MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	V_{IC} = 0, R_S = 50 Ω	25°C		100	500	µV
			Full range			600	
α_{VIO}	Temperature coefficient of input offset voltage		Full range		0.5		µV/°C
	Input offset voltage long-term drift (see Note 4)		25°C		0.001	0.005	µV/mo
I_{IO}	Input offset current		25°C		0.5		pA
			Full range			100	
I_{IB}	Input bias current		25°C		1		pA
			Full range			100	
V_{ICR}	Common-mode input voltage range	R_S = 50 Ω	Full range	0 to 2.7			V
V_{OH}	Maximum high-level output voltage	R_L = 10 kΩ	25°C	4.7	4.8		V
			Full range	4.7			
V_{OL}	Maximum low-level output voltage	I_O = 0	25°C		0	50	mV
			Full range			50	
A_{VD}	Large-signal differential voltage amplification	V_O = 1 V to 4 V, R_L = 500 kΩ,	25°C	150	315		V/mV
			Full range	100			
		V_O = 1 V to 4 V, R_L = 10 kΩ	25°C	25	55		
			Full range	15			
CMRR	Common-mode rejection ratio	V_O = 0, V_{IC} = V_{ICR} min, R_S = 50 Ω	25°C	90	110		dB
			Full range	85			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD\pm}/\Delta V_{IO}$)	V_{DD} = 4.6 V to 16 V	25°C	90	110		dB
			Full range	85			
I_{DD}	Supply current	V_O = 2.5 V, No load	25°C		1	1.5	mA
			Full range			1.5	

operating characteristics at specified free-air temperature, V_{DD} = 5 V

PARAMETER		TEST CONDITIONS	T_A†	MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain	V_O = 0.5 V to 2.5 V, R_L = 10 kΩ, C_L = 100 pF	25°C	1.8	2.5		V/µs
			Full range	1.3			
V_n	Equivalent input noise voltage	f = 10 Hz	25°C		18		nV/√Hz
		f = 1 kHz	25°C		8		
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 to 1 Hz	25°C		0.5		µV
		f = 0.1 to 10 Hz	25°C		0.7		
I_n	Equivalent input noise current		25°C		0.6		fA/√Hz
	Gain-bandwidth product	f = 10 kHz, R_L = 10 kΩ, C_L = 100 pF	25°C		1.8		MHz
ϕ_m	Phase margin at unity gain	R_L = 10 kΩ, C_L = 100 pF	25°C		45°		

† Full range is 0°C to 70°C.

NOTE 4: Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at T_A = 150°C extrapolated to T_A = 25°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

electrical characteristics at specified free-air temperature, V_{DD} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A†	TLC2201AC			TLC2201BC			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_{IC} = 0, R_S = 50 Ω	25°C		80	200		80	200	µV
			Full range			300			300	
α_{VIO}	Temperature coefficient of input offset voltage		Full range		0.5			0.5		µV/°C
	Input offset voltage long-term drift (see Note 4)		25°C		0.001	0.005		0.001	0.005	µV/mo
I_{IO}	Input offset current		25°C		0.5			0.5		pA
			Full range			100			100	
I_{IB}	Input bias current		25°C		1			1		pA
			Full range			100			100	
V_{ICR}	Common-mode input voltage range	R_S = 50 Ω	Full range	0 to 2.7			0 to 2.7			V
V_{OH}	Maximum high-level output voltage	R_L = 10 kΩ	25°C	4.7	4.8		4.7	4.8		V
			Full range	4.7			4.7			
V_{OL}	Maximum low-level output voltage	I_O = 0	25°C		0	50		0	50	mV
			Full range			50			50	
A_{VD}	Large-signal differential voltage amplification	V_O = 1 V to 4 V, R_L = 500 kΩ	25°C	150	315		150	315		V/mV
			Full range	100			100			
		V_O = 1 V to 4 V, R_L = 10 kΩ	25°C	25	55		25	55		
			Full range	15			15			
CMRR	Common-mode rejection ratio	V_O = 0, V_{IC} = V_{ICR} min, R_S = 50 Ω	25°C	90	110		90	110		dB
			Full range	85			85			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD\pm} / \Delta V_{IO}$)	V_{DD} = 4.6 V to 16 V	25°C	90	110		90	110		dB
			Full range	85			85			
I_{DD}	Supply current	V_O = 2.5 V, No load	25°C		1	1.5		1	1.5	mA
			Full range			1.5			1.5	

operating characteristics at specified free-air temperature, V_{DD} = 5 V

PARAMETER		TEST CONDITIONS	T_A†	TLC2201AC			TLC2201BC			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
SR	Slew rate at unity gain	V_O = 0.5 V to 2.5 V, R_L = 10 kΩ, C_L = 100 pF	25°C	1.8	2.5		1.8	2.5		V/µs
			Full range	1.3			1.3			
V_n	Equivalent input noise voltage (see Note 5)	f = 10 Hz	25°C		18	35		18	25	nV/√Hz
		f = 1 kHz	25°C		8	15		8	12	
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 to 1 Hz	25°C		0.5			0.5		µV
		f = 0.1 to 10 Hz	25°C		0.7			0.7		
I_n	Equivalent input noise current		25°C		0.6			0.6		fA/√Hz
	Gain-bandwidth product	f = 10 kHz, R_L = 10 kΩ, C_L = 100 pF	25°C		1.8			1.8		MHz
ϕ_m	Phase margin at unity gain	R_L = 10 kΩ, C_L = 100 pF	25°C		45°			45°		

†Full range is 0°C to 70°C.

NOTES: 4. Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at T_A = 150°C extrapolated to T_A = 25°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

5. This parameter is tested on a sample basis for the TLC2201A and on all devices for the TLC2201B. For other test requirements, please contact the factory. This statement has no bearing on testing or nontesting of other parameters.

electrical characteristics at specified free-air temperature, $V_{DD\pm} = \pm 5$ V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A†	MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	$V_{IC} = 0$, $R_S = 50\ \Omega$	25°C		100	500	µV
			Full range			650	
α_{VIO}	Temperature coefficient of input offset voltage		Full range		0.5		µV/°C
	Input offset voltage long-term drift (see Note 4)		25°C		0.001	0.005	µV/mo
I_{IO}	Input offset current		25°C		0.5		pA
			Full range			150	
I_{IB}	Input bias current		25°C		1		pA
			Full range			150	
V_{ICR}	Common-mode input voltage range	$R_S = 50\ \Omega$	Full range	−5 to 2.7			V
V_{OM+}	Maximum positive peak output voltage swing	$R_L = 10$ kΩ	25°C	4.7	4.8		V
			Full range	4.7			
V_{OM-}	Maximum negative peak output voltage swing		25°C	−4.7	−4.9		V
			Full range	−4.7			
A_{VD}	Large-signal differential voltage amplification	$V_O = \pm 4$ V, $R_L = 500$ kΩ,	25°C	400	560		V/mV
			Full range	250			
		$V_O = \pm 4$ V, $R_L = 10$ kΩ	25°C	90	100		
			Full range	65			
CMRR	Common-mode rejection ratio	$V_O = 0$, $V_{IC} = V_{ICR}$ min, $R_S = 50\ \Omega$	25°C	90	115		dB
			Full range	85			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD\pm} / \Delta V_{IO}$)	$V_{DD\pm} = \pm 2.3$ V to ±8 V	25°C	90	110		dB
			Full range	85			
I_{DD}	Supply current	$V_O = 0$, No load	25°C		1.1	1.5	mA
			Full range			1.5	

operating characteristics at specified free-air temperature, $V_{DD\pm} = \pm 5$ V

PARAMETER		TEST CONDITIONS	T_A†	MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain	$V_O = \pm 2.3$ V, $R_L = 10$ kΩ, $C_L = 100$ pF	25°C	2	2.7		V/µs
			Full range	1.4			
V_n	Equivalent input noise voltage	f = 10 Hz	25°C		18		nV/√Hz
		f = 1 kHz	25°C		8		
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 to 1 Hz	25°C		0.5		µV
		f = 0.1 to 10 Hz	25°C		0.7		
I_n	Equivalent input noise current		25°C		0.6		fA/√Hz
	Gain-bandwidth product	f = 10 kHz, $R_L = 10$ kΩ, $C_L = 100$ pF	25°C		1.9		MHz
ϕ_m	Phase margin at unity gain	$R_L = 10$ kΩ, $C_L = 100$ pF	25°C		48°		

†Full range is − 40°C to 85°C.

NOTE 4: Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at $T_A = 150°C$ extrapolated to $T_A = 25°C$ using the Arrhenius equation and assuming an activation energy of 0.96 eV.

electrical characteristics at specified free-air temperature, $V_{DD\pm} = \pm 5$ V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A†	TLC2201AI			TLC2201BI			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	$V_{IC} = 0$, $R_S = 50\ \Omega$	25°C		80	200		80	200	µV
			Full range			350			350	
α_{VIO}	Temperature coefficient of input offset voltage		Full range		0.5			0.5		µV/°C
	Input offset voltage long-term drift (see Note 4)		25°C		0.001	0.005		0.001	0.005	µV/mo
I_{IO}	Input offset current		25°C		0.5			0.5		pA
			Full range			150			150	
I_{IB}	Input bias current		25°C		1			1		pA
			Full range			150			150	
V_{ICR}	Common-mode input voltage range	$R_S = 50\ \Omega$	Full range	−5 to 2.7			−5 to 2.7			V
V_{OM+}	Maximum positive peak output voltage swing	$R_L = 10\ k\Omega$	25°C	4.7	4.8		4.7	4.8		V
			Full range	4.7			4.7			
V_{OM-}	Maximum negative peak output voltage swing		25°C	−4.7	−4.9		−4.7	−4.9		V
			Full range	−4.7			−4.7			
A_{VD}	Large-signal differential voltage amplification	$V_O = \pm 4$ V, $R_L = 500\ k\Omega$	25°C	400	560		400	560		V/mV
			Full range	250			250			
		$V_O = \pm 4$ V, $R_L = 10\ k\Omega$	25°C	90	100		90	100		
			Full range	65			65			
CMRR	Common-mode rejection ratio	$V_O = 0$, $V_{IC} = V_{ICR}$ min, $R_S = 50\ \Omega$	25°C	90	115		90	115		dB
			Full range	85			85			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD\pm} / \Delta V_{IO}$)	$V_{DD\pm} = \pm 2.3$ V to ± 8 V	25°C	90	110		90	110		dB
			Full range	85			85			
I_{DD}	Supply current	$V_O = 0$, No load	25°C		1.1	1.5		1.1	1.5	mA
			Full range			1.5			1.5	

operating characteristics at specified free-air temperature, $V_{DD\pm} = \pm 5$ V

PARAMETER		TEST CONDITIONS	T_A†	TLC2201AI			TLC2201BI			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
SR	Slew rate at unity gain	$V_O = \pm 2.3$ V, $R_L = 10\ k\Omega$, $C_L = 100$ pF	25°C	2	2.7		2	2.7		V/µs
			Full range	1.4			1.4			
V_n	Equivalent input noise voltage (see Note 5)	f = 10 Hz	25°C		18	35		18	25	nV/√Hz
		f = 1 kHz	25°C		8	15		8	12	
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 to 1 Hz	25°C		0.5			0.5		µV
		f = 0.1 to 10 Hz	25°C		0.7			0.7		
I_n	Equivalent input noise current		25°C		0.6			0.6		fA/√Hz
	Gain-bandwidth product	f = 10 kHz, $R_L = 10\ k\Omega$, $C_L = 100$ pF	25°C		1.9			1.9		MHz
ϕ_m	Phase margin at unity gain	$R_L = 10\ k\Omega$, $C_L = 100$ pF	25°C		48°			48°		

†Full range is – 40°C to 85°C.

NOTES: 4. Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at $T_A = 150°C$ extrapolated to $T_A = 25°C$ using the Arrhenius equation and assuming an activation energy of 0.96 eV.

5. This parameter is tested on a sample basis for the TLC2201A and on all devices for the TLC2201B. For other test requirements, please contact the factory. This statement has no bearing on testing or nontesting of other parameters.

electrical characteristics at specified free-air temperature, V_{DD} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A†	MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	V_{IC} = 0, R_S = 50 Ω	25°C		100	500	µV
			Full range			650	
α_{VIO}	Temperature coefficient of input offset voltage		Full range		0.5		µV/°C
	Input offset voltage long-term drift (see Note 4)		25°C		0.001	0.005	µV/mo
I_{IO}	Input offset current		25°C		0.5		pA
			Full range			150	
I_{IB}	Input bias current		25°C		1		pA
			Full range			150	
V_{ICR}	Common-mode input voltage range	R_S = 50 Ω	Full range	0 to 2.7			V
V_{OH}	Maximum high-level output voltage	R_L = 10 kΩ	25°C	4.7	4.8		V
			Full range	4.7			
V_{OL}	Maximum low-level output voltage	I_O = 0	25°C		0	50	mV
			Full range			50	
A_{VD}	Large-signal differential voltage amplification	V_O = 1 V to 4 V, R_L = 500 kΩ,	25°C	150	315		V/mV
			Full range	100			
		V_O = 1 V to 4 V, R_L = 10 kΩ	25°C	25	55		
			Full range	15			
CMRR	Common-mode rejection ratio	V_O = 0, V_{IC} = V_{ICR} min, R_S = 50 Ω	25°C	90	110		dB
			Full range	85			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD\pm} / \Delta V_{IO}$)	V_{DD} = 4.6 V to 16 V	25°C	90	110		dB
			Full range	85			
I_{DD}	Supply current	V_O = 2.5 V, No load	25°C		1	1.5	mA
			Full range			1.5	

operating characteristics at specified free-air temperature, V_{DD} = 5 V

PARAMETER		TEST CONDITIONS	T_A†	MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain	V_O = 0.5 V to 2.5 V, R_L = 10 kΩ, C_L = 100 pF	25°C	1.8	2.5		V/µs
			Full range	1.2			
V_n	Equivalent input noise voltage	f = 10 Hz	25°C		18		nV/√Hz
		f = 1 kHz	25°C		8		
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 to 1 Hz	25°C		0.5		µV
		f = 0.1 to 10 Hz	25°C		0.7		
I_n	Equivalent input noise current		25°C		0.6		fA/√Hz
	Gain-bandwidth product	f = 10 kHz, R_L = 10 kΩ, C_L = 100 pF	25°C		1.8		MHz
ϕ_m	Phase margin at unity gain	R_L = 10 kΩ, C_L = 100 pF	25°C		45°		

†Full range is – 40°C to 85°C.

NOTE 4: Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at T_A = 150°C extrapolated to T_A = 25°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

electrical characteristics at specified free-air temperature, V_{DD} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A†	TLC2201AI			TLC2201BI			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_{IC} = 0, R_S = 50 Ω	25°C		80	200		80	200	µV
			Full range			350			350	
α_{VIO}	Temperature coefficient of input offset voltage		Full range		0.5			0.5		µV/°C
	Input offset voltage long-term drift (see Note 4)		25°C		0.001	0.005		0.001	0.005	µV/mo
I_{IO}	Input offset current		25°C		0.5			0.5		pA
			Full range			150			150	
I_{IB}	Input bias current		25°C		1			1		pA
			Full range			150			150	
V_{ICR}	Common-mode input voltage range	R_S = 50 Ω	Full range	0 to 2.7			0 to 2.7			V
V_{OH}	Maximum high-level output voltage	R_L = 10 kΩ	25°C	4.7	4.8		4.7	4.8		V
			Full range	4.7			4.7			
V_{OL}	Maximum low-level output voltage	I_O = 0	25°C		0	50		0	50	mV
			Full range			50			50	
A_{VD}	Large-signal differential voltage amplification	V_O = 1 V to 4 V, R_L = 500 kΩ	25°C	150	315		150	315		V/mV
			Full range	100			100			
		V_O = 1 V to 4 V, R_L = 10 kΩ	25°C	25	55		25	55		
			Full range	15			15			
CMRR	Common-mode rejection ratio	V_O = 0, V_{IC} = V_{ICR} min, R_S = 50 Ω	25°C	90	110		90	110		dB
			Full range	85			85			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD\pm}/\Delta V_{IO}$)	V_{DD} = 4.6 V to 16 V	25°C	90	110		90	110		dB
			Full range	85			85			
I_{DD}	Supply current	V_O = 2.5 V, No load	25°C		1	1.5		1	1.5	mA
			Full range			1.5			1.5	

operating characteristics at specified free-air temperature, V_{DD} = 5 V

PARAMETER		TEST CONDITIONS	T_A†	TLC2201AI			TLC2201BI			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
SR	Slew rate at unity gain	V_O = 0.5 V to 2.5 V, R_L = 10 kΩ, C_L = 100 pF	25°C	1.8	2.5		1.8	2.5		V/µs
			Full range	1.2			1.2			
V_n	Equivalent input noise voltage (see Note 5)	f = 10 Hz	25°C		18	35		18	25	nV/√Hz
		f = 1 kHz	25°C		8	15		8	12	
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 to 1 Hz	25°C		0.5			0.5		µV
		f = 0.1 to 10 Hz	25°C		0.7			0.7		
I_n	Equivalent input noise current		25°C		0.6			0.6		fA/√Hz
	Gain-bandwidth product	f = 10 kHz, R_L = 10 kΩ, C_L = 100 pF	25°C		1.8			1.8		MHz
ϕ_m	Phase margin at unity gain	R_L = 10 kΩ, C_L = 100 pF	25°C		45°			45°		

†Full range is – 40°C to 85°C.

NOTES: 4. Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at T_A = 150°C extrapolated to T_A = 25°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

5. This parameter is tested on a sample basis for the TLC2201A and on all devices for the TLC2201B. For other test requirements, please contact the factory. This statement has no bearing on testing or nontesting of other parameters.

electrical characteristics at specified free-air temperature, $V_{DD\pm} = \pm 5$ V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A†	MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	$V_{IC} = 0$, $R_S = 50\ \Omega$	25°C		100	500	µV
			Full range			700	
α_{VIO}	Temperature coefficient of input offset voltage		Full range		0.5		µV/°C
	Input offset voltage long-term drift (see Note 4)		25°C		0.001	0.005	µV/mo
I_{IO}	Input offset current		25°C		0.5		pA
			Full range			500	
I_{IB}	Input bias current		25°C		1		pA
			Full range			500	
V_{ICR}	Common-mode input voltage range	$R_S = 50\ \Omega$	Full range	−5 to 2.7			V
V_{OM+}	Maximum positive peak output voltage swing	$R_L = 10\ k\Omega$	25°C	4.7	4.8		V
			Full range	4.7			
V_{OM-}	Maximum negative peak output voltage swing		25°C	−4.7	−4.9		V
			Full range	−4.7			
A_{VD}	Large-signal differential voltage amplification	$V_O = \pm 4$ V, $R_L = 500\ k\Omega$,	25°C	400	560		V/mV
			Full range	200			
		$V_O = \pm 4$ V, $R_L = 10\ k\Omega$	25°C	90	100		
			Full range	45			
CMRR	Common-mode rejection ratio	$V_O = 0$, $V_{IC} = V_{ICR}$ min, $R_S = 50\ \Omega$	25°C	90	115		dB
			Full range	85			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD\pm} / \Delta V_{IO}$)	$V_{DD\pm} = \pm 2.3$ V to ± 8 V	25°C	90	110		dB
			Full range	85			
I_{DD}	Supply current	$V_O = 0$, No load	25°C		1.1	1.5	mA
			Full range			1.5	

operating characteristics at specified free-air temperature, $V_{DD\pm} = \pm 5$ V

PARAMETER		TEST CONDITIONS	T_A†	MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain	$V_O = \pm 2.3$ V, $R_L = 10\ k\Omega$, $C_L = 100$ pF	25°C	2	2.7		V/µs
			Full range	1.3			
V_n	Equivalent input noise voltage	f = 10 Hz	25°C		18		nV/√Hz
		f = 1 kHz	25°C		8		
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 to 1 Hz	25°C		0.5		µV
		f = 0.1 to 10 Hz	25°C		0.7		
I_n	Equivalent input noise current		25°C		0.6		fA/√Hz
	Gain-bandwidth product	f = 10 kHz, $R_L = 10\ k\Omega$, $C_L = 100$ pF	25°C		1.9		MHz
ϕ_m	Phase margin at unity gain	$R_L = 10\ k\Omega$, $C_L = 100$ pF	25°C		48°		

†Full range is −55°C to 125°C.

NOTE 4: Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at $T_A = 150°C$ extrapolated to $T_A = 25°C$ using the Arrhenius equation and assuming an activation energy of 0.96 eV.

electrical characteristics at specified free-air temperature, $V_{DD\pm}$ = ±5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A†	TLC2201AM			TLC2201BM			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_{IC} = 0, R_S = 50 Ω	25°C		80	200		80	200	µV
			Full range			400			400	
α_{VIO}	Temperature coefficient of input offset voltage		Full range		0.5			0.5		µV/°C
	Input offset voltage long-term drift (see Note 4)		25°C		0.001	0.005		0.001	0.005	µV/mo
I_{IO}	Input offset current		25°C		0.5			0.5		pA
			Full range			500			500	
I_{IB}	Input bias current		25°C		1			1		pA
			Full range			500			500	
V_{ICR}	Common-mode input voltage range	R_S = 50 Ω	Full range	−5 to 2.7			−5 to 2.7			V
V_{OM+}	Maximum positive peak output voltage swing	R_L = 10 kΩ	25°C	4.7	4.8		4.7	4.8		V
			Full range	4.7			4.7			
V_{OM-}	Maximum negative peak output voltage swing		25°C	−4.7	−4.9		−4.7	−4.9		V
			Full range	−4.7			−4.7			
A_{VD}	Large-signal differential voltage amplification	V_O = ±4 V, R_L = 500 kΩ	25°C	400	560		400	560		V/mV
			Full range	200			200			
		V_O = ±4 V, R_L = 10 kΩ	25°C	90	100		90	100		
			Full range	45			45			
CMRR	Common-mode rejection ratio	V_O = 0, V_{IC} = V_{ICR} min, R_S = 50 Ω	25°C	90	115		90	115		dB
			Full range	85			85			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD\pm}/\Delta V_{IO}$)	$V_{DD\pm}$ = ±2.3 V to ±8 V	25°C	90	110		90	110		dB
			Full range	85			85			
I_{DD}	Supply current	V_O = 0, No load	25°C		1.1	1.5		1.1	1.5	mA
			Full range			1.5			1.5	

operating characteristics at specified free-air temperature, $V_{DD\pm}$ = ±5 V

PARAMETER		TEST CONDITIONS	T_A†	TLC2201AM			TLC2201BM			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
SR	Slew rate at unity gain	V_O = ±2.3 V, R_L = 10 kΩ, C_L = 100 pF	25°C	2	2.7		2	2.7		V/µs
			Full range	1.3			1.3			
V_n	Equivalent input noise voltage (see Note 5)	f = 10 Hz	25°C		18	35		18	25	nV/√Hz
		f = 1 kHz	25°C		8	15		8	12	
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 to 1 Hz	25°C		0.5			0.5		µV
		f = 0.1 to 10 Hz	25°C		0.7			0.7		
I_n	Equivalent input noise current		25°C		0.6			0.6		fA/√Hz
	Gain-bandwidth product	f = 10 kHz, R_L = 10 kΩ, C_L = 100 pF	25°C		1.9			1.9		MHz
ϕ_m	Phase margin at unity gain	R_L = 10 kΩ, C_L = 100 pF	25°C		48°			48°		

†Full range is – 55°C to 125°C.

NOTES: 4. Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at T_A = 150°C extrapolated to T_A = 25°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

5. This parameter is tested on a sample basis for the TLC2201A and on all devices for the TLC2201B. For other test requirements, please contact the factory. This statement has no bearing on testing or nontesting of other parameters.

electrical characteristics at specified free-air temperature, V_{DD} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A†	MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	V_{IC} = 0, R_S = 50 Ω	25°C		100	500	µV
			Full range			700	
α_{VIO}	Temperature coefficient of input offset voltage		Full range		0.5		µV/°C
	Input offset voltage long-term drift (see Note 4)		25°C		0.001	0.005	µV/mo
I_{IO}	Input offset current		25°C		0.5		pA
			Full range			500	
I_{IB}	Input bias current		25°C		1		pA
			Full range			500	
V_{ICR}	Common-mode input voltage range	R_S = 50 Ω	Full range	0 to 2.7			V
V_{OH}	Maximum high-level output voltage	R_L = 10 kΩ	25°C	4.7	4.8		V
			Full range	4.7			
V_{OL}	Maximum low-level output voltage	I_O = 0	25°C		0	50	mV
			Full range			50	
A_{VD}	Large-signal differential voltage amplification	V_O = 1 V to 4 V, R_L = 500 kΩ,	25°C	150	315		V/mV
			Full range	75			
		V_O = 1 V to 4 V, R_L = 10 kΩ	25°C	25	55		
			Full range	10			
CMRR	Common-mode rejection ratio	V_O = 0, V_{IC} = V_{ICR} min, R_S = 50 Ω	25°C	90	110		dB
			Full range	85			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD\pm}/\Delta V_{IO}$)	V_{DD} = 4.6 V to 16 V	25°C	90	110		dB
			Full range	85			
I_{DD}	Supply current	V_O = 2.5 V, No load	25°C		1	1.5	mA
			Full range			1.5	

operating characteristics at specified free-air temperature, V_{DD} = 5 V

PARAMETER		TEST CONDITIONS	T_A†	MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain	V_O = 0.5 V to 2.5 V, R_L = 10 kΩ, C_L = 100 pF	25°C	1.8	2.5		V/µs
			Full range	1.1			
V_n	Equivalent input noise voltage	f = 10 Hz	25°C		18		nV/√Hz
		f = 1 kHz	25°C		8		
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 to 1 Hz	25°C		0.5		µV
		f = 0.1 to 10 Hz	25°C		0.7		
I_n	Equivalent input noise current		25°C		0.6		fA/√Hz
	Gain-bandwidth product	f = 10 kHz, R_L = 10 kΩ, C_L = 100 pF	25°C		1.8		MHz
ϕ_m	Phase margin at unity gain	R_L = 10 kΩ, C_L = 100 pF	25°C		45°		

†Full range is – 55°C to 125°C.

NOTE 4: Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at T_A = 150°C extrapolated to T_A = 25°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

electrical characteristics at specified free-air temperature, V_{DD} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A†	TLC2201AM			TLC2201BM			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_{IC} = 0, R_S = 50 Ω	25°C		80	200		80	200	µV
			Full range			400			400	
α_{VIO}	Temperature coefficient of input offset voltage		Full range		0.5			0.5		µV/°C
	Input offset voltage long-term drift (see Note 4)		25°C		0.001	0.005		0.001	0.005	µV/mo
I_{IO}	Input offset current		25°C		0.5			0.5		pA
			Full range			500			500	
I_{IB}	Input bias current		25°C		1			1		pA
			Full range			500			500	
V_{ICR}	Common-mode input voltage range	R_S = 50 Ω	Full range	0 to 2.7			0 to 2.7			V
V_{OH}	Maximum high-level output voltage	R_L = 10 kΩ	25°C	4.7	4.8		4.7	4.8		V
			Full range	4.7			4.7			
V_{OL}	Maximum low-level output voltage	I_O = 0	25°C		0	50		0	50	mV
			Full range			50			50	
A_{VD}	Large-signal differential voltage amplification	V_O = 1 V to 4 V, R_L = 500 kΩ	25°C	150	315		150	315		V/mV
			Full range	75			75			
		V_O = 1 V to 4 V, R_L = 10 kΩ	25°C	25	55		25	55		
			Full range	10			10			
CMRR	Common-mode rejection ratio	V_O = 0, V_{IC} = V_{ICR} min, R_S = 50 Ω	25°C	90	110		90	110		dB
			Full range	85			85			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD\pm} / \Delta V_{IO}$)	V_{DD} = 4.6 V to 16 V	25°C	90	110		90	110		dB
			Full range	85			85			
I_{DD}	Supply current	V_O = 2.5 V, No load	25°C		1	1.5		1	1.5	mA
			Full range			1.5			1.5	

operating characteristics at specified free-air temperature, V_{DD} = 5 V

PARAMETER		TEST CONDITIONS	T_A†	TLC2201AM			TLC2201BM			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
SR	Slew rate at unity gain	V_O = 0.5 V to 2.5 V, R_L = 10 kΩ, C_L = 100 pF	25°C	1.8	2.5		1.8	2.5		V/µs
			Full range	1.1			1.1			
V_n	Equivalent input noise voltage (see Note 5)	f = 10 Hz	25°C		18	35		18	25	nV/√Hz
		f = 1 kHz	25°C		8	15		8	12	
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 to 1 Hz	25°C		0.5			0.5		µV
		f = 0.1 to 10 Hz	25°C		0.7			0.7		
I_n	Equivalent input noise current		25°C		0.6			0.6		fA/√Hz
	Gain-bandwidth product	f = 10 kHz, R_L = 10 kΩ, C_L = 100 pF	25°C		1.8			1.8		MHz
ϕ_m	Phase margin at unity gain	R_L = 10 kΩ, C_L = 100 pF	25°C		45°			45°		

†Full range is – 55°C to 125°C.

NOTES: 4. Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at T_A = 150°C extrapolated to T_A = 25°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

5. This parameter is tested on a sample basis for the TLC2201A and on all devices for the TLC2201B. For other test requirements, please contact the factory. This statement has no bearing on testing or nontesting of other parameters.

electrical characteristics at $V_{DD\pm}$ = ±5 V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	TLC2201Y			UNIT
			MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_{IC} = 0, R_S = 50 Ω		100	500	µV
	Input offset voltage long-term drift (see Note 4)			0.001	0.005	µV/mo
I_{IO}	Input offset current			0.5		pA
I_{IB}	Input bias current			1		pA
V_{ICR}	Common-mode input voltage range	R_S = 50 Ω	0 to 2.7			V
V_{OH}	Maximum high-level output voltage	R_L = 10 kΩ	4.7	4.8		V
V_{OL}	Maximum low-level output voltage	I_O = 0		0	50	mV
A_{VD}	Large-signal differential voltage amplification	V_O = 1 V to 4 V, R_L = 500 kΩ	150	315		V/mV
		V_O = 1 V to 4 V, R_L = 10 kΩ	25	55		
CMRR	Common-mode rejection ratio	V_O = 0, V_{IC} = V_{ICR}min, R_S = 50 Ω	90	110		dB
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD\pm} / \Delta V_{IO}$)	V_{DD} = 4.6 V to 16 V,	90	110		dB
I_{DD}	Supply current	V_O = 2.5 V, No load		1	1.5	mA

operating characteristics at $V_{DD\pm}$ = ± 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SR	Positive slew rate at unity gain	V_O = ± 0.5 to 2.5 V, R_L = 10 kΩ, C_L = 100 pF	1.8	2.5		V/µs
V_n	Equivalent input noise voltage	f = 10 Hz		18		nV/√Hz
		f = 1 kHz		8		
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 to 1 Hz		0.5		µV
		f = 0.1 to 10 Hz		0.7		
I_n	Equivalent input noise current			0.6		pA/√Hz
	Gain-bandwidth product	f = 10 kHz, R_L = 10 kΩ, C_L = 100 pF		1.8		MHz
ϕ_m	Phase margin at unity gain	R_L = 10 kΩ, C_L = 100 pF		48°		

NOTE: 4. Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at T_A = 150°C extrapolated to T_A = 25°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

PARAMETER MEASUREMENT INFORMATION

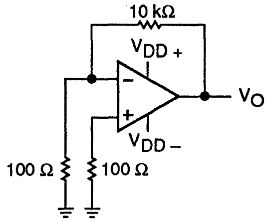
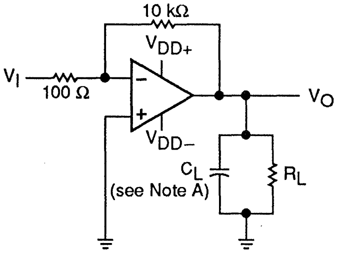
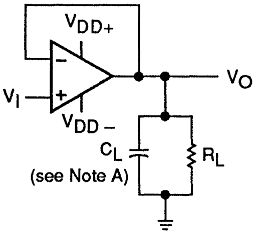


Figure 1. Noise Voltage Test Circuit



NOTE A: C_L includes fixture capacitance.

Figure 2. Phase Margin Test Circuit



NOTE A: C_L includes fixture capacitance.

Figure 3. Slew Rate Test Circuit

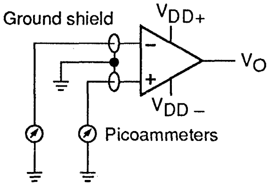


Figure 4. Input Bias and Offset Current Test Circuit

typical values

Typical values presented in this data sheet represent the median (50% point) of device parametric performance.

input bias and offset current

At the picoamp bias current level typical of the TLC2201, TLC2201A, and TLC2201B, accurate measurement of the bias current becomes difficult. Not only does this measurement require a picoammeter, but test socket leakages can easily exceed the actual device bias currents. To measure these small currents, Texas Instruments uses a two-step process. The socket leakage is measured using picoammeters with bias voltages applied but with no device in the socket. The device is then inserted in the socket, and a second test measuring both the socket leakage and the device input bias current is performed. The two measurements are then subtracted algebraically to determine the bias current of the device.

noise

Texas Instruments offers automated production noise testing to meet individual applications requirements. Noise voltage at f = 10 Hz and f = 1 kHz is 100% tested on every TLC2201B device, while lot sample testing is performed on the TLC2201A. For other noise test requirements, please contact the factory.

TYPICAL CHARACTERISTICS

table of graphs

			FIGURE
V_{IO}	Input offset voltage	Distribution	5
I_{IB}	Input bias current	vs Common-mode voltage vs Temperature	6 7
CMRR	Common-mode rejection ratio	vs Frequency	8
V_{OM}	Maximum peak output voltage	vs Output current vs Temperature	9 10
$V_{O(PP)}$	Maximum peak-to-peak output voltage	vs Frequency	11
V_{OH}	High-level output voltage	vs Frequency vs Current vs Temperature	12 13 14
V_{OL}	Low-level output voltage	vs Output current vs Temperature	15 16
A_{VD}	Differential voltage amplification	vs Frequency vs Temperature	17 18
I_{OS}	Short-circuit output current	vs Supply voltage vs Temperature	19 20
I_{DD}	Supply current	vs Supply voltage vs Temperature	21 22
SR	Slew rate	vs Supply voltage vs Temperature	23 24
	Pulse response	Small-signal Large-signal	25, 26 27, 28
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	0.1 to 1 Hz 0.1 to 10 Hz	29 30
	Gain-bandwidth product	vs Supply voltage vs Temperature	31 32
ϕ_m	Phase margin	vs Supply voltage vs Temperature	33 34
	Phase shift	vs Frequency	17

TYPICAL CHARACTERISTICS†

DISTRIBUTION OF TLC2201
INPUT OFFSET VOLTAGE

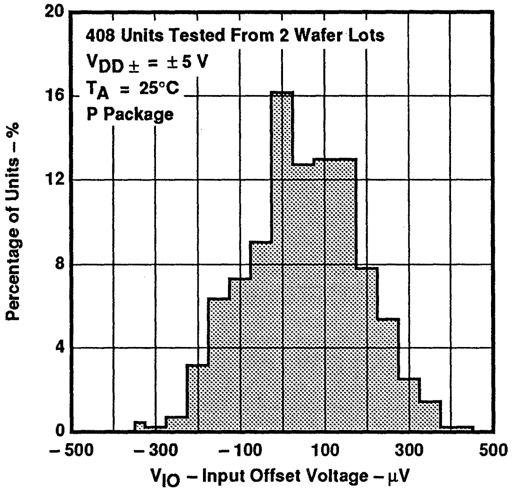


Figure 5

INPUT BIAS CURRENT
vs
COMMON-MODE INPUT VOLTAGE

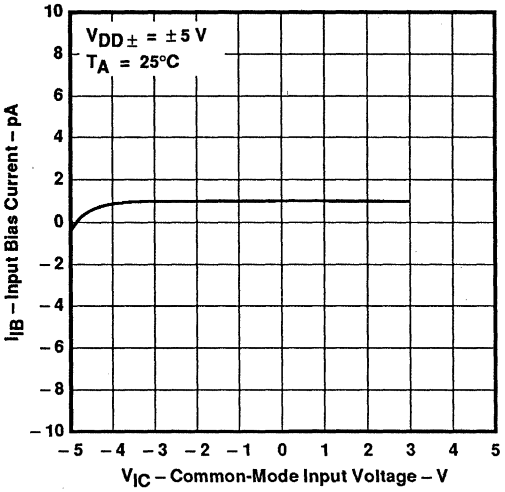


Figure 6

INPUT BIAS CURRENT
vs
FREE-AIR TEMPERATURE

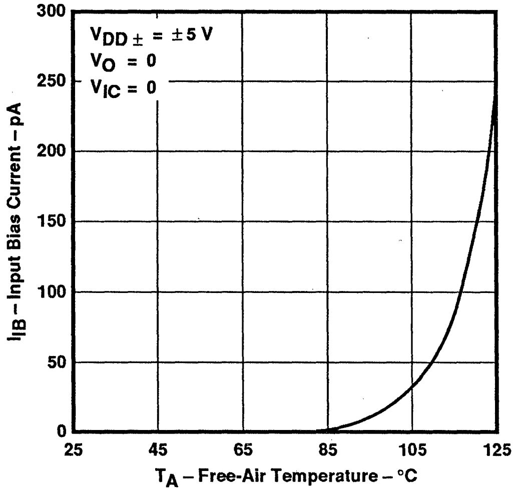


Figure 7

COMMON-MODE REJECTION RATIO
vs
FREQUENCY

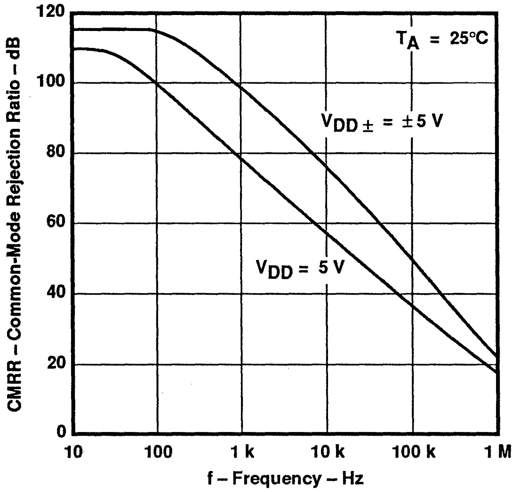
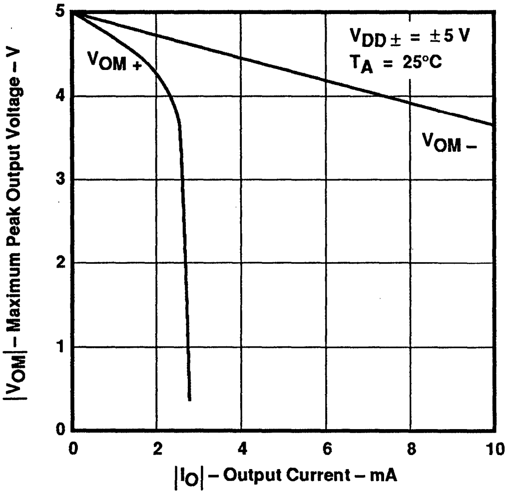


Figure 8

---

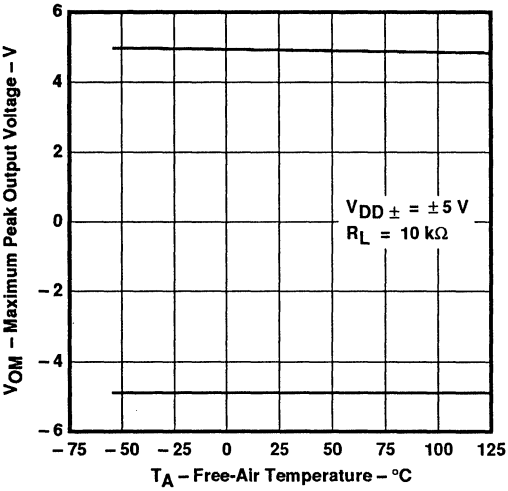
†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†



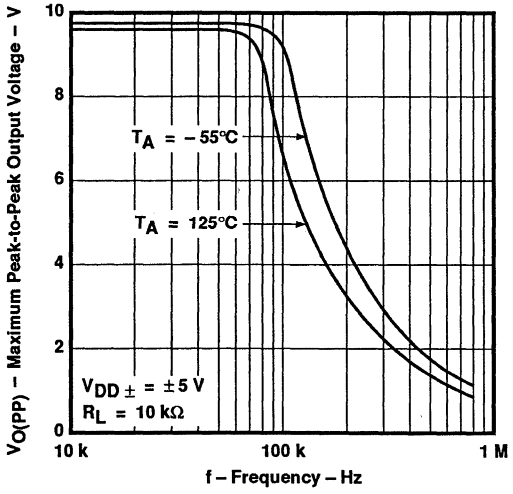
MAXIMUM PEAK OUTPUT VOLTAGE
vs
OUTPUT CURRENT

Figure 9



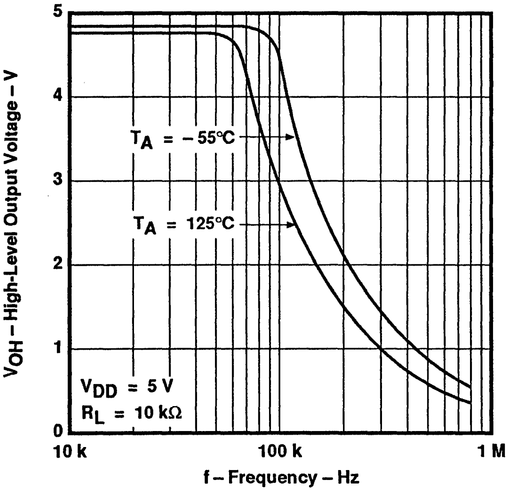
MAXIMUM PEAK OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

Figure 10



MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE
vs
FREQUENCY

Figure 11



HIGH-LEVEL OUTPUT VOLTAGE
vs
FREQUENCY

Figure 12

---

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS[†]

HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

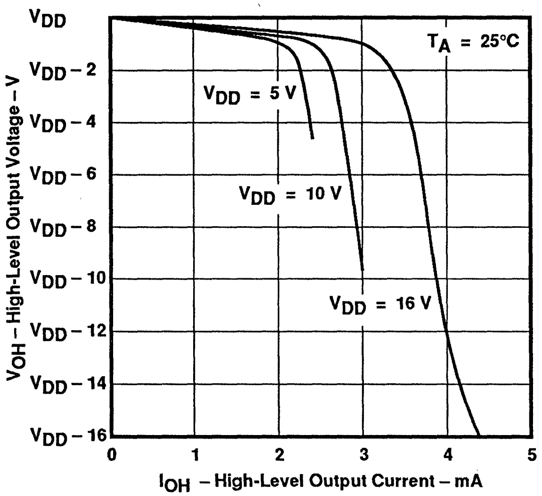


Figure 13

HIGH-LEVEL OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

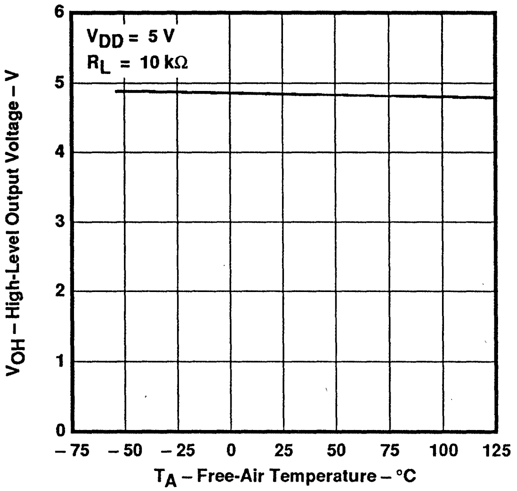


Figure 14

LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

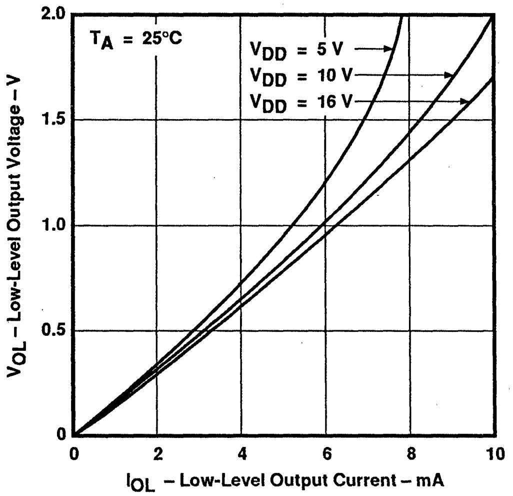


Figure 15

LOW-LEVEL OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

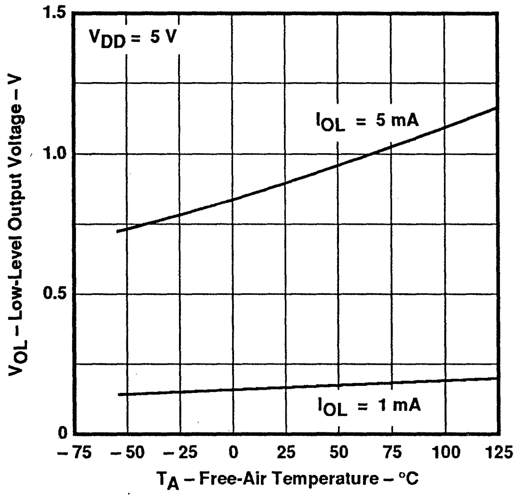


Figure 16

[†] Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION AND PHASE SHIFT
vs
FREQUENCY

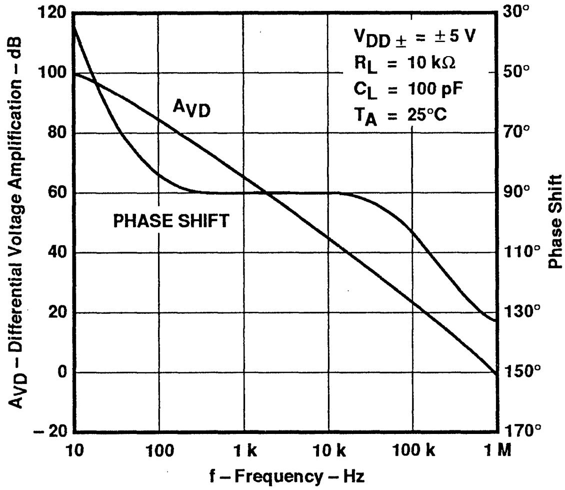


Figure 17

LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION
vs
FREE-AIR TEMPERATURE

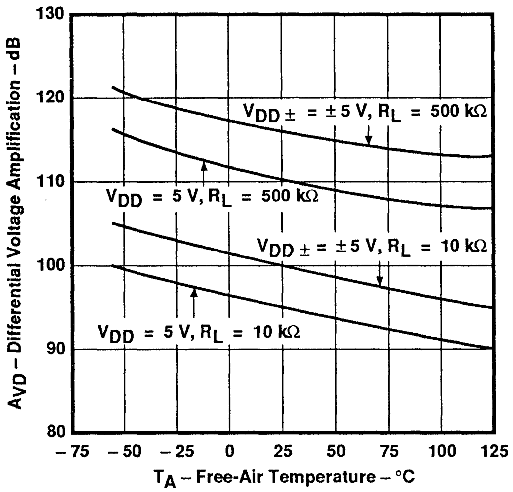


Figure 18

SHORT-CIRCUIT OUTPUT CURRENT
vs
SUPPLY VOLTAGE

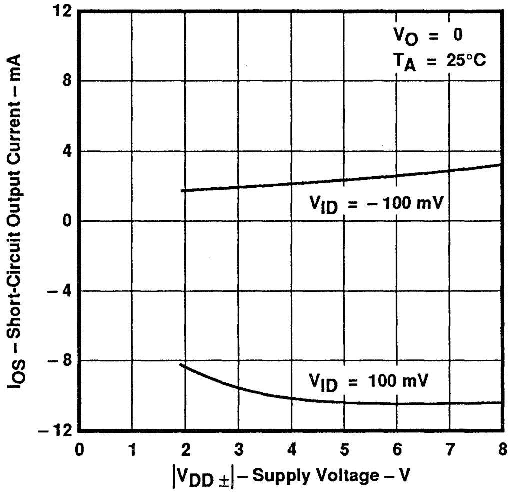


Figure 19

SHORT-CIRCUIT OUTPUT CURRENT
vs
FREE-AIR TEMPERATURE

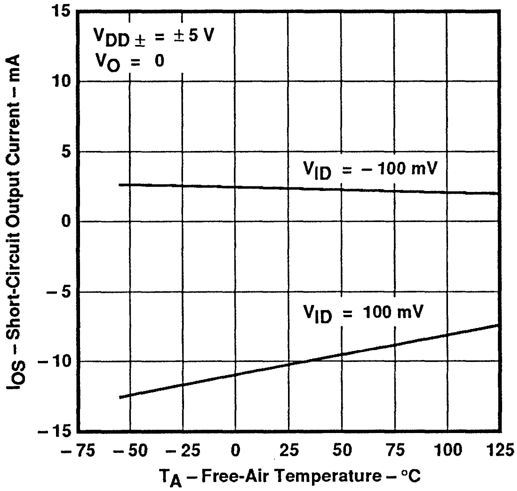


Figure 20

---

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

SUPPLY CURRENT
vs
SUPPLY VOLTAGE

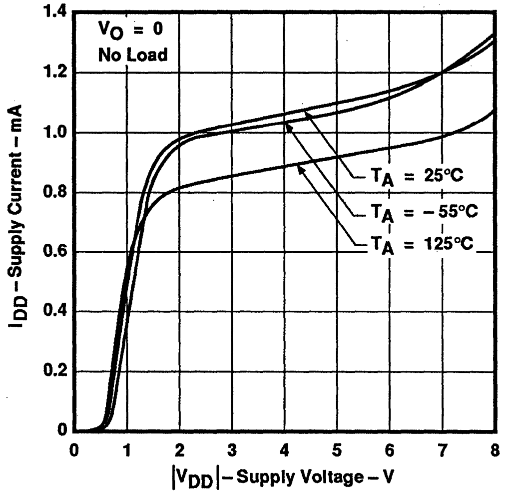


Figure 21

SUPPLY CURRENT
vs
FREE-AIR TEMPERATURE

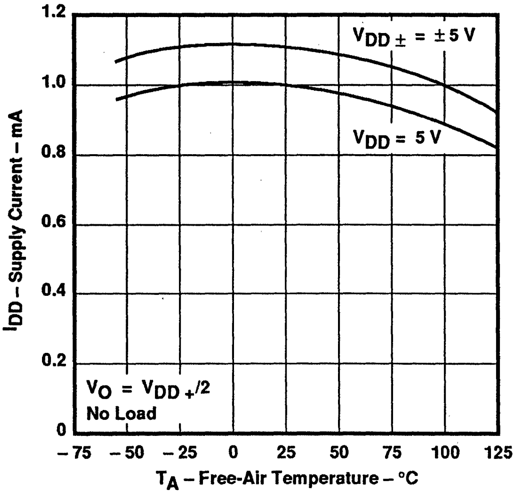


Figure 22

SLEW RATE
vs
SUPPLY VOLTAGE

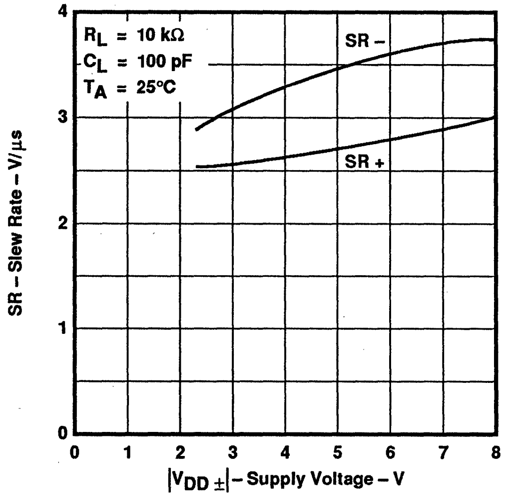


Figure 23

SLEW RATE
vs
FREE-AIR TEMPERATURE

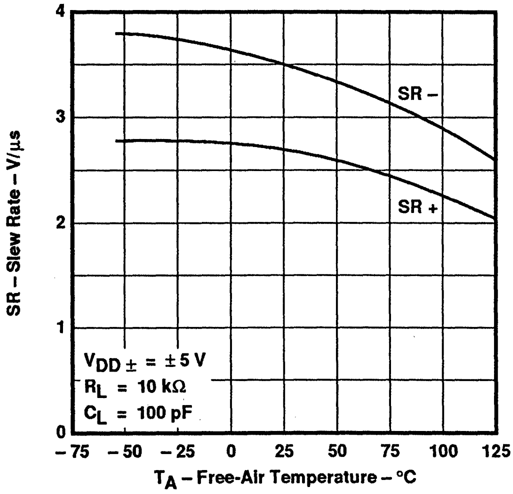


Figure 24

---

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS

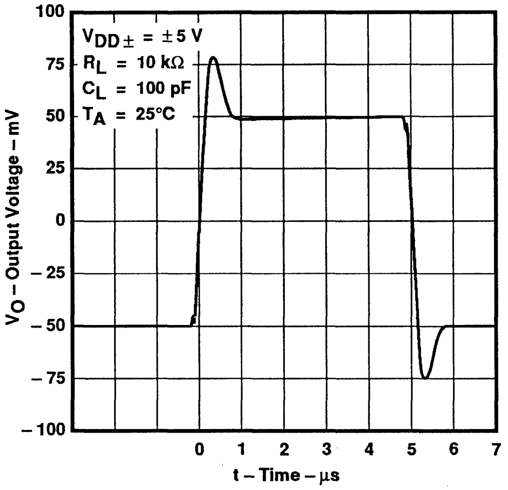

VOLTAGE-FOLLOWER
SMALL-SIGNAL
PULSE RESPONSE

Figure 25

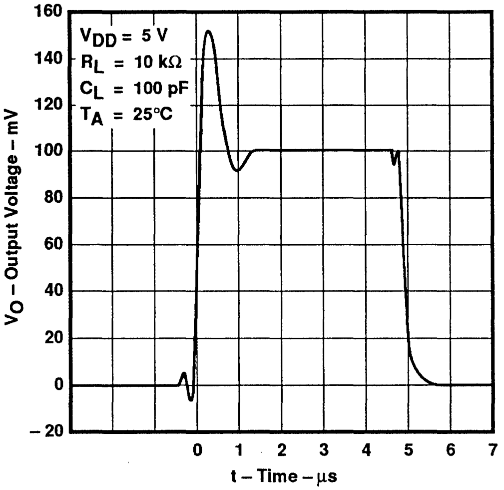

VOLTAGE-FOLLOWER
SMALL-SIGNAL
PULSE RESPONSE

Figure 26

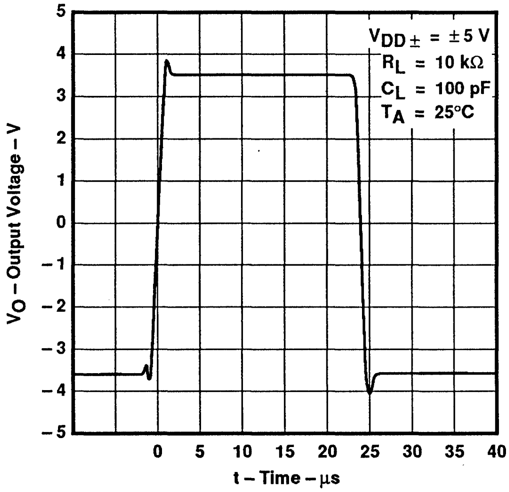

VOLTAGE-FOLLOWER
LARGE-SIGNAL
PULSE RESPONSE

Figure 27

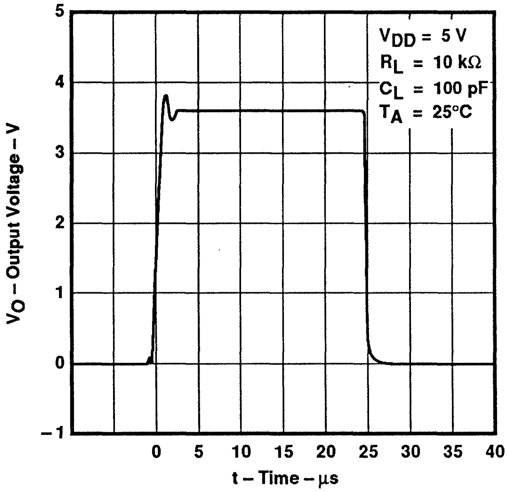

VOLTAGE-FOLLOWER
LARGE-SIGNAL
PULSE RESPONSE

Figure 28

TYPICAL CHARACTERISTICS†

PEAK-TO-PEAK EQUIVALENT
INPUT NOISE VOLTAGE
0.1 TO 1 Hz

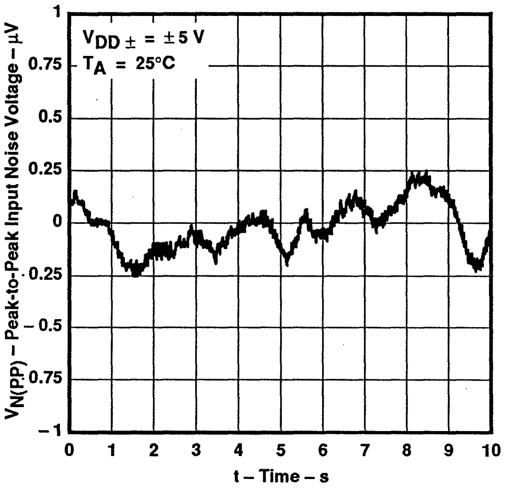


Figure 29

PEAK-TO-PEAK EQUIVALENT
INPUT NOISE VOLTAGE
0.1 TO 10 Hz

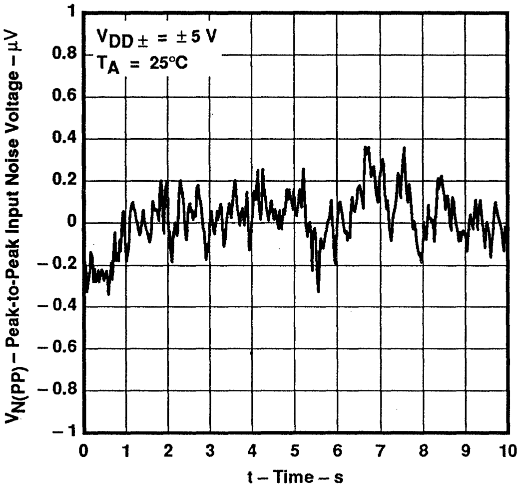


Figure 30

GAIN-BANDWIDTH PRODUCT
VS
SUPPLY VOLTAGE

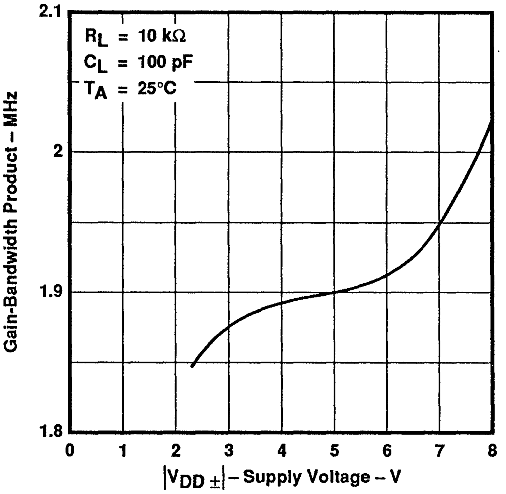


Figure 31

GAIN-BANDWIDTH PRODUCT
VS
FREE-AIR TEMPERATURE

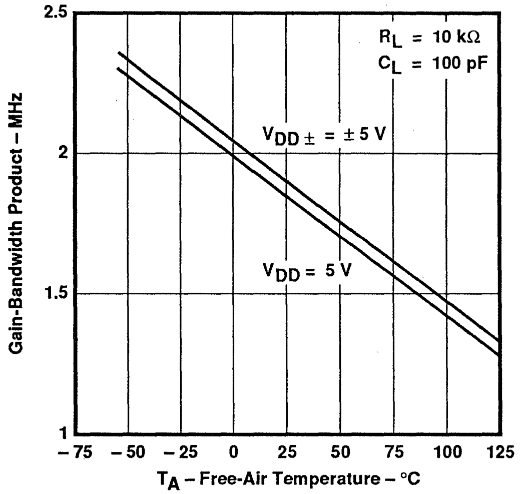


Figure 32

---

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

PHASE MARGIN
vs
SUPPLY VOLTAGE

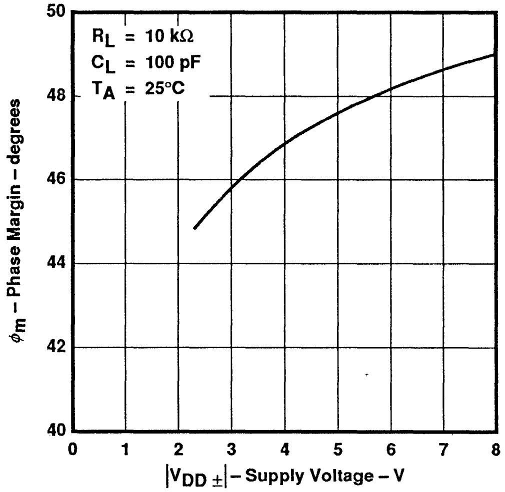


Figure 33

PHASE MARGIN
vs
FREE-AIR TEMPERATURE

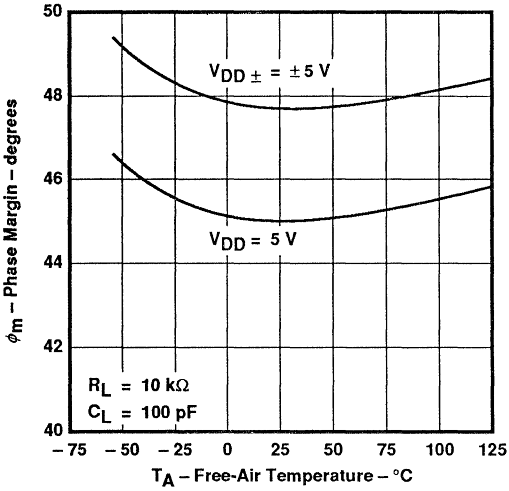


Figure 34

---

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

APPLICATION INFORMATION

latch-up avoidance

Because CMOS devices are susceptible to latch-up due to their inherent parasitic thyristors, the TLC2201, TLC2201A, and TLC2201B inputs and outputs are designed to withstand –100-mA surge currents without sustaining latch-up; however, techniques reducing the chance of latch-up should be used whenever possible. Internal protection diodes should not be forward biased in normal operation. Applied input and output voltages should not exceed the supply voltage by more than 300 mV. Care should be exercised when using capacitive coupling on pulse generators. Supply transients should be shunted by the use of decoupling capacitors (0.1 µF typical) located across the supply rails as close to the device as possible.

electrostatic discharge protection

These devices use internal ESD-protection circuits that prevent functional failures at voltages at or below 2000 V. Care should be exercised in handling these devices as exposure to ESD may result in degradation of the device parametric performance.

TLC2202, TLC2202A,TLC2202B, TLC2202Y
Advanced LinCMOS™ LOW-NOISE PRECISION DUAL OPERATIONAL AMPLIFIERS

D3497, MAY 1990 - REVISED AUGUST 1991

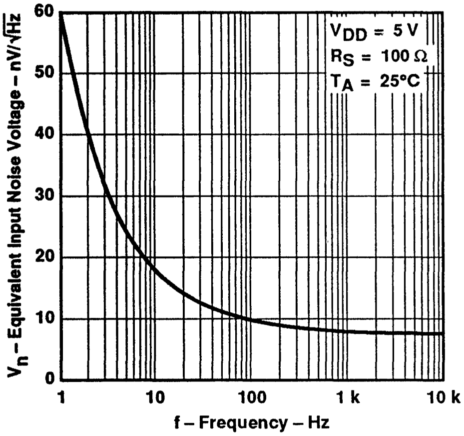
- **TLC2202B Is 100% Tested for Noise:**
  25 nV/√Hz Max at f = 10 Hz
  12 nV/√Hz Max at f = 1 kHz
- **Low Input Offset Voltage . . . 500 µV Max**
- **Excellent Offset Voltage Stability With Temperature . . . 0.5 µV/°C Typ**
- **Rail-to-Rail Output Swing**
- **Low Input Bias Current . . . 1 pA Typ at T_A = 25°C**
- **Common-Mode Input Voltage Range Includes the Negative Rail**

description

The TLC2202, TLC2202A, TLC2202B, and TLC2202Y are precision, low-noise operational amplifiers using Texas Instruments Advanced LinCMOS™ process. These devices combine the noise performance of the lowest-noise JFET amplifiers with the dc precision available previously only in bipolar amplifiers. The Advanced LinCMOS™ process uses silicon-gate technology to obtain input offset voltage stability with temperature and time that far exceeds that obtainable using metal-gate technology. In addition, this technology makes possible input impedance levels that meet or exceed levels offered by top-gate JFET and expensive dielectric-isolated devices.

The combination of excellent dc and noise performance with a common-mode input voltage range that includes the negative rail makes these devices an ideal choice for high-impedance, low-level signal-conditioning applications in either single-supply or split-supply configurations.

TYPICAL EQUIVALENT
INPUT NOISE VOLTAGE
vs
FREQUENCY



The device inputs and outputs are designed to withstand –100-mA surge currents without sustaining latch-up. In addition, internal ESD-protection circuits prevent functional failures at voltages up to 2000 V as tested under MIL-STD-883C, Method 3015.2; however, care should be exercised in handling these devices as exposure to ESD may result in degradation of the device parametric performance.

AVAILABLE OPTIONS

T_A	V_{IO} max AT 25°C	V_n max f = 10 Hz AT 25°C	V_n max f = 1 kHz AT 25°C	PACKAGE				CHIP FORM (Y)
				SMALL-OUTLINE (D)	CHIP CARRIER (FK)	CERAMIC DIP (JG)	PLASTIC DIP (P)	
0°C to 70°C	500 µV	25 nV/√Hz	12 nV/√Hz	TLC2202BCD	——	——	TLC2202BCP	TLC2202Y
	500 µV	35 nV/√Hz	15 nV/√Hz	TLC2202ACD	——	——	TLC2202ACP	
	1 mV	——	——	TLC2202CD	——	——	TLC2202CP	
– 40°C to 85°C	500 µV	25 nV/√Hz	12 nV/√Hz	TLC2202BID	——	——	TLC2202BIP	
	500 µV	35 nV/√Hz	15 nV/√Hz	TLC2202AID	——	——	TLC2202AIP	
	1 mV	——	——	TLC2202ID	——	——	TLC2202IP	
– 55°C to 125°C	500 µV	25 nV/√Hz	12 nV/√Hz	TLC2202BMD	TLC2202BMFK	TLC2202BMJG	TLC2202BMP	
	500 µV	35 nV/√Hz	15 nV/√Hz	TLC2202AMD	TLC2202AMFK	TLC2202AMJG	TLC2202AMP	
	1 mV	——	——	TLC2202MD	TLC2202MFK	TLC2202MJG	TLC2202MP	

D packages are available taped-and-reeled. Add "R" suffix to device type (e.g., TLC2202BCDR). Chips are tested at 25°C.

Advanced LinCMOS is a trademark of Texas Instruments Incorporated.

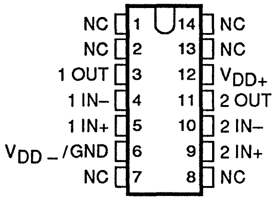
TEXAS INSTRUMENTS
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

On products compliant to MIL-STD-883, Class B, all parameters are tested unless otherwise noted. On all other products, production processing does not necessarily include testing of all parameters.

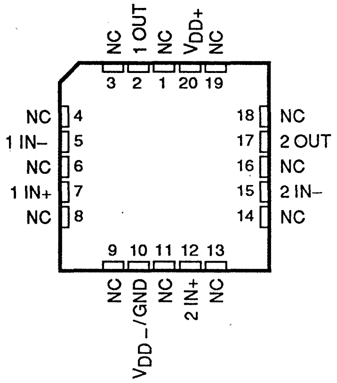
description (continued)

C-suffix devices are characterized for operation from 0°C to 70°C. The I-suffix devices are characterized for operation from −40°C to 85°C. The M-suffix devices are characterized for operation over the full military temperature range of −55°C to 125°C.

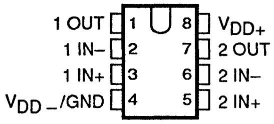
D PACKAGE
(TOP VIEW)



FK PACKAGE
(TOP VIEW)

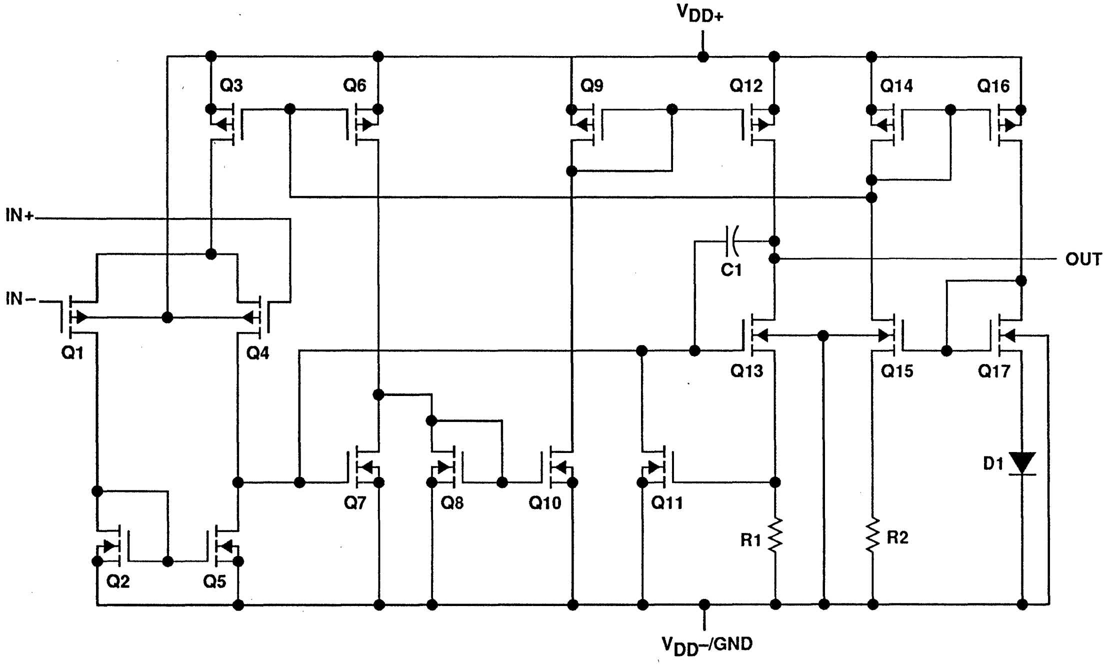


JG OR P PACKAGE
(TOP VIEW)



NC – No internal connection

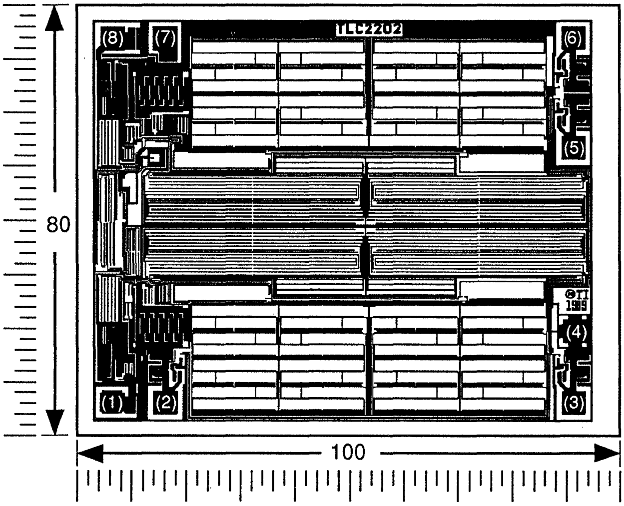
equivalent schematic (each amplifier)

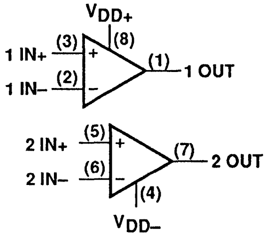


chip information

These chips, properly assembled, display characteristics similar to the TLE2202. Thermal compression or ultrasonic bonding may be used on the doped aluminum bonding pads. Chips may be mounted with conductive epoxy or a gold-silicon preform.

BONDING PAD ASSIGNMENTS





CHIP THICKNESS:
15 TYPICAL

BONDING PADS:
4 X 4 MINIMUM

T_J max = 150°C

TOLERANCES
ARE ± 10%

ALL DIMENSIONS
ARE IN MILS

PIN (4) INTERNALLY
CONNECTED TO
BACKSIDE OF CHIP

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{DD+} (see Note 1)	8 V
Supply voltage, V_{DD-}	– 8 V
Differential input voltage (see Note 2)	± 16 V
Input voltage, V_I (any input)	± 8 V
Input current, I_I (each input)	± 5 mA
Output current, I_O (each output)	± 50 mA
Duration of short-circuit current at (or below) 25°C (see Note 3)	unlimited
Continuous total dissipation	See Dissipation Rating Table
Operating free-air temperature range, T_A: C-suffix	0°C to 70°C
I-suffix	– 40°C to 85°C
M-suffix	– 55°C to 125°C
Storage temperature range	– 65°C to 150°C
Case temperature for 60 seconds: FK package	260°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D or P package	260°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: JG package	300°C

NOTES: 1. All voltage values, except differential voltages, are with respect to the midpoint between V_{DD+} and V_{DD-}.
2. Differential voltages are at the noninverting input with respect to the inverting input.
3. The output may be shorted to either supply. Temperature and/or supply voltages must be limited to ensure that the maximum dissipation rating is not exceeded.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING	$T_A = 125°C$ POWER RATING
D	950 mW	7.6 mW/°C	608 mW	494 mW	190 mW
FK	1375 mW	11.0 mW/°C	880 mW	715 mW	275 mW
JG	1050 mW	8.4 mW/°C	672 mW	546 mW	210 mW
P	1000 mW	8.0 mW/°C	640 mW	520 mW	200 mW

recommended operating conditions

	C-SUFFIX		I-SUFFIX		M-SUFFIX		UNIT
	MIN	MAX	MIN	MAX	MIN	MAX	
Supply voltage, $V_{DD\pm}$	± 2.3	± 8	± 2.3	± 8	± 2.3	± 8	V
Common-mode input voltage, V_{IC}	V_{DD-}	$V_{DD+} - 2.3$	V_{DD-}	$V_{DD+} - 2.3$	V_{DD-}	$V_{DD+} - 2.3$	V
Operating free-air temperature, T_A	0	70	– 40	85	– 55	125	°C

electrical characteristics at specified free-air temperature, $V_{DD\pm}$ = ±5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A	MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	V_{IC} = 0, R_S = 50 Ω	25°C		100	1000	µV
			Full range			1150	
α_{VIO}	Temperature coefficient of input offset voltage		Full range		0.5		µV/°C
	Input offset voltage long-term drift (see Note 4)		25°C		0.001	0.005	
I_{IO}	Input offset current		25°C		0.5		µV/mo
			Full range			100	pA
I_{IB}	Input bias current		25°C		1		
			Full range			100	pA
V_{ICR}	Common-mode input voltage range	R_S = 50 Ω	Full range	−5 to 2.7			V
V_{OM+}	Maximum positive peak output voltage swing	R_L = 10 kΩ	25°C	4.7	4.8		V
			Full range	4.7			
V_{OM-}	Maximum negative peak output voltage swing		25°C	−4.7	−4.9		
			Full range	−4.7			V
A_{VD}	Large-signal differential voltage amplification	V_O = ±4 V, R_L = 500 kΩ	25°C	300	560		V/mV
			Full range	200			
		V_O = ±4 V, R_L = 10 kΩ	25°C	50	100		
			Full range	25			
CMRR	Common-mode rejection ratio	V_O = 0, V_{IC} = V_{ICR} min, R_S = 50 Ω	25°C	80	115		dB
			Full range	80			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD\pm}/\Delta V_{IO}$)	$V_{DD\pm}$ = ±2.3 V to ±8 V	25°C	80	110		dB
			Full range	80			
I_{DD}	Supply current	V_O = 0, No load	25°C		1.8	2.5	mA
			Full range			2.5	

operating characteristics at specified free-air temperature, $V_{DD\pm}$ = ±5 V

PARAMETER		TEST CONDITIONS	T_A	MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain	V_O = ±2.3 V, R_L = 10 kΩ, C_L = 100 pF	25°C	1.8	2.7		V/µs
			Full range	1.3			
V_n	Equivalent input noise voltage	f = 10 Hz	25°C		18		nV/√Hz
		f = 1 kHz	25°C		8		
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 to 1 Hz	25°C		0.5		µV
		f = 0.1 to 10 Hz	25°C		0.7		
I_n	Equivalent input noise current		25°C		0.6		fA/√Hz
	Gain-bandwidth product	f = 10 kHz, R_L = 10 kΩ, C_L = 100 pF	25°C		1.9		MHz
ϕ_m	Phase margin at unity gain	R_L = 10 kΩ, C_L = 100 pF	25°C		48°		

†Full range is 0°C to 70°C.

NOTE 4: Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at T_A = 150°C extrapolated to T_A = 25°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

electrical characteristics at specified free-air temperature, $V_{DD\pm} = \pm 5$ V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A	TLC2202AC			TLC2202BC			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	$V_{IC} = 0$, $R_S = 50\ \Omega$	25°C		80	500		80	500	µV
			Full range			650			650	
α_{VIO}	Temperature coefficient of input offset voltage		Full range		0.5			0.5		µV/°C
	Input offset voltage long-term drift (see Note 4)		25°C		0.001	0.005		0.001	0.005	µV/mo
I_{IO}	Input offset current		25°C		0.5			0.5		pA
			Full range			100			100	
I_{IB}	Input bias current		25°C		1			1		pA
			Full range			100			100	
V_{ICR}	Common-mode input voltage range	$R_S = 50\ \Omega$	Full range	−5 to 2.7			−5 to 2.7			V
V_{OM+}	Maximum positive peak output voltage swing	$R_L = 10\ k\Omega$	25°C	4.7	4.8		4.7	4.8		V
			Full range	4.7			4.7			
V_{OM-}	Maximum negative peak output voltage swing		25°C	−4.7	−4.9		−4.7	−4.9		V
			Full range	−4.7			−4.7			
A_{VD}	Large-signal differential voltage amplification	$V_O = \pm 4$ V, $R_L = 500\ k\Omega$	25°C	300	560		300	560		V/mV
			Full range	200			200			
		$V_O = \pm 4$ V, $R_L = 10\ k\Omega$	25°C	50	100		50	100		
			Full range	25			25			
CMRR	Common-mode rejection ratio	$V_O = 0$, $V_{IC} = V_{ICR}$ min, $R_S = 50\ \Omega$	25°C	80	115		80	115		dB
			Full range	80			80			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD\pm} / \Delta V_{IO}$)	$V_{DD\pm} = \pm 2.3$ V to ± 8 V	25°C	80	110		80	110		dB
			Full range	80			80			
I_{DD}	Supply current	$V_O = 0$, No load	25°C		1.8	2.5		1.8	2.5	mA
			Full range			2.5			2.5	

operating characteristics at specified free-air temperature, $V_{DD\pm} = \pm 5$ V

PARAMETER		TEST CONDITIONS	T_A	TLC2202AC			TLC2202BC			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
SR	Slew rate at unity gain	$V_O = \pm 2.3$ V, $R_L = 10\ k\Omega$, $C_L = 100$ pF	25°C	1.8	2.7		1.8	2.7		V/µs
			Full range	1.3			1.3			
V_n	Equivalent input noise voltage (see Note 5)	f = 10 Hz	25°C		18	35		18	25	nV/√Hz
		f = 1 kHz	25°C		8	15		8	12	
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 to 1 Hz	25°C		0.5			0.5		µV
		f = 0.1 to 10 Hz	25°C		0.7			0.7		
I_n	Equivalent input noise current		25°C		0.6			0.6		fA/√Hz
	Gain-bandwidth product	f = 10 kHz, $R_L = 10\ k\Omega$, $C_L = 100$ pF	25°C		1.9			1.9		MHz
ϕ_m	Phase margin at unity gain	$R_L = 10\ k\Omega$, $C_L = 100$ pF	25°C		48°			48°		

†Full range is 0°C to 70°C.

NOTES: 4. Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at $T_A = 150$°C extrapolated to $T_A = 25$°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

5. This parameter is tested on a sample basis for the TLC2202A and on all devices for the TLC2202B. For other test requirements, please contact the factory. This statement has no bearing on testing or nontesting of other parameters.

electrical characteristics at specified free-air temperature, V_{DD} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A	MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	$V_{IC} = 0$, $R_S = 50\ \Omega$	25°C		100	1000	µV
			Full range			1150	
α_{VIO}	Temperature coefficient of input offset voltage		Full range		0.5		µV/°C
	Input offset voltage long-term drift (see Note 4)		25°C		0.001	0.005	
I_{IO}	Input offset current		25°C		0.5		µV/mo
			Full range			100	pA
I_{IB}	Input bias current		25°C		1		
			Full range			100	pA
V_{ICR}	Common-mode input voltage range	$R_S = 50\ \Omega$	Full range	0 to 2.7			V
V_{OM+}	Maximum positive peak output voltage swing	$R_L = 10\ k\Omega$	25°C	4.7	4.8		V
			Full range	4.7			
V_{OM-}	Maximum negative peak output voltage swing		25°C		0	50	
			Full range			50	V
A_{VD}	Large-signal differential voltage amplification	V_O = 1 V to 4 V, $R_L = 500\ k\Omega$	25°C	150	315		V/mV
			Full range	100			
		V_O = 1 V to 4 V, $R_L = 10\ k\Omega$	25°C	25	55		
			Full range	15			
CMRR	Common-mode rejection ratio	$V_O = 0$, $V_{IC} = V_{ICR}$ min, $R_S = 50\ \Omega$	25°C	75	110		dB
			Full range	75			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD\pm} / \Delta V_{IO}$)	V_{DD} = 4.6 V to 16 V	25°C	80	110		dB
			Full range	80			
I_{DD}	Supply current	$V_O = 0$, No load	25°C		1.7	2.4	mA
			Full range			2.4	

operating characteristics at specified free-air temperature, V_{DD} = 5 V

PARAMETER		TEST CONDITIONS	T_A	MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain	V_O = 0.5 V to 2.5 V, $R_L = 10\ k\Omega$, C_L = 100 pF	25°C	1.6	2.5		V/µs
			Full range	1.1			
V_n	Equivalent input noise voltage	f = 10 Hz	25°C		18		nV/√Hz
		f = 1 kHz	25°C		8		
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 to 1 Hz	25°C		0.5		µV
		f = 0.1 to 10 Hz	25°C		0.7		
I_n	Equivalent input noise current		25°C		0.6		fA/√Hz
	Gain-bandwidth product	f = 10 kHz, $R_L = 10\ k\Omega$, C_L = 100 pF	25°C		1.9		MHz
ϕ_m	Phase margin at unity gain	$R_L = 10\ k\Omega$, C_L = 100 pF	25°C		47°		

† Full range is 0°C to 70°C

NOTE 4: Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at T_A = 150°C extrapolated to T_A = 25°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

electrical characteristics at specified free-air temperature, V_{DD} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A	TLC2202AC			TLC2202BC			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_{IC} = 0, R_S = 50 Ω	25°C		80	500		80	500	μV
			Full range			650			650	
α_{VIO}	Temperature coefficient of input offset voltage		Full range		0.5			0.5		μV/°C
	Input offset voltage long-term drift (see Note 4)		25°C		0.001	0.005		0.001	0.005	μV/mo
I_{IO}	Input offset current		25°C		0.5			0.5		pA
			Full range			100			100	
I_{IB}	Input bias current		25°C		1			1		pA
			Full range			100			100	
V_{ICR}	Common-mode input voltage range	R_S = 50 Ω	Full range	0 to 2.7			0 to 2.7			V
V_{OH}	Maximum high-level output voltage	R_L = 10 kΩ	25°C	4.7	4.8		4.7	4.8		V
			Full range	4.7			4.7			
V_{OL}	Maximum low-level output voltage	I_O = 0	25°C		0	50		0	50	mV
			Full range			50			50	
A_{VD}	Large-signal differential voltage amplification	V_O = 1 V to 4 V, R_L = 500 kΩ	25°C	150	315		150	315		V/mV
			Full range	100			100			
		V_O = 1 V to 4 V, R_L = 10 kΩ	25°C	25	55		25	55		
			Full range	15			15			
CMRR	Common-mode rejection ratio	V_O = 0, V_{IC} = V_{ICR} min, R_S = 50 Ω	25°C	75	110		75	110		dB
			Full range	75			75			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD\pm} / \Delta V_{IO}$)	V_{DD} = 4.6 V to 16 V	25°C	80	110		80	110		dB
			Full range	80			80			
I_{DD}	Supply current	V_O = 2.5 V, No load	25°C		1.7	2.4		1.7	2.4	mA
			Full range			2.4			2.4	

operating characteristics at specified free-air temperature, V_{DD} = 5 V

PARAMETER		TEST CONDITIONS	T_A	TLC2202AC			TLC2202BC			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
SR	Slew rate at unity gain	V_O = 0.5 V to 2.5 V, R_L = 10 kΩ, C_L = 100 pF	25°C	1.6	2.5		1.6	2.5		V/μs
			Full range	1.1			1.1			
V_n	Equivalent input noise voltage (see Note 5)	f = 10 Hz	25°C		18	35		18	25	nV/√Hz
		f = 1 kHz	25°C		8	15		8	12	
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 to 1 Hz	25°C		0.5			0.5		μV
		f = 0.1 to 10 Hz	25°C		0.7			0.7		
I_n	Equivalent input noise current		25°C		0.6			0.6		fA/√Hz
	Gain-bandwidth product	f = 10 kHz, R_L = 10 kΩ, C_L = 100 pF	25°C		1.9			1.9		MHz
ϕ_m	Phase margin at unity gain	R_L = 10 kΩ, C_L = 100 pF	25°C		47°			47°		

†Full range is 0°C to 70°C.

NOTES: 4. Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at T_A = 150°C extrapolated to T_A = 25°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

5. This parameter is tested on a sample basis for the TLC2202A and on all devices for the TLC2202B. For other test requirements, please contact the factory. This statement has no bearing on testing or nontesting of other parameters.

electrical characteristics at specified free-air temperature, $V_{DD\pm}$ = ±5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A	MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	V_{IC} = 0, R_S = 50 Ω	25°C		100	1000	µV
			Full range			1200	
α_{VIO}	Temperature coefficient of input offset voltage		Full range		0.5		µV/°C
	Input offset voltage long-term drift (see Note 4)		25°C		0.001	0.005	
I_{IO}	Input offset current		25°C		0.5		µV/mo
			Full range			150	pA
I_{IB}	Input bias current		25°C		1		
			Full range			150	pA
V_{ICR}	Common-mode input voltage range	R_S = 50 Ω	Full range	−5 to 2.7			V
V_{OM+}	Maximum positive peak output voltage swing	R_L = 10 kΩ	25°C	4.7	4.8		V
			Full range	4.7			
V_{OM-}	Maximum negative peak output voltage swing		25°C	−4.7	−4.9		
			Full range	−4.7			V
A_{VD}	Large-signal differential voltage amplification	V_O = ±4 V, R_L = 500 kΩ	25°C	300	560		V/mV
			Full range	150			
		V_O = ±4 V, R_L = 10 kΩ	25°C	50	100		
			Full range	25			
CMRR	Common-mode rejection ratio	V_O = 0, V_{IC} = V_{ICR} min, R_S = 50 Ω	25°C	80	115		dB
			Full range	80			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD\pm} / \Delta V_{IO}$)	V_{DD} = ±2.3 V to ±8 V	25°C	80	110		dB
			Full range	80			
I_{DD}	Supply current	V_O = 0, No load	25°C		1.8	2.5	mA
			Full range			2.5	

operating characteristics at specified free-air temperature, $V_{DD\pm}$ = ±5 V

PARAMETER		TEST CONDITIONS	T_A	MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain	V_O = ±2.3 V, R_L = 10 kΩ, C_L = 100 pF	25°C	1.8	2.7		V/µs
			Full range	1.2			
V_n	Equivalent input noise voltage	f = 10 Hz	25°C		18		nV/√Hz
		f = 1 kHz	25°C		8		
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 to 1 Hz	25°C		0.5		µV
		f = 0.1 to 10 Hz	25°C		0.7		
I_n	Equivalent input noise current		25°C		0.6		fA/√Hz
	Gain-bandwidth product	f = 10 kHz, R_L = 10 kΩ, C_L = 100 pF	25°C		1.9		MHz
ϕ_m	Phase margin at unity gain	R_L = 10 kΩ, C_L = 100 pF	25°C		48°		

†Full range is −40°C to 85°C.

NOTE 4: Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at T_A = 150°C extrapolated to T_A = 25°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

electrical characteristics at specified free-air temperature, $V_{DD\pm} = \pm 5$ V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A	TLC2202AI			TLC2202BI			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	$V_{IC} = 0$, $R_S = 50\ \Omega$	25°C		80	500		80	500	μV
			Full range			700			700	
α_{VIO}	Temperature coefficient of input offset voltage		Full range		0.5			0.5		μV/°C
	Input offset voltage long-term drift (see Note 4)		25°C		0.001	0.005		0.001	0.005	μV/mo
I_{IO}	Input offset current		25°C		0.5			0.5		pA
			Full range			150			150	
I_{IB}	Input bias current		25°C		1			1		pA
			Full range			150			150	
V_{ICR}	Common-mode input voltage range	$R_S = 50\ \Omega$	Full range	−5 to 2.7			−5 to 2.7			V
V_{OM+}	Maximum positive peak output voltage swing	$R_L = 10\ k\Omega$	25°C	4.7	4.8		4.7	4.8		V
			Full range	4.7			4.7			
V_{OM-}	Maximum negative peak output voltage swing		25°C	−4.7	−4.9		−4.7	−4.9		V
			Full range	−4.7			−4.7			
A_{VD}	Large-signal differential voltage amplification	$V_O = \pm 4$ V, $R_L = 500\ k\Omega$	25°C	300	560		300	560		V/mV
			Full range	150			150			
		$V_O = \pm 4$ V, $R_L = 10\ k\Omega$	25°C	50	100		50	100		
			Full range	25			25			
CMRR	Common-mode rejection ratio	$V_O = 0$, $V_{IC} = V_{ICR}$ min, $R_S = 50\ \Omega$	25°C	80	115		80	115		dB
			Full range	80			80			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD\pm} / \Delta V_{IO}$)	$V_{DD\pm} = \pm 2.3$ V to ± 8 V	25°C	80	110		80	110		dB
			Full range	80			80			
I_{DD}	Supply current	$V_O = 0$, No load	25°C		1.8	2.5		1.8	2.5	mA
			Full range			2.5			2.5	

operating characteristics at specified free-air temperature, $V_{DD\pm} = \pm 5$ V

PARAMETER		TEST CONDITIONS	T_A	TLC2202AI			TLC2202BI			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
SR	Slew rate at unity gain	$V_O = \pm 2.3$ V, $R_L = 10\ k\Omega$, $C_L = 100$ pF	25°C	1.8	2.7		1.8	2.7		V/μs
			Full range	1.2			1.2			
V_n	Equivalent input noise voltage (see Note 5)	f = 10 Hz	25°C		18	35		18	25	nV/√Hz
		f = 1 kHz	25°C		8	15		8	12	
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 to 1 Hz	25°C		0.5			0.5		μV
		f = 0.1 to 10 Hz	25°C		0.7			0.7		
I_n	Equivalent input noise current		25°C		0.6			0.6		fA/√Hz
	Gain-bandwidth product	f = 10 kHz, $R_L = 10\ k\Omega$, $C_L = 100$ pF	25°C		1.9			1.9		MHz
ϕ_m	Phase margin at unity gain	$R_L = 10\ k\Omega$, $C_L = 100$ pF	25°C		48°			48°		

†Full range is −40°C to 85°C.

NOTES: 4. Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at $T_A = 150$°C extrapolated to $T_A = 25$°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

5. This parameter is tested on a sample basis for the TLC2202A and on all devices for the TLC2202B. For other test requirements, please contact the factory. This statement has no bearing on testing or nontesting of other parameters.

electrical characteristics at specified free-air temperature, V_{DD} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A	MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	V_{IC} = 0, R_S = 50 Ω	25°C		100	1000	µV
			Full range			1200	
α_{VIO}	Temperature coefficient of input offset voltage		Full range		0.5		µV/°C
	Input offset voltage long-term drift (see Note 4)		25°C		0.001	0.005	
I_{IO}	Input offset current		25°C		0.5		µV/mo
			Full range			150	pA
I_{IB}	Input bias current		25°C		1		
			Full range			150	pA
V_{ICR}	Common-mode input voltage range	R_S = 50 Ω	Full range	0 to 2.7			V
V_{OM+}	Maximum positive peak output voltage swing	R_L = 10 kΩ	25°C	4.7	4.8		V
			Full range	4.7			
V_{OM-}	Maximum negative peak output voltage swing		25°C		0	50	
			Full range			50	V
A_{VD}	Large-signal differential voltage amplification	V_O = 1 V to 4 V, R_L = 500 kΩ	25°C	150	315		V/mV
			Full range	100			
		V_O = 1 V to 4 V, R_L = 10 kΩ	25°C	25	55		
			Full range	15			
CMRR	Common-mode rejection ratio	V_O = 0, V_{IC} = V_{ICR} min, R_S = 50 Ω	25°C	75	110		dB
			Full range	75			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD\pm}/\Delta V_{IO}$)	V_{DD} = 4.6 V to 16 V	25°C	80	110		dB
			Full range	80			
I_{DD}	Supply current	V_O = 2.5 V, No load	25°C		1.7	2.4	mA
			Full range			2.4	

operating characteristics at specified free-air temperature, V_{DD} = 5 V

PARAMETER		TEST CONDITIONS	T_A	MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain	V_O = 0.5 V to 2.5 V, R_L = 10 kΩ, C_L = 100 pF	25°C	1.6	2.5		V/µs
			Full range	1			
V_n	Equivalent input noise voltage	f = 10 Hz	25°C		18		nV/√Hz
		f = 1 kHz	25°C		8		
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 to 1 Hz	25°C		0.5		µV
		f = 0.1 to 10 Hz	25°C		0.7		
I_n	Equivalent input noise current		25°C		0.6		fA/√Hz
	Gain-bandwidth product	f = 10 kHz, R_L = 10 kΩ, C_L = 100 pF	25°C		1.9		MHz
ϕ_m	Phase margin at unity gain	R_L = 10 kΩ, C_L = 100 pF	25°C		47°		

†Full range is −40°C to 85°C.

NOTE 4: Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at T_A = 150°C extrapolated to T_A = 25°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

electrical characteristics at specified free-air temperature, V_{DD} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A	TLC2202AI			TLC2202BI			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_{IC} = 0, R_S = 50 Ω	25°C		80	500		80	500	µV
			Full range			700			700	
α_{VIO}	Temperature coefficient of input offset voltage		Full range		0.5			0.5		µV/°C
	Input offset voltage long-term drift (see Note 4)		25°C		0.001	0.005		0.001	0.005	µV/mo
I_{IO}	Input offset current		25°C		0.5			0.5		pA
			Full range			150			150	
I_{IB}	Input bias current		25°C		1			1		pA
			Full range			150			150	
V_{ICR}	Common-mode input voltage range	R_S = 50 Ω	Full range	0 to 2.7			0 to 2.7			V
V_{OH}	Maximum high-level output voltage	R_L = 10 kΩ	25°C	4.7	4.8		4.7	4.8		V
			Full range	4.7			4.7			
V_{OL}	Maximum low-level output voltage	I_O = 0	25°C		0	50		0	50	mV
			Full range			50			50	
A_{VD}	Large-signal differential voltage amplification	V_O = 1 V to 4 V, R_L = 500 kΩ	25°C	150	315		150	315		V/mV
			Full range	100			100			
		V_O = 1 V to 4 V, R_L = 10 kΩ	25°C	25	55		25	55		
			Full range	15			15			
CMRR	Common-mode rejection ratio	V_O = 0, V_{IC} = V_{ICR} min, R_S = 50 Ω	25°C	75	110		75	110		dB
			Full range	75			75			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD\pm} / \Delta V_{IO}$)	V_{DD} = 4.6 V to 16 V	25°C	80	110		80	110		dB
			Full range	80			80			
I_{DD}	Supply current	V_O = 2.5 V, No load	25°C		1.7	2.4		1.7	2.4	mA
			Full range			2.4			2.4	

operating characteristics at specified free-air temperature, V_{DD} = 5 V

PARAMETER		TEST CONDITIONS	T_A	TLC2202AI			TLC2202BI			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
SR	Slew rate at unity gain	V_O = 0.5 V to 2.5 V, R_L = 10 kΩ, C_L = 100 pF	25°C	1.6	2.5		1.6	2.5		V/µs
			Full range	1			1			
V_n	Equivalent input noise voltage (see Note 5)	f = 10 Hz	25°C		18	35		18	25	nV/√Hz
		f = 1 kHz	25°C		8	15		8	12	
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 to 1 Hz	25°C		0.5			0.5		µV
		f = 0.1 to 10 Hz	25°C		0.7			0.7		
I_n	Equivalent input noise current		25°C		0.6			0.6		fA/√Hz
	Gain-bandwidth product	f = 10 kHz, R_L = 10 kΩ, C_L = 100 pF	25°C		1.9			1.9		MHz
ϕ_m	Phase margin at unity gain	R_L = 10 kΩ, C_L = 100 pF	25°C		47°			47°		

†Full range is −40°C to 85°C.

NOTES: 4. Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at T_A = 150°C extrapolated to T_A = 25°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

5. This parameter is tested on a sample basis for the TLC2202A and on all devices for the TLC2202B. For other test requirements, please contact the factory. This statement has no bearing on testing or nontesting of other parameters.

electrical characteristics at specified free-air temperature, $V_{DD\pm} = \pm 5$ V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A	MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	$V_{IC} = 0$, $R_S = 50\ \Omega$	25°C		100	1000	µV
			Full range			1200	
α_{VIO}	Temperature coefficient of input offset voltage		Full range		0.5		µV/°C
	Input offset voltage long-term drift (see Note 4)		25°C		0.001	0.005*	
I_{IO}	Input offset current		25°C		0.5		µV/mo
			Full range			500	pA
I_{IB}	Input bias current		25°C		1		
			Full range			500	pA
V_{ICR}	Common-mode input voltage range	$R_S = 50\ \Omega$	Full range	−5 to 2.7			V
V_{OM+}	Maximum positive peak output voltage swing	$R_L = 10\ k\Omega$	25°C	4.7	4.8		V
			Full range	4.7			
V_{OM-}	Maximum negative peak output voltage swing		25°C	−4.7	−4.9		
			Full range	−4.7			V
A_{VD}	Large-signal differential voltage amplification	$V_O = \pm 4$ V, $R_L = 500\ k\Omega$	25°C	300	560		V/mV
			Full range	100			
		$V_O = \pm 4$ V, $R_L = 10\ k\Omega$	25°C	50	100		
			Full range	25			
CMRR	Common-mode rejection ratio	$V_O = 0$, $V_{IC} = V_{ICR}$ min, $R_S = 50\ \Omega$	25°C	80	115		dB
			Full range	80			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD\pm} / \Delta V_{IO}$)	$V_{DD} = \pm 2.3$ V to ± 8 V	25°C	80	110		dB
			Full range	80			
I_{DD}	Supply current	$V_O = 0$, No load	25°C		1.8	2.5	mA
			Full range			2.5	

operating characteristics at specified free-air temperature, $V_{DD\pm} = \pm 5$ V

PARAMETER		TEST CONDITIONS	T_A	MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain	$V_O = \pm 2.3$ V, $R_L = 10\ k\Omega$, $C_L = 100$ pF	25°C	1.8	2.7		V/µs
			Full range	1.1			
V_n	Equivalent input noise voltage	f = 10 Hz	25°C		18		nV/√Hz
		f = 1 kHz	25°C		8		
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 to 1 Hz	25°C		0.5		µV
		f = 0.1 to 10 Hz	25°C		0.7		
I_n	Equivalent input noise current		25°C		0.6		fA/√Hz
	Gain-bandwidth product	f = 10 kHz, $R_L = 10\ k\Omega$, $C_L = 100$ pF	25°C		1.9		MHz
ϕ_m	Phase margin at unity gain	$R_L = 10\ k\Omega$, $C_L = 100$ pF	25°C		48°		

*On products compliant to MIL-STD-883, Class B, this parameter is not production tested.

†Full range is −55°C to 125°C.

NOTE 4: Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at $T_A = 150°C$ extrapolated to $T_A = 25°C$ using the Arrhenius equation and assuming an activation energy of 0.96 eV.

electrical characteristics at specified free-air temperature, $V_{DD\pm}$ = ±5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A	TLC2202AM			TLC2202BM			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_{IC} = 0, R_S = 50 Ω	25°C		80	500		80	500	μV
			Full range			750			750	
α_{VIO}	Temperature coefficient of input offset voltage		Full range		0.5			0.5		μV/°C
	Input offset voltage long-term drift (see Note 4)		25°C		0.001	0.005*		0.001	0.005*	μV/mo
I_{IO}	Input offset current		25°C		0.5			0.5		pA
			Full range			500			500	
I_{IB}	Input bias current		25°C		1			1		pA
			Full range			500			500	
V_{ICR}	Common-mode input voltage range	R_S = 50 Ω	Full range	−5 to 2.7			−5 to 2.7			V
V_{OM+}	Maximum positive peak output voltage swing	R_L = 10 kΩ	25°C	4.7	4.8		4.7	4.8		V
			Full range	4.7			4.7			
V_{OM-}	Maximum negative peak output voltage swing		25°C	−4.7	−4.9		−4.7	−4.9		V
			Full range	−4.7			−4.7			
A_{VD}	Large-signal differential voltage amplification	V_O = ±4 V, R_L = 500 kΩ	25°C	300	560		300	560		V/mV
			Full range	100			100			
		V_O = ±4 V, R_L = 10 kΩ	25°C	50	100		50	100		
			Full range	25			25			
CMRR	Common-mode rejection ratio	V_O = 0, V_{IC} = V_{ICR} min, R_S = 50 Ω	25°C	80	115		80	115		dB
			Full range	80			80			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD\pm} / \Delta V_{IO}$)	$V_{DD\pm}$ = ±2.3 V to ±8 V	25°C	80	110		80	110		dB
			Full range	80			80			
I_{DD}	Supply current	V_O = 0, No load	25°C		1.8	2.5		1.8	2.5	mA
			Full range			2.5			2.5	

operating characteristics at specified free-air temperature, $V_{DD\pm}$ = ±5 V

PARAMETER		TEST CONDITIONS	T_A	TLC2202AM			TLC2202BM			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
SR	Slew rate at unity gain	V_O = ±2.3 V, R_L = 10 kΩ, C_L = 100 pF	25°C	1.8	2.7		1.8	2.7		V/μs
			Full range	1.1			1.1			
V_n	Equivalent input noise voltage (see Note 5)	f = 10 Hz	25°C		18	35*		18	25*	nV/√Hz
		f = 1 kHz	25°C		8	15*		8	12*	
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 to 1 Hz	25°C		0.5			0.5		μV
		f = 0.1 to 10 Hz	25°C		0.7			0.7		
I_n	Equivalent input noise current		25°C		0.6			0.6		fA/√Hz
	Gain-bandwidth product	f = 10 kHz, R_L = 10 kΩ, C_L = 100 pF	25°C		1.9			1.9		MHz
ϕ_m	Phase margin at unity gain	R_L = 10 kΩ, C_L = 100 pF	25°C		48°			48°		

*On products compliant to MIL-STD-883, Class B, this parameter is not production tested.

†Full range is −55°C to 125°C.

NOTES: 4. Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at T_A = 150°C extrapolated to T_A = 25°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

5. This parameter is tested on a sample basis for the TLC2202A and on all devices for the TLC2202B. For other test requirements, please contact the factory. This statement has no bearing on testing or nontesting of other parameters.

electrical characteristics at specified free-air temperature, V_{DD} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A	MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	$V_{IC} = 0$, $R_S = 50\ \Omega$	25°C		100	1000	μV
			Full range			1250	
α_{VIO}	Temperature coefficient of input offset voltage		Full range		0.5		μV/°C
	Input offset voltage long-term drift (see Note 4)		25°C		0.001	0.005*	
I_{IO}	Input offset current		25°C		0.5		μV/mo
			Full range			500	pA
I_{IB}	Input bias current		25°C		1		
			Full range			500	pA
V_{ICR}	Common-mode input voltage range	$R_S = 50\ \Omega$	Full range	0 to 2.7			V
V_{OM+}	Maximum positive peak output voltage swing	$R_L = 10\ k\Omega$	25°C	4.7	4.8		V
			Full range	4.7			
V_{OM-}	Maximum negative peak output voltage swing		25°C		0	50	
			Full range			50	V
A_{VD}	Large-signal differential voltage amplification	$V_O = 1$ V to 4 V, $R_L = 500\ k\Omega$	25°C	150	315		V/mV
			Full range	75			
		$V_O = 1$ V to 4 V, $R_L = 10\ k\Omega$	25°C	25	55		
			Full range	10			
CMRR	Common-mode rejection ratio	$V_{IC} = V_{ICR}$ min, $R_S = 50\ \Omega$	25°C	75	110		dB
			Full range	75			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD\pm} / \Delta V_{IO}$)	$V_{DD} = 4.6$ V to 16 V	25°C	80	110		dB
			Full range	80			
I_{DD}	Supply current	$V_O = 2.5$ V, No load	25°C		1.7	2.4	mA
			Full range			2.4	

operating characteristics at specified free-air temperature, V_{DD} = 5 V

PARAMETER		TEST CONDITIONS	T_A	MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain	$V_O = 0.5$ V to 2.5 V, $R_L = 10\ k\Omega$, $C_L = 100$ pF	25°C	1.6	2.5		V/μs
			Full range	0.9			
V_n	Equivalent input noise voltage	f = 10 Hz	25°C		18		nV/√Hz
		f = 1 kHz	25°C		8		
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 to 1 Hz	25°C		0.5		μV
		f = 0.1 to 10 Hz	25°C		0.7		
I_n	Equivalent input noise current		25°C		0.6		fA/√Hz
	Gain-bandwidth product	f = 10 kHz, $R_L = 10\ k\Omega$, $C_L = 100$ pF	25°C		1.9		MHz
ϕ_m	Phase margin at unity gain	$R_L = 10\ k\Omega$, $C_L = 100$ pF	25°C		47°		

*On products compliant to MIL-STD-883, Class B, this parameter is not production tested.

†Full range is −55°C to 125°C.

NOTE 4: Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at $T_A = 150°C$ extrapolated to $T_A = 25°C$ using the Arrhenius equation and assuming an activation energy of 0.96 eV.

electrical characteristics at specified free-air temperature, V_{DD} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A	TLC2202AM			TLC2202BM			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_{IC} = 0, R_S = 50 Ω	25°C		80	500		80	500	µV
			Full range			750			750	
α_{VIO}	Temperature coefficient of input offset voltage		Full range		0.5			0.5		µV/°C
	Input offset voltage long-term drift (see Note 4)		25°C		0.001	0.005*		0.001	0.005*	µV/mo
I_{IO}	Input offset current		25°C		0.5			0.5		pA
			Full range			500			500	
I_{IB}	Input bias current		25°C		1			1		pA
			Full range			500			500	
V_{ICR}	Common-mode input voltage range	R_S = 50 Ω	Full range	0 to 2.7			0 to 2.7			V
V_{OH}	Maximum high-level output voltage	R_L = 10 kΩ	25°C	4.7	4.8		4.7	4.8		V
			Full range	4.7			4.7			
V_{OL}	Maximum low-level output voltage	I_O = 0	25°C		0	50		0	50	mV
			Full range			50			50	
A_{VD}	Large-signal differential voltage amplification	V_O = 1 V to 4 V, R_L = 500 kΩ	25°C	150	315		150	315		V/mV
			Full range	75			75			
		V_O = 1 V to 4 V, R_L = 10 kΩ	25°C	25	55		25	55		
			Full range	10			10			
CMRR	Common-mode rejection ratio	V_{IC} = V_{ICR} min, R_S = 50 Ω	25°C	75	110		75	110		dB
			Full range	75			75			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD\pm} / \Delta V_{IO}$)	V_{DD} = 4.6 V to 16 V	25°C	80	110		80	110		dB
			Full range	80			80			
I_{DD}	Supply current	V_O = 2.5 V, No load	25°C		1.7	2.4		1.7	2.4	mA
			Full range			2.4			2.4	

operating characteristics at specified free-air temperature, V_{DD} = 5 V

PARAMETER		TEST CONDITIONS	T_A	TLC2202AM			TLC2202BM			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
SR	Slew rate at unity gain	V_O = 0.5 V to 2.5 V, R_L = 10 kΩ, C_L = 100 pF	25°C	1.6	2.5		1.6	2.5		V/µs
			Full range	0.9			0.9			
V_n	Equivalent input noise voltage (see Note 5)	f = 10 Hz	25°C		18	35*		18	25*	nV/√Hz
		f = 1 kHz	25°C		8	15*		8	12*	
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 to 1 Hz	25°C		0.5			0.5		µV
		f = 0.1 to 10 Hz	25°C		0.7			0.7		
I_n	Equivalent input noise current		25°C		0.6			0.6		fA/√Hz
	Gain-bandwidth product	f = 10 kHz, R_L = 10 kΩ, C_L = 100 pF	25°C		1.9			1.9		MHz
ϕ_m	Phase margin at unity gain	R_L = 10 kΩ, C_L = 100 pF	25°C		47°			47°		

*On products compliant to MIL-STD-883, Class B, this parameter is not production tested.

†Full range is −55°C to 125°C.

NOTES: 4. Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at T_A = 150°C extrapolated to T_A = 25°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

5. This parameter is tested on a sample basis for the TLC2202A and on all devices for the TLC2202B. For other test requirements, please contact the factory. This statement has no bearing on testing or nontesting of other parameters.

electrical characteristics, V_{DD} = 5 V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	V_{IC} = 0, R_S = 50 Ω		100	1000	µV
	Input offset voltage long-term drift (see Note 4)			0.001	0.005	µV/mo
I_{IO}	Input offset current			0.5		pA
I_{IB}	Input bias current			1		pA
V_{ICR}	Common-mode input voltage range	R_S = 50 Ω	0 to 2.7			V
V_{OH}	Maximum high-level output voltage	R_L = 10 kΩ	4.7	4.8		V
V_{OL}	Maximum low-level output voltage	I_O = 0		0	50	mV
A_{VD}	Large-signal differential voltage amplification	V_O = 1 V to 4 V, R_L = 500 kΩ	150	315		V/mV
		V_O = 1 V to 4 V, RL = 10 kΩ	25	55		
CMRR	Common-mode rejection ratio	V_O = 0, V_{ICR}min, R_S = 50 Ω	75	110		dB
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC}/\Delta V_{IO}$)	V_{DD}= 4.6 V to 16 V,	80	110		dB
I_{DD}	Supply current	V_O = 2.5 V, No load		1.7	2.4	mA

operating characteristics, V_{DD} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain	V_O = 0.5 V to 2.5 V, RL = 10 kΩ, CL = 100 pF	1.6	2.5		V/µs
V_n	Equivalent input noise voltage	f = 10 Hz		18		nV/√Hz
		f = 1 kHz		8		
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 to 1 Hz		0.5		µV
		f = 0.1 to 10 Hz		0.7		
I_n	Equivalent input noise current			0.6		fA/√Hz
B_1	Gain-bandwidth product	f = 10 Hz, RL = 10 kΩ, CL = 100 pF		1.9		MHz
ϕ_m	Phase margin at unity gain	RL = 10 kΩ, CL = 100 pF		47°		

NOTE 4: Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at T_A = 150°C extrapolated to T_A = 25°C using the Arrhenius equation and assuming and activation energy of 0.96 eV.

PARAMETER MEASUREMENT INFORMATION

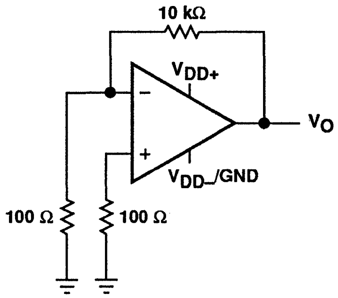
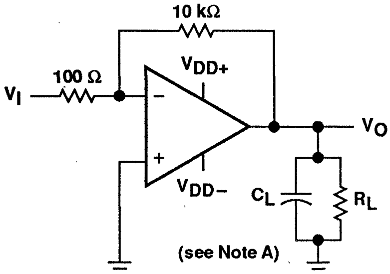
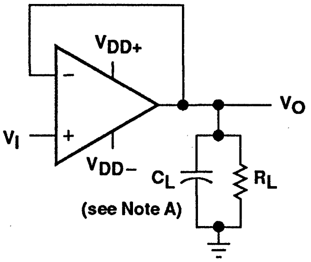


Figure 1. Noise Voltage Test Circuit



NOTE A: C_L includes fixture capacitance.

Figure 2. Phase Margin Test Circuit



NOTE A: C_L includes fixture capacitance.

Figure 3. Slew Rate Test Circuit

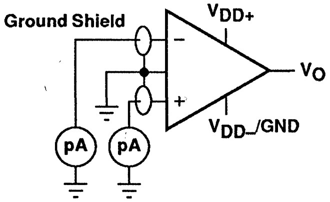


Figure 4. Input Bias and Offset Current Test Circuit

typical values

Typical values as presented in this data sheet represent the median (50% point) of device parametric performance.

input bias and offset current

At the picoamp bias current level typical of the TLC2202, TLC2202A, and TLC2202B, accurate measurement of the bias current becomes difficult. Not only does this measurement require a picoammeter, but test socket leakages can easily exceed the actual device bias currents. To measure these small currents, Texas Instruments uses a two-step process. The socket leakage is measured using picoammeters with bias voltages applied but with no device in the socket. The device is then inserted in the socket and a second test measuring both the socket leakage and the device input bias current is performed. The two measurements are then subtracted algebraically to determine the bias current of the device.

noise

Texas Instruments offers automated production noise testing to meet individual applications requirements. Noise voltage at f = 10 Hz and f = 1 kHz is 100% tested on every TLC2202B device, while lot sample testing is performed on the TLC2202A. For other noise test requirements, please contact the factory.

TYPICAL CHARACTERISTICS

table of graphs

			FIGURE
V_{IO}	Input offset voltage	Distribution	5
I_{IB}	Input bias current	vs Common-mode voltage vs Temperature	6 7
V_{OM}	Maximum peak output voltage	vs Output current vs Temperature	8, 9 10
$V_{O(PP)}$	Maximum peak-to-peak output voltage	vs Frequency	11
V_{OH}	High-level output voltage	vs Frequency vs Current vs Temperature	12 13 14
V_{OL}	Low-level output voltage	vs Output current vs Temperature	15 16
A_{VD}	Differential voltage amplification	vs Frequency vs Temperature	17 18
I_{OS}	Short-circuit output current	vs Supply voltage vs Temperature	19 20
CMRR	Common-mode rejection ratio	vs Frequency	21, 22
I_{DD}	Supply current	vs Supply voltage vs Temperature	23 24
	Pulse response	Small-signal Large-signal	25, 26 27, 28
SR	Slew rate	vs Supply voltage vs Temperature	29 30
	Noise voltage (referred to input)	0.1 to 1 Hz 0.1 to 10 Hz	31 32
	Gain-bandwidth product	vs Supply voltage vs Temperature	33 34
ϕ_m	Phase margin	vs Supply voltage vs Temperature	35 36
	Phase shift	vs Frequency	17

TYPICAL CHARACTERISTICS†

TLC2202
DISTRIBUTION OF
INPUT OFFSET VOLTAGE

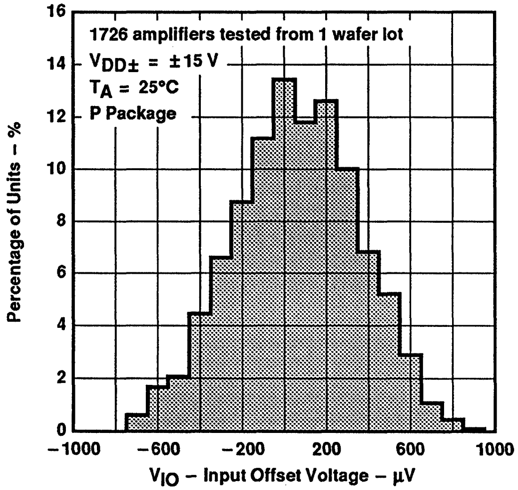


Figure 5

INPUT BIAS CURRENT
vs
COMMON-MODE INPUT VOLTAGE

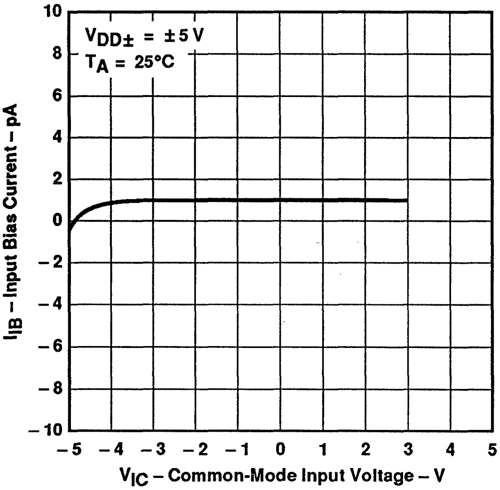


Figure 6

INPUT BIAS CURRENT
vs
FREE-AIR TEMPERATURE

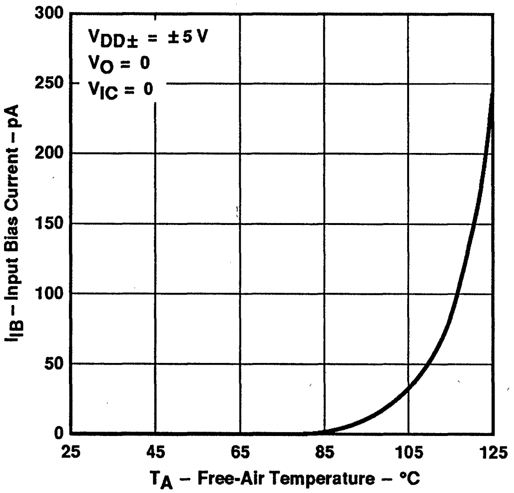


Figure 7

MAXIMUM POSITIVE PEAK
OUTPUT VOLTAGE
vs
OUTPUT CURRENT

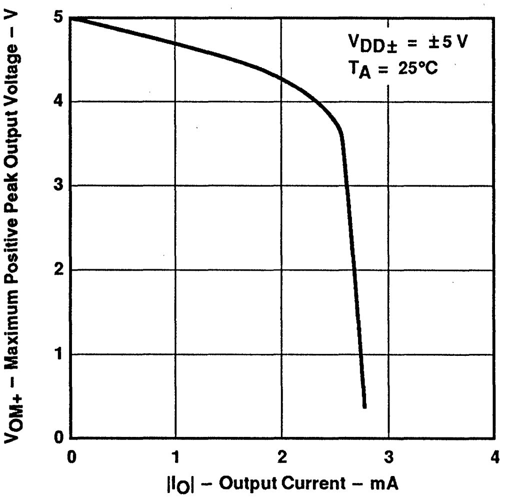


Figure 8

---

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

MAXIMUM NEGATIVE PEAK OUTPUT VOLTAGE vs OUTPUT CURRENT

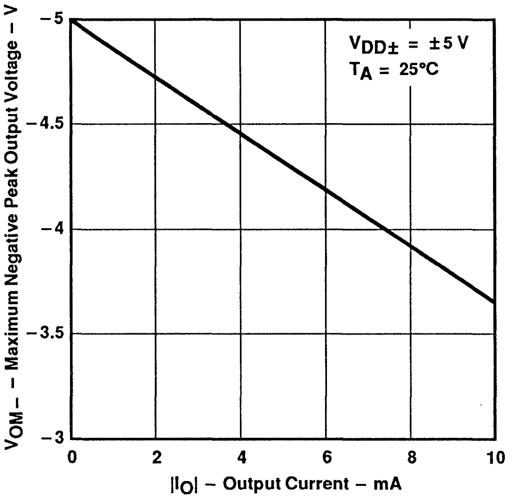


Figure 9

MAXIMUM PEAK OUTPUT VOLTAGE vs FREE-AIR TEMPERATURE

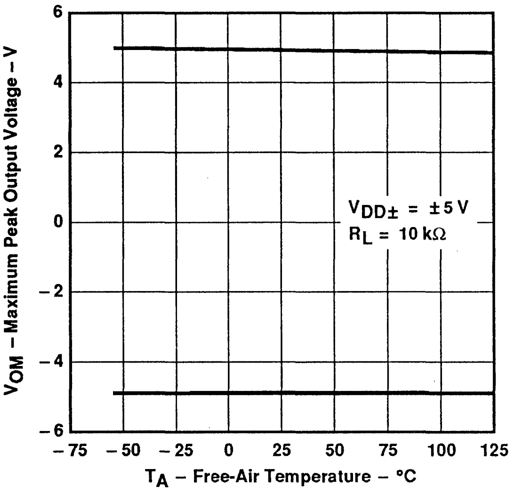


Figure 10

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE vs FREQUENCY

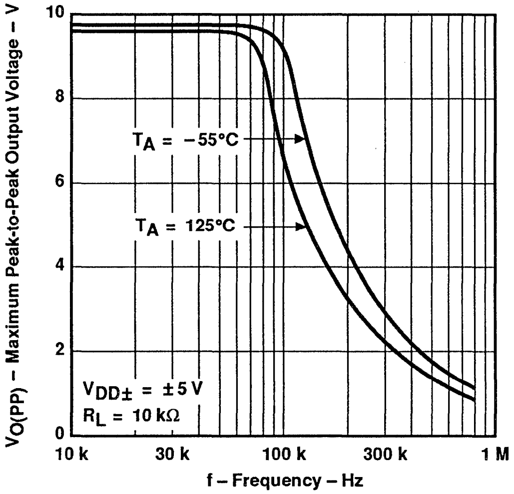


Figure 11

HIGH-LEVEL OUTPUT VOLTAGE vs FREQUENCY

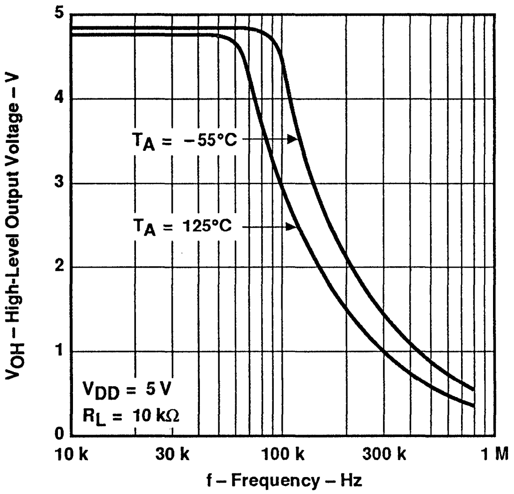


Figure 12

---

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

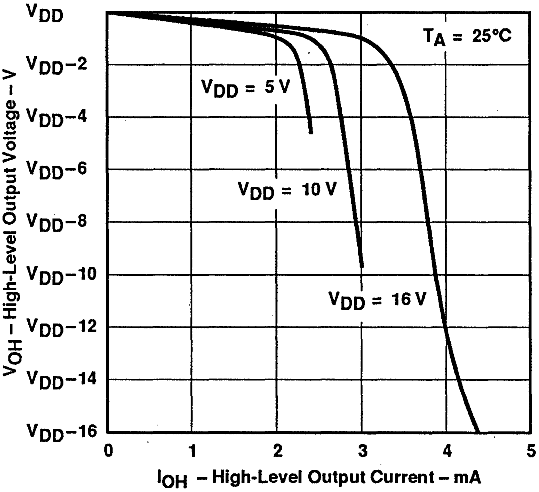


Figure 13

HIGH-LEVEL OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

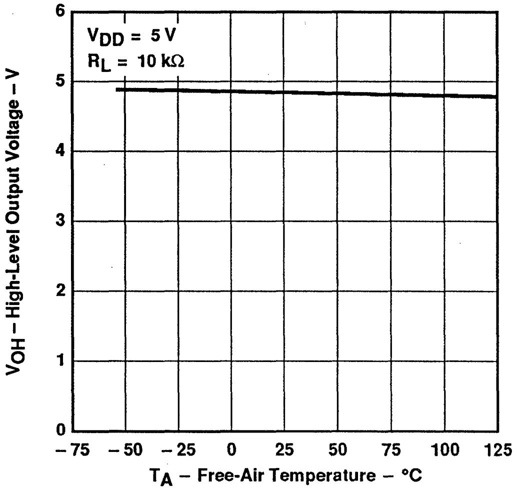


Figure 14

LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

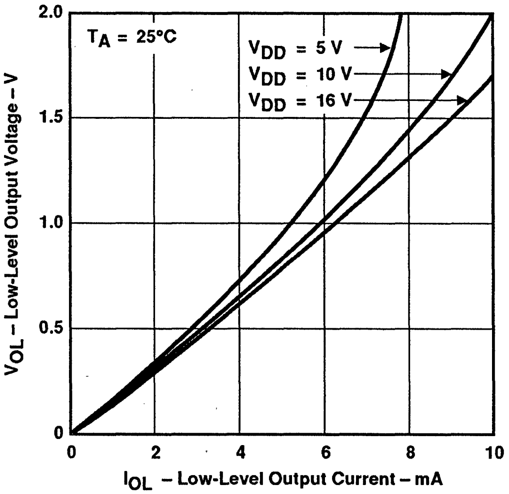


Figure 15

LOW-LEVEL OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

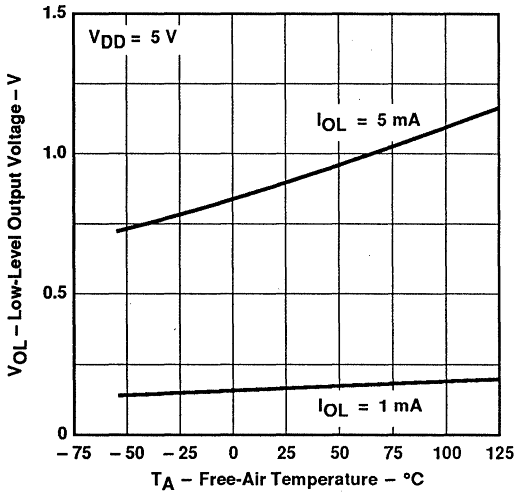


Figure 16

---

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS[†]

LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION AND PHASE SHIFT vs FREQUENCY

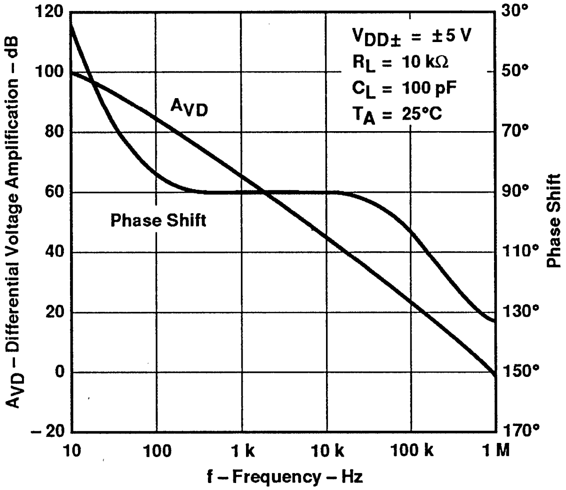


Figure 17

LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION vs FREE-AIR TEMPERATURE

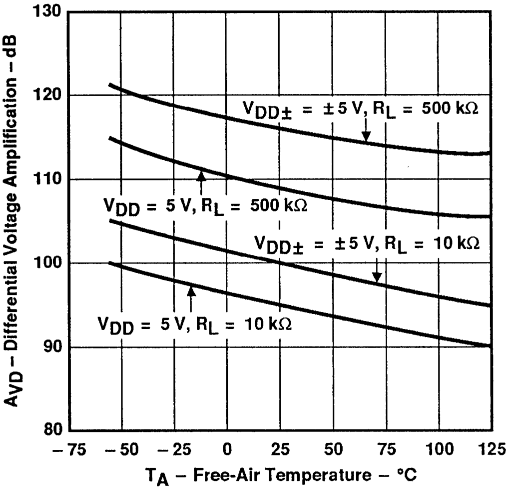


Figure 18

SHORT-CIRCUIT OUTPUT CURRENT vs SUPPLY VOLTAGE

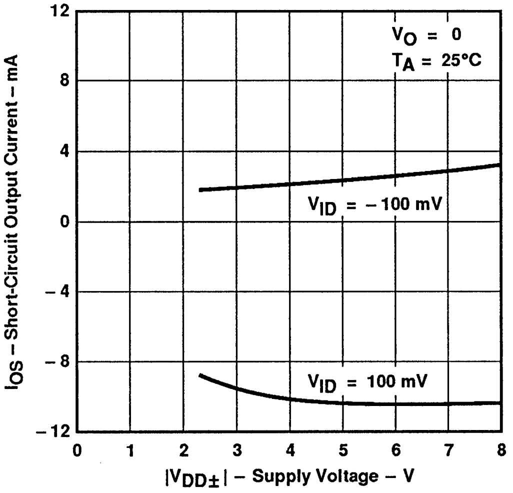


Figure 19

SHORT-CIRCUIT OUTPUT CURRENT vs FREE-AIR TEMPERATURE

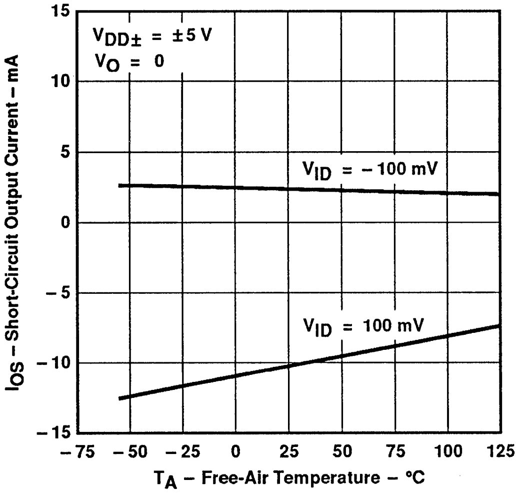


Figure 20

[†] Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

COMMON-MODE REJECTION RATIO
vs
FREQUENCY

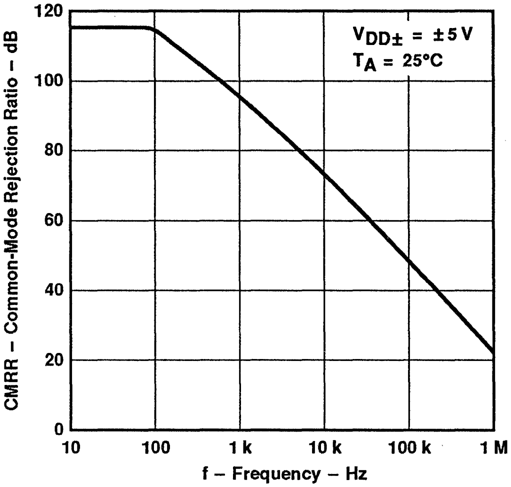


Figure 21

COMMON-MODE REJECTION RATIO
vs
FREQUENCY

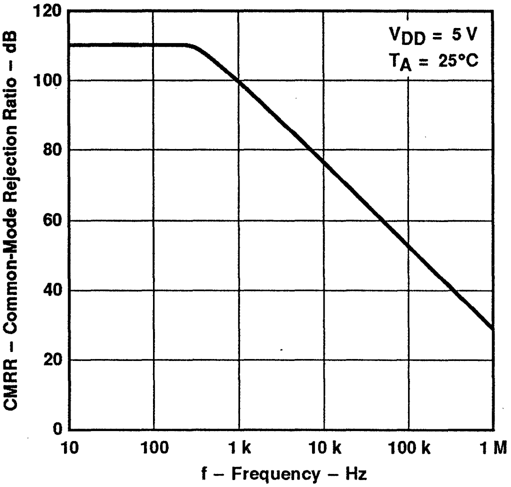


Figure 22

SUPPLY CURRENT
vs
SUPPLY VOLTAGE

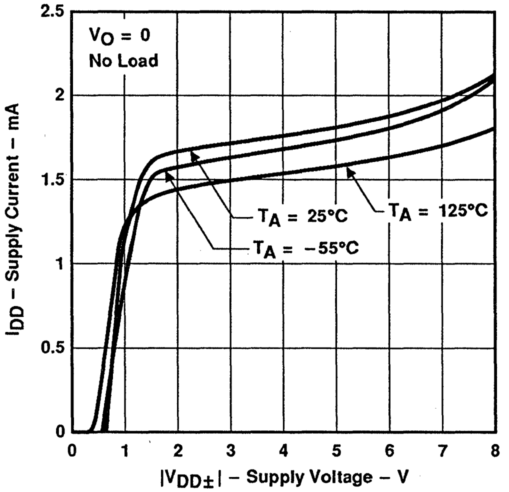


Figure 23

SUPPLY CURRENT
vs
FREE-AIR TEMPERATURE

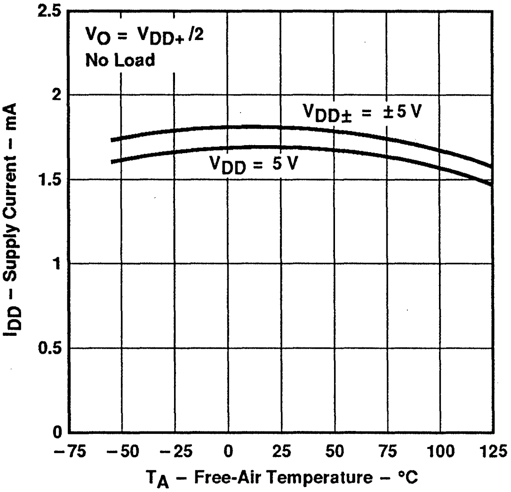


Figure 24

---

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS

VOLTAGE-FOLLOWER
SMALL-SIGNAL
PULSE RESPONSE

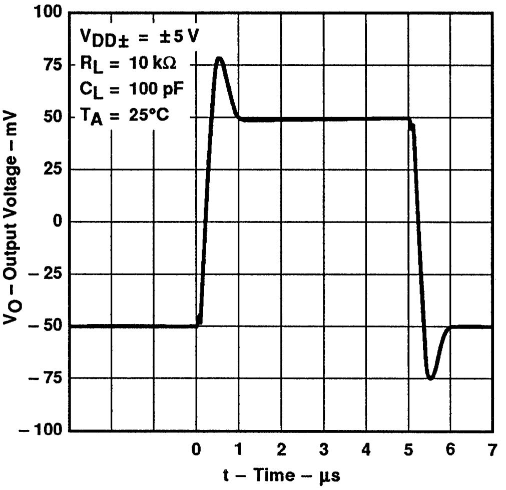


Figure 25

VOLTAGE-FOLLOWER
SMALL-SIGNAL
PULSE RESPONSE

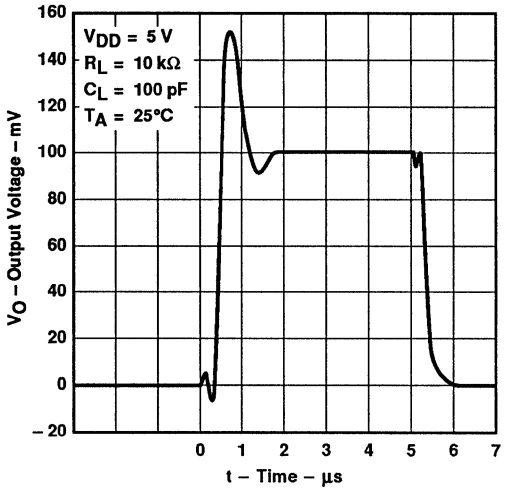


Figure 26

VOLTAGE-FOLLOWER
LARGE-SIGNAL
PULSE RESPONSE

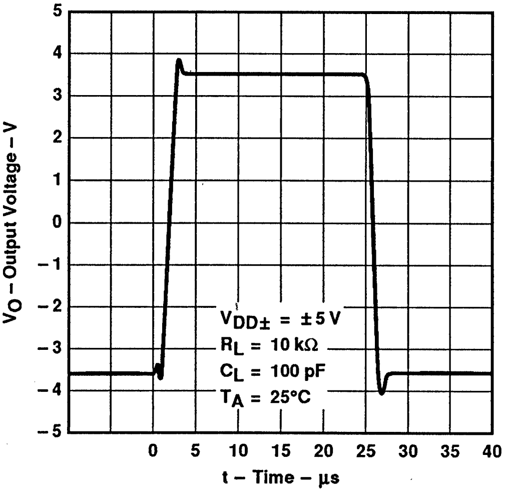


Figure 27

VOLTAGE-FOLLOWER
LARGE-SIGNAL
PULSE RESPONSE

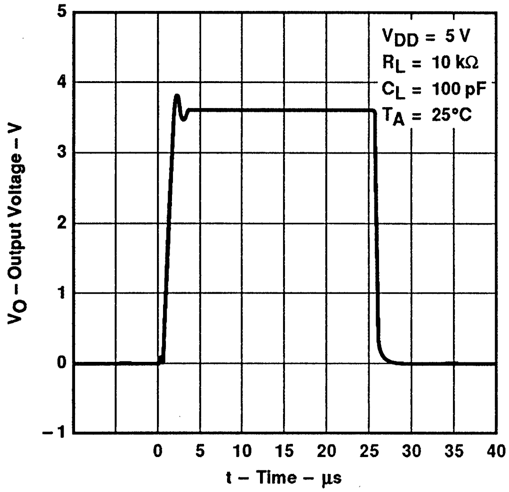


Figure 28

TYPICAL CHARACTERISTICS†

SLEW RATE
vs
SUPPLY VOLTAGE

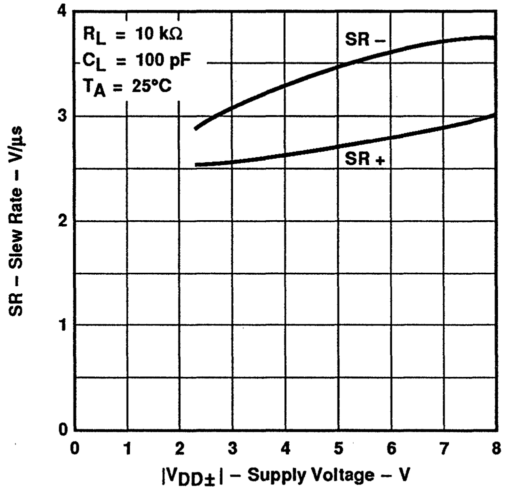


Figure 29

SLEW RATE
vs
FREE-AIR TEMPERATURE

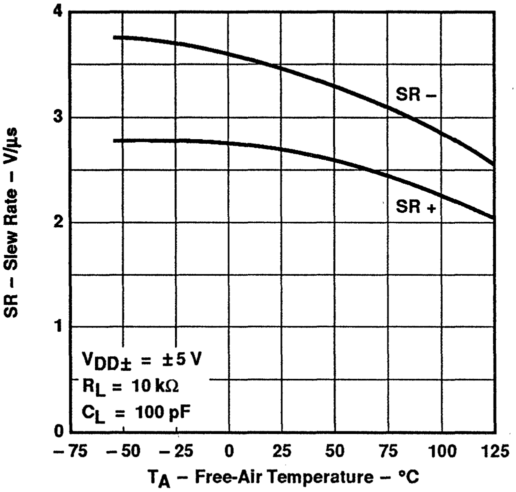


Figure 30

NOISE VOLTAGE
(REFERRED TO INPUT)
OVER A 10-SECOND INTERVAL

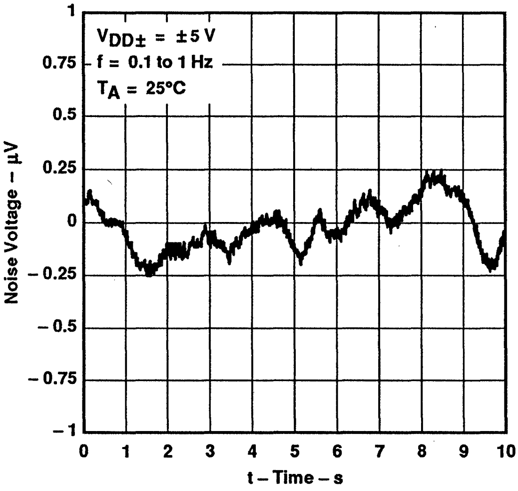


Figure 31

NOISE VOLTAGE
(REFERRED TO INPUT)
OVER A 10-SECOND INTERVAL

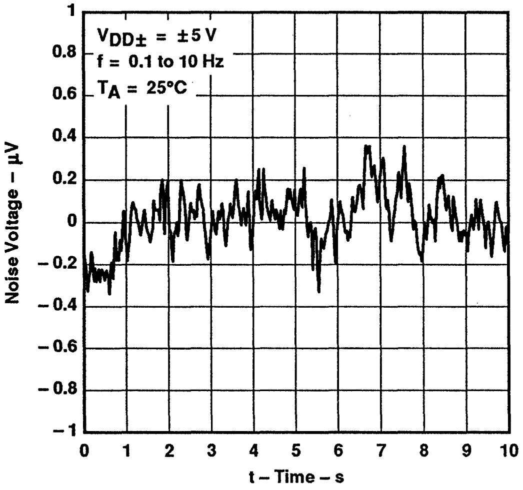
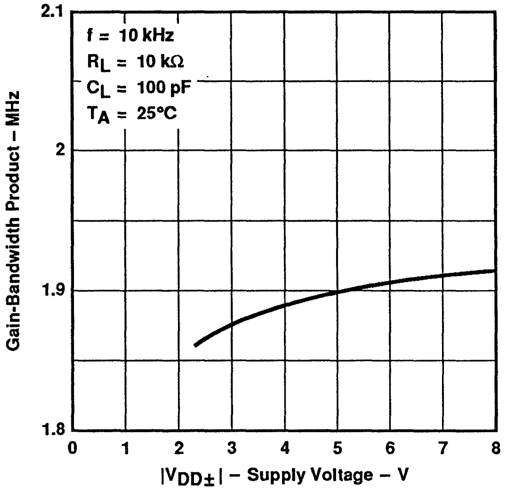


Figure 32

---

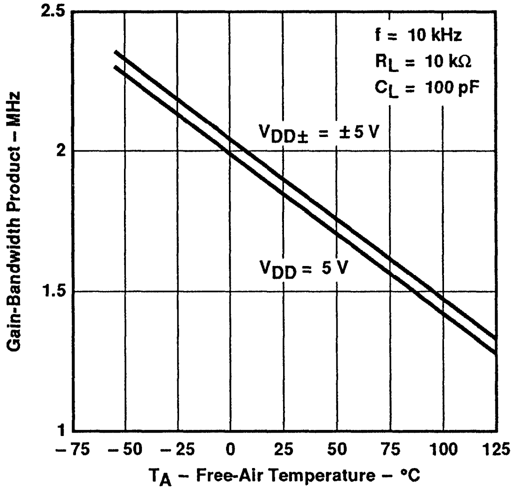
†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS[†]



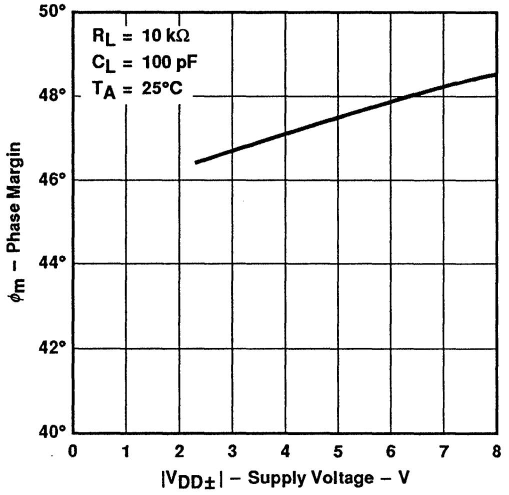
GAIN-BANDWIDTH PRODUCT
vs
SUPPLY VOLTAGE

Figure 33



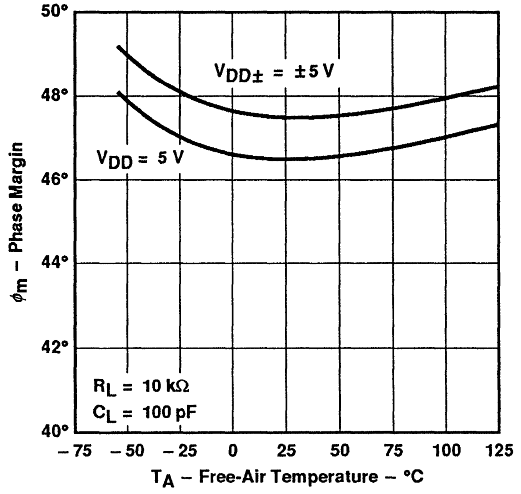
GAIN-BANDWIDTH PRODUCT
vs
FREE-AIR TEMPERATURE

Figure 34



PHASE MARGIN
vs
SUPPLY VOLTAGE

Figure 35



PHASE MARGIN
vs
FREE-AIR TEMPERATURE

Figure 36

[†] Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

APPLICATION INFORMATION

latch-up avoidance

Because CMOS devices are susceptible to latch-up due to their inherent parasitic thyristors, the TLC2202, TLC2202A, and TLC2202B inputs and outputs are designed to withstand –100-mA surge currents without sustaining latch-up; however, techniques reducing the chance of latch-up should be used whenever possible. Internal protection diodes should not be forward biased in normal operation. Applied input and output voltages should not exceed the supply voltage by more than 300 mV. Care should be exercised when using capacitive coupling on pulse generators. Supply transients should be shunted by the use of decoupling capacitors (0.1 µF typical) located across the supply rails as close to the device as possible.

electrostatic discharge protection

These devices use internal ESD-protection circuits that prevent functional failures at voltages at or below 2000 V. Care should be exercised in handling these devices as exposure to ESD may result in degradation of the device parametric performance.

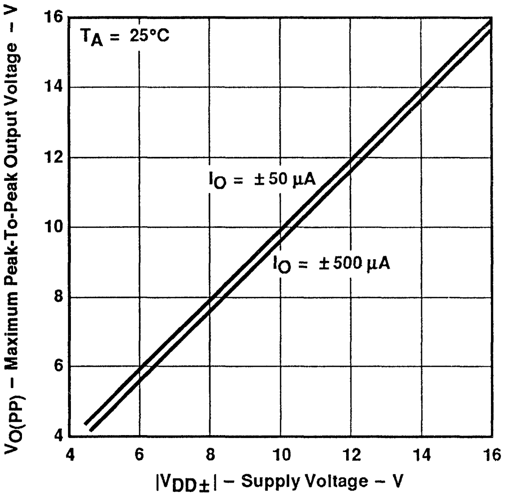
TLC2272, TLC2272A, TLC2272Y
Advanced LinCMOS™ DUAL RAIL-TO-RAIL OPERATIONAL AMPLIFIERS

D3981, NOVEMBER 1991

- **Output Swing Includes Both Supply Rails**
- **Low Noise . . . 9 nV/√Hz Typ at 1 kHz**
- **Low Input Bias Current . . . 1 pA Typ**
- **Single Supply or Split Supply Operating Capability**
- **Common-Mode Input Voltage Range that Includes Negative Rail**
- **High Gain-Bandwidth Product**
  2 MHz at 25°C
- **High Slew Rate . . . 3 V/µs Typ**
- **Low Input Offset Voltage**
  950 µV Max at T_A = 25°C - TLC2272A
  2500 µV Max at T_A = 25°C - TLC2272
- **Macromodel Included**

description

The TLC2272 and TLC2272A are dual rail-to-rail operational amplifiers using Texas Instruments Advanced LinCMOS™ process. These devices offer comparable ac performance to existing CMOS operational amplifiers, but with better noise, input offset voltage, and power dissipation. In addition, the common-mode input voltage range includes the negative rail, while delivering rail-to rail outputs. The Advanced LinCMOS™ process uses a silicon-gate technology to obtain input offset voltage stability with temperature and time that far exceeds that obtainable using metal-gate technology. In addition, this technology makes possible input impedance levels that meet or exceed levels offered by top-gate JFET and expensive dielectric-isolated devices.



MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE
vs
SUPPLY VOLTAGE

With high input impedance and low noise, the TLC2272 and TLC2272A are excellent for small signal conditioning for high-impedance sources, such as piezoelectric transducers. In addition, the rail-to-rail output feature with single or split-supply make these devices great choices for inputs to ADC devices in either the unipolar or bipolar mode of operation. Combining the previous feature with temperature performance, the TLC2272 family can be found in sonobuoys, pressure sensors, temperature control, active VR sensors, accelerometers, and many other applications.

AVAILABLE OPTIONS

T_A	V_{IO} max AT 25°C	PACKAGE				CHIP FORM (Y)
		SMALL OUTLINE (D)	SSOP (DB)	PLASTIC DIP (P)	TSSOP (PW)	
0°C to 70°C	950 µV	TLC2272ACD		TLC2272ACP		
	2500 µV	TLC2272CD	TLC2272DBLE	TLC2272CP	TLC2272PWLE	TLC2272Y

D packages are available taped and reeled. Add "R" suffix to device type, (e.g., TLE2272CDR). The DB and PW packages are only available taped and reeled. The chip form (Y) is tested at T_A = 25°C.

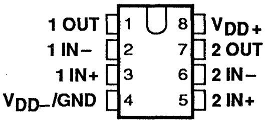
Advanced LinCMOS™ is a trademark of Texas Instruments Incorporated.

TEXAS INSTRUMENTS
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

description (continued)

The device inputs and outputs are designed to withstand 100-mA surge current without sustaining latch-up. In addition, internal ESD protection circuits prevent functional failures up to 2000 V as tested under MIL-STD-883C, Method 3015.2; however, care should be exercised in handling these devices as exposure to ESD may result in degradation of the device parametric performance.

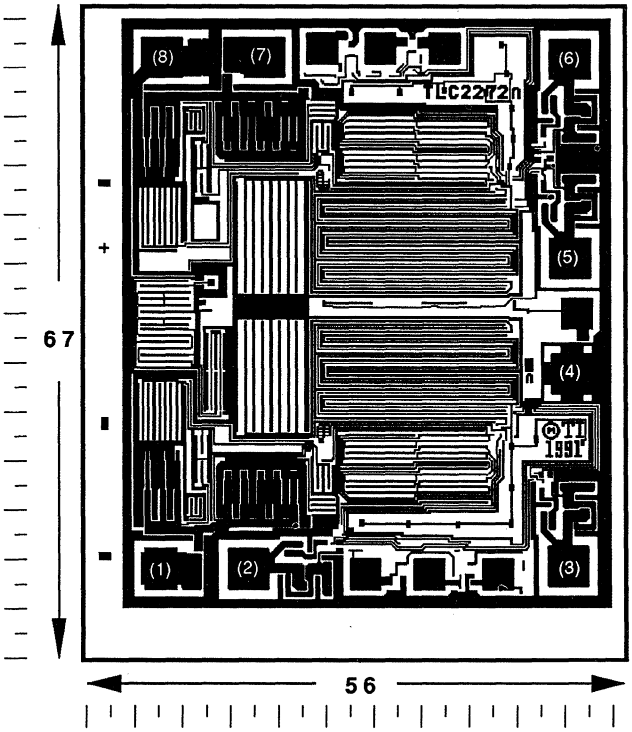
D, DB, P, OR PW PACKAGE
(TOP VIEW)

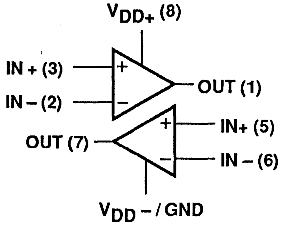


chip information

These chips, properly assembled, display characteristics similar to the TLC2272. Thermal compression or ultrasonic bonding may be used on the doped aluminum bonding pads. Chips may be mounted with conductive epoxy or a gold-silicon preform.

BONDING PAD ASSIGNMENTS





CHIP THICKNESS:
15 TYPICAL

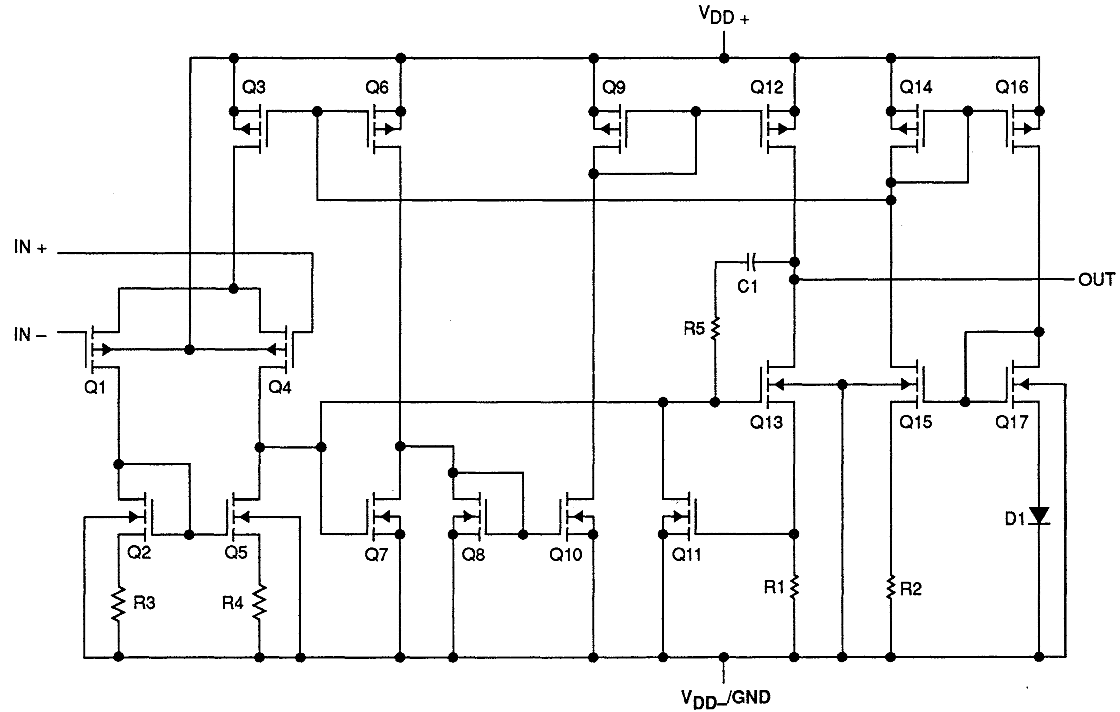
BONDING PADS:
4 X 4 MINIMUM

T_J max = 150°C

TOLERANCES
ARE ±10%

ALL DIMENSIONS
ARE IN MILS

equivalent schematic (each amplifier)



COMPONENT COUNT†	
Transistors	38
Diodes	9
Resistors	26
Capacitors	3

†Includes both amplifiers and all ESD bias and trim circuitry.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{DD+} (see Note 1)	8 V
Supply voltage, V_{DD-} (see Note 1)	−8 V
Differential input voltage (see Note 2)	±16 V
Input voltage, V_I (any input, see Note 1)	±8 V
Input current, I_I (each input)	±5 mA
Output current, I_O	±50 mA
Total current into V_{DD+} terminal	±50 mA
Total current out of V_{DD-} terminal	±50 mA
Duration of short-circuit current at (or below) 25°C (see Note 3)	unlimited
Continuous total dissipation	See Dissipation Rating Table
Operating free-air temperature range	0°C TO 70°C
Storage temperature range	−65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C

NOTES: 1. All voltage values, except differential voltages, are with respect to the midpoint between V_{DD+} and V_{DD-} for split supplies.

2. Differential voltages are at the noninverting input with respect to the inverting input. Excessive current will flow if input is below $V_{DD-} - 0.3$ V.

3. The output may be shorted to either supply. Temperature and/or supply voltages must be limited to ensure that the maximum dissipation rating is not exceeded.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING
D	725 mW	5.8 mW/°C	464 mW
DB	525 mW	4.2 mW/°C	336 mW
P	1000 mW	8 mW/°C	640 mW
PW	525 mW	4.2 mW/°C	336 mW

recommended operating conditions

	MIN	MAX	UNIT
Supply voltage, $V_{DD\pm}$	±2.2	±8	V
Input voltage range	V_{DD-}	$V_{DD+} - 1.5$	V
Common-mode input voltage, V_{IC}	V_{DD-}	$V_{DD+} - 1.5$	V
Operating free-air temperature, T_A	0	70	°C

electrical characteristics at specified free-air temperature, V_{DD+} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A†	TLC2272C			TLC2272AC			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_{IC} = 0, $V_{DD\pm}$ = ±2.5 V V_O = 0, R_S = 50 Ω	25°C		300	2500		300	950	µV
			Full range			3000			1500	
α_{VIO}	Temperature coefficient of input offset voltage		Full range		2			2		µV/°C
	Input offset voltage long-term drift (see Note 4)		25°C		0.002			0.002		µV/mo
I_{IO}	Input offset current		25°C		0.5	100		0.5	100	pA
			Full range			100			100	
I_{IB}	Input bias current		25°C		1	100		1	100	pA
			Full range			100			100	
V_{ICR}	Common-mode input voltage range	R_S = 50 Ω, $\lvert V_{IO} \rvert \le$ 5 mV	25°C	0 to 4	−0.5 to 4.2		0 to 4	−0.5 to 4.2		V
			Full range	0 to 3.5			0 to 3.5			
V_{OM+}	Maximum positive peak output voltage swing	I_{OH} = 20 µA	25°C		4.99			4.99		V
		I_{OH} = 200 µA			4.93			4.93		
		I_{OH} = 1 mA			4.65			4.65		
V_{OM-}	Maximum negative peak output voltage swing	V_{IC} = 2.5 V, I_{OL} = 50 µA	25°C		0.01			0.01		V
		V_{IC} = 2.5 V, I_{OL} = 500 µA			0.09			0.09		
		V_{IC} = 2.5 V, I_{OL} = 5 mA			0.9			0.9		
A_{VD}	Large-signal differential voltage amplification	V_{IC} = 2.5 V, V_O = 1 V to 4 V, R_L = 10 kΩ‡	25°C		35			35		V/mV
		R_L = 1 MΩ‡			175			175		
r_{id}	Differential input resistance		25°C		10^{12}			10^{12}		Ω
r_i	Common-mode input resistance		25°C		10^{12}			10^{12}		Ω
c_i	Common-mode input capacitance	f = 10 kHz, P package	25°C		8			8		pF
z_o	Closed loop output impedance	f = 1 MHz, A_V = 10	25°C		140			140		Ω
CMRR	Common-mode rejection ratio	V_{IC} = 0 V to 2.7 V, V_O = 2.5 V, R_S = 50 Ω	25°C		75			75		dB
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD\pm}/\Delta V_{IO}$)	V_{DD+} = 4.4 V to 16 V, No load, V_{IC} = $V_{DD}/2$	25°C	80	100		80	100		dB
			Full range	80			80			
I_{DD}	Supply current	V_O = 2.5 V, No load	25°C		2.2	3		2.2	3	mA
			Full range			3			3	

†Full range is 0°C to 70°C.

‡Referenced to 2.5 V

NOTE 4: Typical values are based on the input offset voltage shift observed through 168 hours perating life test at T_A = 150°C extrapolated to T_A = 25°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

operating characteristics, V_{DD+} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS		TLC2272C			TLC2272AC			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
SR	Slew rate at unity gain	V_O = 0.5 V to 2.5 V, R_L = 10 kΩ†, C_L = 100 pF†			3.6			3.6		V/µs
V_n	Equivalent input noise voltage	f = 10 Hz			50			50		nV/√Hz
		f = 1 kHz			9			9		
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 to 1 Hz			1			1		µV
		f = 0.1 to 10 Hz			1.4			1.4		
I_n	Equivalent input noise current				0.6			0.6		fA/√Hz
THD + N	Total harmonic distortion plus noise	V_O = 0.5 V to 2.5 V, R_L = 10 kΩ†, f = 20 kHz	A_{VD} = 1		0.0013%			0.0013%		
			A_{VD} = 10		0.004%			0.004%		
			A_{VD} = 100		0.03%			0.03%		
	Gain-bandwidth product	f = 10 kHz, R_L = 10 kΩ†, C_L = 100 pF†			2.18			2.18		MHz
B_{OM}	Maximum output-swing bandwidth	V_O = 0.5 V to 2.5 V, A_{VD} = 1, R_L = 10 kΩ†, C_L = 100 pF†			1			1		MHz
ϕ_m	Phase margin at unity gain	R_L = 10 kΩ†, C_L = 100 pF†			50°			50°		
A_m	Gain margin				10			10		dB

†Referenced to 2.5 V

electrical characteristics at specified free-air temperature, $V_{DD\pm}$ = ±5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A†	TLC2272C			TLC2272C			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_{IC} = 0, V_O = 0, R_S = 50 Ω	25°C		300	2500		300	950	µV
			Full range			3000			1500	
	Temperature coefficient of input offset voltage		Full range		2			2		µV/°C
α_{VIO}	Input offset voltage long-term drift (see Note 4)		25°C		0.002			0.002		µV/mo
I_{IO}	Input offset current		25°C		0.5	100		0.5	100	pA
			Full range			100			100	
I_{IB}	Input bias current		25°C		1	100		1	100	pA
			Full range			100			100	
V_{ICR}	Common-mode input voltage range	R_S = 50 Ω, $\lvert V_{IO} \rvert \le 5$ mV	25°C	−5 to 4	−5.5 to 4.2		−5 to 4	−5.5 to 4.2		V
			Full range	−5 to 3.5			−5 to 3.5			
V_{OM+}	Maximum positive peak output voltage swing	I_O = −20 µA	25°C		4.99			4.99		V
		I_O = −200 µA			4.93			4.93		
		I_O = −1 mA			4.65			4.65		
V_{OM-}	Maximum negative peak output voltage swing	V_{IC} = 0, I_O = 50 µA	25°C		−4.99			−4.99		V
		V_{IC} = 0, I_O = 500 µA			−4.91			−4.91		
		V_{IC} = 0, I_O = 5 mA			−4.1			−4.1		
A_{VD}	Large-signal differential voltage amplification	V_O = ±4 V, R_L = 10 kΩ	25°C		50			50		V/mV
		V_O = ±4 V, R_L = 1 MΩ			300			300		
r_{id}	Differential input resistance		25°C		10^{12}			10^{12}		Ω
r_i	Common-mode input resistance		25°C		10^{12}			10^{12}		Ω
c_i	Common-mode input capacitance	f = 10 kHz, P package	25°C		8			8		pF
z_o	Closed loop output impedance	f = 1 MHz, A_V = 10	25°C		130			130		Ω
CMRR	Common-mode rejection ratio	V_{IC} = −5 V to 2.7 V, V_O = 0, R_S = 50 Ω	25°C		85			85		dB
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD\pm}/\Delta V_{IO}$)	$V_{DD\pm}$ = ±2.2 V to ±8 V, No load	25°C	80	100		80	100		dB
			Full range	80			80			
I_{DD}	Supply current	V_O = 0, No load	25°C		2.4	3		2.4	3	mA
			Full range			3			3	

†Full range is 0°C to 70°C.

NOTE 4: Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at T_A = 150°C extrapolated to T_A = 25°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

operating characteristics, $V_{DD\pm}$ = ±5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS		TLC2272C			TLC2272AC			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
SR	Slew rate at unity gain	V_O = ±2.3 V, R_L = 10 kΩ, C_L = 100 pF			3.6			3.6		V/ µs
V_n	Equivalent input noise voltage	f = 10 Hz			50			50		nV/√Hz
		f = 1 kHz			9			9		
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 to 1 Hz			1			1		µV
		f = 0.1 to 10 Hz			1.4			1.4		
I_n	Equivalent input noise current				0.6			0.6		fA/√Hz
THD + N	Total harmonic distortion plus noise	V_O = ±2.3 V, R_L = 10 kΩ, f = 20 kHz	A_{VD} = 1		0.0011%			0.0011%		
			A_{VD} = 10		0.004%			0.004%		
			A_{VD} = 100		0.03%			0.03%		
	Gain-bandwidth product	f = 10 kHz, R_L = 10 kΩ, C_L = 100 pF			2.25			2.25		MHz
B_{OM}	Maximum output-swing bandwidth	V_O = ±2.3 V, A_{VD} = 1, R_L = 10 kΩ, C_L = 100 pF			0.54			0.54		MHz
ϕ_m	Phase margin at unity gain	R_L = 10 kΩ, C_L = 100 pF			52°			52°		
A_m	Gain margin				10			10		dB

electrical characteristics at V_{DD} = 5 V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	V_{IC} = 0, $V_{DD}\pm$ = ±2.5 V, V_O = 0, R_S = 50 Ω			300	2500	μV
	Input offset voltage long-term drift (see Note 4)				0.002		μV/mo
I_{IO}	Input offset current				0.5	100	pA
I_{IB}	Input bias current				1	100	pA
V_{ICR}	Common-mode input voltage range	R_S = 50 Ω $\lvert V_{IO} \rvert \le 5$ mV		0 to 4	−0.5 to 4.2		V
V_{OH}	High-level output voltage	I_{OH} = 20 μA			4.99		V
		I_{OH} = 200 μA			4.93		
		I_{OH} = 1 mA			4.65		
V_{OL}	Low-level output voltage	V_{IC} = 2.5 V, I_{OL} = 50 μA			0.01		mV
		V_{IC} = 2.5 V, I_{OL} = 500 μA			0.09		
		V_{IC} = 2.5 V, I_{OL} = 5 mA			0.9		
A_{VD}	Large-signal differential voltage amplification	V_{IC} = 2.5 V, V_O = 1 V to 4 V	R_L = 10 kΩ†		35		V/mV
			R_L = 1 MΩ†		175		
r_{id}	Differential input resistance				10^{12}		Ω
r_i	Common-mode input resistance				10^{12}		Ω
c_i	Common-mode input capacitance	f = 10 kHz			8		pF
z_o	Closed loop output impedance	f = 1 MHz, A_V = 10			140		Ω
CMRR	Common-mode rejection ratio	V_{IC} = 0 to 2.7 V, V_O = 2.5 V, R_S = 50 Ω			75		dB
k_{SVR}	Supply-voltage rejection ratio (ΔV_{DD} / ΔV_{IO})	V_{DD} = 4.4 V to 16 V, No load, V_{IC} = V_{DD}/2		80	100		dB
I_{DD}	Supply current	V_O = 2.5 V, No load			2.2	3	mA

† Referenced to 2.5 V

NOTE 4: Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at T_A = 150°C extrapolated to T_A = 25°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

electrical characteristics at $V_{DD\pm} = \pm 5$ V, $T_A = 25°C$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	$V_{IC} = 0$, $V_{DD\pm} = \pm 2.5$ V, $V_O = 0$, $R_S = 50\ \Omega$			300	2500	µV
	Input offset voltage long-term drift (see Note 4)				0.002		µV/mo
I_{IO}	Input offset current				0.5	100	pA
I_{IB}	Input bias current				1	100	pA
V_{ICR}	Common-mode input voltage range	$R_S = 50\ \Omega$, $\lvert V_{IO} \rvert \leq 5$ mV		−5 to 4	−5.5 to 4.2		V
V_{OH}	High-level output voltage	$I_{OH} = 20\ \mu A$			4.99		V
		$I_{OH} = 200\ \mu A$			4.93		
		$I_{OH} = 1$ mA			4.65		
V_{OL}	Low-level output voltage	$V_{IC} = 0$, $I_O = 50\ \mu A$			−4.99		mV
		$V_{IC} = 0$, $I_O = 500\ \mu A$			−4.91		
		$V_{IC} = 0$, $I_O = 5$ mA			−4.1		
A_{VD}	Large-signal differential voltage amplification	$V_{IC} = 2.5$ V, $V_O = 1$ V to 4 V	$R_L = 10\ k\Omega$†		50		V/mV
			$R_L = 1\ M\Omega$†		300		
r_{id}	Differential input resistance				10^{12}		Ω
r_i	Common-mode input resistance				10^{12}		Ω
c_i	Common-mode input capacitance	f = 10 kHz			8		pF
z_o	Closed loop output impedance	f = 1 MHz, $A_V = 10$			130		Ω
CMRR	Common-mode rejection ratio	$V_{IC} = 0$ to 2.7 V, $V_O = 2.5$ V, $R_S = 50\ \Omega$			85		dB
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD} / \Delta V_{IO}$)	$V_{DD} = 4.4$ V to 16 V, No load, $V_{IC} = V_{DD}/2$		80	100		dB
I_{DD}	Supply current	$V_O = 2.5$ V, No load			2.4	3	mA

†Referenced to 0 V.

NOTE 4: Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at $T_A = 150°C$ extrapolated to $T_A = 25°C$ using the Arrhenius equation and assuming an activation energy of 0.96 eV.

TYPICAL CHARACTERISTICS

table of graphs

			FIGURE
V_{IO}	Input offset voltage	Distribution	1, 2
		vs V_{IC}	3, 4
$V_{O(PP)}$	Maximum peak-to-peak output voltage swing	vs Frequency	5
V_{ID}	Differential input voltage	vs Output voltage	6, 7
A_{VD}	Large-signal differential voltage amplification	vs R_L	8
		vs Frequency	9, 10
z_o	Output impedance	vs Frequency	11, 12
CMRR	Common-mode rejection ratio	vs Frequency	13
	Large-signal pulse response	vs Time	14, 15, 16, 17
	Small-signal pulse response	vs Time	18, 19, 20, 21
V_n	Input-referred noise voltage	vs Frequency	22, 23
		vs Over a 10-second time interval	24
THD + N	Total harmonic distortion plus noise	vs Frequency	25
ϕ_m	Phase margin	vs Frequency	9, 10
ϕ_m	Phase margin	vs Load capacitance	26
A_m	Gain margin	vs Load capacitance	27

TYPICAL CHARACTERISTICS

DISTRIBUTION OF TLC2272
INPUT OFFSET VOLTAGE

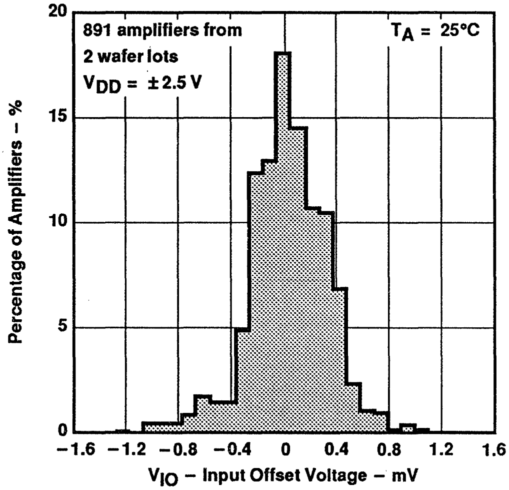


Figure 1

DISTRIBUTION OF TLC2272
INPUT OFFSET VOLTAGE

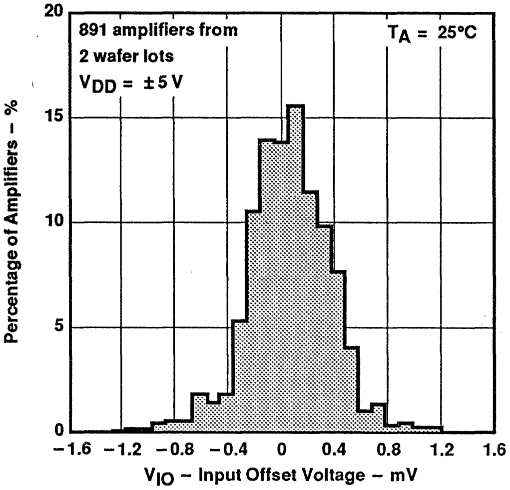


Figure 2

INPUT OFFSET VOLTAGE
vs
COMMON-MODE VOLTAGE

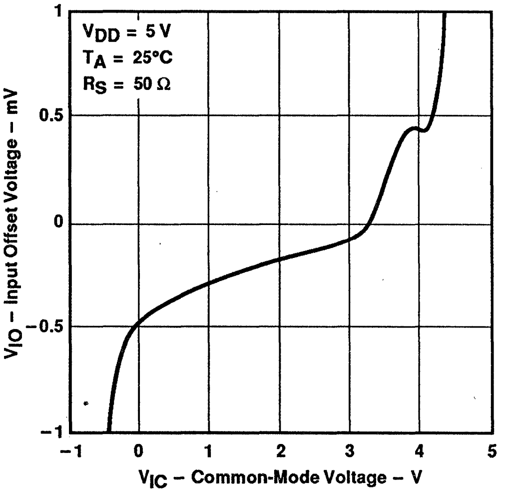


Figure 3

INPUT OFFSET VOLTAGE
vs
COMMON-MODE VOLTAGE

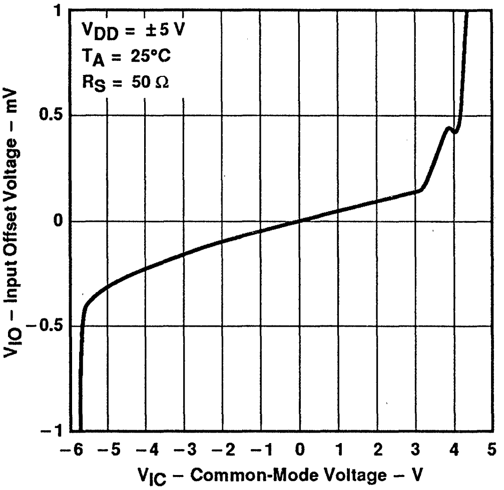


Figure 4

TYPICAL CHARACTERISTICS

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE SWING vs FREQUENCY

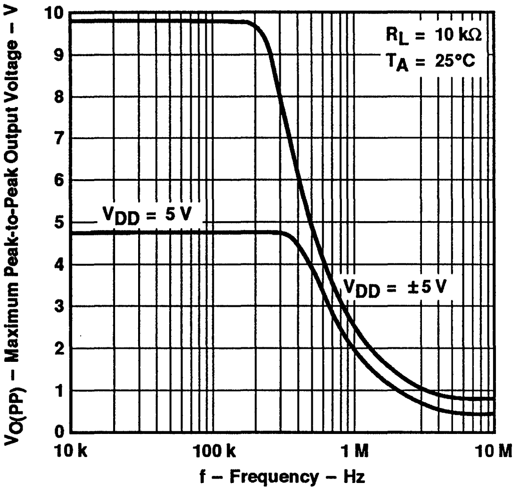


Figure 5

DIFFERENTIAL INPUT VOLTAGE vs OUTPUT VOLTAGE

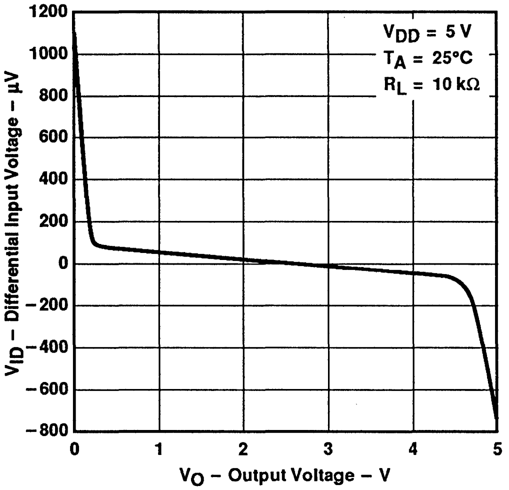


Figure 6

DIFFERENTIAL INPUT VOLTAGE vs OUTPUT VOLTAGE

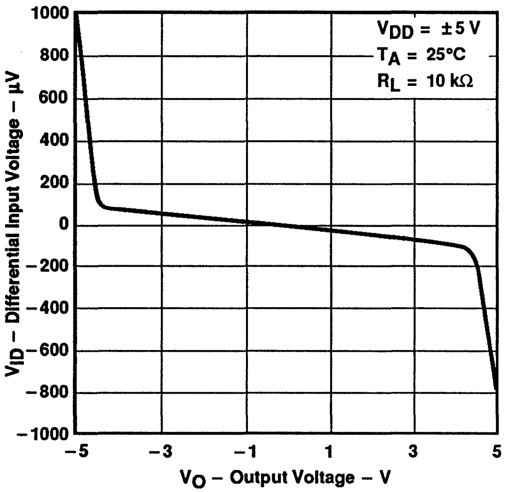


Figure 7

LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION vs LOAD RESISTANCE

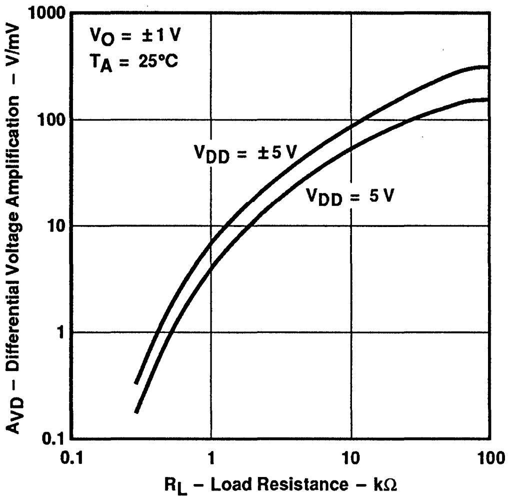


Figure 8

TYPICAL CHARACTERISTICS

LARGE-SIGNAL DIFFERENTIAL VOLTAGE
AMPLIFICATION and PHASE MARGIN
vs
FREQUENCY

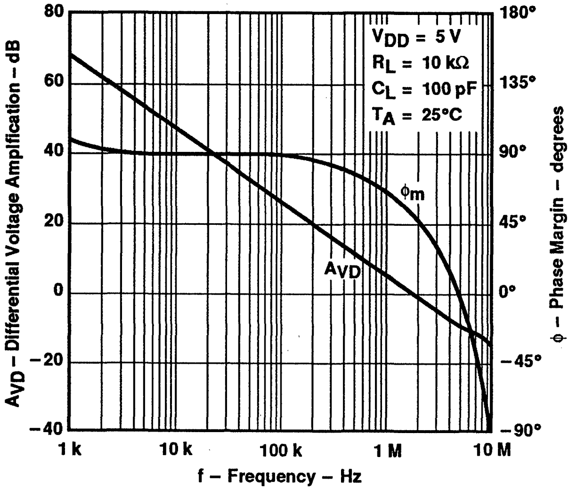


Figure 9

LARGE-SIGNAL DIFFERENTIAL VOLTAGE
AMPLIFICATION and PHASE MARGIN
vs
FREQUENCY

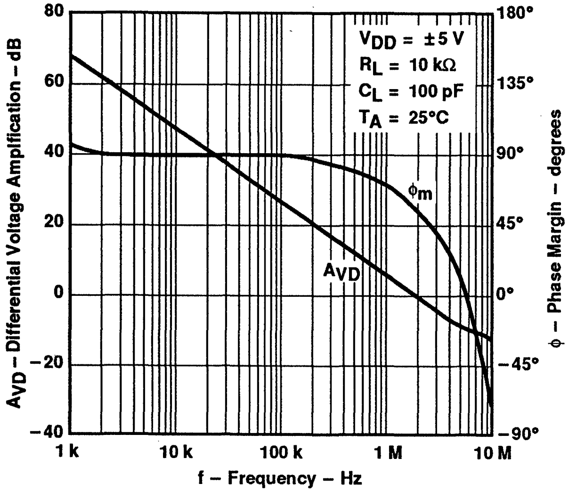


Figure 10

TYPICAL CHARACTERISTICS

OUTPUT IMPEDANCE vs FREQUENCY

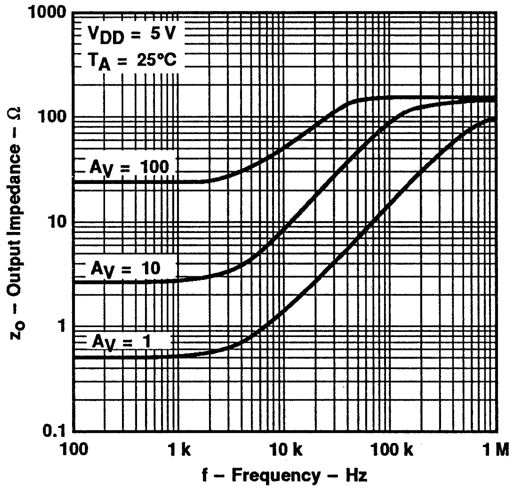


Figure 11

OUTPUT IMPEDANCE vs FREQUENCY

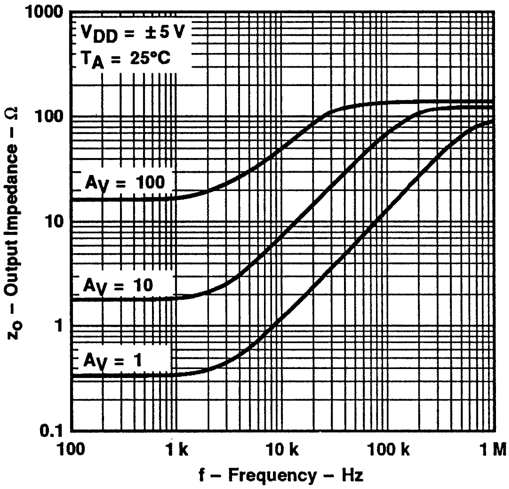


Figure 12

COMMON-MODE REJECTION RATIO vs FREQUENCY

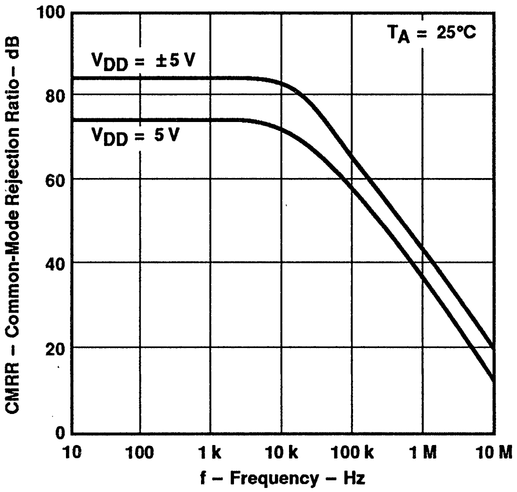


Figure 13

INVERTING LARGE-SIGNAL PULSE RESPONSE

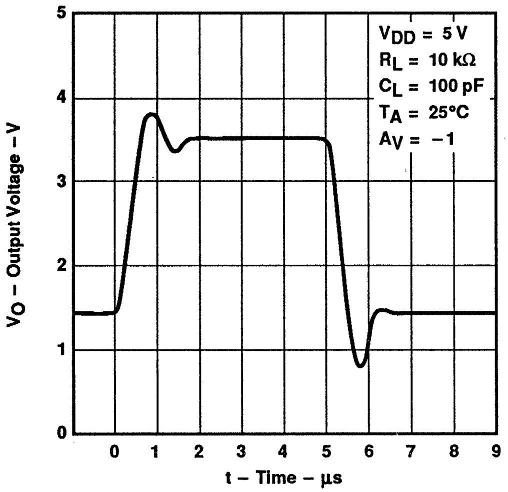


Figure 14

TYPICAL CHARACTERISTICS

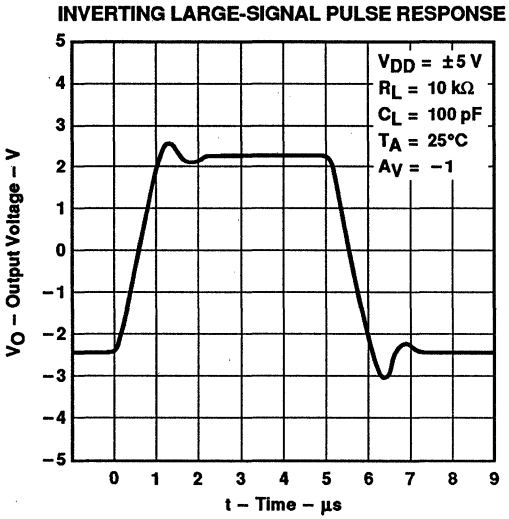


Figure 15

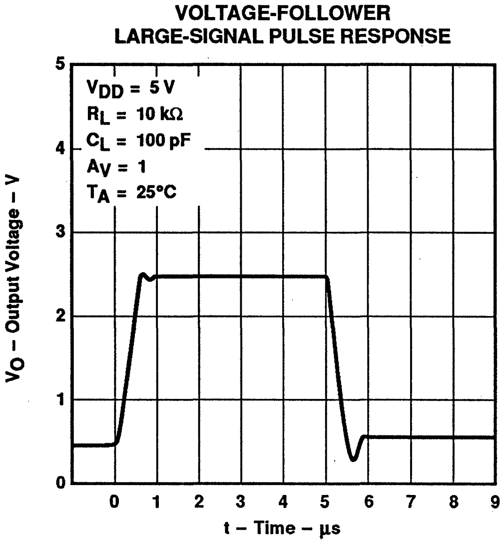


Figure 16

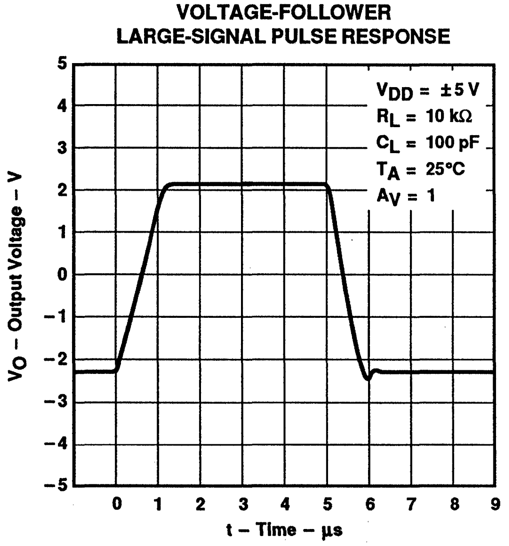


Figure 17

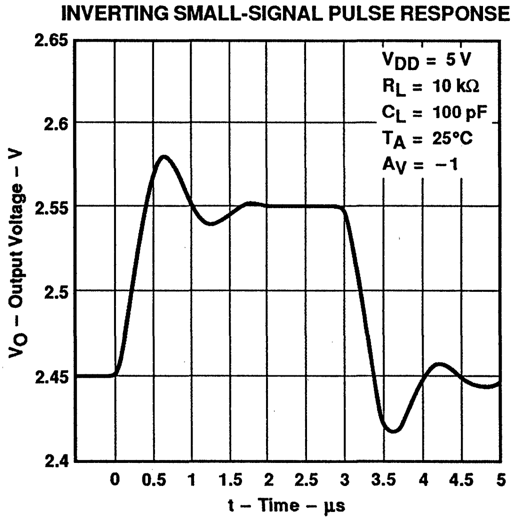


Figure 18

TYPICAL CHARACTERISTICS

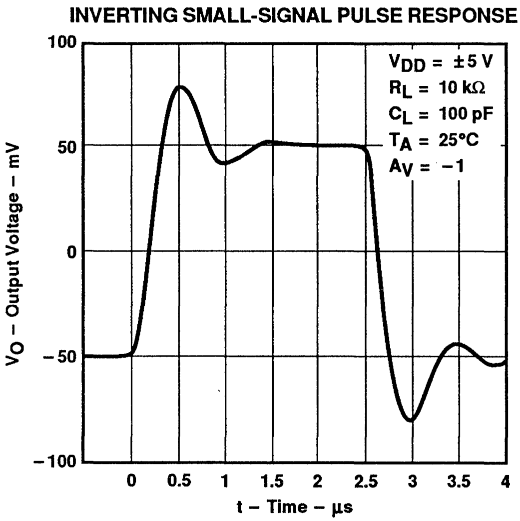


Figure 19

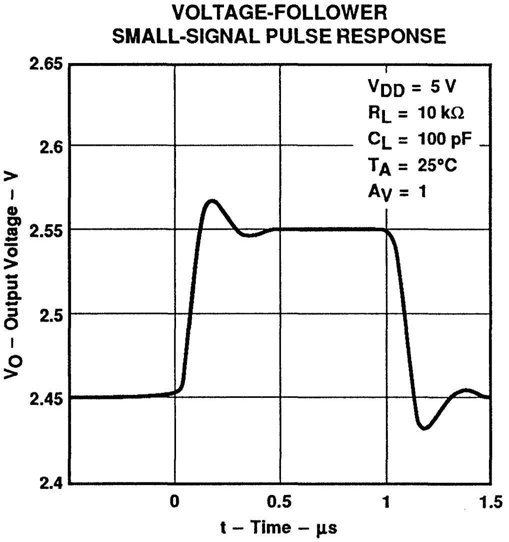


Figure 20

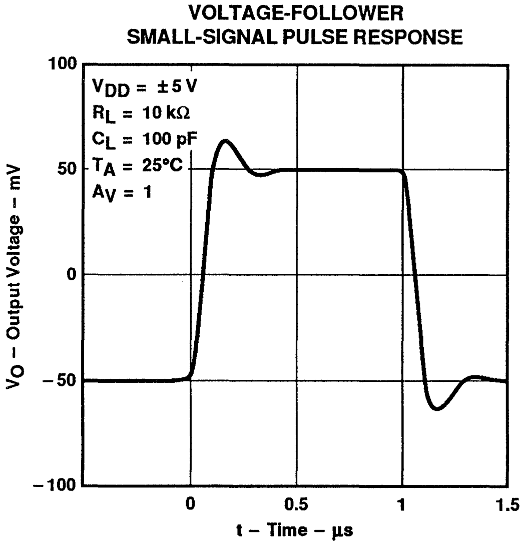


Figure 21

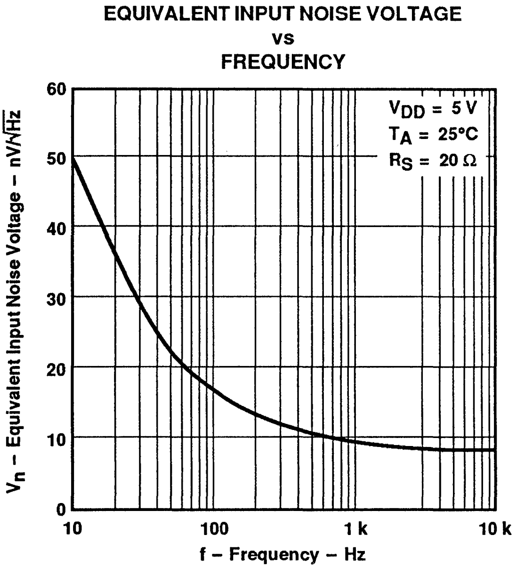


Figure 22

TYPICAL CHARACTERISTICS

EQUIVALENT INPUT NOISE VOLTAGE
vs
FREQUENCY

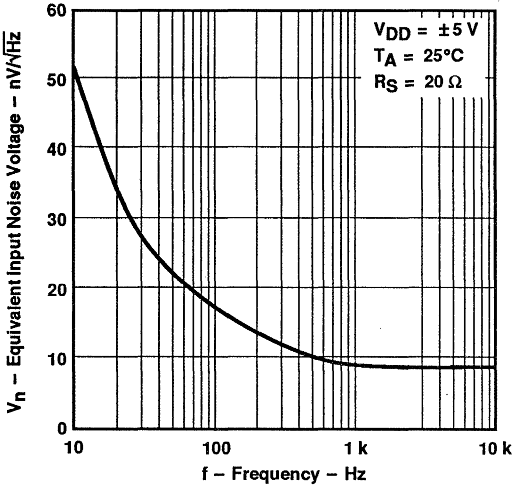


Figure 23

EQUIVALENT INPUT NOISE VOLTAGE
OVER A 10 SECOND PERIOD

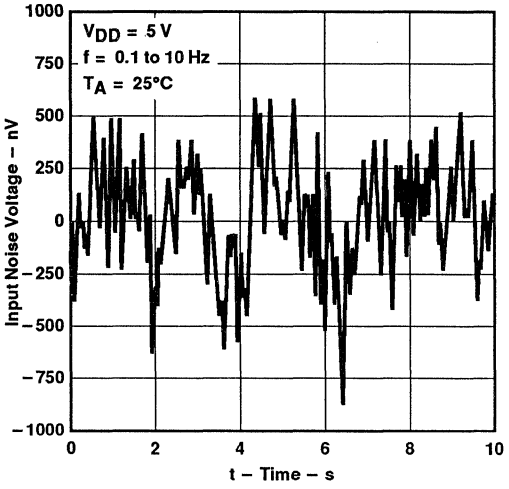


Figure 24

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
FREQUENCY

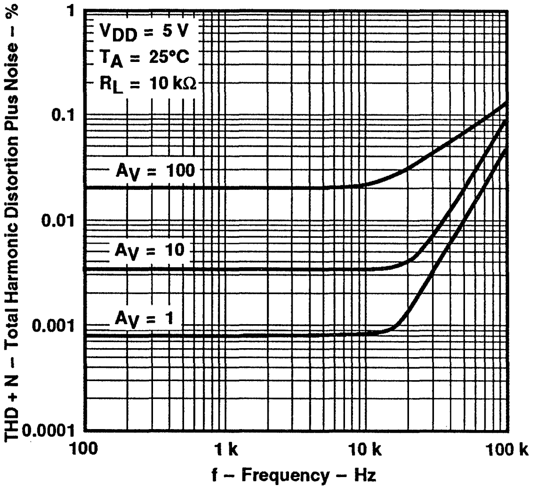


Figure 25

PHASE MARGIN
vs
LOAD CAPACITANCE

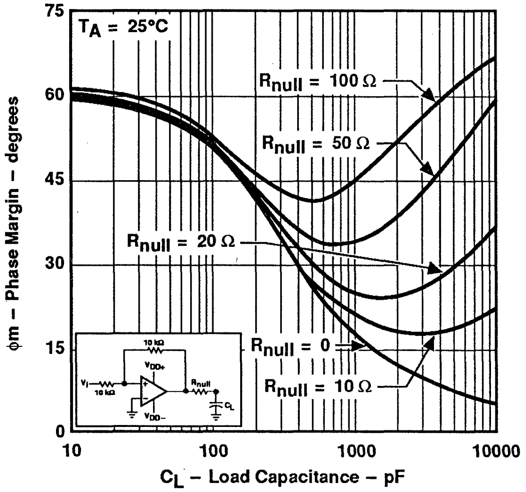


Figure 26

TYPICAL CHARACTERISTICS

GAIN MARGIN
vs
LOAD CAPACITANCE

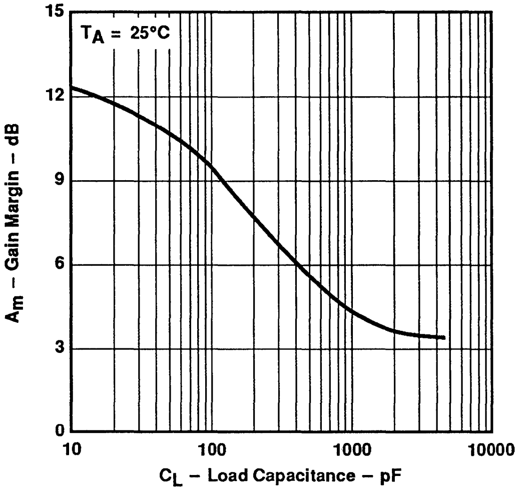


Figure 27

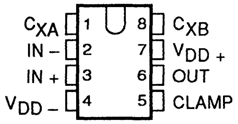
TLC2652, TLC2652A, TLC2652Y
Advanced LinCMOS™ PRECISION CHOPPER-STABILIZED OPERATIONAL AMPLIFIERS

D3157, SEPTEMBER 1988 – REVISED AUGUST 1991

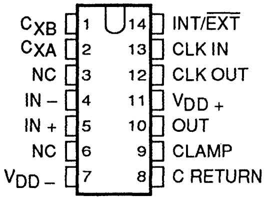
available features

- Extremely Low Offset Voltage . . . 1 µV Max
- Extremely Low Change in Offset Voltage With Temperature . . . 0.003 µV/°C Typ
- Low Input Offset Current . . . 500 pA Max at T_A = –55°C to 125°C
- A_{VD} . . . 135 dB Min
- CMRR and k_{SVR} . . . 120 dB Min
- Single-Supply Operation
- Common-Mode Input Voltage Range Includes the Negative Rail
- No Noise Degradation With External Capacitors Connected to V_{DD-}

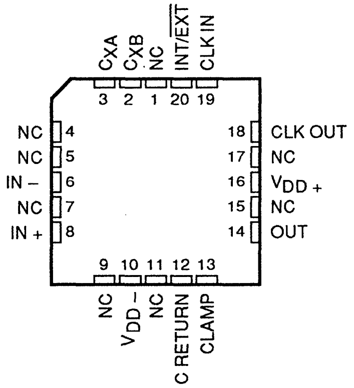
D008, JG, or P PACKAGE
(TOP VIEW)



D014, J, or N PACKAGE
(TOP VIEW)



FK PACKAGE
(TOP VIEW)



NC – No internal connection

description

The TLC2652 and TLC2652A are high-precision chopper-stabilized operational amplifiers using Texas Instruments Advanced LinCMOS™ process. This process in conjunction with unique chopper-stabilization circuitry produces operational amplifiers whose performance matches or exceeds that of similar devices available today.

AVAILABLE OPTIONS

T_A	V_{IO} max AT 25°C	PACKAGE							CHIP FORM (Y)
		8-PIN			14-PIN			20-PIN	
		SMALL-OUTLINE (D008)	CERAMIC DIP (JG)	PLASTIC DIP (P)	SMALL-OUTLINE (D014)	CERAMIC DIP (J)	PLASTIC DIP (N)	CHIP CARRIER (FK)	
0°C to 70°C	1 µV	TLC2652AC-8D	–	TLC2652ACP	TLC2652AC-14D	–	TLC2652ACN	–	TLC2652Y
	3 µV	TLC2652C-8D	–	TLC2652CP	TLC2652C-14D	–	TLC2652CN	–	
– 40°C to 85°C	1 µV	TLC2652AI-8D	–	TLC2652AIP	TLC2652AI-14D	–	TLC2652AIN	–	
	3 µV	TLC2652I-8D	–	TLC2652IP	TLC2652I-14D	–	TLC2652IN	–	
– 55°C to 125°C	1 µV	TLC2652AM-8D	TLC2652AMJG	TLC2652AMP	TLC2652AM-14D	TLC2652AMJ	TLC2652AMN	TLC2652AMFK	
	3 µV	TLC2652M-8D	TLC2652MJG	TLC2652MP	TLC2652M-14D	TLC2652MJ	TLC2652MN	TLC2652MFK	

D008 and D014 packages are available taped and reeled. Add "R" suffix to device type (e.g., TLC2652AC-8DR). Chips are tested at 25°C.

Advanced LinCMOS is a trademark of Texas Instruments Incorporated.

description (continued)

Chopper-stabilization techniques make possible extremely high dc precision by continuously nulling input offset voltage even during variations in temperature, time, common-mode voltage, and power supply voltage. In addition, low-frequency noise voltage is significantly reduced. This high precision, coupled with the extremely high input impedance of the CMOS input stage, makes the TLC2652 and TLC2652A an ideal choice for low-level signal processing applications such as strain gauges, thermocouples, and other transducer amplifiers. (For applications that require extremely low noise and higher usable bandwidth, use the TLC2654 or TLC2654A device, which has a chopping frequency of 10 kHz.)

The TLC2652 and TLC2652A input common-mode range includes the negative rail, thereby providing superior performance in either single-supply or split-supply applications, even at power supply voltage levels as low as ±1.9 V.

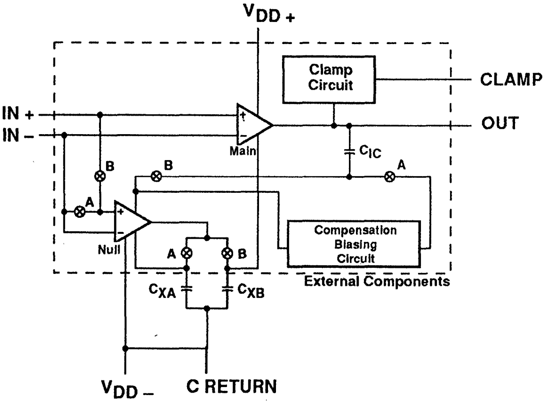
Two external capacitors are required for operation of the device; however, the on-chip chopper control circuitry is transparent to the user. On devices in the 14-pin and 20-pin packages, the control circuitry is made accessible to allow the user the option of controlling the clock frequency with an external frequency source. In addition, the clock threshold level of the TLC2652 and TLC2652A require no level shifting when used in the single-supply configuration with a normal CMOS or TTL clock input.

Innovative circuit techniques are used on the TLC2652 and TLC2652A to allow exceptionally fast overload recovery time. If desired, an output clamp pin is available to reduce the recovery time even further.

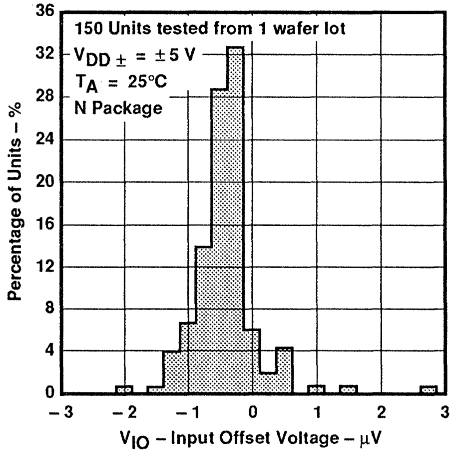
The device inputs and output are designed to withstand –100-mA surge currents without sustaining latch-up. Additionally, the TLC2652 and TLC2652A incorporate internal ESD-protection circuits that prevent functional failures at voltages up to 2000 V as tested under MIL-STD-883C, Method 3015.2; however, care should be exercised in handling these devices as exposure to ESD may result in degradation of the device parametric performance.

The C-suffix devices are characterized for operation from 0°C to 70°C. The I-suffix devices are characterized for operation from –40°C to 85°C. The M-suffix devices are characterized for operation over the full military temperature range of –55°C to 125°C.

functional block diagram



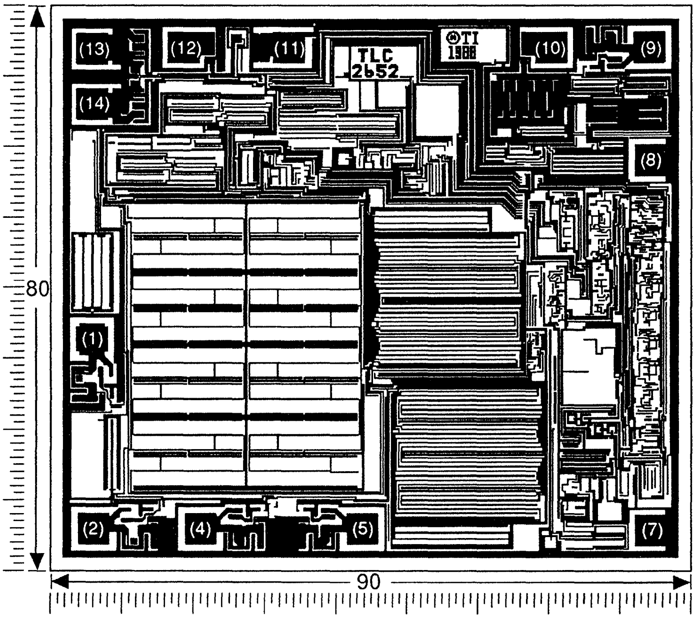
DISTRIBUTION OF TLC2652
INPUT OFFSET VOLTAGE



chip information

These chips, properly assembled, display characteristics similar to the TLE2024. Thermal compression or ultrasonic bonding may be used on the doped aluminum bonding pads. Chips may be mounted with conductive epoxy or a gold-silicon preform.

BONDING PAD ASSIGNMENTS



CHIP THICKNESS:
15 TYPICAL

BONDING PADS:
4 X 4 MINIMUM

$T_J$max = 150°C

TOLERANCES
ARE ± 10%

ALL DIMENSIONS
ARE IN MILS

PIN (7) INTERNALLY
CONNECTED TO
BACKSIDE OF CHIP

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{DD+} (see Note 1)	8 V
Supply voltage, V_{DD-} (see Note 1)	−8 V
Differential input voltage (see Note 2)	±16 V
Input voltage, V_I (any input, see Note 1)	±8 V
Voltage range on CLK IN and INT/$\overline{\text{EXT}}$ pins	V_{DD-} to V_{DD-} +5.2 V
Input current, I_I (each input)	±5 mA
Output current, I_O	±50 mA
Duration of short-circuit current at (or below) 25°C (see Note 3)	Unlimited
Current into CLK IN and INT/$\overline{\text{EXT}}$ pins	±5 mA
Continuous total dissipation	See Dissipation Rating Table
Operating free-air temperature, T_A: C-suffix	0°C to 70°C
I-suffix	−40°C to 85°C
M-suffix	−55°C to 125°C
Storage temperature range	−65°C to 150°C
Case temperature for 60 seconds: FK package	260°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D, N, or P package	260°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: J, or JG package	300°C

NOTES: 1. All voltage values, except differential voltages, are with respect to the midpoint between V_{DD+} and V_{DD-}.
2. Differential voltages are at the noninverting input with respect to the inverting input.
3. The output may be shorted to either supply. Temperature and/or supply voltages must be limited to ensure that the maximum dissipation rating is not exceeded.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING	$T_A = 125°C$ POWER RATING
D008	725 mW	5.8 mW/°C	464 mW	377 mW	145 mW
D014	950 mW	7.6 mW/°C	608 mW	494 mW	190 mW
FK	1375 mW	11 mW/°C	880 mW	715 mW	275 mW
J	1375 mW	11 mW/°C	880 mW	715 mW	275 mW
JG	1050 mW	8.4 mW/°C	672 mW	546 mW	210 mW
N	1575 mW	12.6 mW/°C	1008 mW	819 mW	315 mW
P	1000 mW	8.0 mW/°C	640 mW	520 mW	200 mW

recommended operating conditions

	C-SUFFIX		I-SUFFIX		M-SUFFIX		UNIT
	MIN	MAX	MIN	MAX	MIN	MAX	
Supply voltage, $V_{DD\pm}$	± 1.9	± 8	± 1.9	± 8	± 1.9	± 8	V
Common-mode input voltage, V_{IC}	V_{DD-}	$V_{DD+} - 1.9$	V_{DD-}	$V_{DD+} - 1.9$	V_{DD-}	$V_{DD+} - 1.9$	V
Clock input voltage	V_{DD-}	$V_{DD-} + 5$	V_{DD-}	$V_{DD-} + 5$	V_{DD-}	$V_{DD-} + 5$	V
Operating free-air temperature, T_A	0	70	− 40	85	− 55	125	°C

electrical characteristics at specified free-air temperature, $V_{DD\pm} = \pm 5$ V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A†	TLC2652C			TLC2652AC			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	$V_{IC} = 0$, $R_S = 50\ \Omega$	25°C		0.6	3		0.5	1	μV
			Full range			4.35			2.35	
α_{VIO}	Temperature coefficient of input offset voltage		Full range		0.003	0.03		0.003	0.03	μV/°C
	Input offset voltage long-term drift (see Note 4)		25°C		0.003	0.06		0.003	0.02	μV/mo
I_{IO}	Input offset current		25°C		2			2		pA
			Full range			100			100	
I_{IB}	Input bias current		25°C		4			4		pA
			Full range			100			100	
V_{ICR}	Common-mode input voltage range	$R_S = 50\ \Omega$	Full range	−5 to 3.1			−5 to 3.1			V
V_{OM+}	Maximum positive peak output voltage swing	$R_L = 10$ kΩ, See Note 5	25°C	4.7	4.8		4.7	4.8		V
			Full range	4.7			4.7			
V_{OM-}	Maximum negative peak output voltage swing	$R_L = 10$ kΩ, See Note 5	25°C	−4.7	−4.9		−4.7	−4.9		V
			Full range	−4.7			−4.7			
A_{VD}	Large-signal differential voltage amplification	$V_O = \pm 4$ V, $R_L = 10$ kΩ	25°C	120	150		135	150		dB
			Full range	120			130			
f_{ch}	Internal chopping frequency		25°C		450			450		Hz
	Clamp on-state current	$R_L = 100$ kΩ	25°C	25			25			μA
			Full range	25			25			
	Clamp off-state current	$V_O = -4$ V to 4 V	25°C			100			100	pA
			Full range			100			100	
CMRR	Common-mode rejection ratio	$V_O = 0$, $V_{IC} = V_{ICR}$ min, $R_S = 50\ \Omega$	25°C	120	140		120	140		dB
			Full range	120			120			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD\pm} / \Delta V_{IO}$)	$V_{DD\pm} = \pm 1.9$ V to ± 8 V, $V_O = 0$, $R_S = 50\ \Omega$	25°C	120	135		120	135		dB
			Full range	120			120			
I_{DD}	Supply current		25°C		1.5	2.4		1.5	2.4	mA
			Full range			2.5			2.5	

†Full range is 0°C to 70°C.

NOTES: 4. Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at $T_A = 150$°C extrapolated to $T_A = 25$°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

5. Output clamp is not connected.

operating characteristics at specified free-air temperature, $V_{DD\pm} = \pm5$ V

PARAMETER		TEST CONDITIONS	T_A†	TLC2652C			TLC2652AC			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
SR +	Positive slew rate at unity gain	$V_O = \pm2.3$ V, $R_L = 10$ kΩ, $C_L = 100$ pF	25°C	2	2.8		2	2.8		V/μs
			Full range	1.5			1.5			
SR −	Negative slew rate at unity gain		25°C	2.3	3.1		2.3	3.1		V/μs
			Full range	1.8			1.8			
V_n	Equivalent input noise voltage (see Note 6)	f = 10 Hz	25°C		94			94	140	nV/√Hz
		f = 1 kHz	25°C		23			23	35	
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0 to 1 Hz	25°C		0.8			0.8		μV
		f = 0 to 10 Hz	25°C		2.8			2.8		
I_n	Equivalent input noise current	f = 1 kHz	25°C		0.004			0.004		pA/√Hz
	Gain-bandwidth product	f = 10 kHz, $R_L = 10$ kΩ, $C_L = 100$ pF	25°C		1.9			1.9		MHz
ϕ_m	Phase margin at unity gain	$R_L = 10$ kΩ, $C_L = 100$ pF	25°C		48°			48°		

†Full range is 0°C to 70°C.

NOTE 6: This parameter is tested on a sample basis for the TLC2652A. For other test requirements, please contact the factory. This statement has no bearing on testing or nontesting of other parameters.

electrical characteristics at specified free-air temperature, $V_{DD\pm} = \pm 5$ V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A†	TLC2652I			TLC2652AI			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	$V_{IC} = 0$, $R_S = 50\ \Omega$	25°C		0.6	3		0.5	1	µV
			Full range			4.95			2.95	
α_{VIO}	Temperature coefficient of input offset voltage		Full range		0.003	0.03		0.003	0.03	µV/°C
	Input offset voltage long-term drift (see Note 4)		25°C		0.003	0.06		0.003	0.02	µV/mo
I_{IO}	Input offset current		25°C		2			2		pA
			Full range			150			150	
I_{IB}	Input bias current		25°C		4			4		pA
			Full range			150			150	
V_{ICR}	Common-mode input voltage range	$R_S = 50\ \Omega$	Full range	−5 to 3.1			−5 to 3.1			V
V_{OM+}	Maximum positive peak output voltage swing	$R_L = 10\ k\Omega$, See Note 5	25°C	4.7	4.8		4.7	4.8		V
			Full range	4.7			4.7			
V_{OM-}	Maximum negative peak output voltage swing	$R_L = 10\ k\Omega$, See Note 5	25°C	−4.7	−4.9		−4.7	−4.9		V
			Full range	−4.7			−4.7			
A_{VD}	Large-signal differential voltage amplification	$V_O = \pm 4$ V, $R_L = 10\ k\Omega$	25°C	120	150		135	150		dB
			Full range	120			125			
f_{ch}	Internal chopping frequency		25°C		450			450		Hz
	Clamp on-state current	$R_L = 100\ k\Omega$	25°C	25			25			µA
			Full range	25			25			
	Clamp off-state current	$V_O = -4$ V to 4 V	25°C			100			100	pA
			Full range			100			100	
CMRR	Common-mode rejection ratio	$V_O = 0$, $V_{IC} = V_{ICR}$ min, $R_S = 50\ \Omega$	25°C	120	140		120	140		dB
			Full range	120			120			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD\pm} / \Delta V_{IO}$)	$V_{DD\pm} = \pm 1.9$ V to ± 8 V, $V_O = 0$, $R_S = 50\ \Omega$	25°C	120	135		120	135		dB
			Full range	120			120			
I_{DD}	Supply current	$V_O = 0$, No load	25°C		1.5	2.4		1.5	2.4	mA
			Full range			2.5			2.5	

†Full range is − 40°C to 85°C.

NOTES: 4. Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at $T_A = 150$°C extrapolated to $T_A = 25$°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

5. Output clamp is not connected.

operating characteristics at specified free-air temperature, $V_{DD\pm} = \pm 5$ V

PARAMETER		TEST CONDITIONS	T_A†	TLC2652I			TLC2652AI			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
SR +	Positive slew rate at unity gain	V_O = ± 2.3 V, R_L = 10 kΩ, C_L = 100 pF	25°C	2	2.8		2	2.8		V/μs
			Full range	1.4			1.4			
SR −	Negative slew rate at unity gain		25°C	2.3	3.1		2.3	3.1		V/μs
			Full range	1.7			1.7			
V_n	Equivalent input noise voltage (see Note 6)	f = 10 Hz	25°C		94			94	140	nV/√Hz
		f = 1 kHz	25°C		23			23	35	
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0 to 1 Hz	25°C		0.8			0.8		μV
		f = 0 to 10 Hz	25°C		2.8			2.8		
I_n	Equivalent input noise current	f = 1 kHz	25°C		0.004			0.004		pA/√Hz
	Gain-bandwidth product	f = 10 kHz, R_L = 10 kΩ, C_L = 100 pF	25°C		1.9			1.9		MHz
ϕ_m	Phase margin at unity gain	R_L = 10 kΩ, C_L = 100 pF	25°C		48°			48°		

†Full range is – 40°C to 85°C.

NOTE 6: This parameter is tested on a sample basis for the TLC2652A. For other test requirements, please contact the factory. This statement has no bearing on testing or nontesting of other parameters.

electrical characteristics at specified free-air temperature, $V_{DD\pm} = \pm 5$ V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A†	TLC2652M			TLC2652AM			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage (see Note 7)	$V_{IC} = 0$, $R_S = 50\ \Omega$	25°C		0.6	3.5		0.5	3	μV
			Full range			10			8	
α_{VIO}	Temperature coefficient of input offset voltage		Full range		0.003	0.03*		0.003	0.03*	μV/°C
	Input offset voltage long-term drift (see Note 4)		25°C		0.003	0.06*		0.003	0.02*	μV/mo
I_{IO}	Input offset current		25°C		2			2		pA
			Full range			500			500	
I_{IB}	Input bias current		25°C		4			4		pA
			Full range			500			500	
V_{ICR}	Common-mode input voltage range	$R_S = 50\ \Omega$	Full range	−5 to 3.1			−5 to 3.1			V
V_{OM+}	Maximum positive peak output voltage swing	$R_L = 10$ kΩ, See Note 5	25°C	4.7	4.8		4.7	4.8		V
			Full range	4.7			4.7			
V_{OM-}	Maximum negative peak output voltage swing	$R_L = 10$ kΩ, See Note 5	25°C	−4.7	−4.9		−4.7	−4.9		V
			Full range	−4.7			−4.7			
A_{VD}	Large-signal differential voltage amplification	$V_O = \pm 4$ V, $R_L = 10$ kΩ	25°C	120	150		135	150		dB
			Full range	120			120			
f_{ch}	Internal chopping frequency		25°C		450			450		Hz
	Clamp on-state current	$R_L = 100$ kΩ	25°C	25			25			μA
			Full range	25			25			
	Clamp off-state current	$V_O = -4$ V to 4 V	25°C			100			100	pA
			Full range			500			500	
CMRR	Common-mode rejection ratio	$V_O = 0$, $V_{IC} = V_{ICR}$ min, $R_S = 50\ \Omega$	25°C	120	140		120	140		dB
			Full range	120			120			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD\pm} / \Delta V_{IO}$)	$V_{DD\pm} = \pm 1.9$ V to ± 8 V, $V_O = 0$, $R_S = 50\ \Omega$	25°C	120	135		120	135		dB
			Full range	120			120			
I_{DD}	Supply current	$V_O = 0$, No load	25°C		1.5	2.4		1.5	2.4	mA
			Full range			2.5			2.5	

* On products compliant to MIL-STD-883, Class B, this parameter is not production tested.

† Full range is – 55°C to 125°C.

NOTES: 4. Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at $T_A = 150$°C extrapolated to $T_A = 25$°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

5. Output clamp is not connected.

7. This parameter is not production tested. Thermocouple effects preclude measurement of the actual V_{IO} of these devices in high speed automated testing. V_{IO} is measured to a limit determined by the test equipment capability at the temperature extremes. The test ensures that the stabilization circuitry is performing properly.

operating characteristics at specified free-air temperature, $V_{DD\pm} = \pm 5$ V

PARAMETER		TEST CONDITIONS	T_A†	MIN	TYP	MAX	UNIT
SR +	Positive slew rate at unity gain	$V_O = \pm 2.3$ V, $R_L = 10$ kΩ, $C_L = 100$ pF	25°C	2	2.8		V/μs
			Full range	1.3			
SR −	Negative slew rate at unity gain		25°C	2.3	3.1		V/μs
			Full range	1.6			
V_n	Equivalent input noise voltage	f = 10 Hz	25°C		94		nV/√Hz
		f = 1 kHz	25°C		23		
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0 to 1 Hz	25°C		0.8		μV
		f = 0 to 10 Hz	25°C		2.8		
I_n	Equivalent input noise current	f = 1 kHz	25°C		0.004		pA/√Hz
	Gain-bandwidth product	f = 10 kHz, $R_L = 10$ kΩ, $C_L = 100$ pF	25°C		1.9		MHz
ϕ_m	Phase margin at unity gain	$R_L = 10$ kΩ, $C_L = 100$ pF	25°C		48°		

†Full range is – 55°C to 125°C.

electrical characteristics at $V_{DD\pm}$ = ± 5 V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	V_{IC} = 0, R_S = 50 Ω		0.6	3	µV
	Input offset voltage long-term drift (see Note 4)			0.003	0.006	µV/mo
I_{IO}	Input offset current			2		pA
I_{IB}	Input bias current			4		pA
V_{ICR}	Common-mode input voltage range	R_S = 50 Ω	−5 to 3.1			V
V_{OM+}	Maximum positive peak output voltage swing	R_L = 10 kΩ, See Note 5	4.7	4.8		V
V_{OM-}	Maximum negative peak output voltage swing	R_L = 10 kΩ, See Note 5	−4.7	−4.9		V
A_{VD}	Large-signal-differential voltage amplification	V_O = ± 4 V, R_L = 10 kΩ	120	150		dB
f_{ch}	Internal chopping frequency			450		Hz
	Clamp on-state current	R_L = 100 kΩ	25			µA
	Clamp off-state current	V_O = − 4 V to 4 V			100	pA
CMRR	Common-mode rejection ratio	V_O = 0, V_{IC} = V_{ICR}min, R_S = 50 Ω	120	140		dB
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD\pm}/\Delta V_{IO}$)	$V_{DD\pm}$ = ± 1.9 V to ± 8 V, V_O = 0, R_S = 50 Ω	120	135		dB
I_{DD}	Supply current	V_O = 0, no load		1.5	2.4	mA

NOTES: 4. Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at T_A = 150°C extrapolated to T_A = 25°C using the Arrhenius equation and assuming an activation energy of 0.096 eV.

5. Output clamp is not connected.

operating characteristics at $V_{DD\pm}$ = ± 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SR +	Positive slew rate at unity gain	V_O = ± 2.3 V, R_L = 10 kΩ, C_L = 100 pF	2	2.8		V/µs
SR −	Negative slew rate at unity gain		2.3	3.1		V/µs
V_n	Equivalent input noise voltage	f = 10 Hz		94		nV/√Hz
		f = 1 kHz		23		
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0 to 1 Hz		0.8		µV
		f = 0 to 10 Hz		2.8		
I_n	Equivalent input noise current	f = 1 kHz				pA/√Hz
	Gain-bandwidth product	f = 10 kHz, R_L = 10 kΩ, C_L = 100 pF		1.9		MHz
ϕ_m	Phase margin at unity gain	R_L = 10 kΩ, C_L = 100 pF		48°		

TYPICAL CHARACTERISTICS

table of graphs

			FIGURE
V_{IO}	Normalized input offset voltage	vs Chopping frequency	1
I_{IB}	Input bias current	vs Common-mode input voltage	2
		vs Chopping frequency	3
		vs Temperature	4
I_{IO}	Input offset current	vs Chopping frequency	5
		vs Temperature	6
	Clamp current	vs Output voltage	7
$V_{O(PP)}$	Maximum peak-to-peak output voltage swing	vs Frequency	8
V_{OM}	Maximum peak output voltage swing	vs Output current	9, 10
		vs Temperature	11, 12
A_{VD}	Differential voltage amplification	vs Frequency	13
		vs Temperature	14
f_{ch}	Chopping frequency	vs Supply voltage	15
		vs Temperature	16
I_{DD}	Supply current	vs Supply voltage	17
		vs Temperature	18
I_{OS}	Short-circuit output current	vs Supply voltage	19
		vs Temperature	20
SR	Slew rate	vs Supply voltage	21
		vs Temperature	22
	Pulse response	Small-signal	23
		Large-signal	24
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	vs Chopping frequency	25, 26
V_n	Equivalent input noise voltage	vs Frequency	27
	Gain-bandwidth product	vs Supply voltage	28
		vs Temperature	29
ϕ_m	Phase margin	vs Supply voltage	30
		vs Temperature	31
		vs Load capacitance	32
	Phase shift	vs Frequency	13

TYPICAL CHARACTERISTICS†

NORMALIZED INPUT OFFSET VOLTAGE vs CHOPPING FREQUENCY

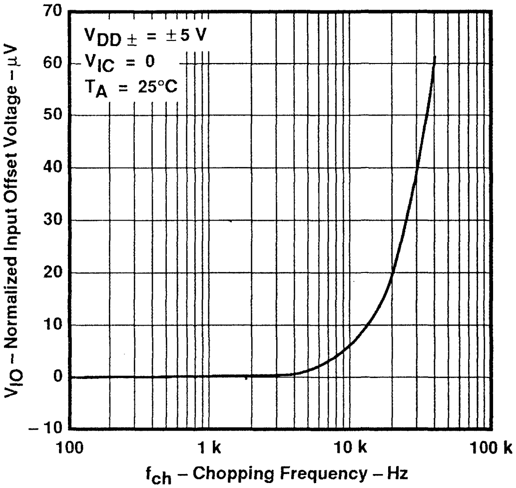


Figure 1

INPUT BIAS CURRENT vs COMMON-MODE INPUT VOLTAGE

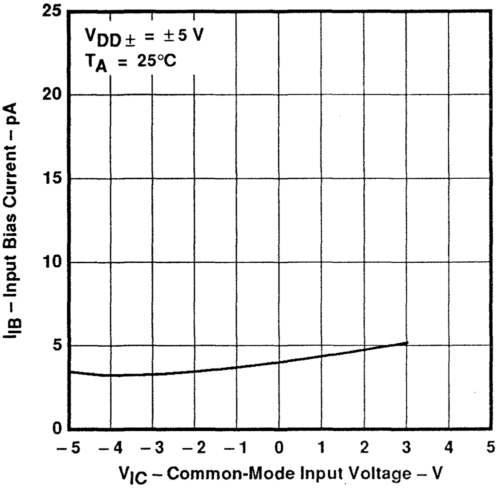


Figure 2

INPUT BIAS CURRENT vs CHOPPING FREQUENCY

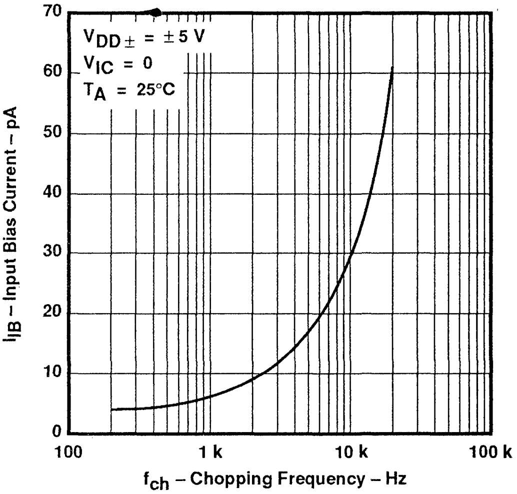


Figure 3

INPUT BIAS CURRENT vs FREE-AIR TEMPERATURE

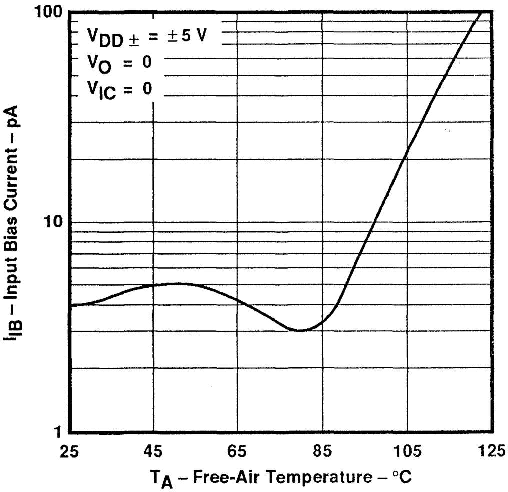


Figure 4

---

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

INPUT OFFSET CURRENT
vs
CHOPPING FREQUENCY

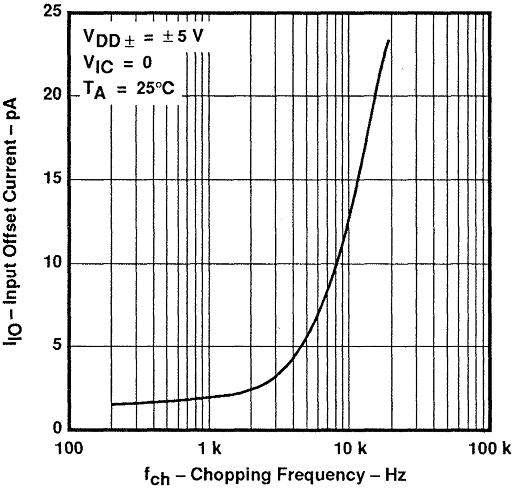


Figure 5

INPUT OFFSET CURRENT
vs
FREE-AIR TEMPERATURE

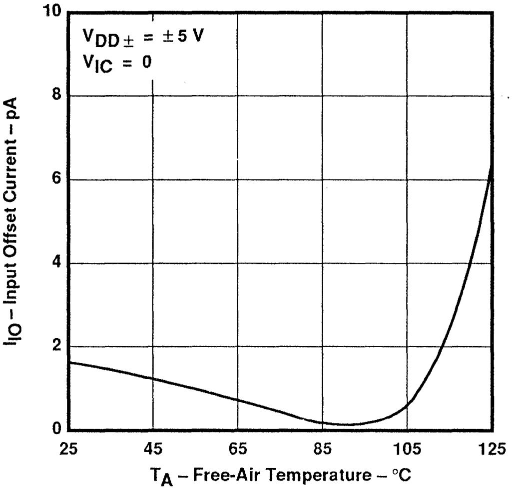


Figure 6

CLAMP CURRENT
vs
OUTPUT VOLTAGE

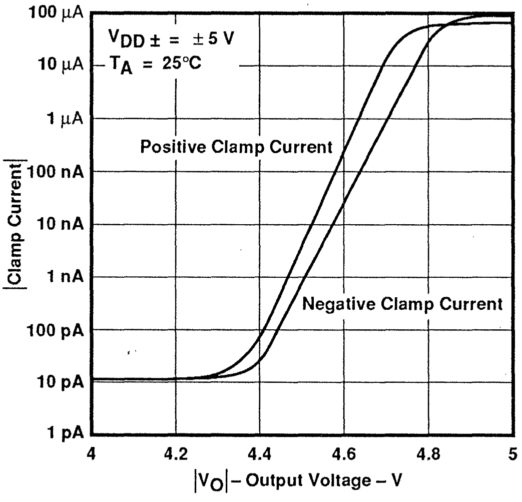


Figure 7

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE
vs
FREQUENCY

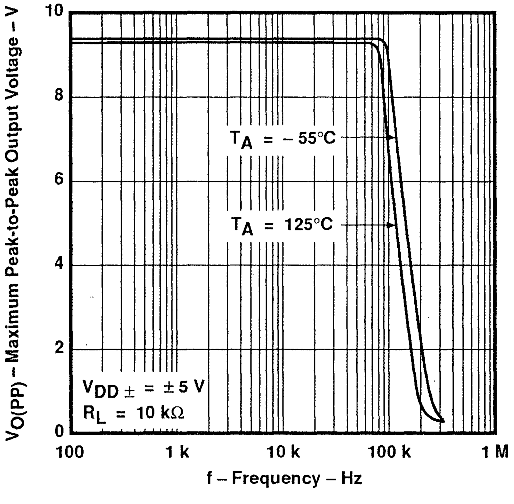


Figure 8

---

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

MAXIMUM PEAK OUTPUT VOLTAGE
vs
OUTPUT CURRENT

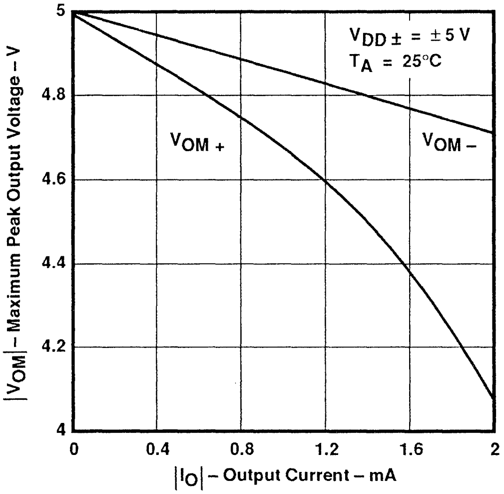


Figure 9

MAXIMUM PEAK OUTPUT VOLTAGE
vs
OUTPUT CURRENT

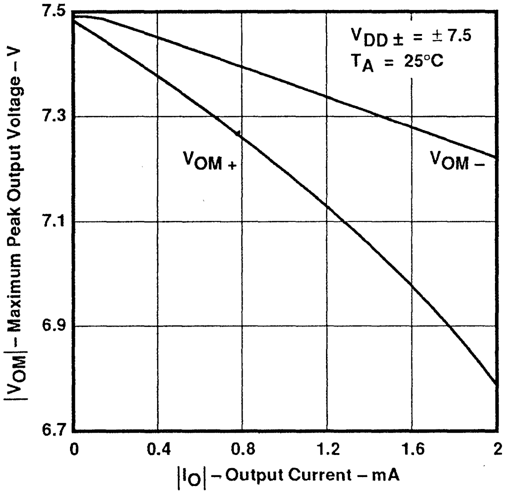


Figure 10

MAXIMUM PEAK OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

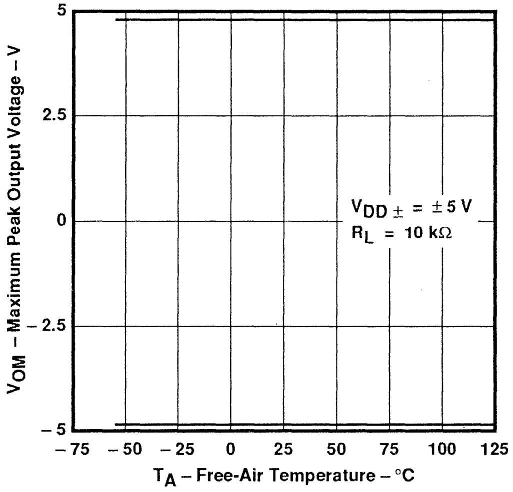


Figure 11

MAXIMUM PEAK OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

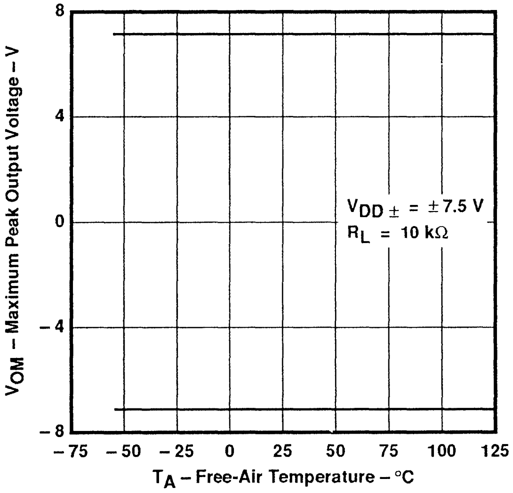


Figure 12

---

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION AND PHASE SHIFT
vs
FREQUENCY

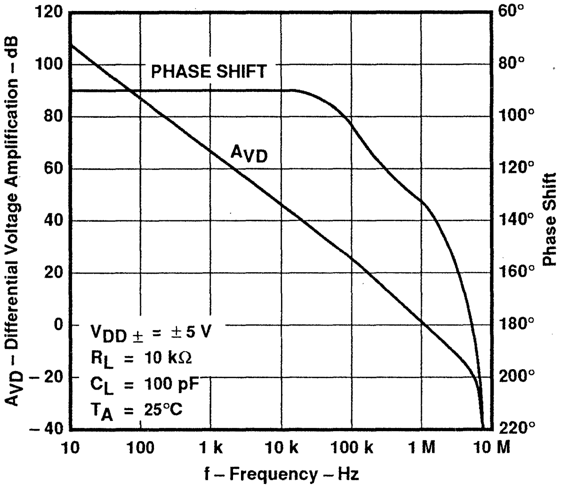


Figure 13

LARGE-SIGNAL VOLTAGE AMPLIFICATION
vs
FREE-AIR TEMPERATURE

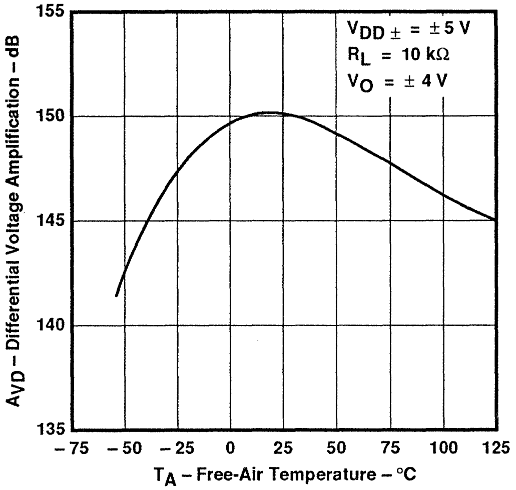


Figure 14

CHOPPING FREQUENCY
vs
SUPPLY VOLTAGE

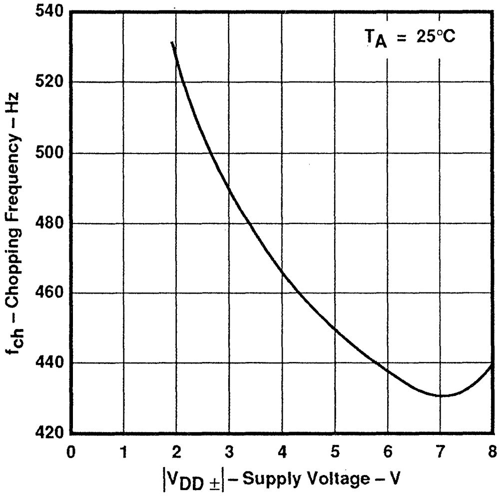


Figure 15

CHOPPING FREQUENCY
vs
FREE-AIR TEMPERATURE

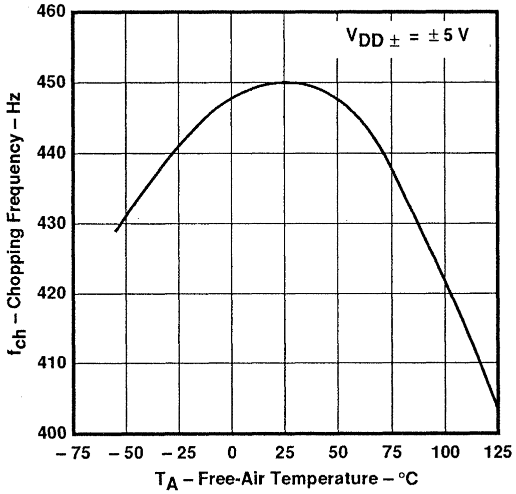


Figure 16

---

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

SUPPLY CURRENT
vs
SUPPLY VOLTAGE

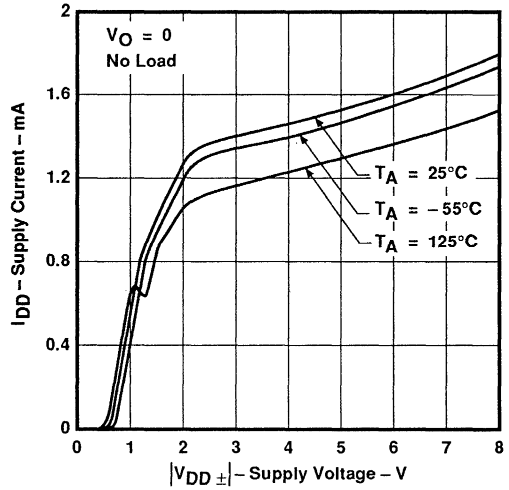


Figure 17

SUPPLY CURRENT
vs
FREE-AIR TEMPERATURE

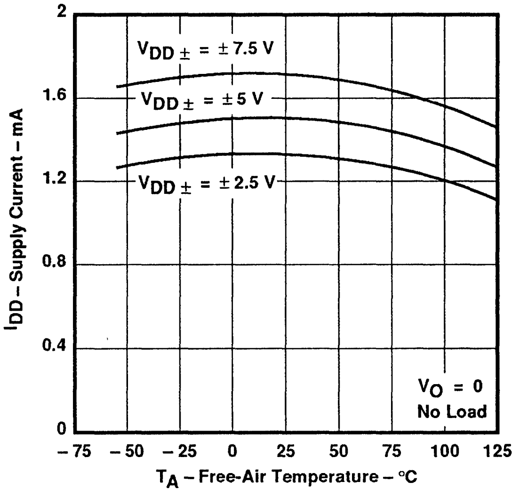


Figure 18

SHORT-CIRCUIT OUTPUT CURRENT
vs
SUPPLY VOLTAGE

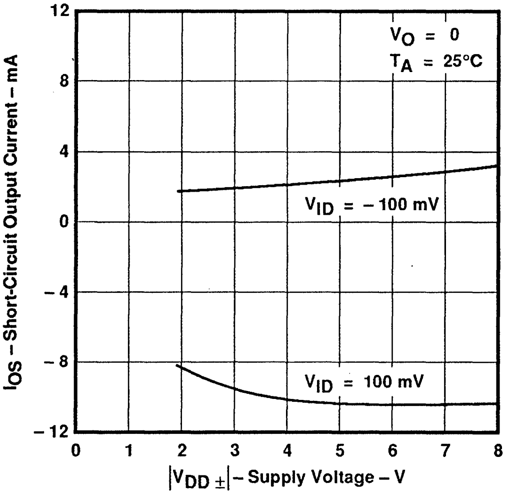


Figure 19

SHORT-CIRCUIT OUTPUT CURRENT
vs
FREE-AIR TEMPERATURE

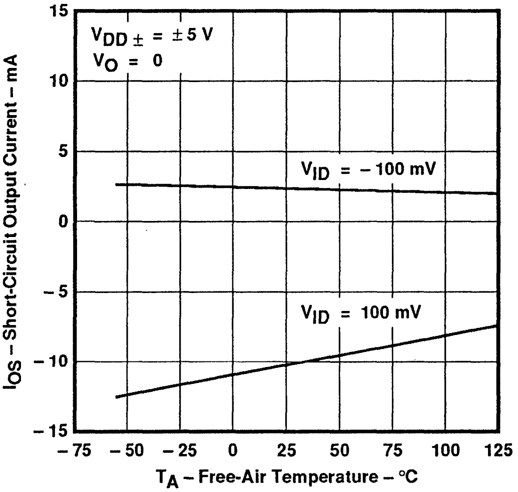


Figure 20

---

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

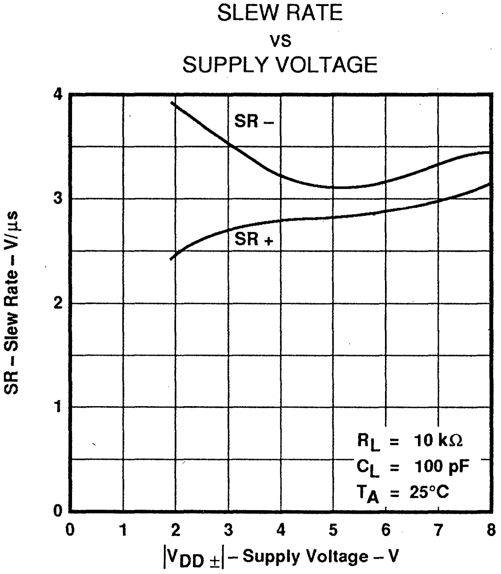


Figure 21

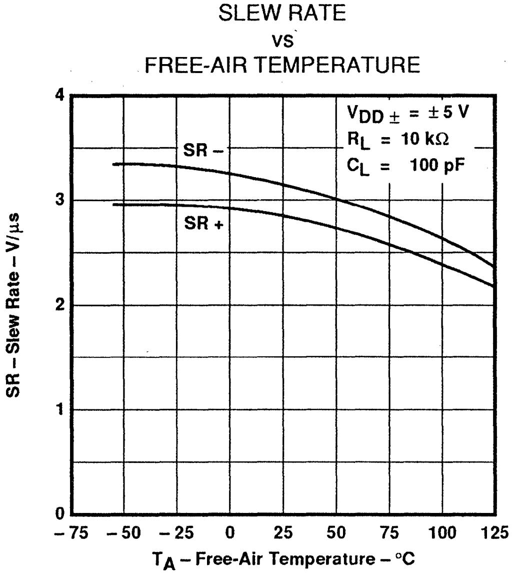


Figure 22

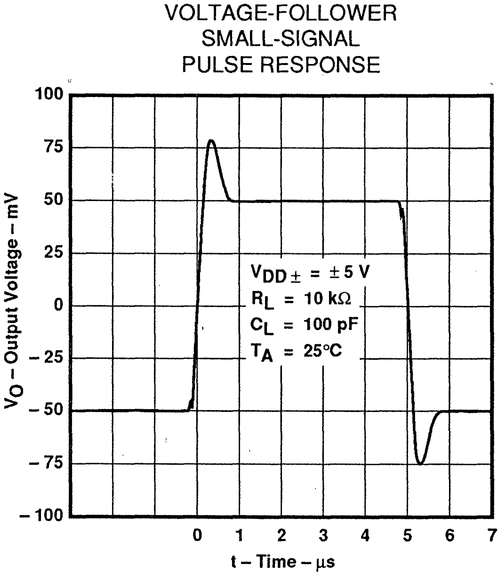


Figure 23

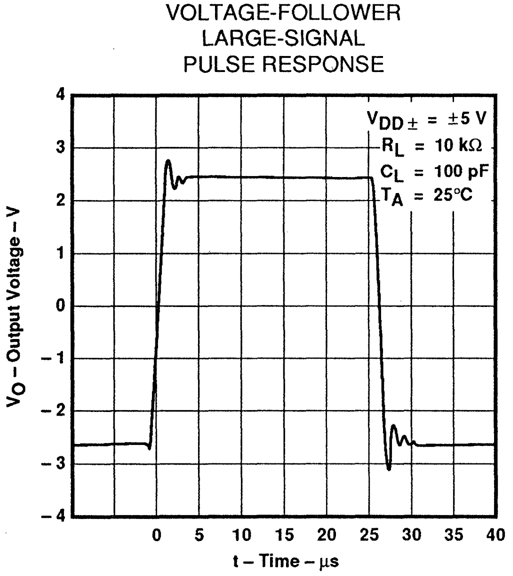


Figure 24

---

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS

PEAK-TO-PEAK INPUT NOISE VOLTAGE
vs
CHOPPING FREQUENCY

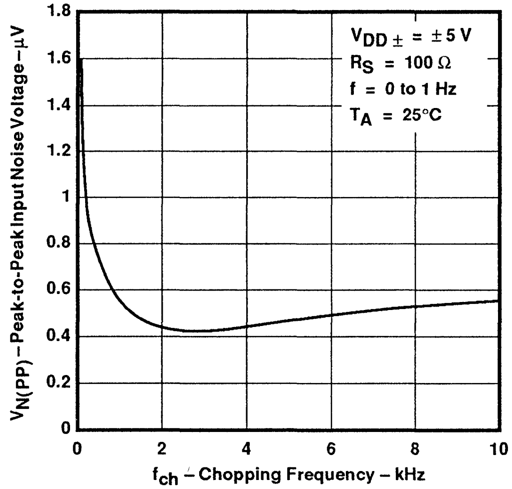


Figure 25

PEAK-TO-PEAK INPUT NOISE VOLTAGE
vs
CHOPPING FREQUENCY

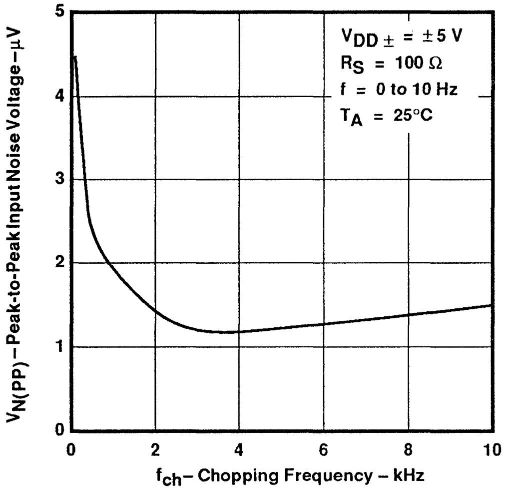


Figure 26

EQUIVALENT INPUT NOISE VOLTAGE
vs
FREQUENCY

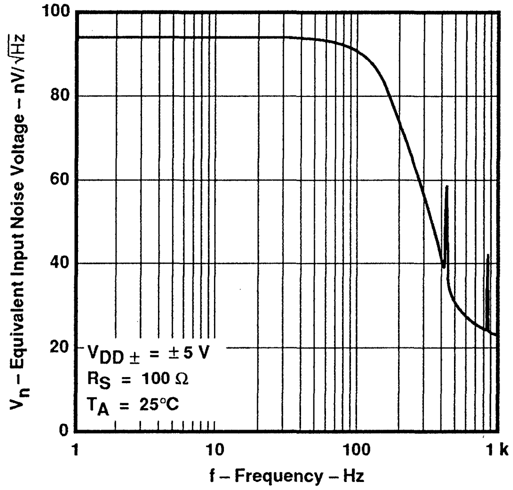


Figure 27

GAIN-BANDWIDTH PRODUCT
vs
SUPPLY VOLTAGE

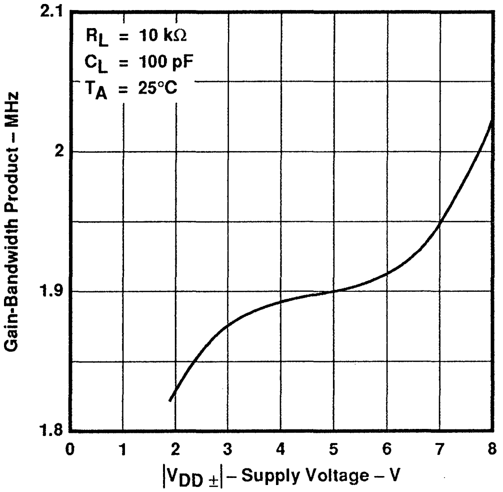


Figure 28

TYPICAL CHARACTERISTICS†

GAIN-BANDWIDTH PRODUCT
vs
FREE-AIR TEMPERATURE

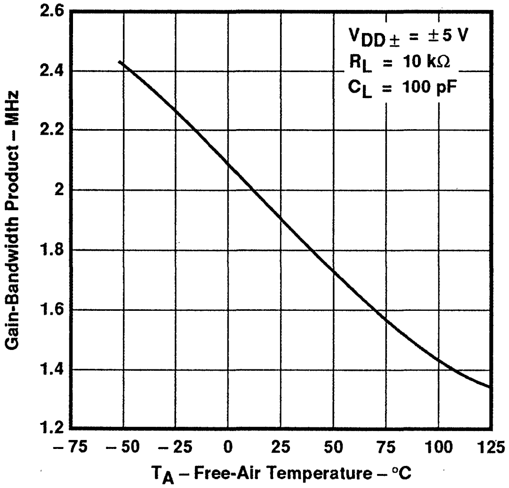


Figure 29

PHASE MARGIN
vs
SUPPLY VOLTAGE

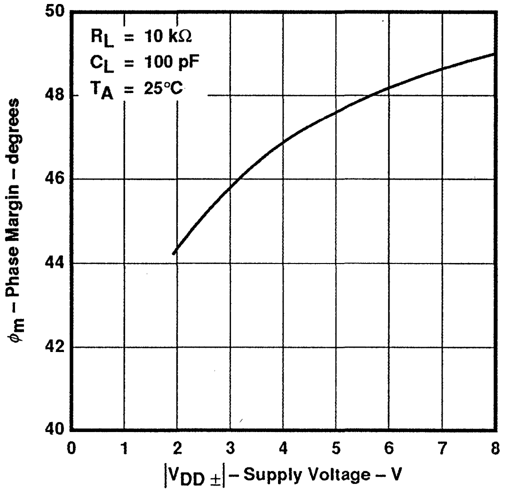


Figure 30

PHASE MARGIN
vs
FREE-AIR TEMPERATURE

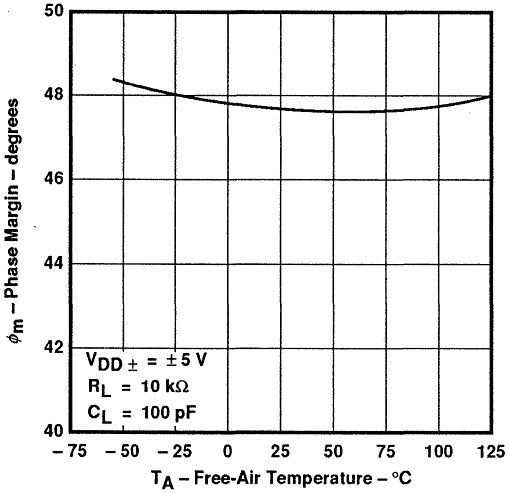


Figure 31

PHASE MARGIN
vs
LOAD CAPACITANCE

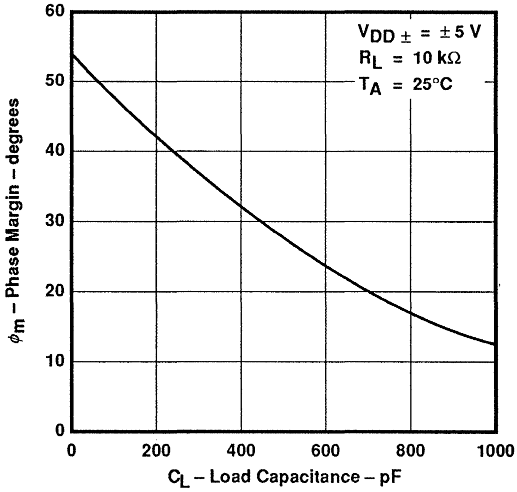


Figure 32

---

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

APPLICATION INFORMATION

capacitor selection and placement

The two important factors to consider when selecting external capacitors C_{XA} and C_{XB} are leakage and dielectric absorption. Both factors can cause system degradation, negating the performance advantages realized by using the TLC2652.

Degradation from capacitor leakage becomes more apparent with increasing temperatures. Low-leakage capacitors and standoffs are recommended for operation at T_A = 125°C. In addition, guard bands are recommended around the capacitor connections on both sides of the printed circuit board to alleviate problems caused by surface leakage on circuit boards.

Capacitors with high dielectric absorption tend to take several seconds to settle upon application of power, which directly affects input offset voltage. In applications where fast settling of input offset voltage is needed, it is recommended that high-quality film capacitors, such as mylar, polystyrene, or polypropylene, be used. In other applications, however, a ceramic or other low-grade capacitor may suffice.

Unlike many choppers available today, the TLC2652 is designed to function with values of C_{XA} and C_{XB} in the range of 0.1 µF to 1 µF without degradation to input offset voltage or input noise voltage. These capacitors should be located as close as possible to the C_{XA} and C_{XB} pins and returned to either the V_{DD-} pin or the C RETURN pin. Note that on many choppers, connecting these capacitors to the V_{DD-} pin causes degradation in noise performance. This problem is eliminated on the TLC2652.

internal/external clock

The TLC2652 has an internal clock that sets the chopping frequency to a nominal value of 450 Hz. On 8-pin packages, the chopping frequency can only be controlled by the internal clock; however, on all 14-pin packages and the 20-pin FK package, the device chopping frequency may be set by the internal clock or controlled externally by use of the INT/$\overline{\text{EXT}}$ and CLK IN pins. To use the internal 450-Hz clock, no connection is necessary. If external clocking is desired, connect the INT/$\overline{\text{EXT}}$ pin to V_{DD-} and the external clock to CLK IN. The external clock trip point is 2.5 V above the negative rail; however, the CLK IN pin may be driven from the negative rail to 5 V above the negative rail. If this level is exceeded, damage could occur to the device unless the current into the CLK IN pin is limited to ±5 mA. When operating in the single-supply configuration, this feature allows the TLC2652 to be driven directly by 5-V TTL and CMOS logic. A divide-by-two frequency divider interfaces with the CLK IN pin and sets the chopping frequency. The duty cycle of the external clock is not critical but should be kept between 30% and 60%.

overload recovery/output clamp

When large differential input voltage conditions are applied to the TLC2652, the nulling loop will attempt to prevent the output from saturating by driving C_{XA} and C_{XB} to internally-clamped voltage levels. Once the overdrive condition is removed, a period of time is required to allow the built-up charge to dissipate. This time period is defined as overload recovery time (see Figure 33). Typical overload recovery time for the TLC2652 is significantly faster than competitive products; however, if required, this time can be reduced further by use of internal clamp circuitry accessible through the CLAMP pin.

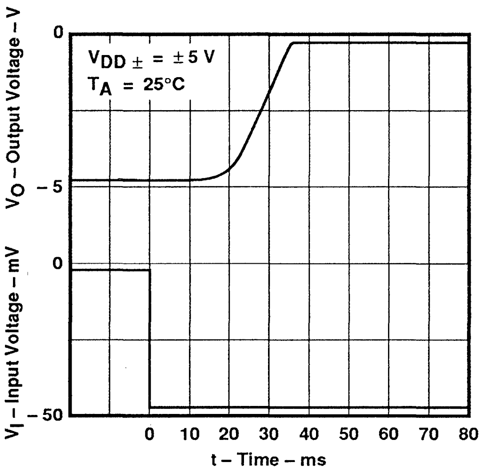


Figure 33. Overload Recovery

APPLICATION INFORMATION

The clamp is simply a switch that is automatically activated when the output is approximately 1 V from either supply rail. When connected to the inverting input (in parallel with the closed-loop feedback resistor), the closed-loop gain is reduced and the TLC2652 output is prevented from going into saturation. Since the output must source or sink current through the switch (see Figure 7), the maximum output voltage swing is slightly reduced.

thermoelectric effects

To take advantage of the extremely low offset voltage drift of the TLC2652, care must be taken to compensate for the thermoelectric effects present when two dissimilar metals are brought into contact with each other (such as device leads being soldered to a printed circuit board). Dissimilar metal junctions can produce thermoelectric voltages in the range of several microvolts per degree Celsius (orders of magnitude greater than the 0.01-µV/°C typical of the TLC2652).

To help minimize thermoelectric effects, careful attention should be paid to component selection and circuit board layout. Avoid the use of nonsoldered connections (such as sockets, relays, switches, etc.) in the input signal path. Cancel thermoelectric effects by duplicating the number of components and junctions in each device input. The use of low-thermoelectric-coefficient components, such as wire-wound resistors, is also beneficial.

latch-up avoidance

Because CMOS devices are susceptible to latch-up due to their inherent parasitic thyristors, the TLC2652 inputs and output are designed to withstand –100-mA surge currents without sustaining latch-up; however, techniques to reduce the chance of latch-up should be used whenever possible. Internal protection diodes should not, by design, be forward biased. Applied input and output voltages should not exceed the supply voltage by more than 300 mV. Care should be exercised when using capacitive coupling on pulse generators. Supply transients should be shunted by the use of decoupling capacitors (0.1 µF typical) located across the supply rails as close to the device as possible.

The current path established if latch-up occurs is usually between the supply rails and is limited only by the impedance of the power supply and the forward resistance of the parasitic thyristor. The chance of latch-up occurring increases with increasing temperature and supply voltage.

electrostatic discharge protection

The TLC2652 incorporates internal ESD-protection circuits that prevent functional failures at voltages at or below 2000 V. Care should be exercised in handling these devices, as exposure to ESD may result in degradation of the device parametric performance.

theory of operation

Chopper-stabilized operational amplifiers offer the best dc performance of any monolithic operational amplifier. This superior performance is the result of using two operational amplifiers – a main amplifier and a nulling amplifier – plus oscillator-controlled logic and two external capacitors to create a system that behaves as a single amplifier. With this approach, the TLC2652 achieves submicrovolt input offset voltage, submicrovolt noise voltage, and offset voltage variations with temperature in the nV/°C range.

The TLC2652 on-chip control logic produces two dominant clock phases: a nulling phase and an amplifying phase. The term "chopper-stabilized" derives from the process of switching between these two clock phases. Figure 34 shows a simplified block diagram of the TLC2652. Switches A and B are make-before-break types. During the nulling phase, switch A is closed, shorting the nulling amplifier inputs together and allowing the nulling amplifier to reduce its own input offset voltage by feeding its output signal back to an inverting input

APPLICATION INFORMATION

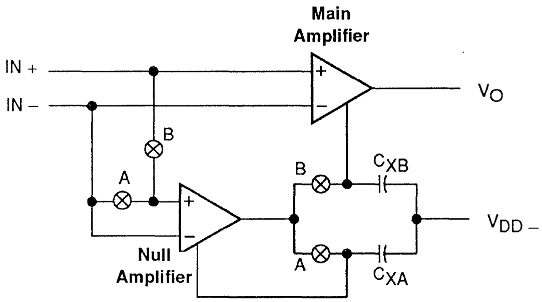


Figure 34. TLC2652 Simplified Block Diagram

node. Simultaneously, external capacitor C_{XA} stores the nulling potential to allow the offset voltage of the amplifier to remain nulled during the amplifying phase.

During the amplifying phase, switch B is closed, connecting the output of the nulling amplifier to a noninverting input of the main amplifier. In this configuration, the input offset voltage of the main amplifier is nulled. Also, external capacitor C_{XB} stores the nulling potential to allow the offset voltage of the main amplifier to remain nulled during the next nulling phase.

This continuous chopping process allows offset voltage nulling during variations in time and temperature and over the common-mode input voltage range and power supply range. In addition, because the low-frequency signal path is through both the null and main amplifiers, extremely high gain is achieved.

The low-frequency noise of a chopper amplifier depends on the magnitude of the component noise prior to chopping and the capability of the circuit to reduce this noise while chopping. The use of the Advanced LinCMOS process, with its low-noise analog MOS transistors and patent-pending input stage design, significantly reduces the input noise voltage.

The primary source of nonideal operation in chopper-stabilized amplifiers is error charge from the switches.

As charge imbalance accumulates on critical nodes, input offset voltage can increase, especially with increasing chopping frequency. This problem has been significantly reduced in the TLC2652 by use of a patent-pending compensation circuit and the Advanced LinCMOS process.

The TLC2652 incorporates a feed-forward design that ensures continuous frequency response. Essentially, the gain magnitude of the nulling amplifier and compensation network crosses unity at the break frequency of the main amplifier. As a result, the high-frequency response of the system is the same as the frequency response of the main amplifier. This approach also ensures that the slewing characteristics remain the same during both the nulling and amplifying phases.

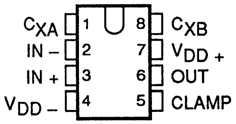
TLC2654, TLC2654A, TLC2654Y
Advanced LinCMOS™ LOW-NOISE CHOPPER-STABILIZED OPERATIONAL AMPLIFIERS

D3174, NOVEMBER 1988 – REVISED AUGUST 1991

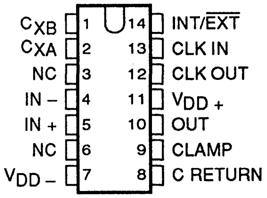
available features

- Input Noise Voltage
  0.5 µV p-p Typ, f = 0 to 1 Hz
  1.5 µV p-p Typ, f = 0 to 10 Hz
  47 nV/√Hz Typ, f = 10 Hz
  13 nV/√Hz Typ, f = 1 kHz
- High Chopping Frequency . . . 10 kHz Typ
- No Clock Noise Below 10 kHz
- No Intermodulation Error Below 5 kHz
- Low Input Offset Voltage . . . 10 µV Max
- Excellent Offset Voltage Stability With Temperature . . . 0.05 µV/°C Max
- A_{VD} . . . 135 dB Min
- CMRR . . . 110 dB Min
- k_{SVR} . . . 120 dB Min
- Single-Supply Operation
- Common-Mode Input Voltage Range Includes the Negative Rail
- No Noise Degradation With External Capacitors Connected to V_{DD-}

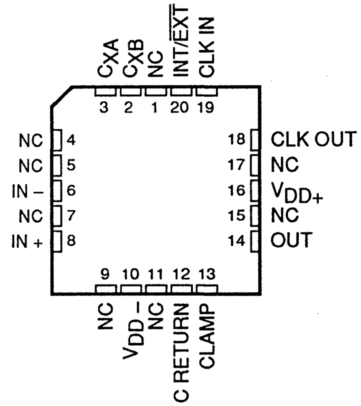
D008, JG, OR P PACKAGE
(TOP VIEW)



D014, J, OR N PACKAGE
(TOP VIEW)



FK PACKAGE
(TOP VIEW)



NC – No internal connection

AVAILABLE OPTIONS

T_A	V_{IO} max AT 25°C	PACKAGE							CHIP FORM (Y)
		8-PIN			14-PIN			20-PIN	
		SMALL-OUTLINE (D008)	CERAMIC DIP (JG)	PLASTIC DIP (P)	SMALL-OUTLINE (D014)	CERAMIC DIP (J)	PLASTIC DIP (N)	CHIP CARRIER (FK)	
0°C to 70°C	10 µV	TLC2654AC-8D	–	TLC2654ACP	TLC2654AC-14D	–	TLC2654ACN	–	TLC2654Y
	20 µV	TLC2654C-8D	–	TLC2654CP	TLC2654C-14D	–	TLC2654CN	–	
– 40°C to 85°C	10 µV	TLC2654AI-8D	–	TLC2654AIP	TLC2654AI-14D	–	TLC2654AIN	–	
	20 µV	TLC2654I-8D	–	TLC2654IP	TLC2654I-14D	–	TLC2654IN	–	
– 55°C to 125°C	10 µV	TLC2654AM-8D	TLC2654AMJG	TLC2654AMP	TLC2654AM-14D	TLC2654AMJ	TLC2654AMN	TLC2654AMFK	
	20 µV	TLC2654M-8D	TLC2654MJG	TLC2654MP	TLC2654M-14D	TLC2654MJ	TLC2654MN	TLC2654MFK	

D008 and D014 packages are available taped and reeled. Add "R" suffix to device type (e.g., TLC2654AC-8DR).

Advanced LinCMOS is a trademark of Texas Instruments Incorporated.

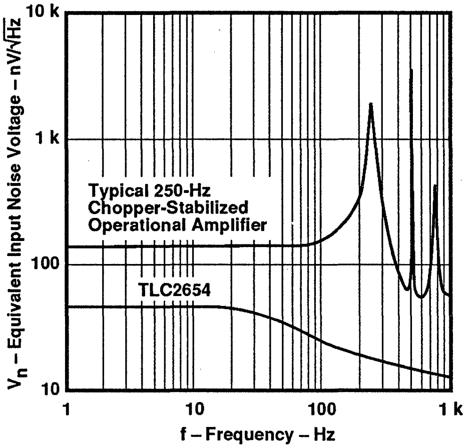
TEXAS INSTRUMENTS
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

description

The TLC2654 and TLC2654A are low-noise chopper-stabilized operational amplifiers using the Advanced LinCMOS™ process. Combining this process with chopper stabilization circuitry makes excellent dc precision possible. In addition, circuit techniques are added that give the TLC2654 and TLC2654A noise performance unsurpassed by similar devices.

Chopper stabilization techniques provide for extremely high dc precision by continuously nulling input offset voltage even during variations in temperature, time, common-mode voltage, and power supply voltage. The high chopping frequency of the TLC2654 and TLC2654A provides excellent noise performance in a frequency spectrum from near dc to 10 kHz. In addition, intermodulation or aliasing error is eliminated from frequencies up to 5 kHz.

EQUIVALENT INPUT NOISE VOLTAGE
vs
FREQUENCY



This high dc precision and low noise, coupled with the extremely high input impedance of the CMOS input stage, make the TLC2654 and TLC2654A ideal choices for a broad range of applications such as low-level, low-frequency thermocouple amplifiers and strain gauges and wide-bandwidth and subsonic circuits. (For applications requiring even greater dc precision, use the TLC2652 or TLC2652A devices, which have a chopping frequency of 450 Hz.)

The TLC2654 and TLC2654A common-mode input voltage range includes the negative rail, thereby providing superior performance in either single-supply or split-supply applications, even at power supply voltage levels as low as ±2.3 V.

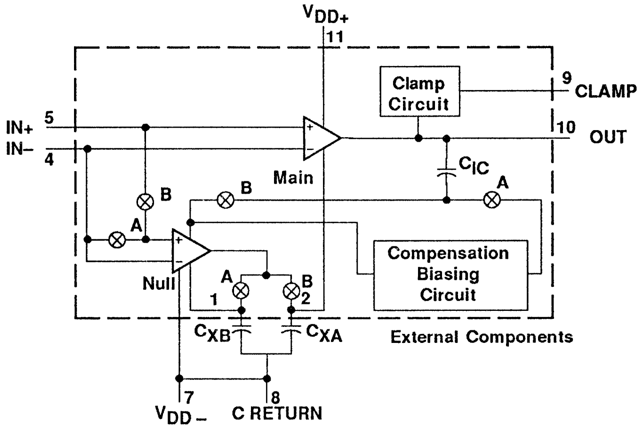
Two external capacitors are required to operate the device; however, the on-chip chopper control circuitry is transparent to the user. On devices in the 14-pin and 20-pin packages, the control circuitry is accessible, allowing the user the option of controlling the clock frequency with an external frequency source. In addition, the clock threshold of the TLC2654 and TLC2654A requires no level shifting when used in the single-supply configuration with a normal CMOS or TTL clock input.

Innovative circuit techniques used on the TLC2654 and TLC2654A allow exceptionally fast overload recovery time. An output clamp pin is available to reduce the recovery time further.

The device inputs and output are designed to withstand −100-mA surge currents without sustaining latch-up. In addition, the TLC2654 and TLC2654A incorporate internal ESD-protection circuits that prevent functional failures at voltages up to 2000 V as tested under MIL-STD-883C, Method 3015; however, care should be exercised in handling these devices, as exposure to ESD may result in degradation of the device parametric performance.

The C-suffix devices are characterized for operation from 0°C to 70°C. The I-suffix devices are characterized for operation from −40°C to 85°C. The M-suffix devices are characterized for operation over the full military temperature range of −55°C to 125°C.

functional block diagram

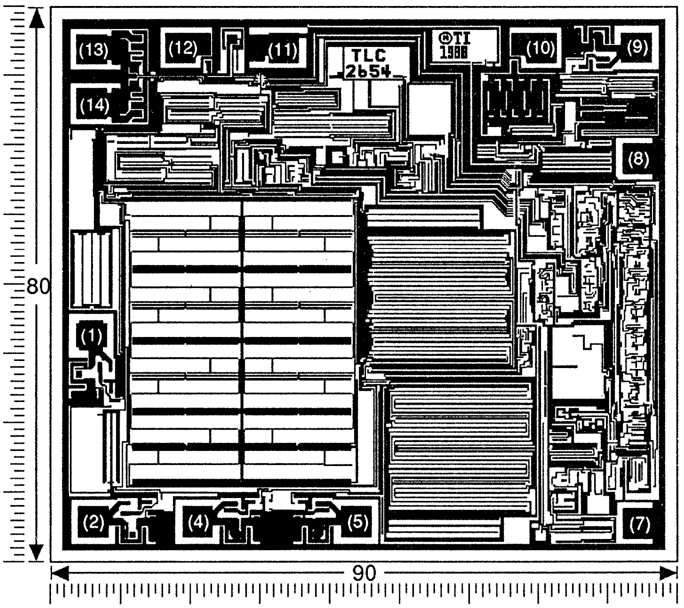


Pin numbers shown are for D014, J, and N packages.

TLC2654Y chip information

These chips, properly assembled, display characteristics similar to the TLC2654. Thermal compression or ultrasonic bonding may be used on the doped aluminum bonding pads. Chips may be mounted with conductive epoxy or a gold-silicon preform.

BONDING PAD ASSIGNMENTS



**CHIP THICKNESS:
15 TYPICAL**

**BONDING PADS:
4 X 4 MINIMUM**

T_J max = 150°C

**TOLERANCES
ARE ± 10%**

**ALL DIMENSIONS
ARE IN MILS**

**PIN (7) INTERNALLY
CONNECTED TO
BACKSIDE OF CHIP**

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{DD+} (see Note 1) . . . . 8 V
Supply voltage, V_{DD-} (see Note 1) . . . . –8 V
Differential input voltage (see Note 2) . . . . ±16 V
Input voltage, V_I (any input, see Note 1) . . . . ±8 V
Voltage on CLK IN and INT/$\overline{\text{EXT}}$ pins . . . . V_{DD-} to V_{DD-} + 5.2 V
Input current, I_I (each input) . . . . ±5 mA
Output current, I_O . . . . ±50 mA
Duration of short-circuit current at (or below) 25°C (see Note 3) . . . . unlimited
Current into CLK IN and INT/$\overline{\text{EXT}}$ pins . . . . ±5 mA
Continuous total dissipation . . . . See Dissipation Rating Table
Operating free-air temperature range, T_A: C-suffix . . . . 0°C to 70°C
I-suffix . . . . – 40°C to 85°C
M-suffix . . . . – 55°C to 125°C
Storage temperature range . . . . – 65°C to 150°C
Case temperature for 60 seconds: FK package . . . . 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D, N, or P package . . . . 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: J or JG package . . . . 300°C

NOTES: 1. All voltage values, except differential voltages, are with respect to the midpoint between V_{DD+} and V_{DD-}.
2. Differential voltages are at the noninverting input with respect to the inverting input.
3. The output may be shorted to either supply. Temperature and/or supply voltages must be limited that the maximum dissipation rating is not exceeded.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING	$T_A = 125°C$ POWER RATING
D008	725 mW	5.8 mW/°C	464 mW	377 mW	145 mW
D014	950 mW	7.6 mW/°C	608 mW	494 mW	190 mW
FK	1375 mW	11 mW/°C	880 mW	715 mW	275 mW
J	1375 mW	11 mW/°C	880 mW	715 mW	275 mW
JG	1050 mW	8.4 mW/°C	672 mW	546 mW	210 mW
N	1150 mW	9.2 mW/°C	736 mW	598 mW	230 mW
P	1000 mW	8 mW/°C	640 mW	520 mW	200 mW

recommended operating conditions

	C-SUFFIX		I-SUFFIX		M-SUFFIX		UNIT
	MIN	MAX	MIN	MAX	MIN	MAX	
Supply voltage, $V_{DD\pm}$	±2.3	±8	± 2.3	±8	±2.3	±8	V
Common-mode input voltage, V_{IC}	V_{DD-}	$V_{DD+} - 2.3$	V_{DD-}	$V_{DD+} - 2.3$	V_{DD-}	$V_{DD+} - 2.3$	V
Clock input voltage	V_{DD-}	$V_{DD-} + 5$	V_{DD-}	$V_{DD-} + 5$	V_{DD-}	$V_{DD-} + 5$	V
Operating free-air temperature, T_A	0	70	– 40	85	– 55	125	°C

electrical characteristics at specified free-air temperature, $V_{DD\pm}$ = ±5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A†	TLC2654C			TLC2654AC			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage (see Note 4)	V_{IC} = 0, R_S = 50 Ω	25°C		5	20		4	10	μV
			Full range			34			24	
α_{VIO}	Temperature coefficient of input offset voltage		Full range		0.004	0.3		0.004	0.3	μV/°C
	Input offset voltage long-term drift (see Note 5)		25°C		0.003	0.06		0.003	0.02	μV/mo
I_{IO}	Input offset current		25°C		30			30		pA
			Full range			150			150	
I_{IB}	Input bias current		25°C		50			50		pA
			Full range			150			150	
V_{ICR}	Common-mode input voltage range	R_S = 50 Ω	Full range	−5 to 2.7			−5 to 2.7			V
V_{OM+}	Maximum positive peak output voltage swing	R_L = 10 kΩ, See Note 6	25°C	4.7	4.8		4.7	4.8		V
			Full range	4.7			4.7			
V_{OM-}	Maximum negative peak output voltage swing	R_L = 10 kΩ, See Note 6	25°C	−4.7	−4.9		−4.7	−4.9		V
			Full range	−4.7			−4.7			
A_{VD}	Large-signal differential voltage amplification	V_O = ±4 V, R_L = 10 kΩ	25°C	120	155		135	155		dB
			Full range	120			130			
f_{ch}	Internal chopping frequency		25°C		10			10		kHz
	Clamp on-state current	R_L = 100 kΩ	25°C	25			25			μA
			Full range	25			25			
	Clamp off-state current	V_O = −4 V to 4 V	25°C			100			100	pA
			Full range			100			100	
CMRR	Common-mode rejection ratio	V_O = 0, V_{IC} = V_{ICR} min, R_S = 50 Ω	25°C	105	125		110	125		dB
			Full range	105			110			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD\pm} / \Delta V_{IO}$)	$V_{DD\pm}$ = ±2.3 V to ±8 V, V_O = 0, R_S = 50 Ω	25°C	110	125		120	125		dB
			Full range	110			120			
I_{DD}	Supply current	V_O = 0, No load	25°C		1.5	2.4		1.5	2.4	mA
			Full range			2.5			2.5	

†Full range is 0°C to 70°C.

NOTES: 4. This parameter is not production tested full range. Thermocouple effects preclude measurement of the acutal V_{IO} of these devices in high-speed automated testing. V_{IO} is measured to a limit determined by the test equipment capbility at the temperature extremes. The test ensures that the stabilization circuitry is performing properly.

5. Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at T_A = 150°C extrapolated to T_A = 25°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

6. Output clamp is not connected.

operating characteristics at specified free-air temperature, V_{DD} ± = ±5 V

PARAMETER		TEST CONDITIONS	T_A†	TLC2654C			TLC2654AC			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
SR +	Positive slew rate at unity gain	V_O = ±2.3 V, R_L = 10 kΩ, C_L = 100 pF	25°C	1.5	2		1.5	2		V/μs
			Full range	1.3			1.3			
SR −	Negative slew rate at unity gain		25°C	2.3	3.7		2.3	3.7		V/μs
			Full range	1.7			1.7			
V_n	Equivalent input noise voltage (see Note 7)	f = 10 Hz	25°C		47			47	75	nV/√Hz
		f = 1 kHz	25°C		13			13	20	
	Peak-to-peak equivalent input noise voltage	f = 0 to 1 Hz	25°C		0.5			0.5		μV
		f = 0 to 10 Hz	25°C		1.5			1.5		
$V_{N(PP)}$	Equivalent input noise current	f = 1 kHz	25°C		0.004			0.004		pA/√Hz
I_n	Gain-bandwidth product	f = 10 kHz, R_L = 10 kΩ, C_L = 100 pF	25°C		1.9			1.9		MHz
ϕm	Phase margin at unity gain	R_L = 10 kΩ, C_L = 100 pF	25°C		48°			48°		

† Full range is 0°C to 70°C.

NOTE 7: This parameter is tested on a sample basis for the TLC2654A. For other test requirements, please contact the factory. This statement has no bearing on testing or nontesting of other parameters.

electrical characteristics at specified free-air temperature, $V_{DD\pm} = \pm 5$ V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A†	TLC2654I			TLC2654AI			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	$V_{IC} = 0$, $R_S = 50\ \Omega$	25°C		5	20		4	10	µV
			Full range			40			30	
α_{VIO}	Temperature coefficient of input offset voltage		Full range		0.004	0.3		0.004	0.3	µV/°C
	Input offset voltage long-term drift (see Note 5)		25°C		0.003	0.06		0.003	0.02	µV/mo
I_{IO}	Input offset current		25°C		30			30		pA
			Full range			200			200	
I_{IB}	Input bias current		25°C		50			50		pA
			Full range			200			200	
V_{ICR}	Common-mode input voltage range	$R_S = 50\ \Omega$	Full range	−5 to 2.7			−5 to 2.7			V
V_{OM+}	Maximum positive peak output voltage swing	$R_L = 10\ k\Omega$, See Note 6	25°C	4.7	4.8		4.7	4.8		V
			Full range	4.7			4.7			
V_{OM-}	Maximum negative peak output voltage swing	$R_L = 10\ k\Omega$, See Note 6	25°C	−4.7	−4.9		−4.7	−4.9		V
			Full range	−4.7			−4.7			
A_{VD}	Large-signal differential voltage amplification	$V_O = \pm 4$ V, $R_L = 10\ k\Omega$	25°C	120	155		135	155		dB
			Full range	120			125			
f_{ch}	Internal chopping frequency		25°C		10			10		kHz
	Clamp on-state current	$R_L = 100\ k\Omega$	25°C	25			25			µA
			Full range	25			25			
	Clamp off-state current	$V_O = -4$ V to 4 V	25°C			100			100	pA
			Full range			100			100	
CMRR	Common-mode rejection ratio	$V_O = 0$, $V_{IC} = V_{ICR}$ min, $R_S = 50\ \Omega$	25°C	105	125		110	125		dB
			Full range	105			110			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD\pm} / \Delta V_{IO}$)	$V_{DD\pm} = \pm 2.3$ V to ± 8 V, $V_O = 0$, $R_S = 50\ \Omega$	25°C	110	125		120	125		dB
			Full range	110			120			
I_{DD}	Supply current	$V_O = 0$, No load	25°C		1.5	2.4		1.5	2.4	mA
			Full range			2.5			2.5	

†Full range is − 40°C to 85°C.

NOTES: 5. Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at $T_A = 150°C$ extrapolated to $T_A = 25°C$ using the Arrhenius equation and assuming an activation energy of 0.96 eV.

6. Output clamp is not connected.

operating characteristics at specified free-air temperature, $V_{DD\pm} = \pm 5$ V

	PARAMETER	TEST CONDITIONS	T_A†	TLC2654I			TLC2654AI			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
SR +	Positive slew rate at unity gain	$V_O = \pm 2.3$ V, $R_L = 10$ kΩ, $C_L = 100$ pF	25°C	1.5	2		1.5	2		V/μs
			Full range	1.2			1.2			
SR –	Negative slew rate at unity gain		25°C	2.3	3.7		2.3	3.7		V/μs
			Full range	1.5			1.5			
V_n	Equivalent input noise voltage (see Note 7)	f = 10 Hz	25°C		47			47	75	nV/√Hz
		f = 1 kHz	25°C		13			13	20	
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0 to 1 Hz	25°C		0.5			0.5		μV
		f = 0 to 10 Hz	25°C		1.5			1.5		
I_n	Equivalent input noise current	f = 1 kHz	25°C		0.004			0.004		pA/√Hz
	Gain-bandwidth product	f = 10 kHz, $R_L = 10$ kΩ, $C_L = 100$ pF	25°C		1.9			1.9		MHz
ϕ_m	Phase margin at unity gain	$R_L = 10$ kΩ, $C_L = 100$ pF	25°C		48°			48°		

†Full range is – 40°C to 85°C.

NOTE 7: This parameter is tested on a sample basis for the TLC2654A. For other test requirements, please contact the factory. This statement has no bearing on testing or nontesting of other parameters.

electrical characteristics at specified free-air temperature, $V_{DD\pm} = \pm 5$ V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A†	TLC2654M			TLC2654AM			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage (see Note 4)	$V_{IC} = 0$, $R_S = 50\ \Omega$	25°C		5	20		4	10	μV
			Full range			50			40	
α_{VIO}	Temperature coefficient of input offset voltage		Full range		0.004	0.3*		0.004	0.3*	μV/°C
	Input offset voltage long-term drift (see Note 5)		25°C		0.003	0.06*		0.003	0.02*	μV/mo
I_{IO}	Input offset current		25°C		30			30		pA
			Full range			500			500	
I_{IB}	Input bias current		25°C		50			50		pA
			Full range			500			500	
V_{ICR}	Common-mode input voltage range	$R_S = 50\ \Omega$	Full range	−5 to 2.7			−5 to 2.7			V
V_{OM+}	Maximum positive peak output voltage swing	$R_L = 10\ k\Omega$, See Note 6	25°C	4.7	4.8		4.7	4.8		V
			Full range	4.7			4.7			
V_{OM-}	Maximum negative peak output voltage swing	$R_L = 10\ k\Omega$, See Note 6	25°C	−4.7	−4.9		−4.7	−4.9		V
			Full range	−4.7			−4.7			
A_{VD}	Large-signal differential voltage amplification	$V_O = \pm 4$ V, $R_L = 10\ k\Omega$	25°C	120	155		135	155		dB
			Full range	120			120			
f_{ch}	Internal chopping frequency		25°C		10			10		kHz
	Clamp on-state current	$R_L = 100\ k\Omega$	25°C	25			25			μA
			Full range	25			25			
	Clamp off-state current	$V_O = -4$ V to 4 V	25°C			100			100	pA
			Full range			500			500	
CMRR	Common-mode rejection ratio	$V_O = 0$, $V_{IC} = V_{ICR}$ min, $R_S = 50\ \Omega$	25°C	105	125		110	125		dB
			Full range	105			110			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD\pm} / \Delta V_{IO}$)	$V_{DD\pm} = \pm 2.3$ V to ± 8 V, $V_O = 0$, $R_S = 50\ \Omega$	25°C	110	125		120	125		dB
			Full range	105			115			
I_{DD}	Supply current	$V_O = 0$, No load	25°C		1.5	2.4		1.5	2.4	mA
			Full range			2.5			2.5	

*On products compliant to MIL-STD-883, Class B, this parameter is not production tested.

†Full range is − 55°C to 125°C.

NOTES: 4. This parameter is not production tested full range. Thermocouple effects preclude measurement of the actual V_{IO} of these devices in high-speed automated testing. V_{IO} is measured to a limit determined by the test equipment capability at the temperature extremes. The test ensures that the stabilization circuitry is performing properly.

5. Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at $T_A = 150°C$ extrapolated to $T_A = 25°C$ using the Arrhenius equation and assuming an activation energy of 0.96 eV.

6. Output clamp is not connected.

operating characteristics at specified free-air temperature, $V_{DD\pm} = \pm 5$ V

PARAMETER		TEST CONDITIONS	T_A†	MIN	TYP	MAX	UNIT
SR +	Positive slew rate at unity gain	$V_O = \pm 2.3$ V, $R_L = 10$ kΩ, $C_L = 100$ pF	25°C	1.5	2		V/µs
			Full range	1.1			
SR −	Negative slew rate at unity gain		25°C	2.3	3.7		V/µs
			Full range	1.3			
V_n	Equivalent input noise voltage	f = 10 Hz	25°C		47		nV/√Hz
		f = 1 kHz	25°C		13		
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0 to 1 Hz	25°C		0.5		µV
		f = 0 to 10 Hz	25°C		1.5		
I_n	Equivalent input noise current	f = 1 kHz	25°C		0.004		pA/√Hz
	Gain-bandwidth product	f = 10 kHz, $R_L = 10$ kΩ, $C_L = 100$ pF	25°C		1.9		MHz
ϕ_m	Phase margin at unity gain	$R_L = 10$ kΩ, $C_L = 100$ pF	25°C		48°		

†Full range is – 55°C to 125°C.

electrical characteristics at specified free-air temperature, $V_{DD\pm}$ = ±5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	$V_{IC} = 0$,	$R_S = 50\ \Omega$		5	20	µV
	Input offset voltage long-term drift (see Note 4)				0.003	0.06	µV/mo
I_{IO}	Input offset current				30		pA
I_{IB}	Input bias current				50		pA
V_{ICR}	Common-mode input voltage range	$R_S = 50$		−5 to 2.7			V
V_{OM+}	Maximum positive peak output voltage swing	$R_L = 10\ k\Omega$,	See Note 5	4.7	4.8		V
V_{OM-}	Maximum negative peak output voltage swing	$R_L = 10\ k\Omega$,	See Note 5	−4.7	−4.9		V
A_{VD}	Large-signal differential voltage amplification	$V_O = \pm 4$ V,	$R_L = 10\ k\Omega$	120	155		dB
f_{ch}	Internal chopping frequency				10		Hz
	Clamp on-state current	$R_L = 100\ k\Omega$		25			µA
	Clamp off-state current	$V_O = -4$ V to 4 V				100	pA
CMRR	Common-mode rejection ratio	$V_O = 0$, $V_{IC} = V_{ICR}min$,	$R_S = 50\ \Omega$	105	125		dB
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD\pm}/\Delta V_{IO}$)	$V_{DD\pm} = \pm 2.3$ V to ±8 V, $V_O = 0$,	$R_S = 50\ \Omega$	110	125		dB
I_{DD}	Supply current	$V_O = 0$,	No load		1.5	2.4	mA

NOTES: 4. Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at T_A = 150°C extrapolated to T_A = 25°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.
5. Output clamp is not connected.

operating characteristics at $V_{DD\pm}$ = ±5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SR +	Positive slew rate at unity gain	$V_O = \pm 2.3$ V, $R_L = 10\ k\Omega$, $C_L = 100$ pF	1.5	2		V/µs
SR −	Negative slew rate at unity gain		2.3	3.7		V/µs
V_n	Equivalent input noise voltage	f = 10 Hz		47		nV/√Hz
		f = 1 kHz		13		
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0 to 1 Hz		0.5		µV
		f = 0 to 10 Hz		1.5		
I_n	Equivalent input noise current	f = 1 kHz		0.004		pA/√Hz
	Gain-bandwidth product	f = 10 kHz, $R_L = 10\ k\Omega$, $C_L = 100$ pF		1.9		MHz
ϕ_m	Phase margin at unity gain	$R_L = 10\ k\Omega$, $C_L = 100$ pF		48°		

TYPICAL CHARACTERISTICS

table of graphs

			FIGURE
V_{IO}	Input offset voltage	Distribution	1
	Normalized input offset voltage	vs Chopping frequency	2
I_{IO}	Input offset current	vs Chopping frequency	3
		vs Temperature	4
I_{IB}	Input bias current	vs Common-mode voltage	5
		vs Chopping frequency	6
		vs Temperature	7
	Clamp current	vs Output voltage	8
V_{OM}	Maximum peak output voltage swing	vs Output current	9
		vs Temperature	10
V_{OPP}	Maximum peak-to-peak output voltage swing	vs Frequency	11
CMRR	Common-mode rejection ratio	vs Frequency	12
A_{VD}	Differential voltage amplification	vs Frequency	13
		vs Temperature	14
f_{ch}	Chopping frequency	vs Supply voltage	15
		vs Temperature	16
I_{DD}	Supply current	vs Supply voltage	17
		vs Temperature	18
I_{OS}	Short-circuit output current	vs Supply voltage	19
		vs Temperature	20
SR	Slew rate	vs Supply voltage	21
		vs Temperature	22
	Pulse response	Small-signal	23
		Large-signal	24
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	vs Chopping frequency	25, 26
V_n	Equivalent input noise voltage	vs Frequency	27
k_{SVR}	Supply-voltage rejection ratio	vs Frequency	28
	Gain-bandwidth product	vs Supply voltage	29
		vs Temperature	30
	Phase margin	vs Supply voltage	31
		vs Load capacitance	32
ϕ_m	Phase shift	vs Frequency	13

TYPICAL CHARACTERISTICS†

DISTRIBUTION OF TLC2654
INPUT OFFSET VOLTAGE

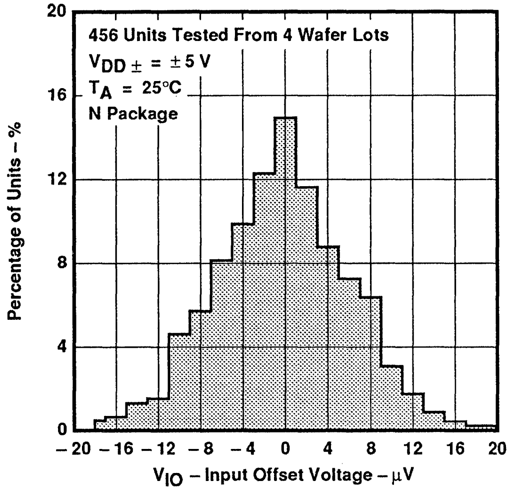


Figure 1

NORMALIZED INPUT OFFSET VOLTAGE
vs
CHOPPING FREQUENCY

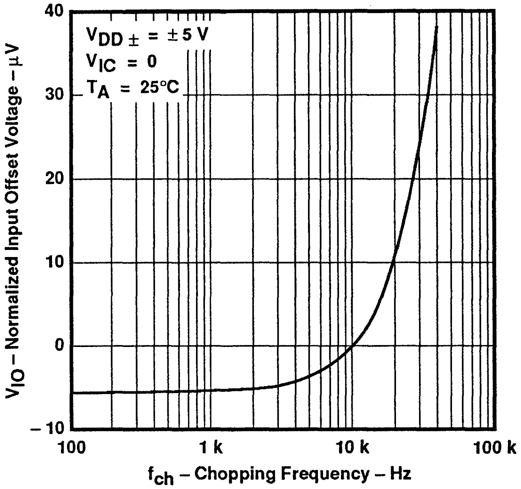


Figure 2

INPUT OFFSET CURRENT
vs
CHOPPING FREQUENCY

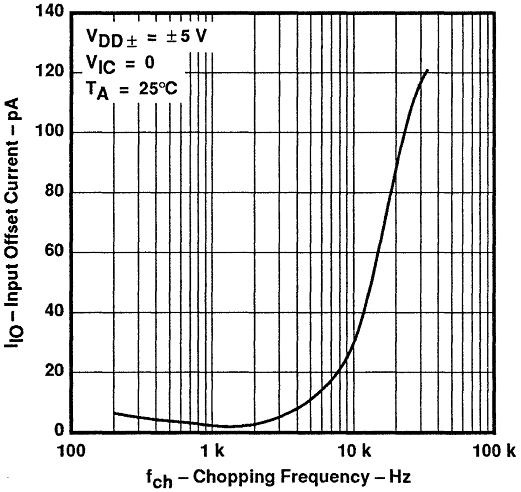


Figure 3

INPUT OFFSET CURRENT
vs
FREE-AIR TEMPERATURE

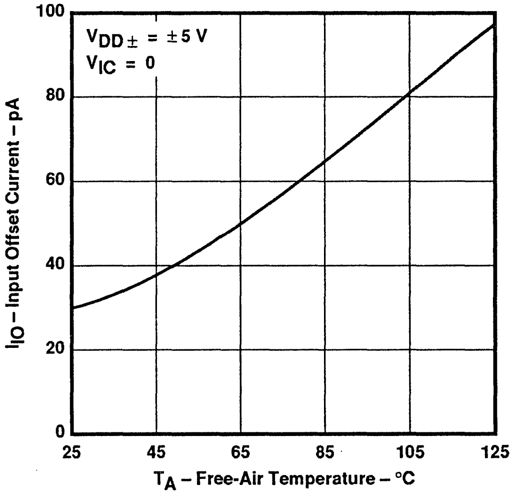


Figure 4

---

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

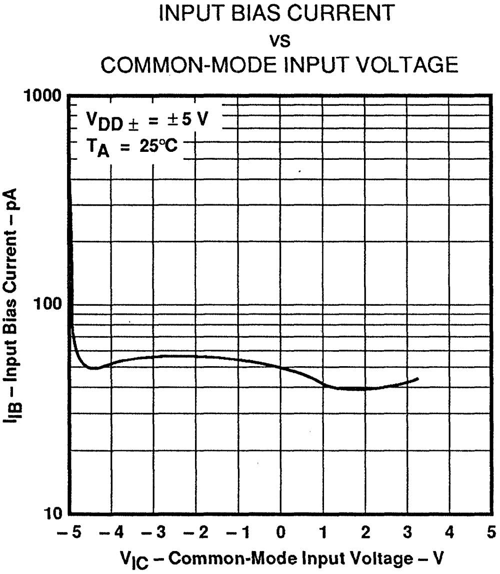


Figure 5

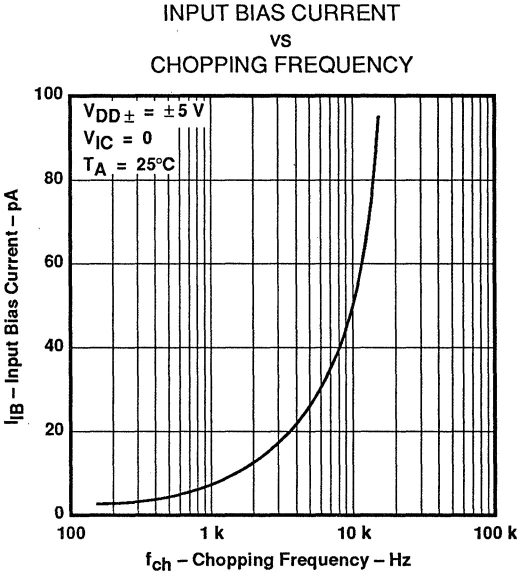


Figure 6

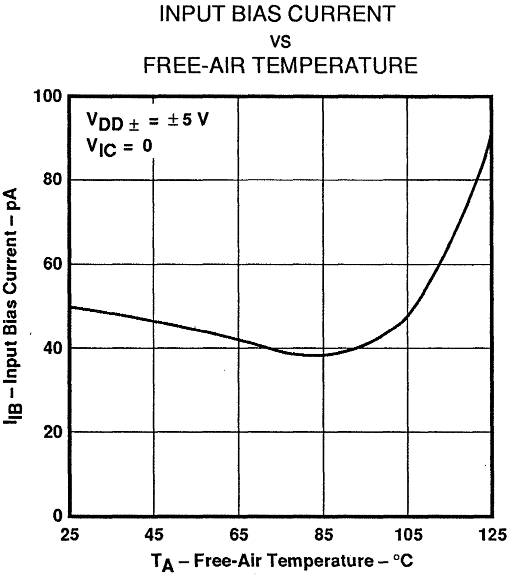


Figure 7

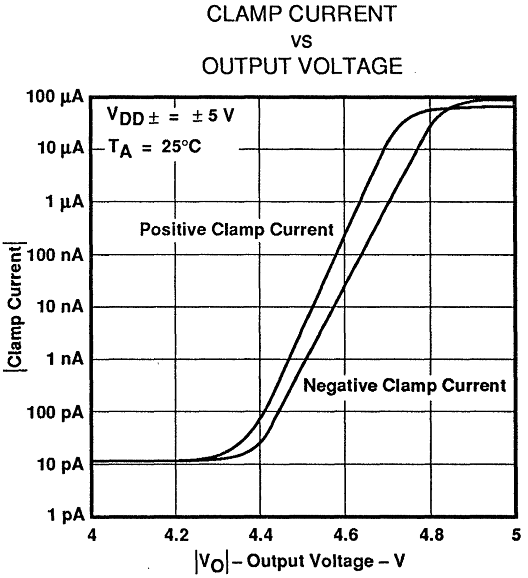


Figure 8

---

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

MAXIMUM PEAK OUTPUT VOLTAGE
vs
OUTPUT CURRENT

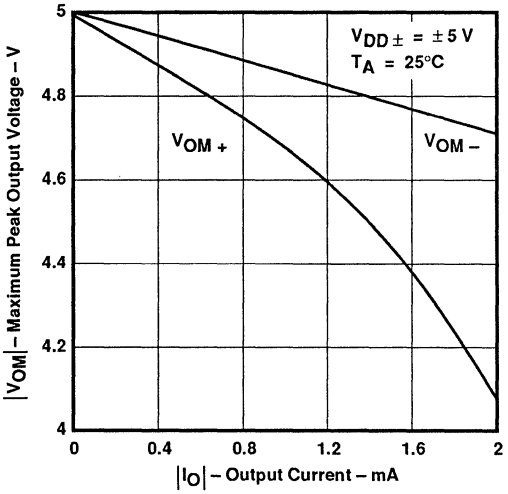


Figure 9

MAXIMUM PEAK OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

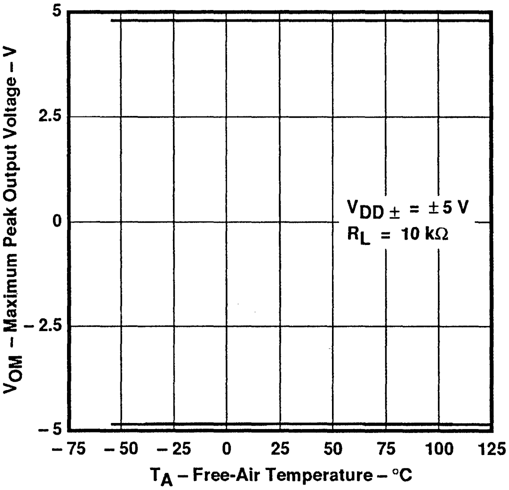


Figure 10

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE
vs
FREQUENCY

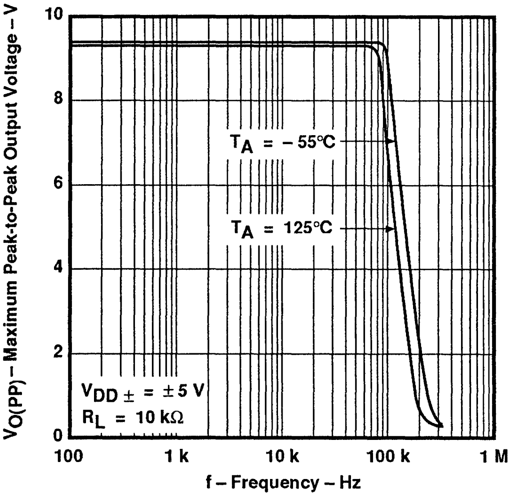


Figure 11

COMMON-MODE REJECTION RATIO
vs
FREQUENCY

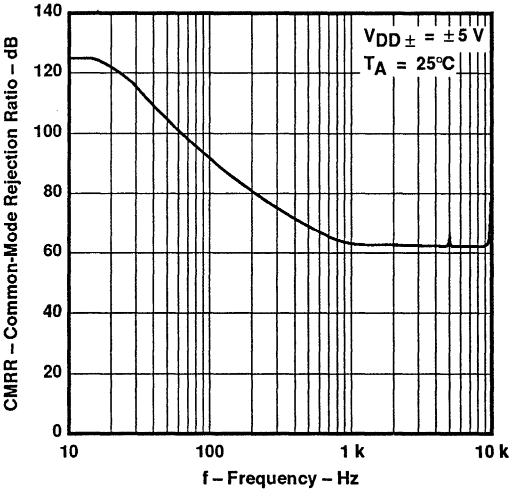


Figure 12

---

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION AND PHASE SHIFT
vs
FREQUENCY

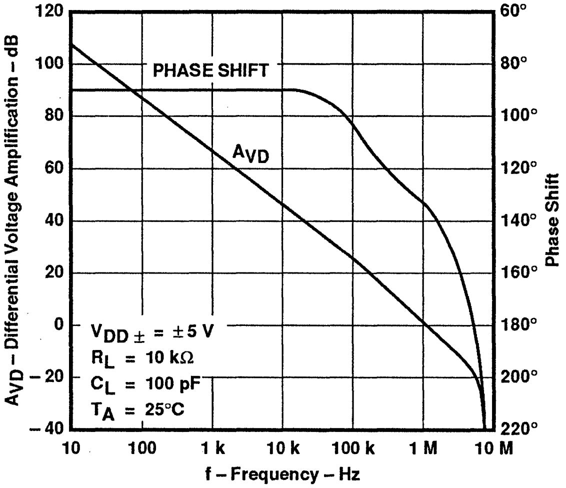


Figure 13

LARGE-SIGNAL VOLTAGE AMPLIFICATION
vs
FREE-AIR TEMPERATURE

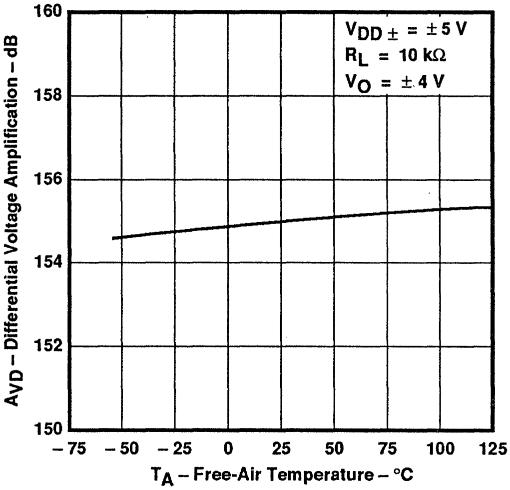


Figure 14

CHOPPING FREQUENCY
vs
SUPPLY VOLTAGE

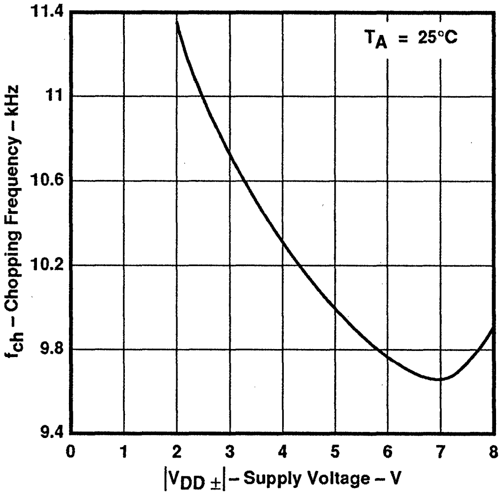


Figure 15

CHOPPING FREQUENCY
vs
FREE-AIR TEMPERATURE

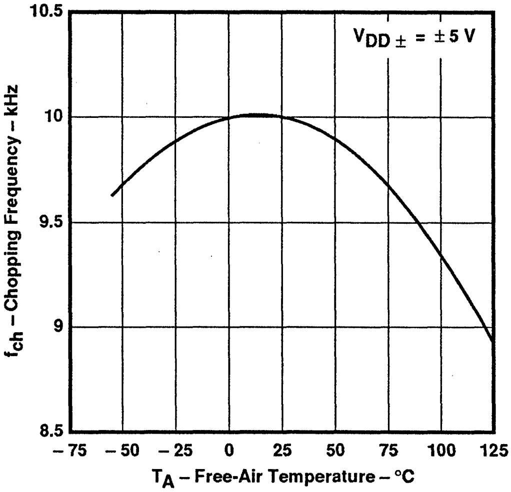


Figure 16

---

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

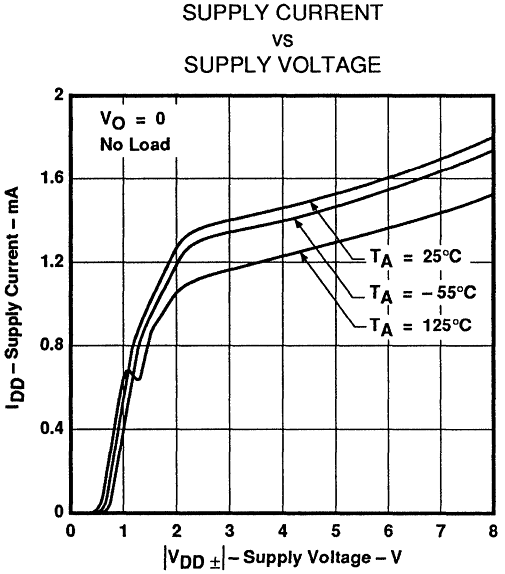


Figure 17

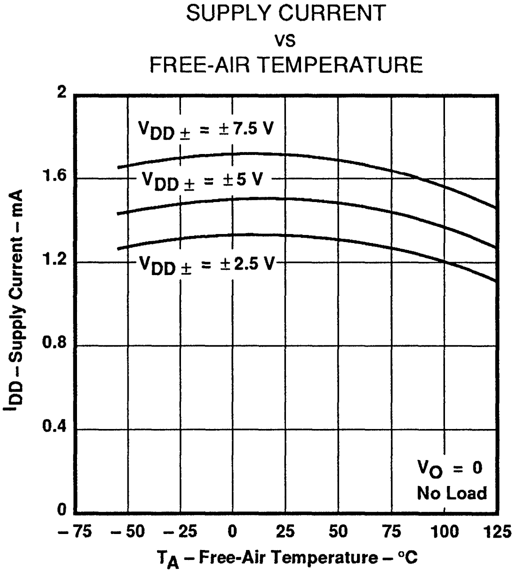


Figure 18

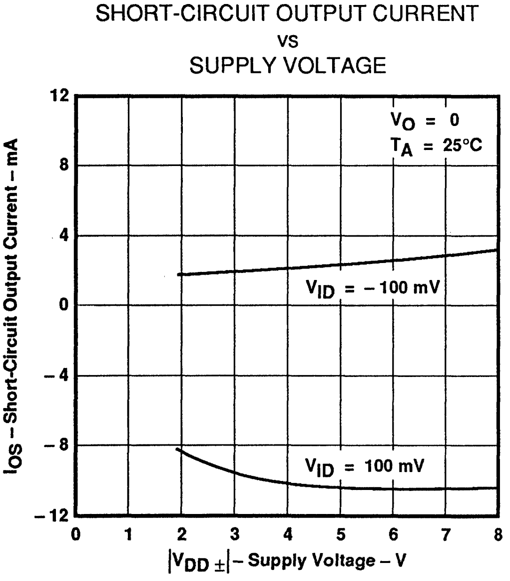


Figure 19

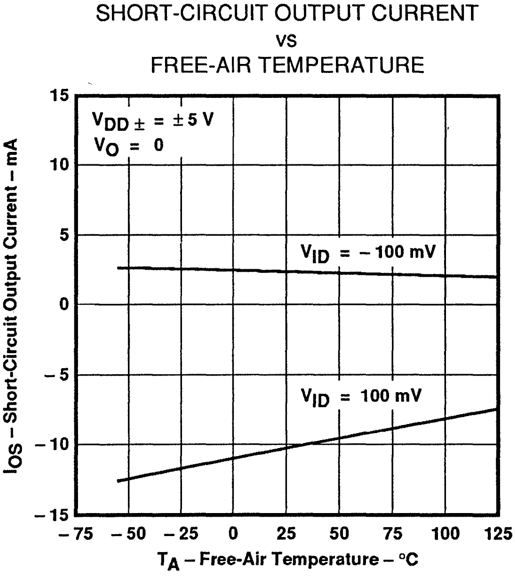


Figure 20

---

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

SLEW RATE
vs
SUPPLY VOLTAGE

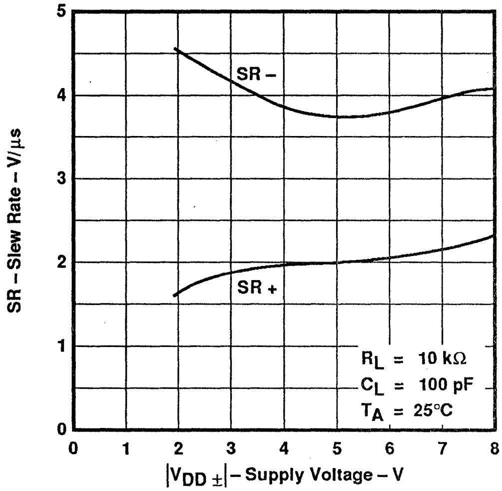


Figure 21

SLEW RATE
vs
FREE-AIR TEMPERATURE

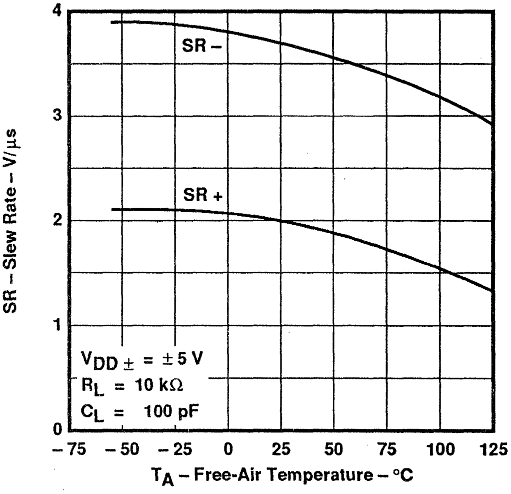


Figure 22

VOLTAGE-FOLLOWER
SMALL-SIGNAL
PULSE RESPONSE

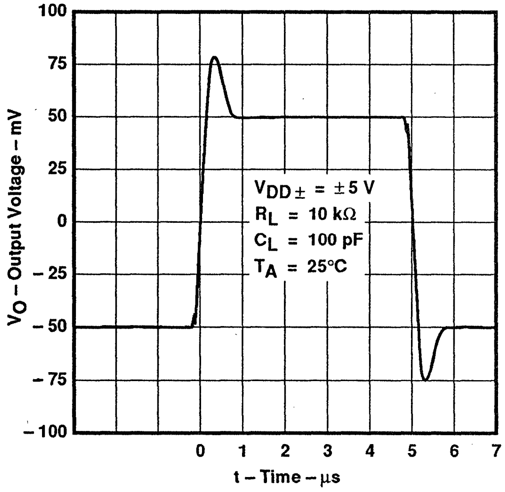


Figure 23

VOLTAGE-FOLLOWER
LARGE-SIGNAL
PULSE RESPONSE

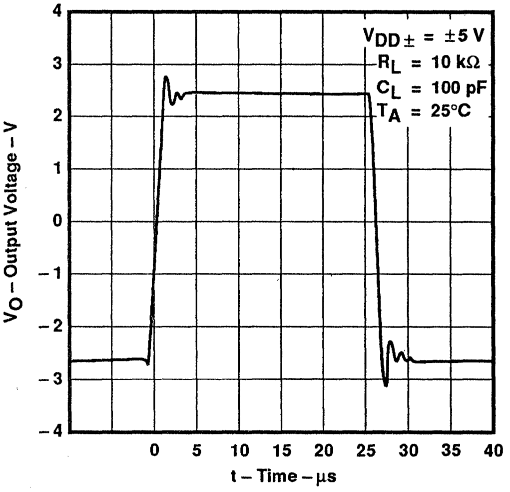


Figure 24

---

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS

PEAK-TO-PEAK INPUT NOISE VOLTAGE
vs
CHOPPING FREQUENCY

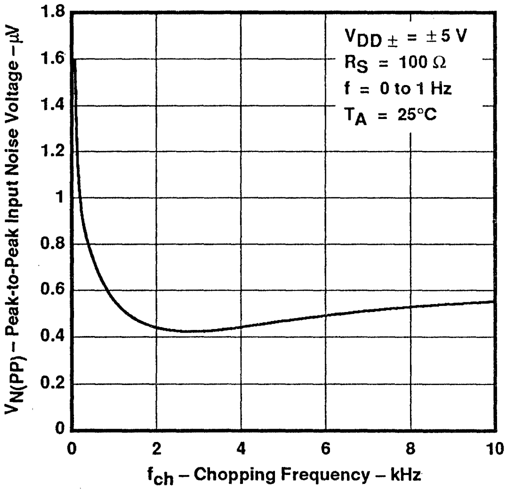


Figure 25

PEAK-TO-PEAK INPUT NOISE VOLTAGE
vs
CHOPPING FREQUENCY

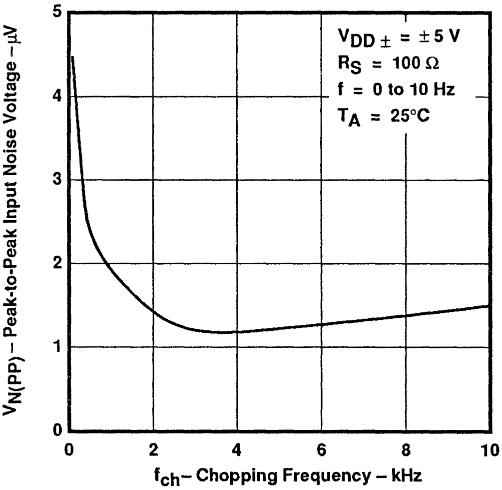


Figure 26

EQUIVALENT INPUT NOISE VOLTAGE
vs
FREQUENCY

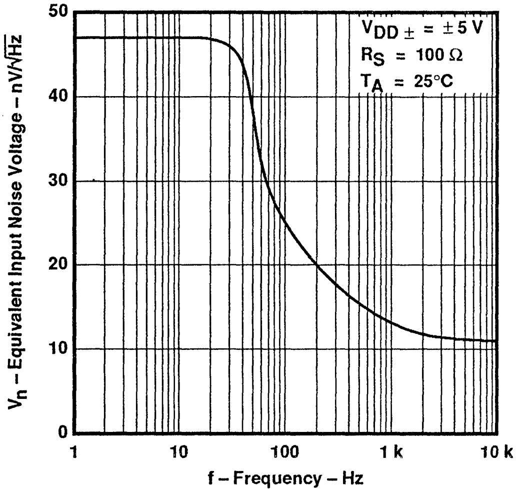


Figure 27

SUPPLY-VOLTAGE REJECTION RATIO
vs
FREQUENCY

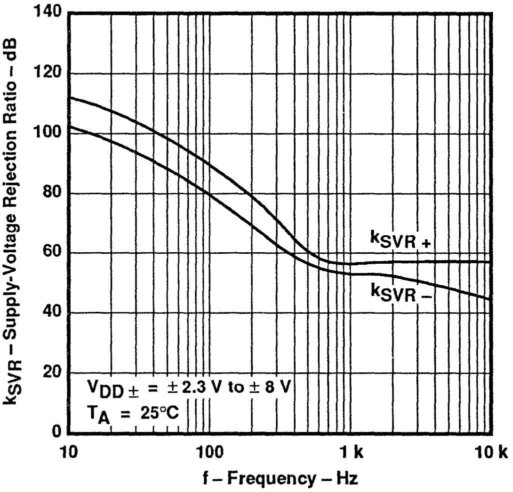


Figure 28

TYPICAL CHARACTERISTICS†

GAIN-BANDWIDTH PRODUCT
vs
SUPPLY VOLTAGE

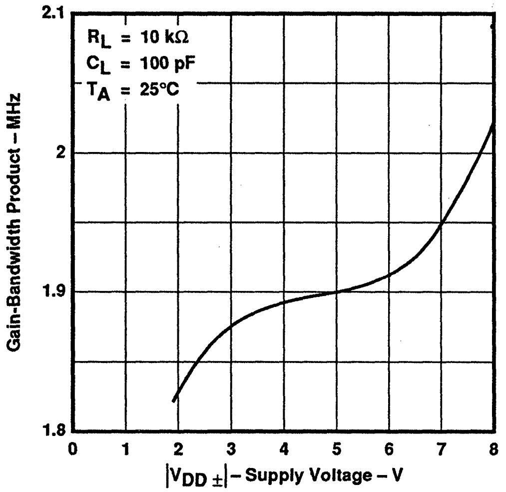


Figure 29

GAIN-BANDWIDTH PRODUCT
vs
FREE-AIR TEMPERATURE

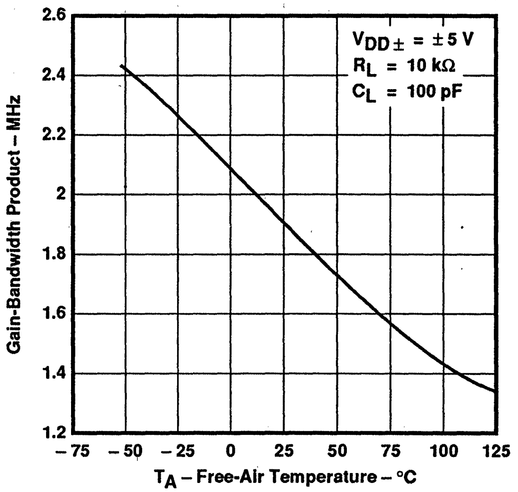


Figure 30

PHASE MARGIN
vs
SUPPLY VOLTAGE

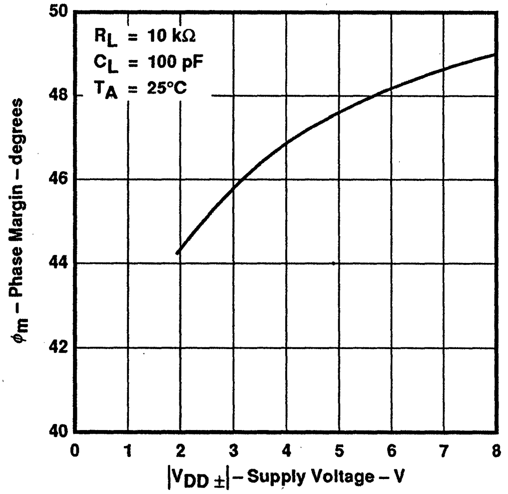


Figure 31

PHASE MARGIN
vs
LOAD CAPACITANCE

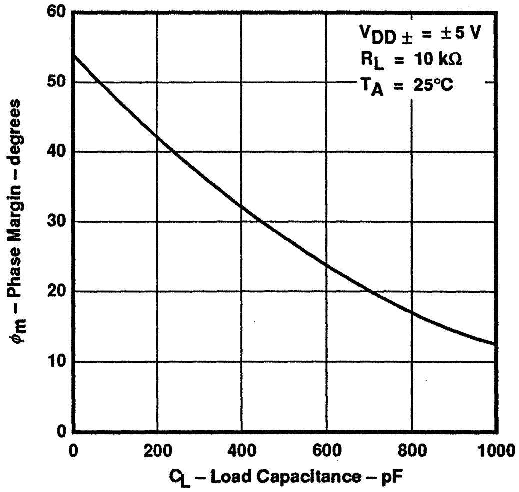


Figure 32

---

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

APPLICATION INFORMATION

capacitor selection and placement

Leakage and dielectric absorption are the two important factors to consider when selecting external capacitors C_{XA} and C_{XB}. Both factors can cause system degradation, negating the performance advantages realized by using the TLC2654.

Degradation from capacitor leakage becomes more apparent with increasing temperatures. Low-leakage capacitors and standoffs are recommended for operation at T_A = 125°C. In addition, guard bands around the capacitor connections on both sides of the printed circuit board are recommended to alleviate problems caused by surface leakage on circuit boards.

Capacitors with high dielectric absorption tend to take several seconds to settle upon application of power, which directly affects input offset voltage. In applications needing fast settling of input offset voltage, it is recommended that high-quality film capacitors, such as mylar, polystyrene, or polypropylene, be used. In other applications, however, a ceramic or other low-grade capacitor may suffice.

Unlike many choppers available today, the TLC2654 is designed to function with values of C_{XA} and C_{XB} in the range of 0.1 µF to 1 µF without degradation to input offset voltage or input noise voltage. These capacitors should be located as close as possible to the C_{XA} and C_{XB} pins and returned to either the V_{DD-} pin or the C RETURN pin. Note that on many choppers, connecting these capacitors to the V_{DD-} pin causes degradation in noise performance, a problem that is eliminated on the TLC2654.

internal/external clock

The TLC2654 has an internal clock that sets the chopping frequency to a nominal value of 10 kHz. On 8-pin packages, the chopping frequency can only be controlled by the internal clock; however, on all 14-pin packages and the 20-pin FK package, the device chopping frequency may be set by the internal clock or controlled externally by use of the INT/$\overline{\text{EXT}}$ and CLK IN pins. To use the internal 10-kHz clock, no connection is necessary. If external clocking is desired, connect the INT/$\overline{\text{EXT}}$ pin to V_{DD-} and the external clock to CLK IN. The external clock trip point is 2.5 V above the negative rail; however, the CLK IN pin may be driven from the negative rail to 5 V above the negative rail. This allows the TLC2654 to be driven directly by 5-V TTL and CMOS logic when operating in the single-supply configuration. If this 5-V level is exceeded, damage could occur to the device unless the current into the CLK IN pin is limited to ±5 mA. A divide-by-two frequency divider interfaces with the CLK IN pin and sets the chopping frequency. The chopping frequency appears on the CLK OUT pin.

overload recovery/output clamp

When large differential input voltage conditions are applied to the TLC2654, the nulling loop attempts to prevent the output from saturating by driving C_{XA} and C_{XB} to internally-clamped voltage levels. Once the overdrive condition is removed, a period of time is required to allow the built-up charge to dissipate. This time period is defined as overload recovery time (see Figure 33). Typical overload recovery time for the TLC2654 is significantly faster than competitive products; however, if required, this time can be reduced further by use of internal clamp circuitry accessible through the CLAMP pin.

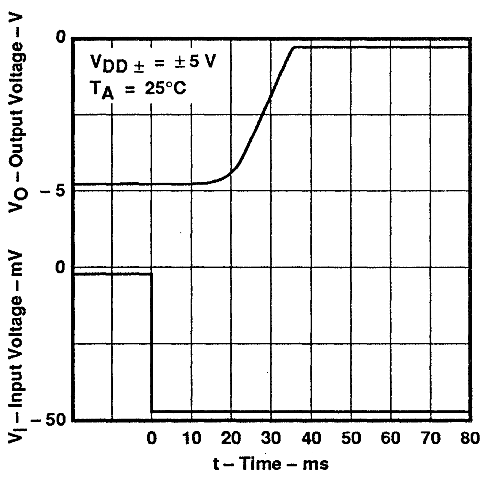


Figure 33. Overload Recovery

APPLICATION INFORMATION

The clamp is simply a switch that is automatically activated when the output is approximately 1 V from either supply rail. When connected to the inverting input (in parallel with the closed-loop feedback resistor), the closed-loop gain is reduced, and the TLC2654 output is prevented from going into saturation. Since the output must source or sink current through the switch (see Figure 8), the maximum output voltage swing is slightly reduced.

thermoelectric effects

To take advantage of the extremely low offset voltage temperature coefficient of the TLC2654, care must be taken to compensate for the thermoelectric effects present when two dissimilar metals are brought into contact with each other (such as device leads being soldered to a printed circuit board). It is not uncommon for dissimilar metal junctions to produce thermoelectric voltages in the range of several microvolts per degree Celsius (orders of magnitude greater than the 0.01-µV/°C typical of the TLC2654).

To help minimize thermoelectric effects, careful attention should be paid to component selection and circuit board layout. Avoid the use of nonsoldered connections (such as sockets, relays, switches, etc.) in the input signal path. Cancel thermoelectric effects by duplicating the number of components and junctions in each device input. The use of low-thermoelectric-coefficient components, such as wire-wound resistors, is also beneficial.

latch-up avoidance

Because CMOS devices are susceptible to latch-up due to their inherent parasitic thyristors, the TLC2654 inputs and output are designed to withstand –100-mA surge currents without sustaining latch-up; however, techniques to reduce the chance of latch-up should be used whenever possible. Internal protection diodes should not be forward biased in normal operation. Applied input and output voltages should not exceed the supply voltage by more than 300 mV. Care should be exercised when using capacitive coupling on pulse generators. Supply transients should be shunted by using decoupling capacitors (0.1 µF typical) located across the supply rails as close to the device as possible.

The current path established if latch-up occurs is usually between the supply rails and is limited only by the impedance of the power supply and the forward resistance of the parasitic thyristor. The chance of latch-up occurring increases with increasing temperature and supply voltage.

electrostatic discharge protection

The TLC2654 incorporates internal ESD-protection circuits that prevent functional failures at voltages at or below 2000 V. Care should be exercised in handling these devices, as exposure to ESD may result in degradation of the device parametric performance.

theory of operation

Chopper-stabilized operational amplifiers offer the best dc performance of any monolithic operational amplifiers. This superior performance is the result of using two operational amplifiers – a main amplifier and a nulling amplifier – plus oscillator-controlled logic and two external capacitors to create a system that behaves as a single amplifier. With this approach, the TLC2654 achieves submicrovolt input offset voltage, submicrovolt noise voltage, and offset voltage variations with temperature in the nV/°C range.

The TLC2654 on-chip control logic produces two dominant clock phases – a nulling phase and an amplifying phase. The term "chopper-stabilized" derives from the process of switching between these two clock phases. Figure 34 shows a simplified block diagram of the TLC2654. Switches A and B are make-before-break types. During the nulling phase, switch A is closed, shorting the nulling amplifier inputs together and allowing the nulling amplifier to reduce its own input offset voltage by feeding its output signal back to an inverting input

APPLICATION INFORMATION

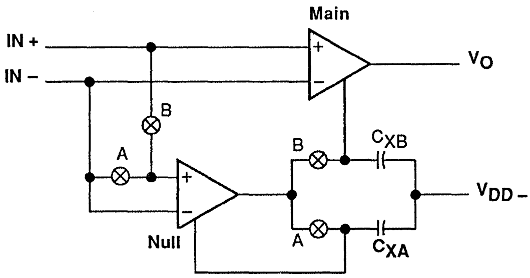


Figure 34. TLC2654 Simplified Block Diagram

node. Simultaneously, external capacitor C_{XA} stores the nulling potential to allow the offset voltage of the amplifier to remain nulled during the amplifying phase.

During the amplifying phase, switch B is closed, connecting the output of the nulling amplifier to a noninverting input of the main amplifier. In this configuration, the input offset voltage of the main amplifier is nulled. Also, external capacitor C_{XB} stores the nulling potential to allow the offset voltage of the main amplifier to remain nulled during the next nulling phase.

This continuous chopping process allows offset voltage nulling during variations in time and temperature and over the common-mode input voltage range and power supply range. In addition, because the low-frequency signal path is through both the null and main amplifiers, extremely high gain is achieved.

The low-frequency noise of a chopper amplifier depends on the magnitude of the component noise prior to chopping and the capability of the circuit to reduce this noise while chopping. The use of the Advanced LinCMOS process, with its low-noise analog MOS transistors and patent-pending input stage design, significantly reduces the input noise voltage.

The primary source of nonideal operation in chopper-stabilized amplifiers is error charge from the switches. As charge imbalance accumulates on critical nodes, input offset voltage can increase, especially with increasing chopping frequency. This problem has been significantly reduced in the TLC2654 by use of a patent-pending compensation circuit and the Advanced LinCMOS process.

The TLC2654 incorporates a feed-forward design that ensures continuous frequency response. Essentially, the gain magnitude of the nulling amplifier and compensation network crosses unity at the break frequency of the main amplifier. As a result, the high-frequency response of the system is the same as the frequency response of the main amplifier. This approach also ensures that the slewing characteristics remain the same during both the nulling and amplifying phases.

The primary limitation on ac performance is the chopping frequency. As the input signal frequency approaches the chopper's clock frequency, intermodulation (or aliasing) errors result from the mixing of these frequencies. To avoid these error signals, the input frequency must be less than half the clock frequency. Most choppers available today limit the internal chopping frequency to less than 500 Hz in order to eliminate errors due to the charge imbalancing phenomenon mentioned previously. However, to avoid intermodulation errors on a 500-Hz chopper, the input signal frequency must be limited to less than 250 Hz. The TLC2654 removes this restriction on ac performance by using a 10-kHz internal clock frequency. This high chopping frequency allows amplification of input signals up to 5 kHz without errors due to intermodulation and greatly reduces low-frequency noise.

THERMAL INFORMATION

temperature coefficient of input offset voltage

Figure 35 shows the effects of package-induced thermal EMF. The TLC2654 can null only the offset voltage within its nulling loop. There are metal-to-metal junctions outside the nulling loop (bonding wires, solder joints, etc.) which produce EMF. In Figure 35, a TLC2654 packaged in a 14-pin plastic package (N package) was placed in an oven at 25°C at t = 0, biased up and allowed to stabilize. At t = 3 min, the oven was turned on and allowed to rise in temperature to 125°C. As evidenced by the curve, the overall change in input offset voltage with temperature is much less than the specified maximum limit of 0.05 µV/°C.

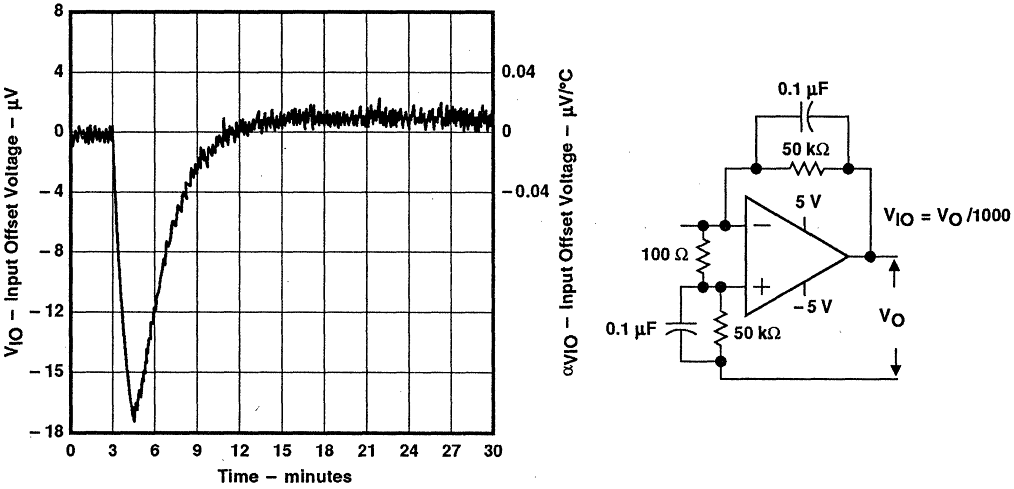


Figure 35. Effects of Package-Induced Thermal EMF

TLE2021, TLE2021A, TLE2021B, TLE2021Y
EXCALIBUR HIGH-SPEED LOW-POWER PRECISION OPERATIONAL AMPLIFIERS

D3197, FEBRUARY 1989 – REVISED OCTOBER 1991

available features

- Supply Current . . . 230 µA Max
- High Unity-Gain Bandwidth . . . 2 MHz Typ
- High Slew Rate . . . 0.45 V/µs Min
- Supply Current Change Over Military Temp Range . . . 10 µA Typ
- Specified for Both 5-V Single-Supply and ± 15-V Operation
- Phase-Reversal Protection
- High Open-Loop Gain . . . 6.5 V/µV (136 dB) Typ
- Low Offset Voltage . . . 100 µV Max
- Offset Voltage Drift With Time 0.005 µV/mo Typ
- Low Input Bias Current . . . 50 nA Max
- Low Noise Voltage . . . 19 nV/√Hz Typ

description

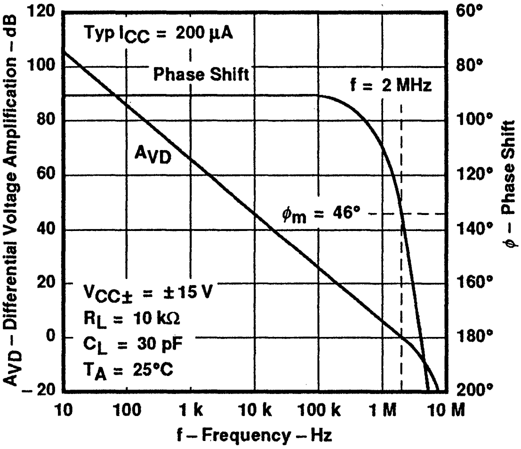
The TLE2021, TLE2021A, and TLE2021B devices are precision, high-speed, low-power operational amplifiers using a new Texas Instruments patent-pending Excalibur process. These devices combine the best features of the OP21 with highly improved slew rate and unity-gain bandwidth.

The complementary bipolar Excalibur process utilizes isolated vertical P-N-P transistors that yield dramatic improvement in unity-gain bandwidth and slew rate over similar devices.

The addition of a patent-pending bias circuit in conjunction with this process results in extremely stable parameters with both time and temperature. This means that a "precision" device remains a precision device even with changes in temperature and over years of use.

This combination of excellent dc performance with a common-mode input voltage range that includes

LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION AND PHASE SHIFT
vs
FREQUENCY



AVAILABLE OPTIONS

T_A	V_{IO} max AT 25°C	PACKAGE						CHIP FORM (Y)
		SMALL OUTLINE (D)	SSOP (DBLE)	CHIP CARRIER (FK)	CERAMIC DIP (JG)	PLASTIC DIP (P)	TSSOP (PWLE)	
0°C to 70°C	200 µV 500 µV	TLE2021ACD TLE2021CD	TLE2021CDBLE			TLE2021ACP TLE2021CP	TLE2021CPWLE	TLE2021Y
– 40°C to 85°C	200 µV 500 µV	TLE2021AID TLE2021ID				TLE2021AIP TLE2021IP		
– 55°C to 125°C	100 µV 200 µV 500 µV	TLE2021AMD TLE2021MD		TLE2021AMFK TLE2021MFK	TLE2021BMJG TLE2021AMJG TLE2021MJG	TLE2021AMP TLE2021MP		

The D package is available taped and reeled. Add the suffix R, (e.g., TLE2021CDR). The DB and PW packages are only available left-end taped and reeled. Chips are tested at 25°C.

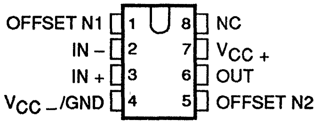
description (continued)

includes the negative rail makes these devices the ideal choice for low-level signal-conditioning applications in either single-supply or split-supply configurations. In addition, these devices offer phase-reversal protection circuitry that eliminates an unexpected change in output states when one of the inputs goes below the negative supply rail.

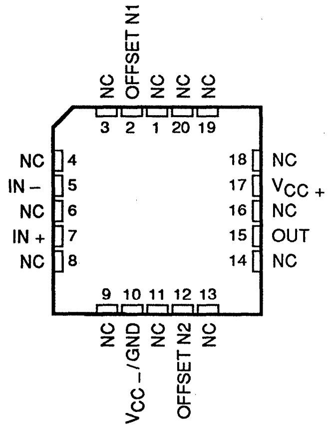
A variety of available options includes small-outline and chip carrier versions for high-density systems applications.

The C-suffix devices are characterized for operation from 0°C to 70°C. The I-suffix devices are characterized for operation from – 40°C to 85°C. The M-suffix devices are characterized for operation over the full military temperature range of –55°C to 125°C.

D, DB, JG, P, OR PW PACKAGE
(TOP VIEW)



FK PACKAGE
(TOP VIEW)

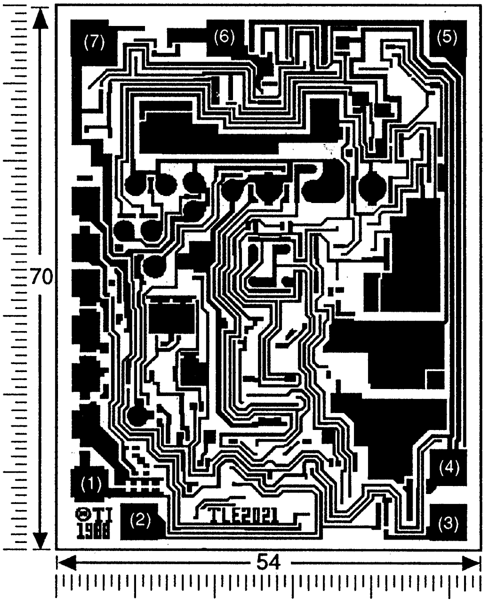


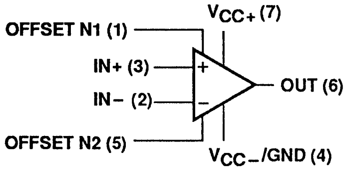
NC – No internal connection

chip information

These chips, properly assembled, display characteristics similar to the TLE2021. Thermal compression or ultrasonic bonding may be used on the doped aluminum bonding pads. Chips may be mounted with conductive epoxy or a gold-silicon preform.

BONDING PAD ASSIGNMENTS





CHIP THICKNESS:
15 TYPICAL

BONDING PADS:
4 X 4 MINIMUM

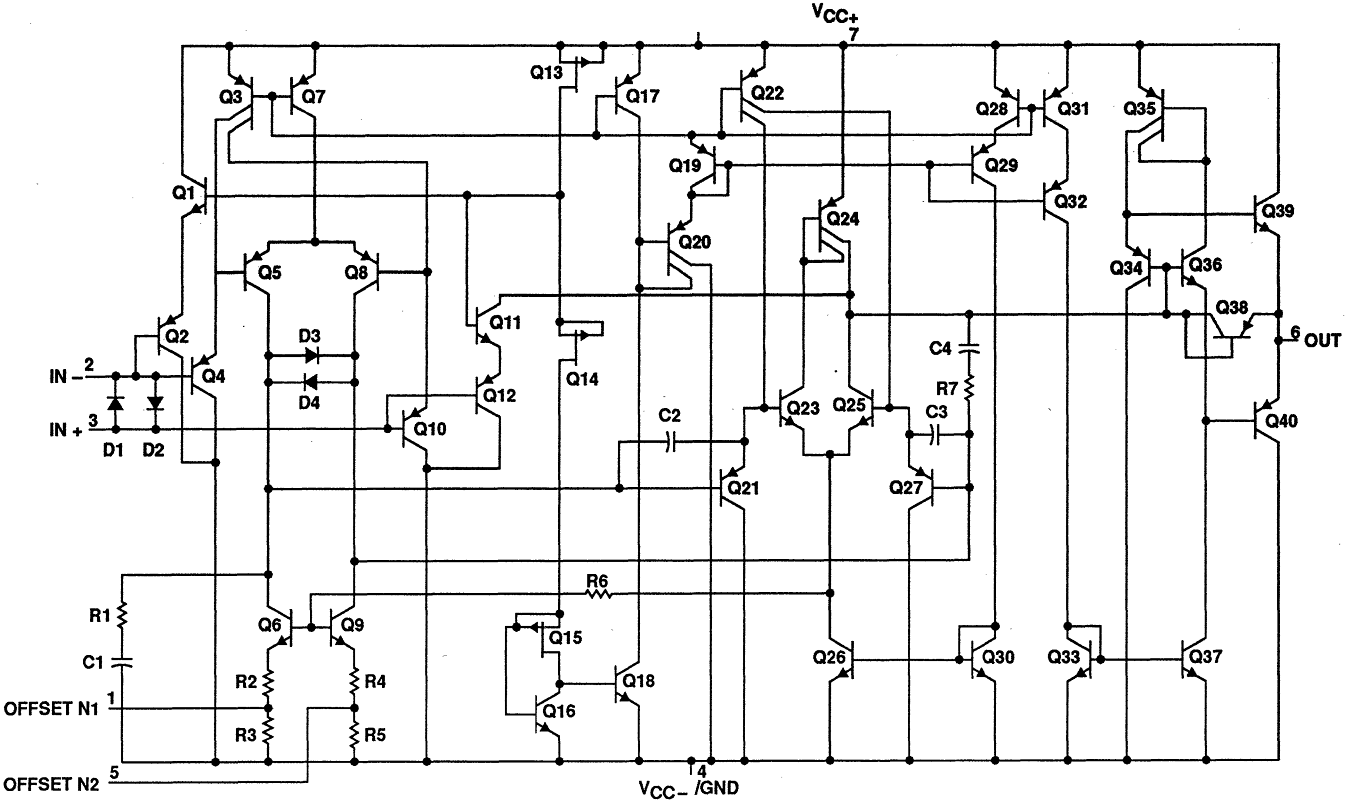
T_J max = 150°C

TOLERANCES
ARE ±10%

ALL DIMENSIONS
ARE IN MILS

PIN (4) INTERNALLY CONNECTED
TO BACKSIDE OF CHIP

equivalent schematic



Pin numbers shown are for the D, DB, JG, P, and PW packages.

Component count: Diodes — 4 Capacitors — 4
Resistors — 7 Transistors — 40

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC+} (see Note 1)	20 V
Supply voltage, V_{CC-} (see Note 1)	−20 V
Differential input voltage (see Note 2)	±0.6 V
Input voltage range, V_I (any input, see Note 1)	$\pm V_{CC}$
Input current, I_I (each input)	±1 mA
Output current, I_O	±20 mA
Total current into V_{CC+} terminal	20 mA
Total current out of V_{CC-} terminal	−20 mA
Duration of short-circuit current at (or below) 25°C (see Note 3)	unlimited
Continuous total dissipation	See Dissipation Rating Table
Operating free-air temperature range, T_A: C-suffix	0°C to 70°C
I-suffix	− 40°C to 85°C
M-suffix	− 55°C to 125°C
Storage temperature range	−65°C to 150°C
Case temperature for 60 seconds: FK package	260°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D, DB, P, or PW package	260°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: JG package	300°C

NOTES:
1. All voltage values, except differential voltages, are with respect to the midpoint between V_{CC+} and V_{CC-}.
2. Differential voltages are at the noninverting input with respect to the inverting input. Excessive current will flow if a differential input voltage in excess of approximately ± 600 mV is applied between the inputs unless some limiting resistance is used.
3. The output may be shorted to either supply. Temperature and/or supply voltages must be limited to ensure that the maximum dissipation rating is not exceeded.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING	$T_A = 125°C$ POWER RATING
D	725 mW	5.8 mW/°C	464 mW	377 mW	145 mW
DB or PW	525 mW	4.2 mW/°C	336 mW	—	—
FK	1375 mW	11.0 mW/°C	880 mW	715 mW	275 mW
JG	1050 mW	8.4 mW/°C	672 mW	546 mW	210 mW
P	1000 mW	8.0 mW/°C	640 mW	520 mW	200 mW

recommended operating conditions

		C-SUFFIX			I-SUFFIX			M-SUFFIX			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, $V_{CC\pm}$		±2		±20	±2		±20	±2		±20	V
Common-mode input voltage, V_{IC}	$V_{CC\pm} = \pm 5$ V	0		3.5	0		3.2	0		3.2	V
	$V_{CC\pm} = \pm 15$ V	− 15		13.5	− 15		13.2	− 15		13.2	
Operating free-air temperature, T_A		0		70	− 40		85	− 55		125	°C

electrical characteristics at specified free-air temperature, V_{CC} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A†	TLE2021C			TLE2021AC			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_{IC} = 0, R_S = 50 Ω	25°C		120	600		100	300	µV
			Full range			850			600	
α_{VIO}	Temperature coefficient of input offset voltage		Full range		2			2		µV/°C
	Input offset voltage long-term drift (see Note 4)		25°C		0.005			0.005		µV/mo
I_{IO}	Input offset current		25°C		0.2	3		0.2	3	nA
			Full range			3			3	
I_{IB}	Input bias current		25°C		25	50		25	50	nA
			Full range			50			50	
V_{ICR}	Common-mode input voltage range	R_S = 50 Ω	25°C	0 to 3.5	−0.3 to 4		0 to 3.5	−0.3 to 4		V
			Full range	0 to 3.5			0 to 3.5			
V_{OH}	High-level output voltage	R_L = 10 kΩ	25°C	4	4.3		4	4.3		V
			Full range	3.9			3.9			
V_{OL}	Low-level output voltage		25°C		0.7	0.8		0.7	0.8	V
			Full range			0.85			0.85	
A_{VD}	Large-signal differential voltage amplification	V_O = 1.4 V to 4 V, R_L = 10 kΩ	25°C	0.3	1.5		0.3	1.5		V/µV
			Full range	0.3			0.3			
CMRR	Common-mode rejection ratio	V_{IC} = V_{ICR} min, R_S = 50 Ω	25°C	85	110		85	110		dB
			Full range	80			80			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm}$ / ΔV_{IO})	V_{CC} = 5 V to 30 V	25°C	105	120		105	120		dB
			Full range	100			100			
I_{CC}	Supply current	V_O = 2.5 V, No load	25°C		170	230		170	230	µA
			Full range			230			230	
ΔI_{CC}	Supply current change over operating temperature range		Full range		5			5		µA

†Full range is 0°C to 70°C.

NOTE 4: Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at T_A = 150°C extrapolated to T_A = 25°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

electrical characteristics at specified free-air temperature, $V_{CC\pm}$ = ±15 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A†	TLE2021C			TLE2021AC			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_{IC} = 0, R_S = 50 Ω	25°C		120	500		80	200	µV
			Full range			750			500	
α_{VIO}	Temperature coefficient of input offset voltage		Full range		2			2		µV/°C
	Input offset voltage long-term drift (see Note 4)		25°C		0.006			0.006		µV/mo
I_{IO}	Input offset current		25°C		0.2	3		0.2	3	nA
			Full range			3			3	
I_{IB}	Input bias current		25°C		25	50		25	50	nA
			Full range			50			50	
V_{ICR}	Common-mode input voltage range	R_S = 50 Ω	25°C	– 15 to 13.5	–15.3 to 14		– 15 to 13.5	–15.3 to 14		V
			Full range	–15 to 13.5			–15 to 13.5			
V_{OM+}	Maximum positive peak output voltage swing	R_L = 10 kΩ	25°C	14	14.3		14	14.3		V
			Full range	13.9			13.9			
V_{OM-}	Maximum negative peak output voltage swing		25°C	–13.7	–14.1		–13.7	–14.1		V
			Full range	–13.7			–13.7			
A_{VD}	Large-signal differential voltage amplification	V_O = ±10 V, R_L = 10 kΩ	25°C	1	6.5		1	6.5		V/µV
			Full range	1			1			
CMRR	Common-mode rejection ratio	V_{IC} = V_{ICR} min, R_S = 50 Ω	25°C	100	115		100	115		dB
			Full range	96			96			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm} / \Delta V_{IO}$)	$V_{CC\pm}$ = ±2.5 V to ±15 V	25°C	105	120		105	120		dB
			Full range	100			100			
I_{CC}	Supply current	V_O = 0, No load	25°C		200	300		200	300	µA
			Full range			300			300	
ΔI_{CC}	Supply current change over operating temperature range		Full range		6			6		µA

†Full range is 0°C to 70°C.

NOTE 4: Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at T_A = 150°C extrapolated to T_A = 25°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

electrical characteristics at specified free-air temperature, V_{CC} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A†	TLE2021I			TLE2021AI			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_{IC} = 0, R_S = 50 Ω	25°C		120	600		100	300	µV
			Full range			950			600	
α_{VIO}	Temperature coefficient of input offset voltage		Full range		2			2		µV/°C
	Input offset voltage long-term drift (see Note 4)		25°C		0.005			0.005		µV/mo
I_{IO}	Input offset current		25°C		0.2	3		0.2	3	nA
			Full range			4			4	
I_{IB}	Input bias current		25°C		25	50		25	50	nA
			Full range			50			50	
V_{ICR}	Common-mode input voltage range	R_S = 50 Ω	25°C	0 to 3.5	−0.3 to 4		0 to 3.5	−0.3 to 4		V
			Full range	0 to 3.2			0 to 3.2			
V_{OH}	High-level output voltage	R_L = 10 kΩ	25°C	4	4.3		4	4.3		V
			Full range	3.9			3.9			
V_{OL}	Low-level output voltage		25°C		0.7	0.8		0.7	0.8	V
			Full range			0.9			0.9	
A_{VD}	Large-signal differential voltage amplification	V_O = 1.4 V to 4 V, R_L = 10 kΩ	25°C	0.3	1.5		0.3	1.5		V/µV
			Full range	0.25			0.25			
CMRR	Common-mode rejection ratio	V_{IC} = V_{ICR} min, R_S = 50 Ω	25°C	85	110		85	110		dB
			Full range	80			80			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm}/\Delta V_{IO}$)	V_{CC} = 5 V to 30 V	25°C	105	120		105	120		dB
			Full range	100			100			
I_{CC}	Supply current	V_O = 2.5 V, No load	25°C		170	230		170	230	µA
			Full range			230			230	
ΔI_{CC}	Supply current change over operating temperature range		Full range		6			6		µA

†Full range is –40°C to 85°C.

NOTE 4: Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at T_A = 150°C extrapolated to T_A = 25°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

electrical characteristics at specified free-air temperature, $V_{CC\pm}$ = ± 15 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A†	TLE2021I			TLE2021AI			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_{IC} = 0, R_S = 50 Ω	25°C		120	500		80	200	µV
			Full range			850			500	
α_{VIO}	Temperature coefficient of input offset voltage		Full range		2			2		µV/°C
	Input offset voltage long-term drift (see Note 4)		25°C		0.006			0.006		µV/mo
I_{IO}	Input offset current		25°C		0.2	3		0.2	3	nA
			Full range			4			4	
I_{IB}	Input bias current		25°C		25	50		25	50	nA
			Full range			50			50	
V_{ICR}	Common-mode input voltage range	R_S = 50 Ω	25°C	−15 to 13.5	−15.3 to 14		−15 to 13.5	−15.3 to 14		V
			Full range	−15 to 13.2			−15 to 13.2			
V_{OM+}	Maximum positive peak output voltage swing	R_L = 10 kΩ	25°C	14	14.3		14	14.3		V
			Full range	13.9			13.9			
V_{OM-}	Maximum negative peak output voltage swing		25°C	−13.7	−14.1		−13.7	−14.1		V
			Full range	−13.6			−13.6			
A_{VD}	Large-signal differential voltage amplification	V_O = 10 V, R_L = 10 kΩ	25°C	1	6.5		1	6.5		V/µV
			Full range	0.75			0.75			
CMRR	Common-mode rejection ratio	$V_{IC} = V_{ICR}$ min, R_S = 50 Ω	25°C	100	115		100	115		dB
			Full range	96			96			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm} / \Delta V_{IO}$)	$V_{CC\pm}$ = ±2.5 V to ±15 V	25°C	105	120		105	120		dB
			Full range	100			100			
I_{CC}	Supply current	V_O = 0, No load	25°C		200	300		200	300	µA
			Full range			300			300	
ΔI_{CC}	Supply current change over operating temperature range		Full range		7			7		µA

†Full range is −40°C to 85°C.

NOTE 4: Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at T_A = 150°C extrapolated to T_A = 25°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

electrical characteristics at specified free-air temperature, V_{CC} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A†	TLE2021M			TLE2021AM			TLE2021BM			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_{IC} = 0, R_S = 50 Ω	25°C		120	600		100	300		80	200	µV
			Full range			1100			600			300	
α_{VIO}	Temperature coefficient of input offset voltage		Full range		2			2			2		µV/°C
	Input offset voltage long-term drift (see Note 4)		25°C		0.005			0.005			0.005		µV/mo
I_{IO}	Input offset current		25°C		0.2	3		0.2	3		0.2	3	nA
			Full range			5			5			5	
I_{IB}	Input bias current		25°C		25	50		25	50		25	50	nA
			Full range			50			50			50	
V_{ICR}	Common-mode input voltage range	R_S = 50 Ω	25°C	0 to 3.5	−0.3 to 4		0 to 3.5	−0.3 to 4		0 to 3.5	−0.3 to 4		V
			Full range	0 to 3.2			0 to 3.2			0 to 3.2			
V_{OH}	High-level output voltage	R_L = 10 kΩ	25°C	4	4.3		4	4.3		4	4.3		V
			Full range	3.8			3.8			3.8			
V_{OL}	Low-level output voltage		25°C		0.7	0.8		0.7	0.8		0.7	0.8	V
			Full range			0.95			0.95			0.95	
A_{VD}	Large-signal differential voltage amplification	V_O = 1.4 V to 4 V, R_L = 10 kΩ	25°C	0.3	1.5		0.3	1.5		0.3	1.5		V/µV
			Full range	0.1			0.1			0.1			
CMRR	Common-mode rejection ratio	V_{IC} = V_{ICR} min, R_S = 50 Ω	25°C	85	110		85	110		85	110		dB
			Full range	80			80			80			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm} / \Delta V_{IO}$)	V_{CC} = 5 V to 30 V	25°C	105	120		105	120		105	120		dB
			Full range	100			100			100			
I_{CC}	Supply current	V_O = 2.5 V, No load	25°C		170	230		170	230		170	230	µA
			Full range			230			230			230	
ΔI_{CC}	Supply current change over operating temperature range		Full range		9			9			9		µA

†Full range is − 55°C to 125°C.

NOTE 4: Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at T_A = 150°C extrapolated to T_A = 25°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

electrical characteristics at specified free-air temperature, $V_{CC\pm} = \pm 15$ V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A†	TLE2021M			TLE2021AM			TLE2021BM			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	$V_{IC} = 0$, $R_S = 50\ \Omega$	25°C		120	500		80	200		40	100	μV
			Full range			1000			500			200	
α_{VIO}	Temperature coefficient of input offset voltage		Full range		2			2			2		μV/°C
	Input offset voltage long-term drift (see Note 4)		25°C		0.006			0.006			0.006		μV/mo
I_{IO}	Input offset current		25°C		0.2	3		0.2	3		0.2	3	nA
			Full range			5			5			5	
I_{IB}	Input bias current		25°C		25	50		25	50		25	50	nA
			Full range			50			50			50	
V_{ICR}	Common-mode input voltage range	$R_S = 50\ \Omega$	25°C	– 15 to – 15	– 15.3 to 14		– 15 to 13.5	– 15.3 to 14		– 15 to 13.5	– 15.3 to 14		V
			Full range	– 15 to 13.2			– 15 to 13.2			– 15 to 13.2			
V_{OM+}	Maximum positive peak output voltage swing	$R_L = 10\ k\Omega$	25°C	14	14.3		14	14.3		14	14.3		V
			Full range	13.8			13.8			13.8			
V_{OM-}	Maximum negative peak output voltage swing		25°C	– 13.7	– 14.1		– 13.7	– 14.1		– 13.7	– 14.1		V
			Full range	– 13.6			– 13.6			– 13.6			
A_{VD}	Large-signal differential voltage amplification	$V_O = \pm 10$ V, $R_L = 10\ k\Omega$	25°C	1	6.5		1	6.5		1	6.5		V/μV
			Full range	0.5			0.5			0.5			
CMRR	Common-mode rejection ratio	$V_{IC} = V_{ICR}$ min, $R_S = 50\ \Omega$	25°C	100	115		100	115		100	115		dB
			Full range	96			96			96			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm} / \Delta V_{IO}$)	$V_{CC\pm} = \pm 2.5$ V to ± 15 V	25°C	105	120		105	120		105	120		dB
			Full range	100			100			100			
I_{CC}	Supply current	$V_O = 0$ V, No load	25°C		200	300		200	300		200	300	μA
			Full range			300			300			300	
ΔI_{CC}	Supply current change over operating temperature range		Full range		10			10			10		μA

†Full range is – 55°C to 125°C.

NOTE 4: Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at $T_A = 150°C$ extrapolated to $T_A = 25°C$ using the Arrhenius equation and assuming an activation energy of 0.96 eV.

operating characteristics at specified free-air temperature, V_{CC} = 5 V

PARAMETER		TEST CONDITIONS	T_A	C-SUFFIX			I-SUFFIX			M-SUFFIX			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
SR	Slew rate at unity gain	V_O = 1 V to 3 V, See Figure 1	25°C		0.5			0.5			0.5		V/µs
V_n	Equivalent input noise voltage (see Figure 2)	f = 10 Hz	25°C		21	50		21	50		21		nV/√Hz
		f = 1 kHz	25°C		17	30		17	30		17		
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 to 1 Hz	25°C		0.16			0.16			0.16		µV
		f = 0.1 to 10 Hz	25°C		0.47			0.47			0.47		
I_n	Equivalent input noise current		25°C		0.09			0.09			0.9		pA/√Hz
B_1	Unity-gain bandwidth	See Figure 3	25°C		1.2			1.2			1.2		MHz
ϕ_m	Phase margin at unity gain	See Figure 3	25°C		42°			42°			42°		

operating characteristics at specified free-air temperature, $V_{CC\pm}$ = ±15 V

PARAMETER		TEST CONDITIONS	T_A†	C-SUFFIX			I-SUFFIX			M-SUFFIX			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
SR	Slew rate at unity gain	V_O = ±10 V, See Figure 1	25°C	0.45	0.65		0.45	0.65		0.45	0.65		V/µs
			Full range	0.45			0.42			0.4			
V_n	Equivalent input noise voltage (see Figure 2)	f = 10 Hz	25°C		19	50		19	50		19		nV/√Hz
		f = 1 kHz	25°C		15	30		15	30		15		
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 to 1 Hz	25°C		0.16			0.16			0.16		µV
		f = 0.1 to 10 Hz	25°C		0.47			0.47			0.47		
I_n	Equivalent input noise current		25°C		0.09			0.09			0.09		pA/√Hz
B_1	Unity-gain bandwidth	See Figure 3	25°C		2			2			2		MHz
ϕ_m	Phase margin at unity gain	See Figure 3	25°C		46°			46°			46°		

†Full range is 0°C to 70°C for the C-suffix devices, – 40°C to 85°C for the I-suffix devices, and – 55°C to 125°C for the M-suffix devices.

electrical characteristics at V_{CC} = 5 V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	V_{IC} = 0, R_S = 50 Ω		150	600	µV
	Input offset voltage long-term drift (see Note 4)			0.005		µV/mo
I_{IO}	Input offset current			0.5	5	nA
I_{IB}	Input bias current			35	60	nA
V_{ICR}	Common-mode input voltage range	R_S = 50 Ω	0 to 3.5	−0.3 to 4		V
V_{OH}	Maximum high-level output voltage	R_L = 10 kΩ	4	4.3		V
V_{OL}	Maximum low-level output voltage			0.7	0.8	V
A_{VD}	Large-signal differential voltage amplification	V_O = 1.4 V to 4 V, R_L = 10 kΩ	0.3	1.5		V/µV
CMRR	Common-mode rejection ratio	V_{IC} = V_{ICR}min, R_S = 50 Ω	85	100		dB
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm}/\Delta V_{IO}$)	V_{CC} = 5 V to 30 V	100	115		dB
I_{CC}	Supply current	V_O = 2.5 V, No load		400	500	µA

NOTE 4: Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at T_A = 150°C extrapolated to T_A = 25°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

operating characteristics at V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain	V_O = 1 V to 3 V		0.5		V/µs
V_n	Equivalent input noise voltage	f = 10 Hz		21	50	nV/√Hz
		f = 1 kHz		17	30	
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 to 1 Hz		0.16		µV
		f = 0.1 to 10 Hz		0.47		
I_n	Equivalent input noise current			0.1		pA/√Hz
B_1	Unity-gain bandwidth			1.7		MHz
ϕ_m	Phase margin at unity gain			47°		

PARAMETER MEASUREMENT INFORMATION

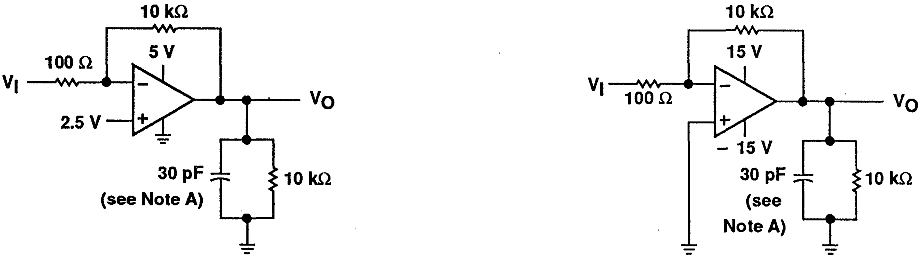
NOTE A: C_L includes fixture capacitance.

(a) SINGLE-SUPPLY (b) SPLIT-SUPPLY

Figure 1. Slew Rate Test Circuit

(a) SINGLE-SUPPLY (b) SPLIT-SUPPLY

Figure 2. Noise Voltage Test Circuit

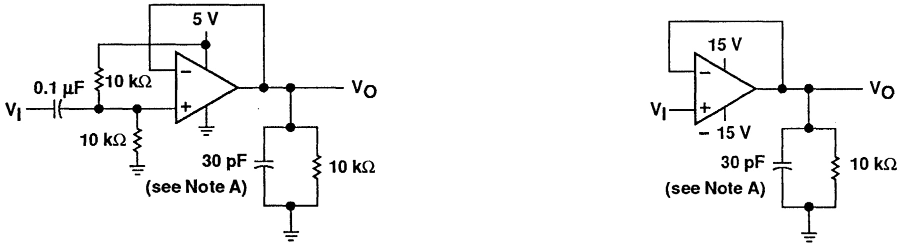


NOTE A: C_L includes fixture capacitance.

(a) SINGLE-SUPPLY (b) SPLIT-SUPPLY

Figure 3. Unity-Gain Bandwidth and Phase Margin Test Circuit

PARAMETER MEASUREMENT INFORMATION



NOTE A: C_L includes fixture capacitance.

(a) SINGLE-SUPPLY

(b) SPLIT-SUPPLY

Figure 4. Small-Signal Pulse Response Test Circuit

typical values

Typical values as presented in this data sheet represent the median (50% point) of device parametric performance of initial devices from three wafer lots used for characterization.

TYPICAL CHARACTERISTICS

table of graphs

			FIGURE
V_{IO}	Input offset voltage	Distribution	5
I_{IB}	Input bias current	vs Common-mode voltage	6
		vs Temperature	7
I_I	Input current	vs Differential input voltage	8
V_{OM}	Maximum peak output voltage	vs Output current	9
		vs Temperature	10
V_{OH}	High-level output voltage	vs High-level output current	11
		vs Temperature	12
V_{OL}	Low-level output voltage	vs Low-level output current	13
		vs Temperature	14
$V_{O(PP)}$	Maximum peak-to-peak output voltage swing	vs Frequency	15, 16
A_{VD}	Differential voltage amplification	vs Frequency	17
		vs Temperature	18
I_{OS}	Short-circuit output current	vs Supply voltage	19, 20
		vs Temperature	21, 22
I_{CC}	Supply current	vs Supply voltage	23
		vs Temperature	24
CMRR	Common-mode rejection ratio	vs Frequency	25
SR	Slew rate	vs Temperature	26
	Pulse response	Small-signal	27, 28
		Large-signal	29, 30
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	0.1 to 1 Hz	31
		0.1 to 10 Hz	32
V_n	Equivalent input noise voltage	vs Frequency	33
B_1	Unity-gain bandwidth	vs Supply voltage	34
		vs Temperature	35
ϕ_m	Phase margin	vs Supply voltage	36
		vs Temperature	37
		vs Capacitive load	38
	Phase shift	vs Frequency	17

TYPICAL CHARACTERISTICS†

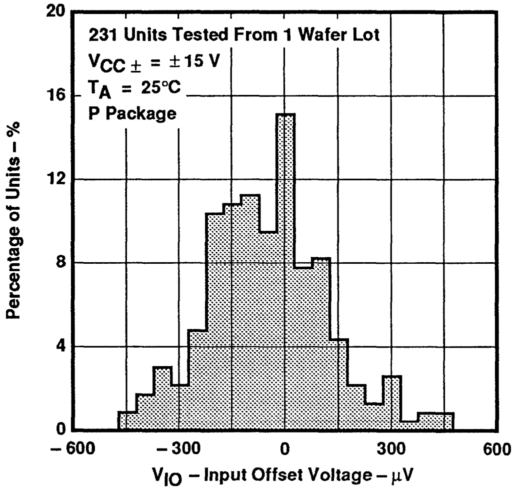

DISTRIBUTION OF TLE2021
INPUT OFFSET VOLTAGE

Figure 5

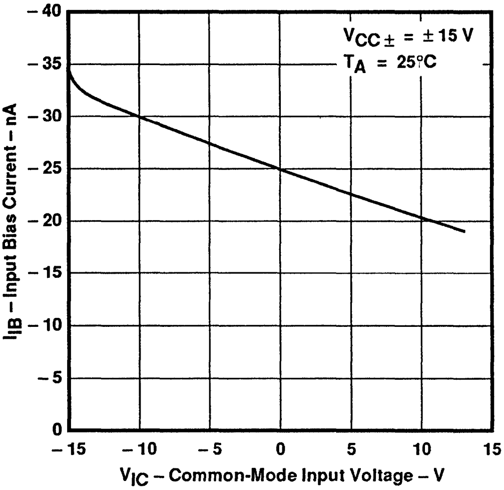

INPUT BIAS CURRENT
vs
COMMON-MODE INPUT VOLTAGE

Figure 6

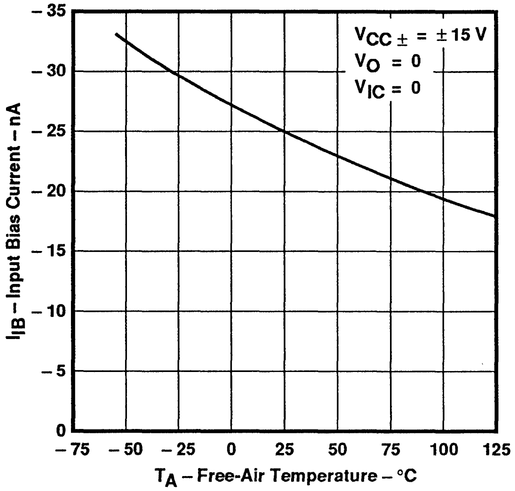

INPUT BIAS CURRENT
vs
FREE-AIR TEMPERATURE

Figure 7

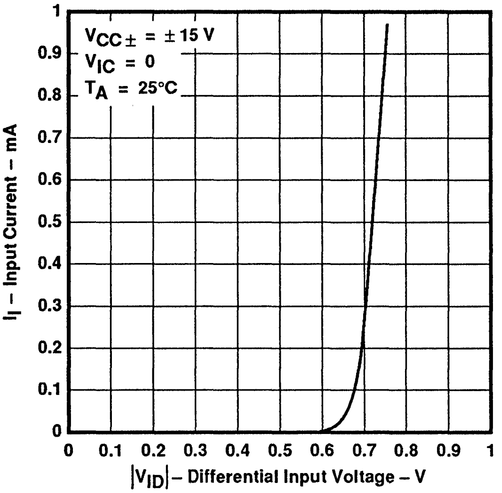

INPUT CURRENT
vs
DIFFERENTIAL INPUT VOLTAGE

Figure 8

---

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

MAXIMUM PEAK OUTPUT VOLTAGE
vs
OUTPUT CURRENT

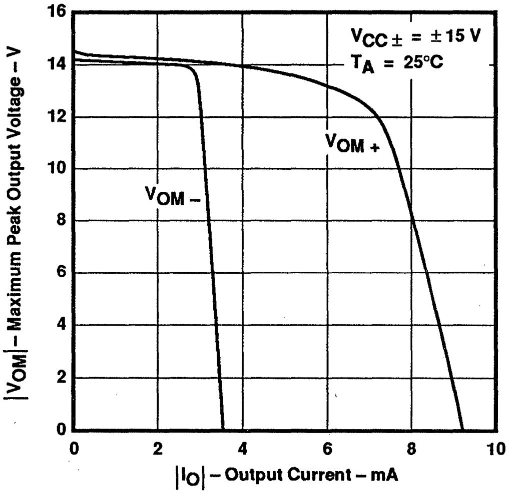


Figure 9

MAXIMUM PEAK OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

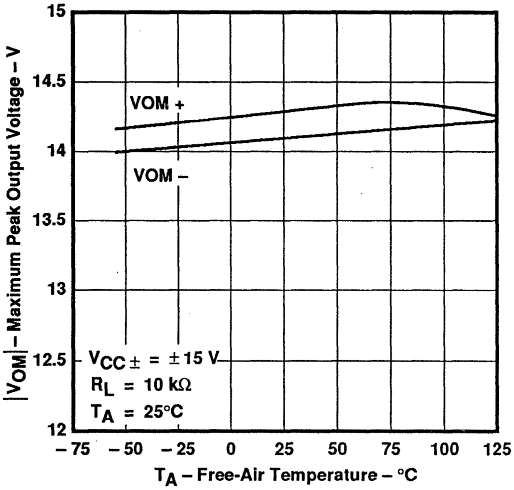


Figure 10

HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

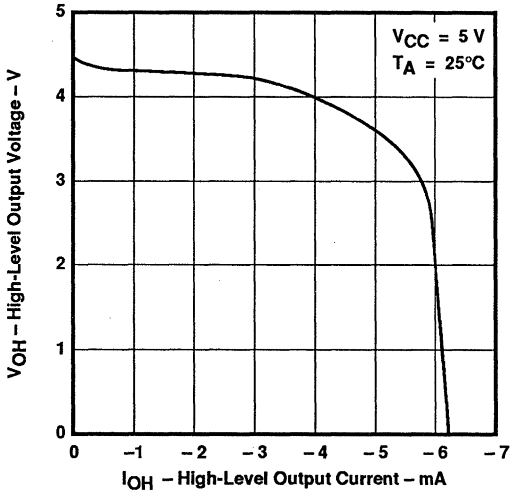


Figure 11

HIGH-LEVEL OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

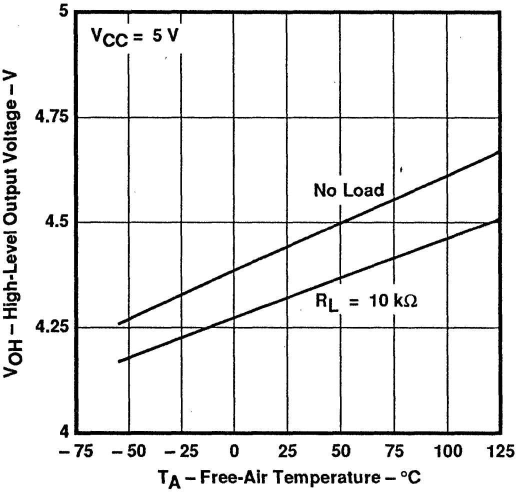


Figure 12

---

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

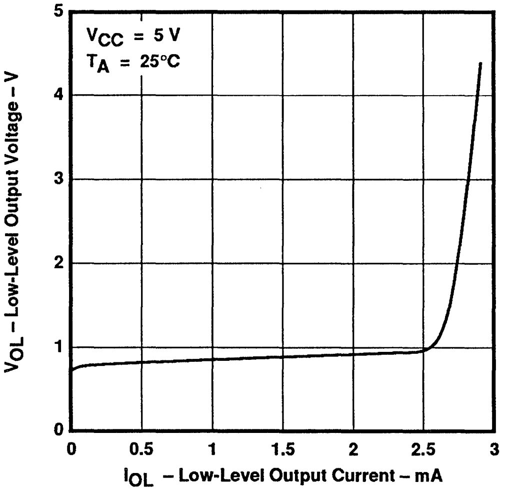


Figure 13

LOW-LEVEL OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

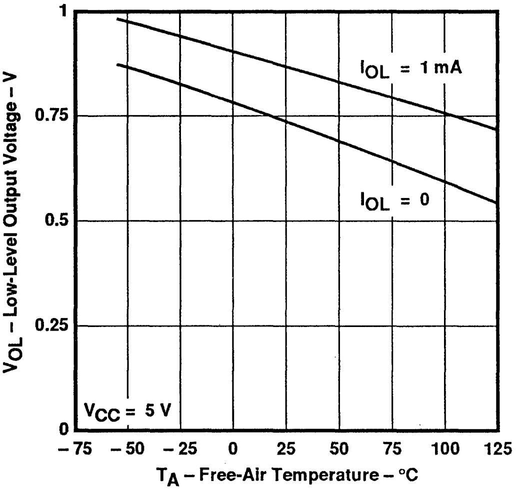


Figure 14

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE
vs
FREQUENCY

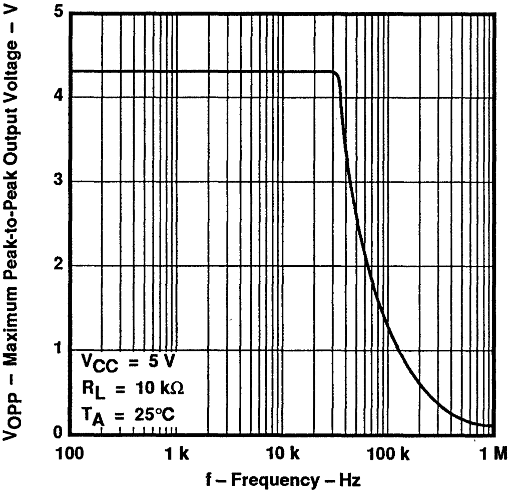


Figure 15

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE
vs
FREQUENCY

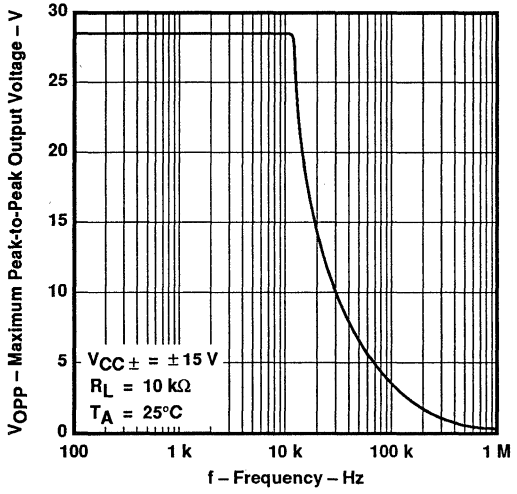


Figure 16

---

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION AND PHASE SHIFT
vs
FREQUENCY

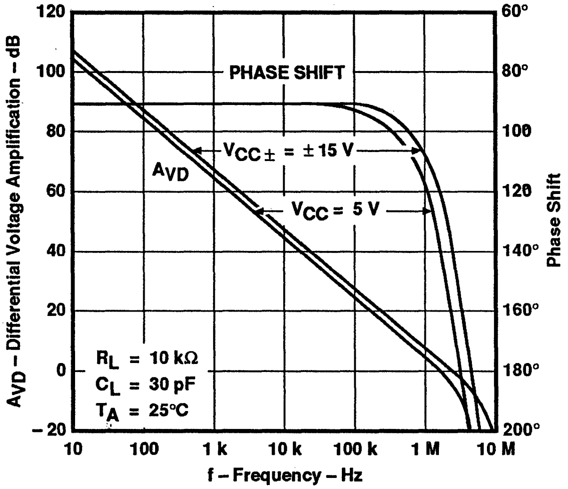


Figure 17

LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION
vs
FREE-AIR TEMPERATURE

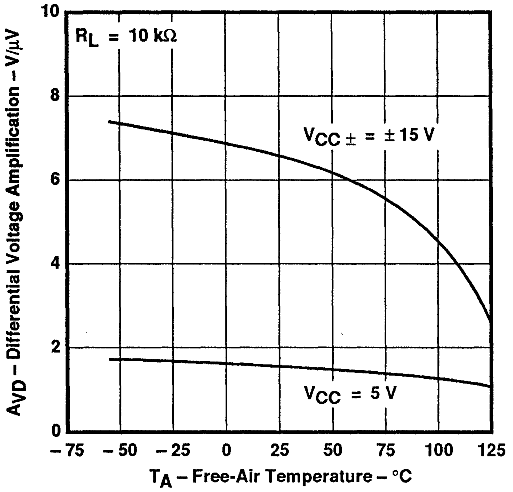


Figure 18

SHORT-CIRCUIT OUTPUT CURRENT
vs
SUPPLY VOLTAGE

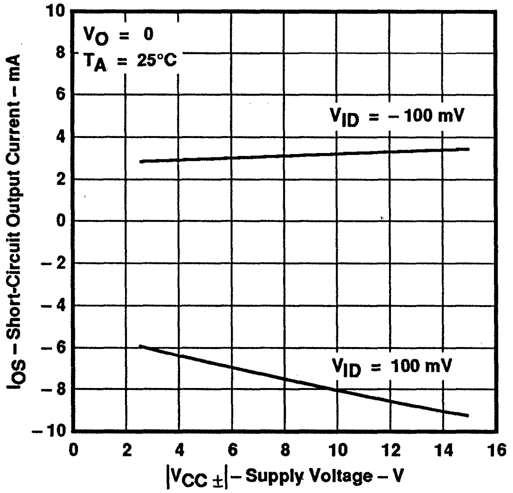


Figure 19

SHORT-CIRCUIT OUTPUT CURRENT
vs
SUPPLY VOLTAGE

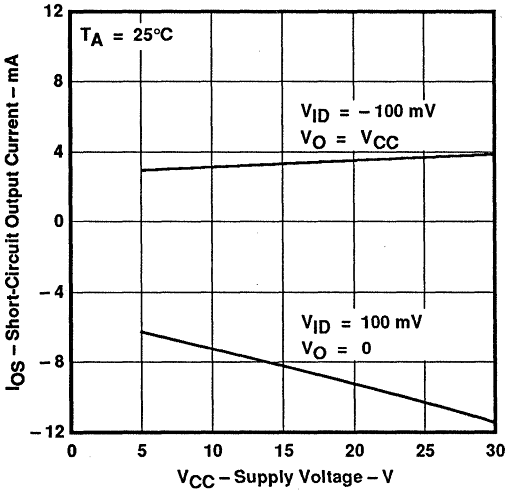


Figure 20

---

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

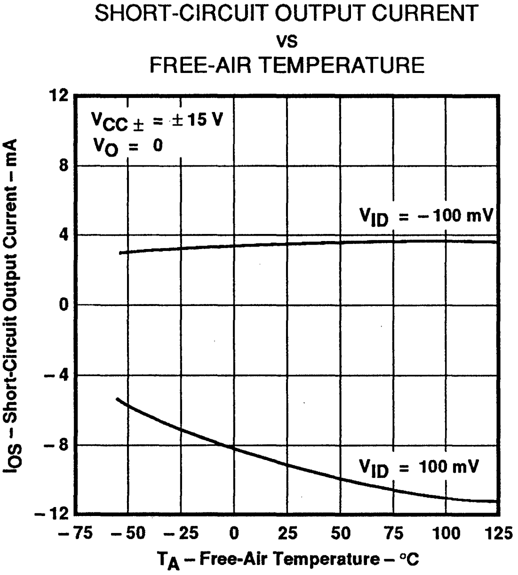


Figure 21

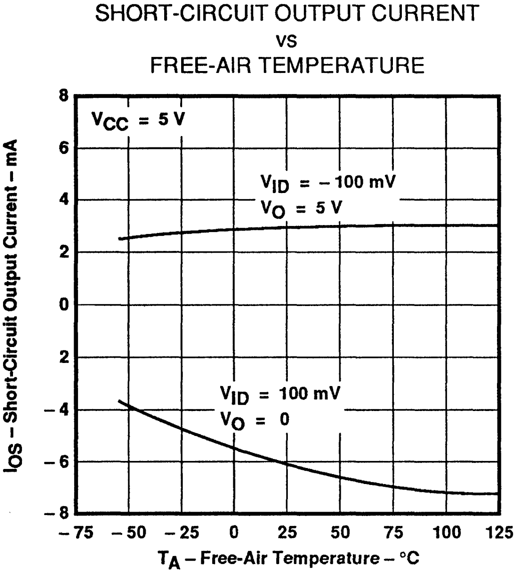


Figure 22

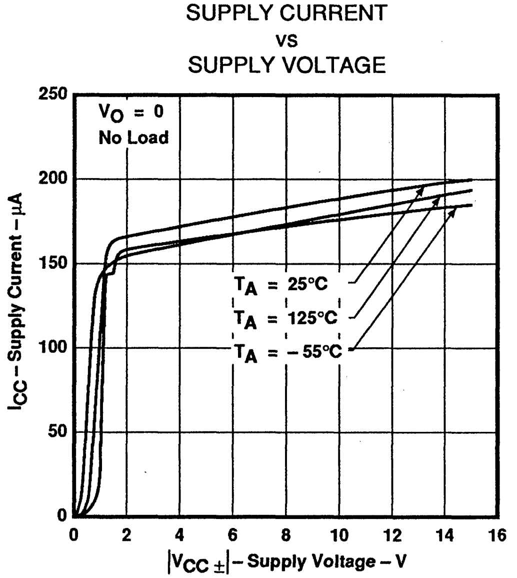


Figure 23

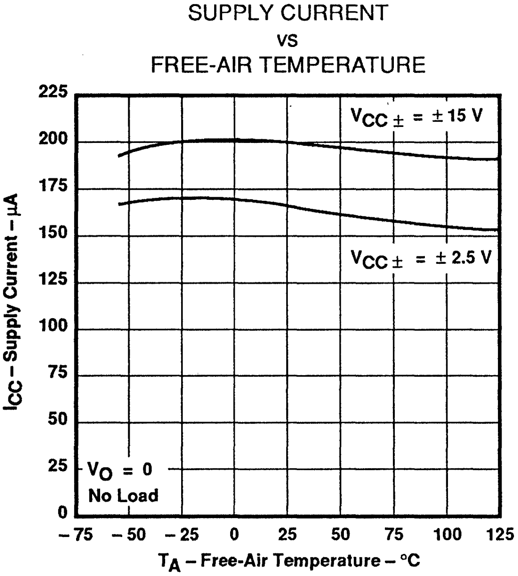


Figure 24

---

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

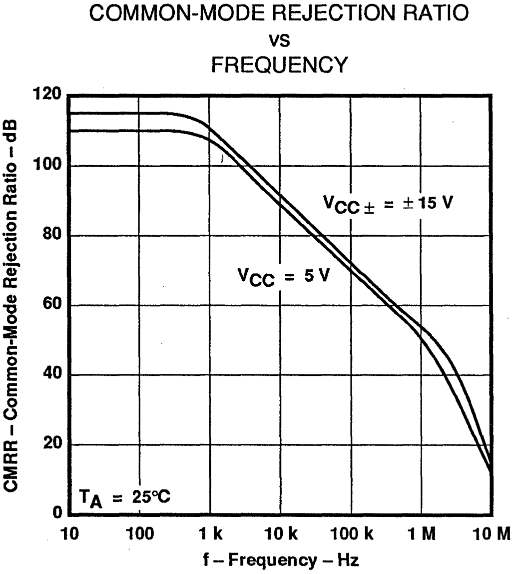


Figure 25

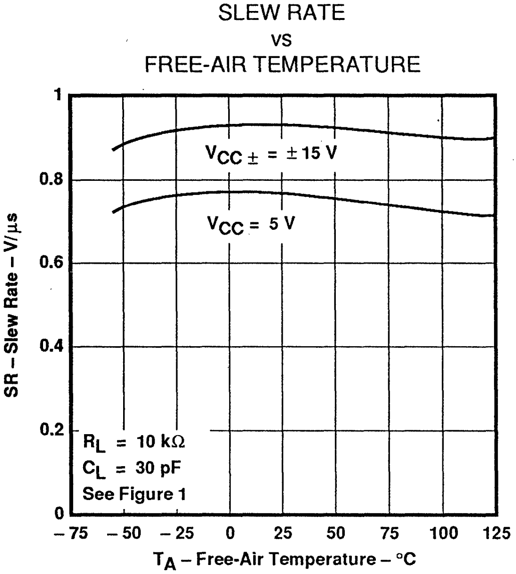


Figure 26

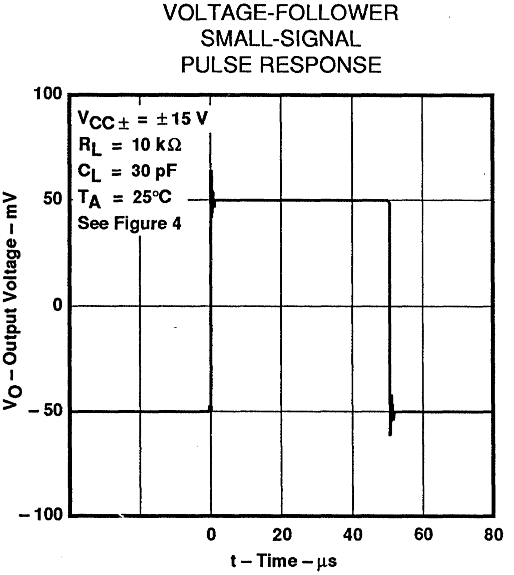


Figure 27

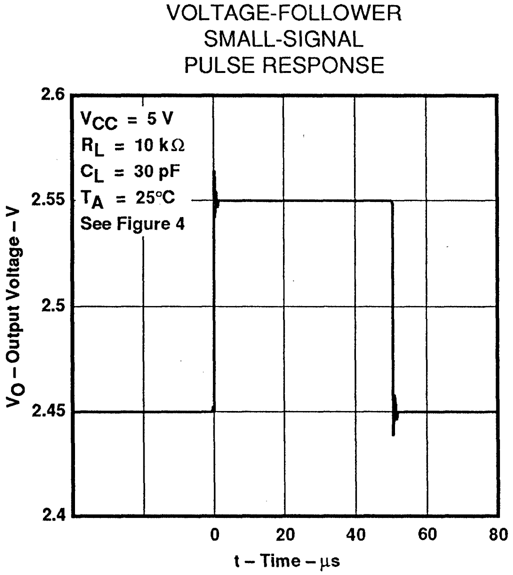


Figure 28

---

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS

VOLTAGE-FOLLOWER
LARGE-SIGNAL
PULSE RESPONSE

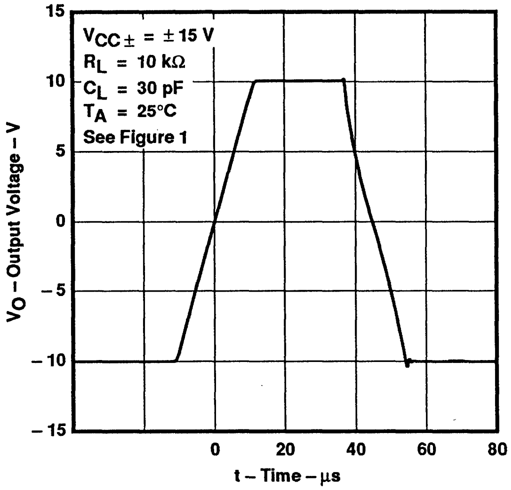


Figure 29

VOLTAGE-FOLLOWER
LARGE-SIGNAL
PULSE RESPONSE

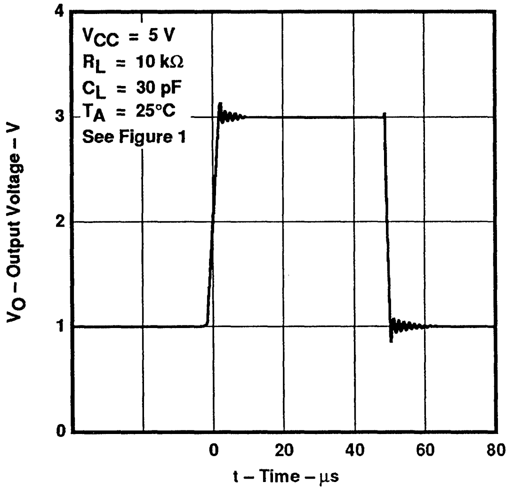


Figure 30

PEAK-TO-PEAK EQUIVALENT
INPUT NOISE VOLTAGE
0.1 TO 1 Hz

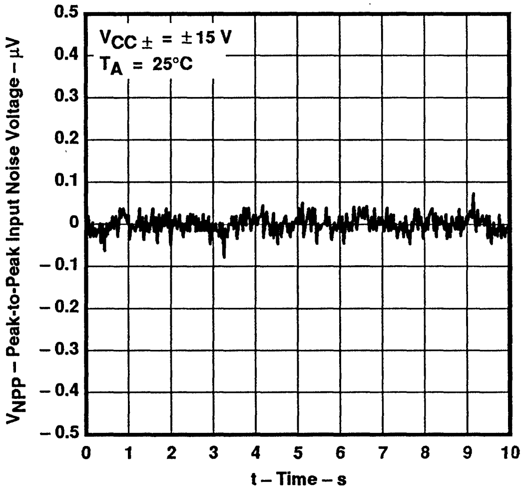


Figure 31

PEAK-TO-PEAK EQUIVALENT
INPUT NOISE VOLTAGE
0.1 TO 10 Hz

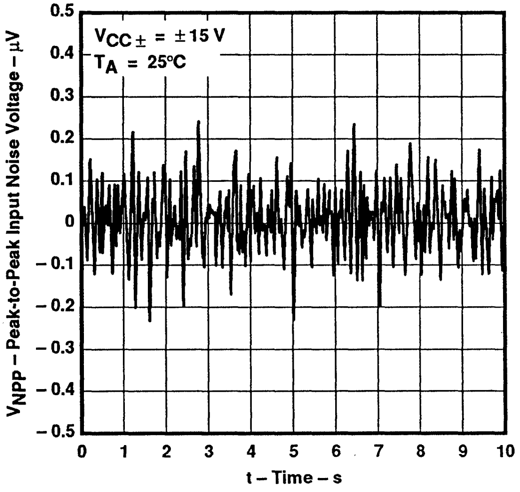


Figure 32

TYPICAL CHARACTERISTICS†

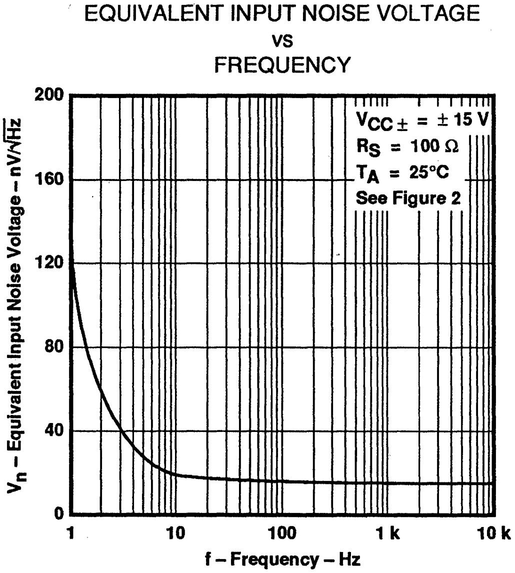


Figure 33

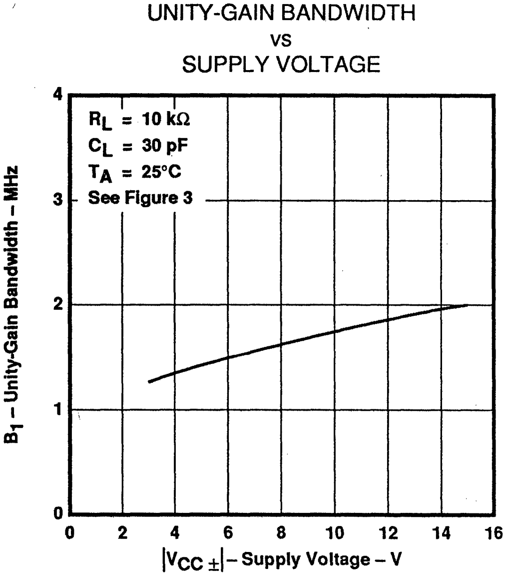


Figure 34

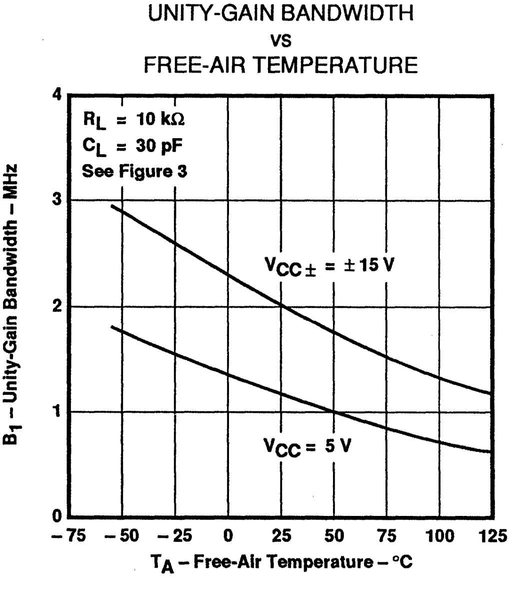


Figure 35

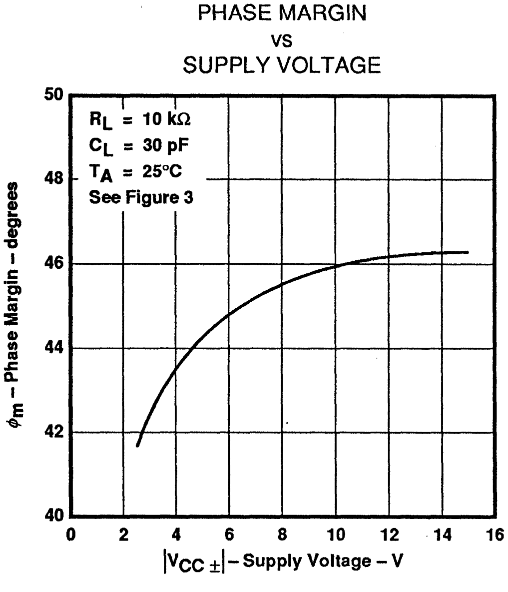


Figure 36

---

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

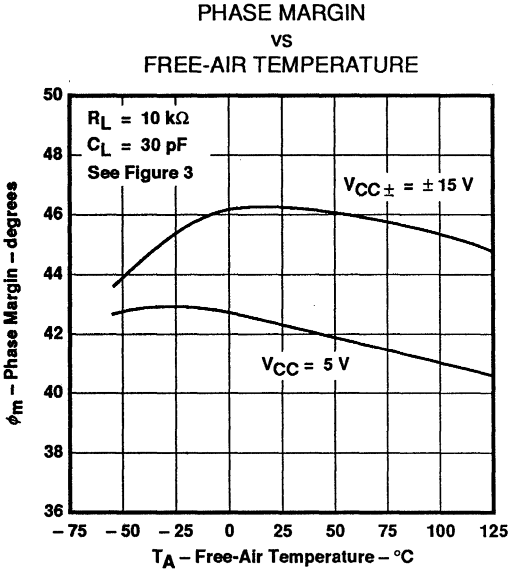


Figure 37

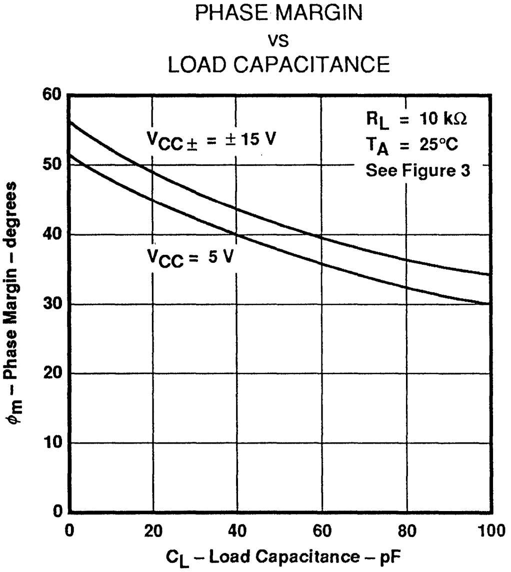


Figure 38

---

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

APPLICATION INFORMATION

voltage-follower applications

The TLE2021 circuitry includes input protection diodes to limit the voltage across the input transistors; however, no provision is made in the circuit to limit the current if these diodes are forward-biased. Note that this condition can occur when the device is operated in the voltage-follower configuration and driven with a fast, large-signal pulse. It is recommended that a feedback resistor be used to limit the current to a maximum of 1 mA to prevent degradation of the device. Also, remember that this feedback resistor will form a pole with the input capacitance of the device. For feedback resistor values greater than 10 kΩ, this pole will degrade the amplifier's phase margin. This problem can be alleviated by adding a capacitor (20 pF to 50 pF) in parallel with the feedback resistor (see Figure 39).

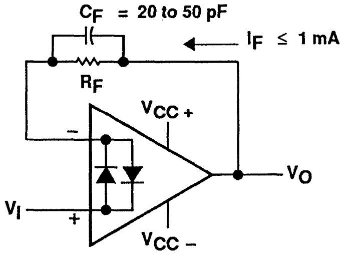


Figure 39. Voltage Follower

APPLICATION INFORMATION

input offset voltage nulling

The TLE2021 series offers external null pins that can be used to further reduce the input offset voltage. The circuit of Figure 40 can be connected as shown if this feature is desired. If external nulling is not needed, the null pins may be left unconnected.

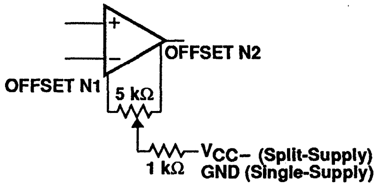


Figure 40. Input Offset Voltage Null Circuit

TLE2022, TLE2022A, TLE2022B, TLE2022Y
EXCALIBUR HIGH-SPEED LOW-POWER PRECISION DUAL OPERATIONAL AMPLIFIERS

D3264, MAY 1989 – REVISED OCTOBER 1991

available features

- Supply Current . . . 500 µA Max
- High Unity-Gain Bandwidth . . . 2.8 MHz Typ
- High Slew Rate . . . 0.7 V/µs Min
- Supply Current Change Over Military Temp Range . . . 37 µA Typ
- Specified for Both 5-V Single-Supply and ± 15-V Operation
- Phase-Reversal Protection
- High Open-Loop Gain . . . 10 V/µV (140 dB) Typ
- Low Offset Voltage . . . 150 µV Max
- Offset Voltage Drift With Time 0.005 µV/mo Typ
- Low Input Bias Current . . . 50 nA Max
- Low Noise Voltage . . . 19 $\mathrm{nV}/\sqrt{\mathrm{Hz}}$ Typ at f = 10 Hz

description

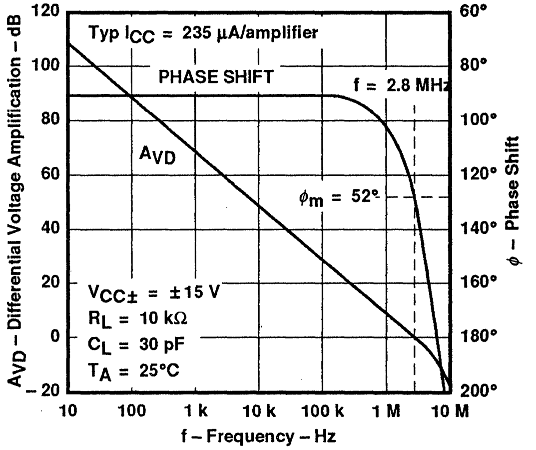
The TLE2022, TLE2022A, and TLE2022B devices are precision, high-speed, low-power operational amplifiers using Texas Instruments patent-pending Excalibur process. These devices combine the best features of the OP221 with highly improved slew rate and unity-gain bandwidth.

The complementary bipolar Excalibur process utilizes isolated vertical P-N-P transistors that yield dramatic improvement in unity-gain bandwidth and slew rate over similar devices.

The addition of a patent-pending bias circuit in conjunction with this process results in extremely stable parameters with both time and temperature. This means that a "precision" device remains a precision device even with changes in temperature and over years of use.

This combination of excellent dc performance with a common-mode input voltage range that includes the negative rail makes these devices

LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION and PHASE SHIFT
vs
FREQUENCY



AVAILABLE OPTIONS

T_A	V_{IO} max AT 25°C	PACKAGE						
		SMALL OUTLINE (D)	SSOP (DBLE)	CHIP CARRIER (FK)	CERAMIC DIP (JG)	PLASTIC DIP (P)	TSSOP (PWLE)	CHIP FORM (Y)
0°C to 70°C	300 µV	TLE2022ACD				TLE2022ACP		
	500 µV	TLE2022CD	TLE2022CDBLE			TLE2022CP	TLE2022PWLE	TLE2022Y
– 40°C to 85°C	300 µV	TLE2022AID				TLE2022AIP		
	500 µV	TLE2022ID				TLE2022IP		
– 55°C to 125°C	150 µV				TLE2022BMJG			
	300 µV	TLE2022AMD		TLE2022AMFK	TLE2022AMJG	TLE2022AMP		
	500 µV	TLE2022MD		TLE2022MFK	TLE2022MJG	TLE2022MP		

The D package is available taped and reeled. Add the suffix R, (e.g., TLE2022CDR). The DB and PW packages are only available left-end taped and reeled. Chips are tested at 25°C.

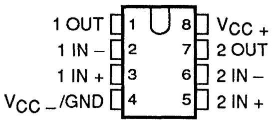
description (continued)

the ideal choice for low-level signal conditioning applications in either single-supply or split-supply configurations. In addition, these devices offer phase-reversal protection circuitry that eliminates an unexpected change in output states when one of the inputs goes below the negative supply rail.

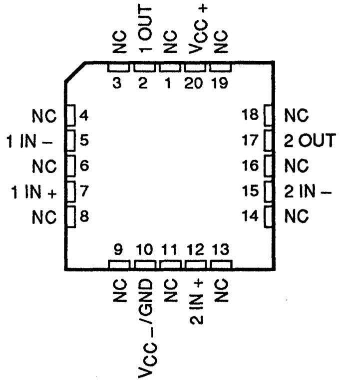
Available packaging options include small-outline and chip-carrier versions for high-density systems applications.

The C-suffix devices are characterized for operation from 0°C to 70°C. The I-suffix devices are characterized for operation from −40°C to 85°C. The M-suffix devices are characterized for operation over the full military temperature range of −55°C to 125°C.

D, DB, JG, P, or PW PACKAGE
(TOP VIEW)



FK PACKAGE
(TOP VIEW)

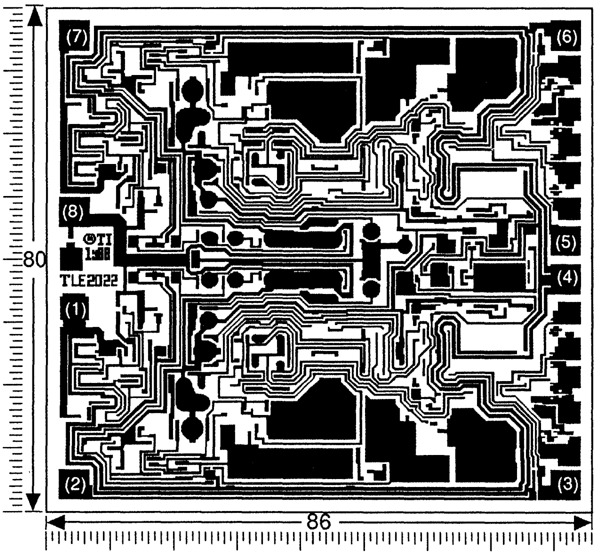


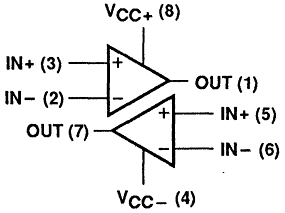
NC – No internal connection

chip information

These chips, properly assembled, display characteristics similar to the TLE2022. Thermal compression or ultrasonic bonding may be used on the doped aluminum bonding pads. Chips may be mounted with conductive epoxy or a gold-silicon preform.

BONDING PAD ASSIGNMENTS





CHIP THICKNESS:
15 TYPICAL

BONDING PADS:
4 X 4 MINIMUM

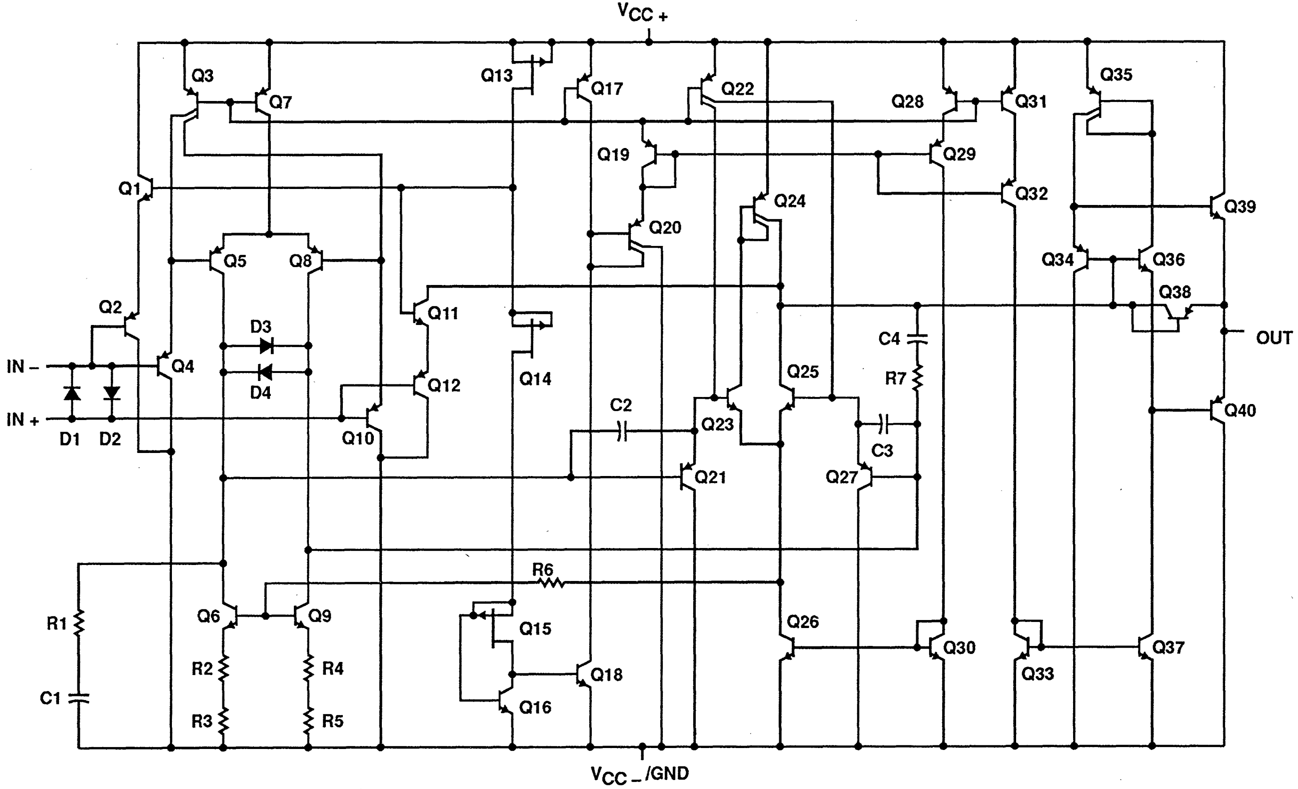
T_J max = 150°C

TOLERANCES
ARE ±10%

ALL DIMENSIONS
ARE IN MILS

PIN (4) INTERNALLY
CONNECTED TO
BACKSIDE OF CHIP

equivalent schematic (each amplifier)



Component count: Diodes — 8
Resistors — 14
Capacitors — 8
Transistors — 80

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC+} (see Note 1)	20 V
Supply voltage, V_{CC-} (see Note 1)	−20 V
Differential input voltage (see Note 2)	±0.6 V
Input voltage range, V_I (any input, see Note1)	$V_{CC\pm}$
Input current, I_I (each input)	±1 mA
Output current, I_O (each output)	±30 mA
Total current into V_{CC+} terminal	80 mA
Total current out of V_{CC-} terminal	80 mA
Duration of short-circuit current at (or below) 25°C (see Note 3)	unlimited
Continuous total dissipation	See Dissipation Rating Table
Operating free-air temperature range, T_A: C-suffix	0°C to 70°C
I-suffix	−40°C to 85°C
M-suffix	−55°C to 125°C
Storage temperature range	−65°C to 150°C
Case temperature for 60 seconds: FK package	260°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D, DB, P, or PW package	260°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: JG package	300°C

NOTES: 1. All voltage values, except differential voltages, are with respect to the midpoint between V_{CC+} and V_{CC-}.
2. Differential voltages are at the noninverting input with respect to the inverting input. Excessive current will flow if a differential input voltage in excess of approximately ± 600 mV is applied between the inputs unless some limiting resistance is used.
3. The output may be shorted to either supply. Temperature and/or supply voltages must be limited to ensure that the maximum dissipation rating is not exceeded.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING	$T_A = 125°C$ POWER RATING
D	725 mW	5.8 mW/°C	464 mW	377 mW	145 mW
DB, PW	525 mW	4.2 mW/°C	336 mW	273 mW	—
FK	1375 mW	11.0 mW/°C	880 mW	715 mW	275 mW
JG	1050 mW	8.4 mW/°C	672 mW	546 mW	210 mW
P	1000 mW	8.0 mW/°C	640 mW	520 mW	200 mW

recommended operating conditions

		C-SUFFIX			I-SUFFIX			M-SUFFIX			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, $V_{CC\pm}$		± 2		± 20	± 2		± 20	± 2		± 20	V
Common-mode input voltage, V_{IC}	$V_{CC} = 5$ V	0		3.5	0		3.2	0		3.2	V
	$V_{CC\pm} = \pm 15$ V	− 15		13.5	− 15		13.2	− 15		13.2	
Operating free-air temperature, T_A		0		70	− 40		85	− 55		125	°C

electrical characteristics at specified free-air temperature, V_{CC} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A†	TLE2022			TLE2022A			TLE2022B			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_{IC} = 0, R_S = 50 Ω	25°C			600			400			250	µV
			Full range			800			550			400	
α_{VIO}	Temperature coefficient of input offset voltage		Full range		2			2			2		µV/°C
	Input offset voltage long-term drift (see Note 4)		25°C		0.005			0.005			0.005		µV/mo
I_{IO}	Input offset current		25°C		0.5	5		0.4	4		0.3	3	nA
			Full range			5			4			3	
I_{IB}	Input bias current		25°C		35	60		33	55		30	50	nA
			Full range			60			55			50	
V_{ICR}	Common-mode input voltage range	R_S = 50 Ω	25°C	0 to 3.5	−0.3 to 4		0 to 3.5	−0.3 to 4		0 to 3.5	−0.3 to 4		V
			Full range	0 to 3.5			0 to 3.5			0 to 3.5			
V_{OH}	High-level output voltage	R_L = 10 kΩ	25°C	4	4.3		4	4.3		4	4.3		V
			Full range	3.9			3.9			3.9			
V_{OL}	Low-level output voltage		25°C		0.7	0.8		0.7	0.8		0.7	0.8	V
			Full range			0.85			0.85			0.85	
A_{VD}	Large-signal differential voltage amplification	V_O = 1.4 V to 4 V, R_L = 10 kΩ	25°C	0.3	1.5		0.4	1.5		0.5	1.5		V/µV
			Full range	0.3			0.4			0.5			
CMRR	Common-mode rejection ratio	V_{IC} = V_{ICR} min, R_S = 50 Ω	25°C	85	100		87	102		90	105		dB
			Full range	80			82			85			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm}/\Delta V_{IO}$)	V_{CC} = 5 V to 30 V	25°C	100	115		103	118		105	120		dB
			Full range	95			98			100			
I_{CC}	Supply current	V_O = 2.5 V, No load	25°C		450	600		450	600		450	600	µA
			Full range			600			600			600	
ΔI_{CC}	Supply current change over operating temperature range		Full range		7			7			7		µA

†Full range is 0°C to 70°C.

NOTE 4: Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at T_A = 150°C extrapolated to T_A = 25°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

electrical characteristics at specified free-air temperature, $V_{CC\pm} = \pm 15$ V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A†	TLE2022			TLE2022A			TLE2022B			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	$V_{IC} = 0$, $R_S = 50\ \Omega$	25°C		150	500		120	300		70	150	µV
			Full range			700			450			300	
α_{VIO}	Temperature coefficient of input offset voltage		Full range		2			2			2		µV/°C
	Input offset voltage long-term drift (see Note 4)		25°C		0.006			0.006			0.006		µV/mo
I_{IO}	Input offset current		25°C		0.5	5		0.4	4		0.3	3	nA
			Full range			5			4			3	
I_{IB}	Input bias current		25°C		35	60		33	55		30	50	nA
			Full range			60			55			50	
V_{ICR}	Common-mode input voltage range	$R_S = 50\ \Omega$	25°C	− 15 to 13.5	− 15.3 to 14		− 15 to 13.5	− 15.3 to 14		− 15 to 13.5	− 15.3 to 14		V
			Full range	− 15 to 13.5			− 15 to 13.5			− 15 to 13.5			
V_{OM+}	Maximum positive peak output voltage swing	$R_L = 10\ k\Omega$	25°C	14	14.3		14	14.3		14	14.3		V
			Full range	13.9			13.9			13.9			
V_{OM-}	Maximum negative peak output voltage swing		25°C	− 13.7	− 14.1		− 13.7	− 14.1		− 13.7	− 14.1		V
			Full range	− 13.7			− 13.7			− 13.7			
A_{VD}	Large-signal differential voltage amplification	$V_O = \pm 10$ V, $R_L = 10\ k\Omega$	25°C	0.8	4		1	7		1.5	10		V/µV
			Full range	0.8			1			1.5			
CMRR	Common-mode rejection ratio	$V_{IC} = V_{ICR}$ min, $R_S = 50\ \Omega$	25°C	95	106		97	109		100	112		dB
			Full range	91			93			96			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm} / \Delta V_{IO}$)	$V_{CC\pm} = \pm 2.5$ V to ± 15 V	25°C	100	115		103	118		105	120		dB
			Full range	95			98			100			
I_{CC}	Supply current	$V_O = 0$, No load	25°C		550	700		550	700		550	700	µA
			Full range			700			700			700	
ΔI_{CC}	Supply current change over operating temperature range		Full range		9			9			9		µA

†Full range is 0°C to 70°C.

NOTE 4: Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at $T_A = 150$°C extrapolated to $T_A = 25$°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

operating characteristics at specified free-air temperature, V_{CC} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A	TLE2022			TLE2022A			TLE2022B			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
SR	Slew rate at unity gain	V_O = 1 V to 3 V, See Figure 1	25°C		0.5			0.5			0.5		V/μs
V_n	Equivalent input noise voltage (see Figure 2)	f = 10 Hz	25°C		21	50		21	50		21	50	nV/√Hz
		f = 1 kHz	25°C		17	30		17	30		17	30	
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 to 1 Hz	25°C		0.16			0.16			0.16		μV
		f = 0.1 to 10 Hz	25°C		0.47			0.47			0.47		
I_n	Equivalent input noise current		25°C		0.1			0.1			0.1		pA/√Hz
B_1	Unity-gain bandwidth	See Figure 3	25°C		1.7			1.7			1.7		MHz
ϕ_m	Phase margin at unity gain	See Figure 3	25°C		47°			47°			47°		

operating characteristics at specified free-air temperature, $V_{CC\pm}$ = ± 15 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A†	TLE2022			TLE2022A			TLE2022B			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
SR	Slew rate at unity gain	V_O = ± 10 V, See Figure 1	25°C	0.45	0.65		0.45	0.65		0.45	0.65		V/μs
			Full range	0.45			0.45			0.45			
V_n	Equivalent input noise voltage (see Figure 2)	f = 10 Hz	25°C		19	50		19	50		19	50	nV/√Hz
		f = 1 kHz	25°C		15	30		15	30		15	30	
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 to 1 Hz	25°C		0.16			0.16			0.16		μV
		f = 0.1 to 10 Hz	25°C		0.47			0.47			0.47		
I_n	Equivalent input noise current		25°C		0.1			0.1			0.1		pA/√Hz
B_1	Unity-gain bandwidth	See Figure 3	25°C		2.8			2.8			2.8		MHz
ϕ_m	Phase margin at unity gain	See Figure 3	25°C		52°			52°			52°		

†Full range is 0°C to 70°C.

electrical characteristics at specified free-air temperature, V_{CC} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A†	TLE2022			TLE2022A			TLE2022B			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_{IC} = 0, R_S = 50 Ω	25°C			600			400			250	µV
			Full range			800			550			400	
α_{VIO}	Temperature coefficient of input offset voltage		Full range		2			2			2		µV/°C
	Input offset voltage long-term drift (see Note 4)		25°C		0.005			0.005			0.005		µV/mo
I_{IO}	Input offset current		25°C		0.5	5		0.4	4		0.3	3	nA
			Full range			5			4			3	
I_{IB}	Input bias current		25°C		35	60		33	55		30	50	nA
			Full range			60			55			50	
V_{ICR}	Common-mode input voltage range	R_S = 50 Ω	25°C	0 to 3.5	−0.3 to 4		0 to 3.5	−0.3 to 4		0 to 3.5	−0.3 to 4		V
			Full range	0 to 3.2			0 to 3.2			0 to 3.2			
V_{OH}	High-level output voltage	R_L = 10 kΩ	25°C	4	4.3		4	4.3		4	4.3		V
			Full range	3.9			3.9			3.9			
V_{OL}	Low-level output voltage		25°C		0.7	0.8		0.7	0.8		0.7	0.8	V
			Full range			0.9			0.9			0.9	
A_{VD}	Large-signal differential voltage amplification	V_O = 1.4 V to 4 V, R_L = 10 kΩ	25°C	0.3	1.5		0.4	1.5		0.5	1.5		V/µV
			Full range	0.2			0.2			0.2			
CMRR	Common-mode rejection ratio	$V_{IC} = V_{ICR}$ min, R_S = 50 Ω	25°C	85	100		87	102		90	105		dB
			Full range	80			82			85			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm} / \Delta V_{IO}$)	V_{CC} = 5 V to 30 V	25°C	100	115		103	118		105	120		dB
			Full range	95			98			100			
I_{CC}	Supply current	V_O = 2.5 V, No load	25°C		450	600		450	600		450	600	µA
			Full range			600			600			600	
ΔI_{CC}	Supply current change over operating temperature range		Full range		15			15			15		µA

†Full range is − 40°C to 85°C.

NOTE 4: Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at T_A = 150°C extrapolated to T_A = 25°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

electrical characteristics at specified free-air temperature, $V_{CC\pm} = \pm 15$ V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A†	TLE2022			TLE2022A			TLE2022B			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	$V_{IC} = 0$, $R_S = 50\ \Omega$	25°C		150	500		120	300		70	150	μV
			Full range			700			450			300	
α_{VIO}	Temperature coefficient of input offset voltage		Full range		2			2			2		μV/°C
	Input offset voltage long-term drift (see Note 4)		25°C		0.006			0.006			0.006		μV/mo
I_{IO}	Input offset current		25°C		0.5	5		0.4	4		0.3	3	nA
			Full range			5			4			3	
I_{IB}	Input bias current		25°C		35	60		33	55		30	50	nA
			Full range			60			55			50	
V_{ICR}	Common-mode input voltage range	$R_S = 50\ \Omega$	25°C	−15 to 13.5	−15.3 to 14		−15 to 13.5	−15.3 to 14		−15 to 13.5	−15.3 to 14		V
			Full range	−15 to 13.2			−15 to 13.2			−15 to 13.2			
V_{OM+}	Maximum positive peak output voltage swing	$R_L = 10\ k\Omega$	25°C	14	14.3		14	14.3		14	14.3		V
			Full range	13.9			13.9			13.9			
V_{OM-}	Maximum negative peak output voltage swing		25°C	−13.7	−14.1		−13.7	−14.1		−13.7	−14.1		V
			Full range	−13.6			−13.6			−13.6			
A_{VD}	Large-signal differential voltage amplification	$V_O = \pm 10$ V, $R_L = 10\ k\Omega$	25°C	0.8	4		1	7		1.5	10		V/μV
			Full range	0.8			1			1.5			
CMRR	Common-mode rejection ratio	$V_{IC} = V_{ICR}$ min, $R_S = 50\ \Omega$	25°C	95	106		97	109		100	112		dB
			Full range	91			93			96			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm} / \Delta V_{IO}$)	$V_{CC\pm} = \pm 2.5$ V to ± 15 V	25°C	100	115		103	118		105	120		dB
			Full range	95			98			100			
I_{CC}	Supply current	$V_O = 0$, No load	25°C		550	700		550	700		550	700	μA
			Full range			700			700			700	
ΔI_{CC}	Supply current change over operating temperature range		Full range		30			30			30		μA

†Full range is − 40°C to 85°C.

NOTE 4: Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at $T_A = 150°C$ extrapolated to $T_A = 25°C$ using the Arrhenius equation and assuming an activation energy of 0.96 eV.

operating characteristics at specified free-air temperature, V_{CC} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A	TLE2022			TLE2022A			TLE2022B			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
SR	Slew rate at unity gain	V_O = 1 V to 3 V, See Figure 1	25°C		0.5			0.5			0.5		V/µs
V_n	Equivalent input noise voltage (see Figure 2)	f = 10 Hz	25°C		21	50		21	50		21	50	nV/√Hz
		f = 1 kHz	25°C		17	30		17	30		17	30	
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 to 1 Hz	25°C		0.16			0.16			0.16		µV
		f = 0.1 to 10 Hz	25°C		0.47			0.47			0.47		
I_n	Equivalent input noise current		25°C		0.1			0.1			0.1		pA/√Hz
B_1	Unity-gain bandwidth	See Figure 3	25°C		1.7			1.7			1.7		MHz
ϕ_m	Phase margin at unity gain	See Figure 3	25°C		47°			47°			47°		

operating characteristics at specified free-air temperature, $V_{CC\pm}$ = ± 15 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A†	TLE2022			TLE2022A			TLE2022B			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
SR	Slew rate at unity gain	V_O = ± 10 V, See Figure 1	25°C	0.45	0.65		0.45	0.65		0.45	0.65		V/µs
			Full range	0.42			0.42			0.42			
V_n	Equivalent input noise voltage (see Figure 2)	f = 10 Hz	25°C		19	50		19	50		19	50	nV/√Hz
		f = 1 kHz	25°C		15	30		15	30		15	30	
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 to 1 Hz	25°C		0.16			0.16			0.16		µV
		f = 0.1 to 10 Hz	25°C		0.47			0.47			0.47		
I_n	Equivalent input noise current		25°C		0.1			0.1			0.1		pA/√Hz
B_1	Unity-gain bandwidth	See Figure 3	25°C		2.8			2.8			2.8		MHz
ϕ_m	Phase margin at unity gain	See Figure 3	25°C		52°			52°			52°		

†Full range is – 40°C to 85°C.

electrical characteristics at specified free-air temperature, V_{CC} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A†	TLE2022			TLE2022A			TLE2022B			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_{IC} = 0, R_S = 50 Ω	25°C			600			400			250	µV
			Full range			800			550			400	
α_{VIO}	Temperature coefficient of input offset voltage		Full range		2			2			2		µV/°C
	Input offset voltage long-term drift (see Note 4)		25°C		0.005			0.005			0.005		µV/mo
I_{IO}	Input offset current		25°C		0.5	5		0.4	4		0.3	3	nA
			Full range			5			4			3	
I_{IB}	Input bias current		25°C		35	60		33	55		30	50	nA
			Full range			60			55			50	
V_{ICR}	Common-mode input voltage range	R_S = 50 Ω	25°C	0 to 3.5	−0.3 to 4		0 to 3.5	−0.3 to 4		0 to 3.5	−0.3 to 4		V
			Full range	0 to 3.2			0 to 3.2			0 to 3.2			
V_{OH}	High-level output voltage	R_L = 10 kΩ	25°C	4	4.3		4	4.3		4	4.3		V
			Full range	3.8			3.8			3.8			
V_{OL}	Low-level output voltage		25°C		0.7	0.8		0.7	0.8		0.7	0.8	V
			Full range			0.95			0.95			0.95	
A_{VD}	Large-signal differential voltage amplification	V_O = 1.4 V to 4 V, R_L = 10 kΩ	25°C	0.3	1.5		0.4	1.5		0.5	1.5		V/µV
			Full range	0.1			0.1			0.1			
CMRR	Common-mode rejection ratio	V_{IC} = V_{ICR} min, R_S = 50 Ω	25°C	85	100		87	102		90	105		dB
			Full range	80			82			85			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm}/\Delta V_{IO}$)	V_{CC} = 5 V to 30 V	25°C	100	115		103	118		105	120		dB
			Full range	95			98			100			
I_{CC}	Supply current	V_O = 2.5 V, No load	25°C		450	600		450	600		450	600	µA
			Full range			600			600			600	
ΔI_{CC}	Supply current change over operating temperature range		Full range		37			37			37		µA

†Full range is − 55°C to 125°C.

NOTE 4: Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at T_A = 150°C extrapolated to T_A = 25°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

electrical characteristics at specified free-air temperature, $V_{CC\pm} = \pm 15$ V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A†	TLE2022			TLE2022A			TLE2022B			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	$V_{IC} = 0$, $R_S = 50\ \Omega$	25°C		150	500		120	300		70	150	μV
			Full range			700			450			300	
α_{VIO}	Temperature coefficient of input offset voltage		Full range		2			2			2		μV/°C
	Input offset voltage long-term drift (see Note 4)		25°C		0.006			0.006			0.006		μV/mo
I_{IO}	Input offset current		25°C		0.5	5		0.4	4		0.3	3	nA
			Full range			5			4			3	
I_{IB}	Input bias current		25°C		35	60		33	55		30	50	nA
			Full range			60			55			50	
V_{ICR}	Common-mode input voltage range	$R_S = 50\ \Omega$	25°C	− 15 to 13.5	− 15.3 to 14		− 15 to 13.5	− 15.3 to 14		− 15 to 13.5	− 15.3 to 14		V
			Full range	− 15 to 13.2			− 15 to 13.2			− 15 to 13.2			
V_{OM+}	Maximum positive peak output voltage swing	$R_L = 10\ k\Omega$	25°C	14	14.3		14	14.3		14	14.3		V
			Full range	13.9			13.9			13.9			
V_{OM-}	Maximum negative peak output voltage swing		25°C	− 13.7	− 14.1		− 13.7	− 14.1		− 13.7	− 14.1		V
			Full range	− 13.6			− 13.6			− 13.6			
A_{VD}	Large-signal differential voltage amplification	$V_O = \pm 10$ V, $R_L = 10\ k\Omega$	25°C	0.8	4		1	7		1.5	10		V/μV
			Full range	0.8			1			1.5			
CMRR	Common-mode rejection ratio	$V_{IC} = V_{ICR}$ min, $R_S = 50\ \Omega$	25°C	95	106		97	109		100	112		dB
			Full range	91			93			96			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm} / \Delta V_{IO}$)	$V_{CC\pm} = \pm 2.5$ V to ± 15 V	25°C	100	115		103	118		105	120		dB
			Full range	95			98			100			
I_{CC}	Supply current	$V_O = 0$, No load	25°C		550	700		550	700		550	700	μA
			Full range			700			700			700	
ΔI_{CC}	Supply current change over operating temperature range		Full range		60			60			60		μA

†Full range is – 55°C to 125°C.

NOTE 4: Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at $T_A = 150°C$ extrapolated to $T_A = 25°C$ using the Arrhenius equation and assuming an activation energy of 0.96 eV.

operating characteristics at specified free-air temperature, V_{CC} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A	TLE2022			TLE2022A			TLE2022B			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
SR	Slew rate at unity gain	V_O = 1 V to 3 V, See Figure 1	25°C		0.5			0.5			0.5		V/μs
V_n	Equivalent input noise voltage (see Figure 2)	f = 10 Hz	25°C		21			21			21		$\mathrm{nV}/\sqrt{\mathrm{Hz}}$
		f = 1 kHz	25°C		17			17			17		
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 to 1 Hz	25°C		0.16			0.16			0.16		μV
		f = 0.1 to 10 Hz	25°C		0.47			0.47			0.47		
I_n	Equivalent input noise current		25°C		0.1			0.1			0.1		$\mathrm{pA}/\sqrt{\mathrm{Hz}}$
B_1	Unity-gain bandwidth	See Figure 3	25°C		1.7			1.7			1.7		MHz
ϕ_m	Phase margin at unity gain	See Figure 3	25°C		47°			47°			47°		

operating characteristics at specified free-air temperature, $V_{CC\pm}$ = ± 15 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A†	TLE2022			TLE2022A			TLE2022B			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
SR	Slew rate at unity gain	V_O = ± 10 V, See Figure 1	25°C	0.45	0.65		0.45	0.65		0.45	0.65		V/μs
			Full range	0.4			0.4			0.4			
V_n	Equivalent input noise voltage (see Figure 2)	f = 10 Hz	25°C		19			19			19		$\mathrm{nV}/\sqrt{\mathrm{Hz}}$
		f = 1 kHz	25°C		15			15			15		
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 to 1 Hz	25°C		0.16			0.16			0.16		μV
		f = 0.1 to 10 Hz	25°C		0.47			0.47			0.47		
I_n	Equivalent input noise current		25°C		0.1			0.1			0.1		$\mathrm{pA}/\sqrt{\mathrm{Hz}}$
B_1	Unity-gain bandwidth	See Figure 3	25°C		2.8			2.8			2.8		MHz
ϕ_m	Phase margin at unity gain	See Figure 3	25°C		52°			52°			52°		

†Full range is – 55°C to 125°C.

electrical characteristics at V_{CC} = 5 V, T_A = 25°C, (unless otherwise noted)

PARAMETER		TEST CONDITIONS	TLE2022Y			UNIT
			MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_{IC} = 0, R_S = 50 Ω		150	600	μV
	Input offset voltage long-term drift (see Note 4)			0.005		μV/mo
I_{IO}	Input offset current			0.5	5	nA
I_{IB}	Input bias current			35	60	nA
V_{ICR}	Common-mode input voltage range	R_S = 50 Ω	0 to 3.5	−0.3 to 4		V
V_{OH}	Maximum high-level output voltage	R_L = 10 kΩ	4	4.3		V
V_{OL}	Maximum low-level output voltage			0.7	0.8	V
A_{VD}	Large-signal differential voltage amplification	V_O = 1.4 V to 4 V, R_L = 10 kΩ	0.3	1.5		V/μV
CMRR	Common-mode rejection ratio	V_{IC} = V_{ICR}min, R_S = 50 Ω	85	100		dB
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm}/\Delta V_{IO}$)	V_{CC} = 5 V to 30 V	100	115		dB
I_{CC}	Supply current	V_O = 2.5 V, No load		450	600	μA

NOTE: 4. Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at T_A = 150°C extrapolated to T_A = 25°C using the Arrhenius equation and assuming and activation energy of 0.96 eV.

operating characteristics at V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain	V_O = 1 V to 3 V, See Figure 1		0.5		V/μs
V_n	Equivalent input noise voltage (see Figure 2)	f = 10 Hz		21	50	nV/√Hz
		f = 1 kHz		17	30	
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 to 1 Hz		0.16		μV
		f = 0.1 to 10 Hz		0.47		
I_n	Equivalent input noise current			0.1		pA/√Hz
B_1	Unity gain-bandwidth	See Figure 3		1.7		MHz
ϕ_m	Phase margin at unity gain	See Figure 3		47°		

PARAMETER MEASUREMENT INFORMATION

NOTE A: C_L includes fixture capacitance.

(a) SINGLE-SUPPLY

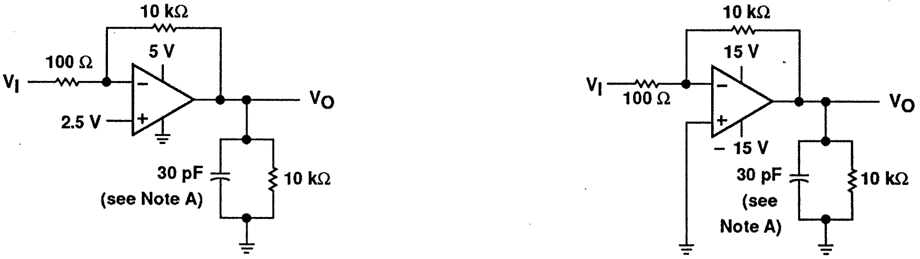
(b) SPLIT-SUPPLY

Figure 1. Slew Rate Test Circuit

(a) SINGLE-SUPPLY

(b) SPLIT-SUPPLY

Figure 2. Noise Voltage Test Circuit



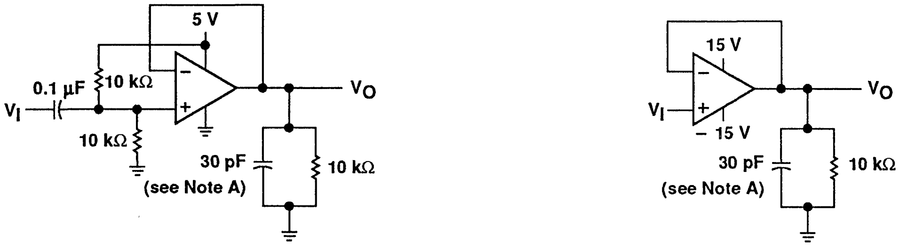
NOTE A: C_L includes fixture capacitance.

(a) SINGLE-SUPPLY

(b) SPLIT-SUPPLY

Figure 3. Unity-Gain Bandwidth and Phase Margin Test Circuit

PARAMETER MEASUREMENT INFORMATION



NOTE A: C_L includes fixture capacitance.

(a) SINGLE-SUPPLY

(b) SPLIT-SUPPLY

Figure 4. Small-Signal Pulse Response Test Circuit

typical values

Typical values as presented in this data sheet represent the median (50% point) of device parametric performance.

TYPICAL CHARACTERISTICS

table of graphs

			FIGURE
V_{IO}	Input offset voltage	Distribution	5
I_{IB}	Input bias current	vs Common-mode voltage	6
		vs Temperature	7
I_I	Input current	vs Differential input voltage	8
V_{OM}	Maximum peak output voltage	vs Output current	9
		vs Temperature	10
V_{OH}	High-level output voltage	vs High-level output current	11
		vs Temperature	12
V_{OL}	Low-level output voltage	vs Low-level output current	13
		vs Temperature	14
$V_{O(PP)}$	Maximum peak-to-peak output voltage swing	vs Frequency	15, 16
A_{VD}	Differential voltage amplification	vs Frequency	17
		vs Temperature	18
I_{OS}	Short-circuit output current	vs Supply voltage	19, 21
		vs Temperature	20, 22
I_{CC}	Supply current	vs Supply voltage	23
		vs Temperature	24
CMRR	Common-mode rejection ratio	vs Frequency	25
SR	Slew rate	vs Temperature	26
	Pulse response	Small-signal	27, 28
		Large-signal	29, 30
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	0.1 to 1 Hz	31
		0.1 to 10 Hz	32
V_n	Equivalent input noise voltage	vs Frequency	33
B_1	Unity-gain bandwidth	vs Supply voltage	34
		vs Temperature	35
ϕ_m	Phase margin	vs Supply voltage	36
		vs Capacitive load	37
		vs Temperature	38
	Phase shift	vs Frequency	17

TYPICAL CHARACTERISTICS†

TLE2022
DISTRIBUTION OF
INPUT OFFSET VOLTAGE

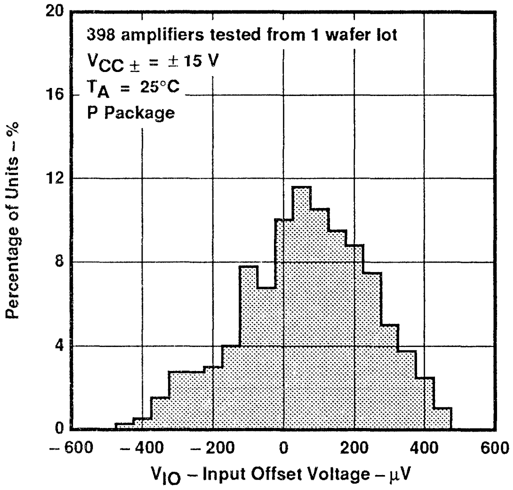


Figure 5

TLE2022
INPUT BIAS CURRENT
vs
COMMON-MODE INPUT VOLTAGE

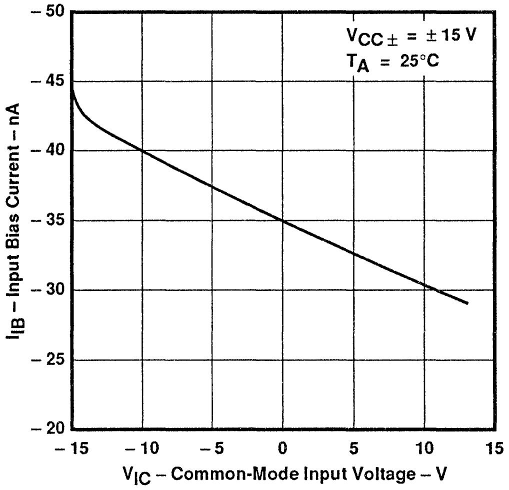


Figure 6

TLE2022
INPUT BIAS CURRENT
vs
FREE-AIR TEMPERATURE

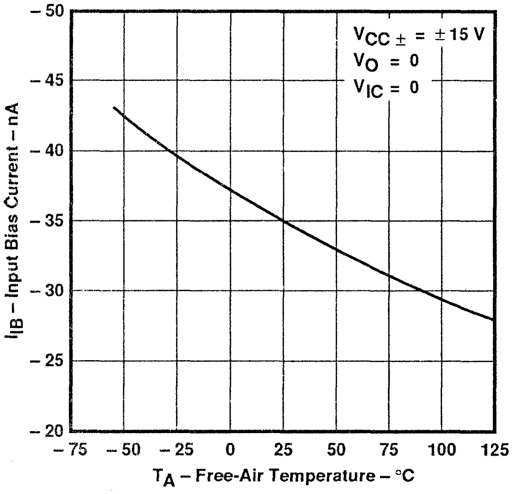


Figure 7

INPUT CURRENT
vs
DIFFERENTIAL INPUT VOLTAGE

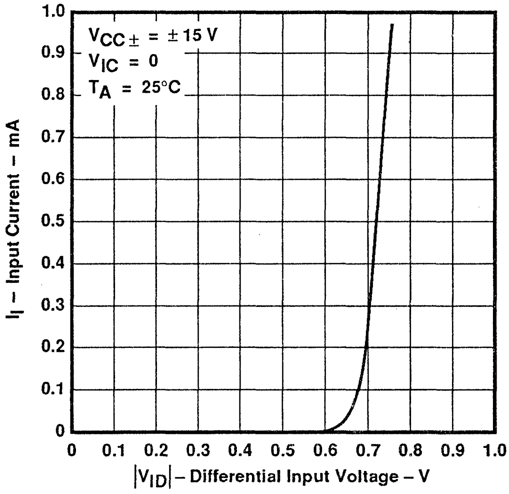


Figure 8

---

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

MAXIMUM PEAK OUTPUT VOLTAGE
vs
OUTPUT CURRENT

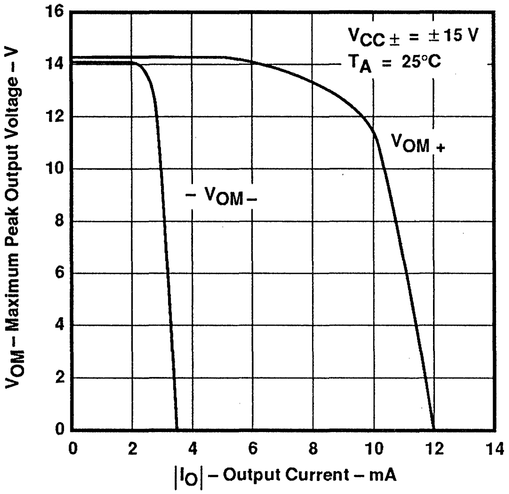


Figure 9

MAXIMUM PEAK OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

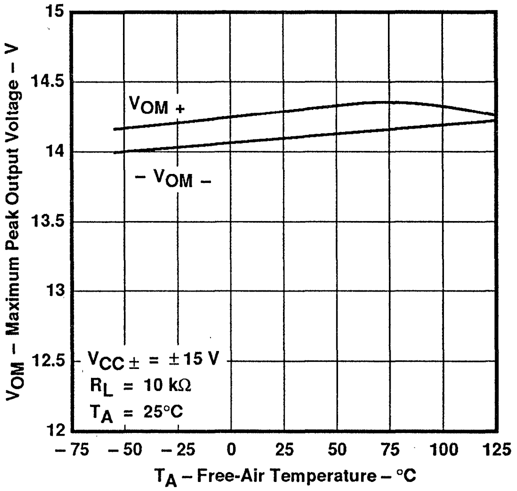


Figure 10

HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

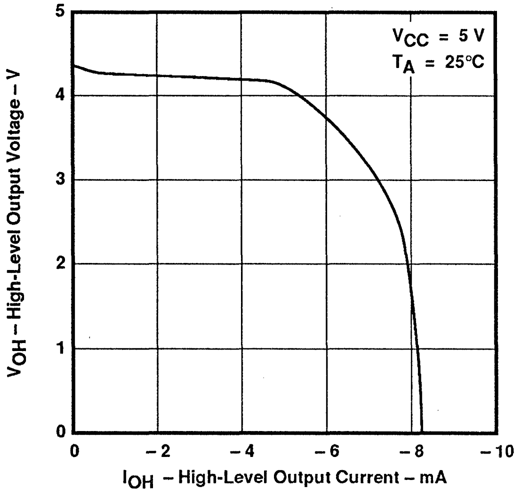


Figure 11

HIGH-LEVEL OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

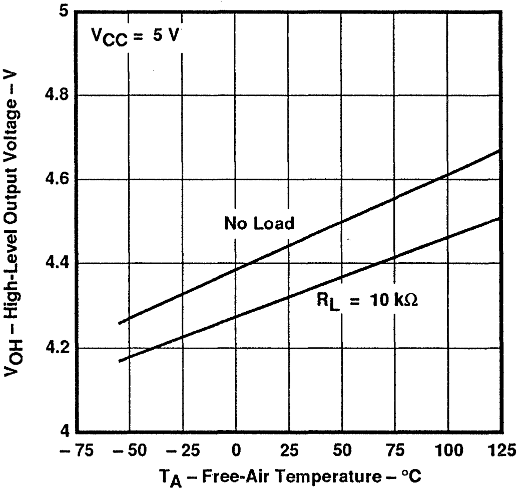


Figure 12

---

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

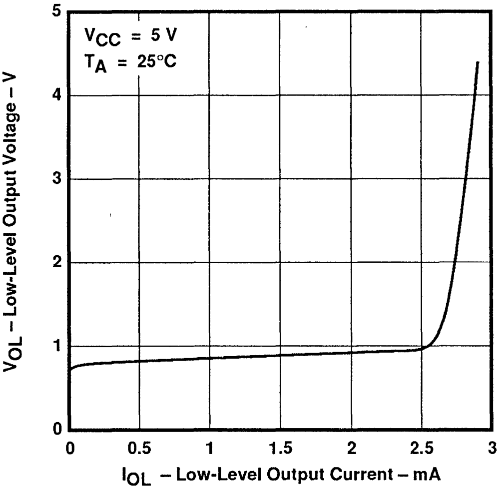


Figure 13

LOW-LEVEL OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

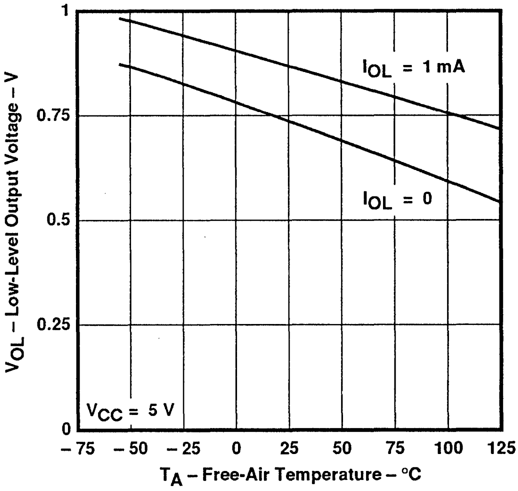


Figure 14

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE
vs
FREQUENCY

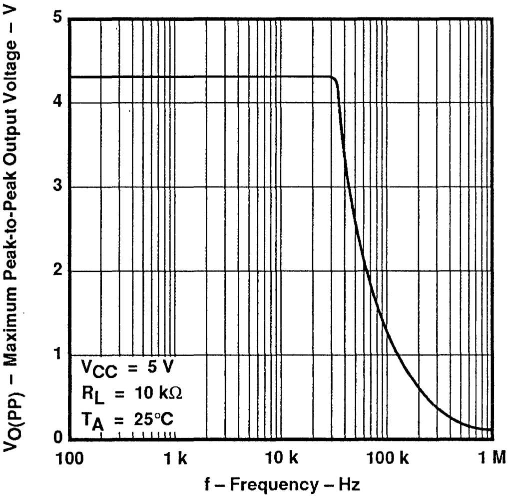


Figure 15

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE
vs
FREQUENCY

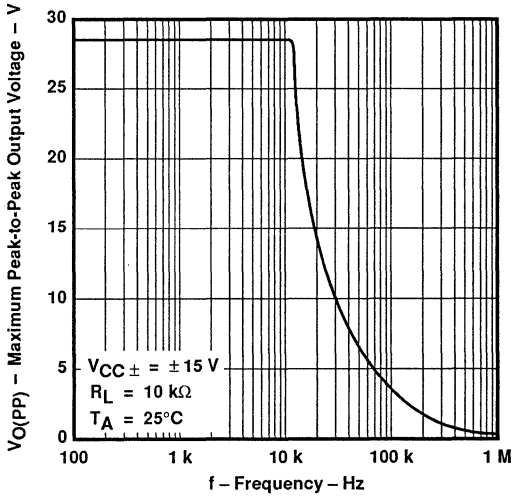


Figure 16

---

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

TLE2022
LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION and PHASE SHIFT
vs
FREQUENCY

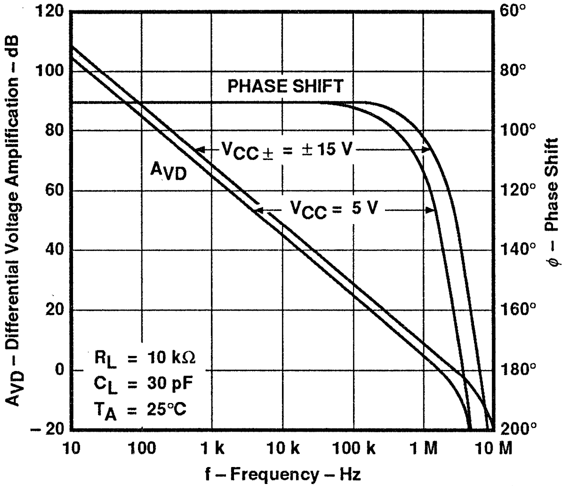


Figure 17

TLE2022
LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION
vs
FREE-AIR TEMPERATURE

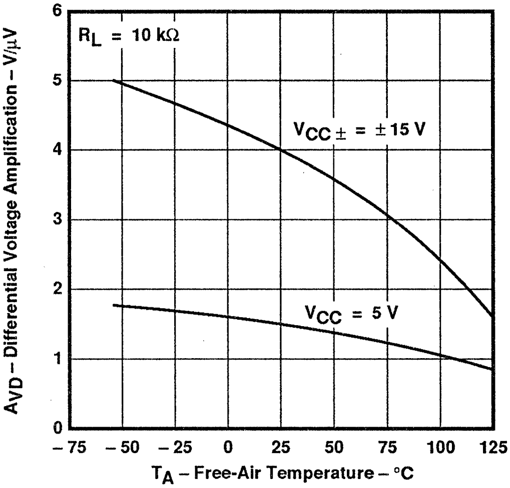


Figure 18

SHORT-CIRCUIT OUTPUT CURRENT
vs
SUPPLY VOLTAGE

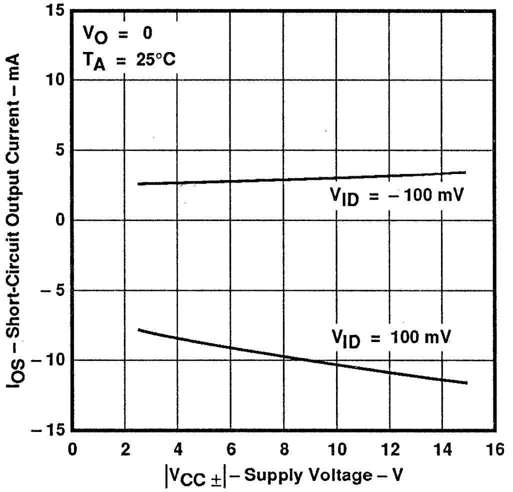


Figure 19

SHORT-CIRCUIT OUTPUT CURRENT
vs
FREE-AIR TEMPERATURE

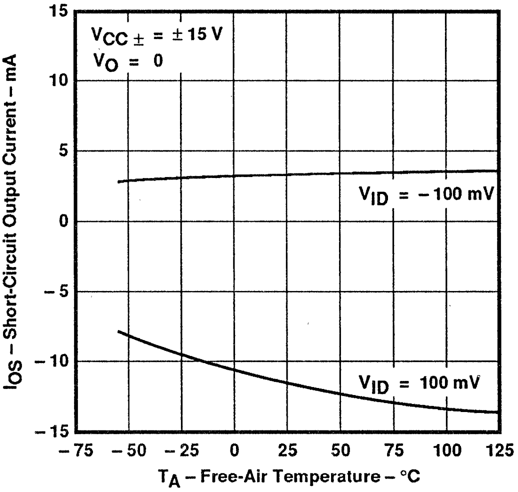


Figure 20

---

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

SHORT-CIRCUIT OUTPUT CURRENT
vs
SUPPLY VOLTAGE

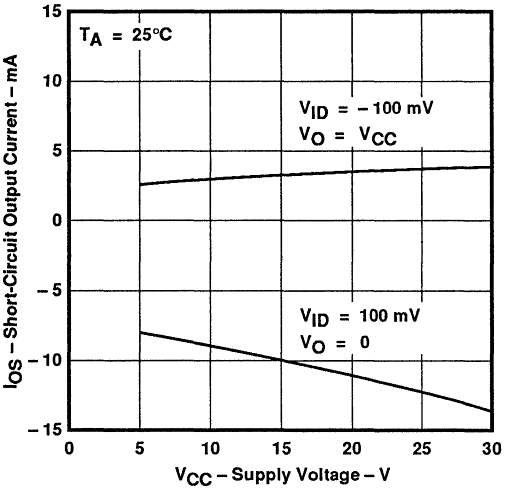


Figure 21

SHORT-CIRCUIT OUTPUT CURRENT
vs
FREE-AIR TEMPERATURE

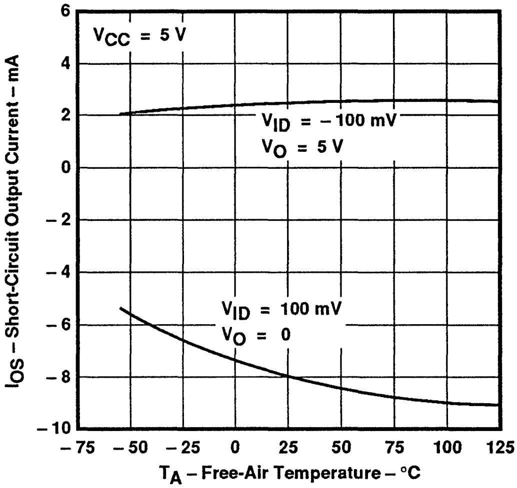


Figure 22

SUPPLY CURRENT
vs
SUPPLY VOLTAGE

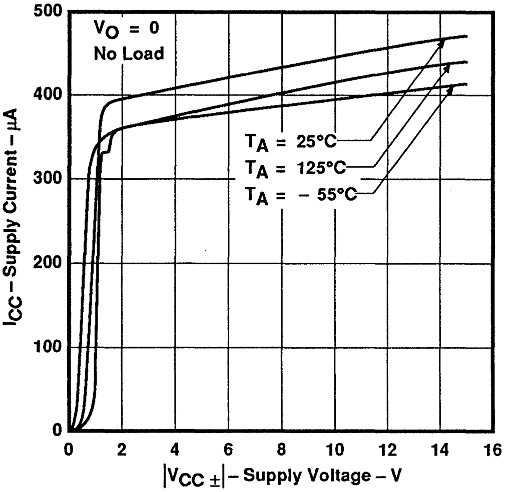


Figure 23

SUPPLY CURRENT
vs
FREE-AIR TEMPERATURE

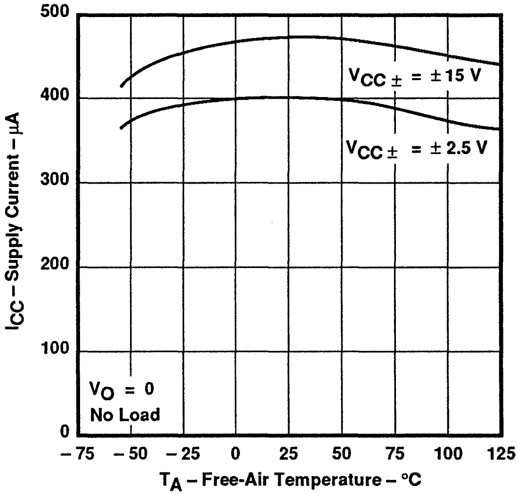


Figure 24

---

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

TLE2022
COMMON-MODE REJECTION RATIO vs FREQUENCY

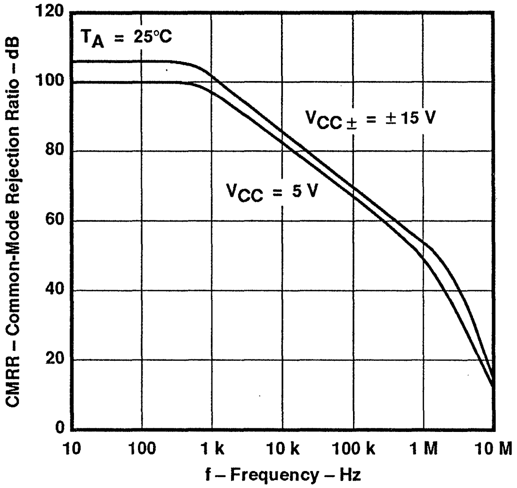


Figure 25

SLEW RATE vs FREE-AIR TEMPERATURE

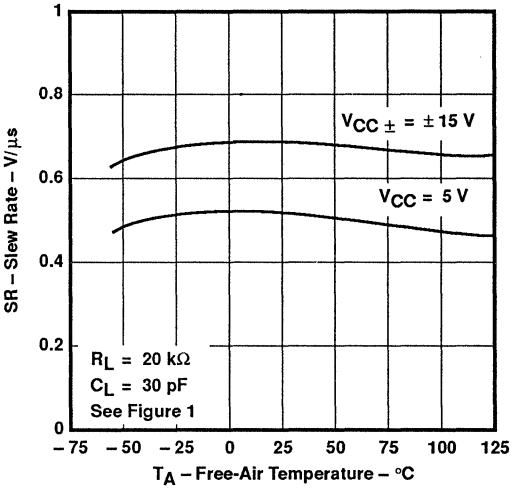


Figure 26

VOLTAGE-FOLLOWER SMALL-SIGNAL PULSE RESPONSE

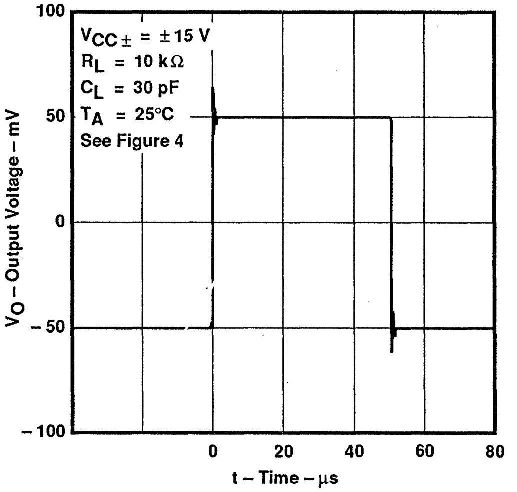


Figure 27

VOLTAGE-FOLLOWER SMALL-SIGNAL PULSE RESPONSE

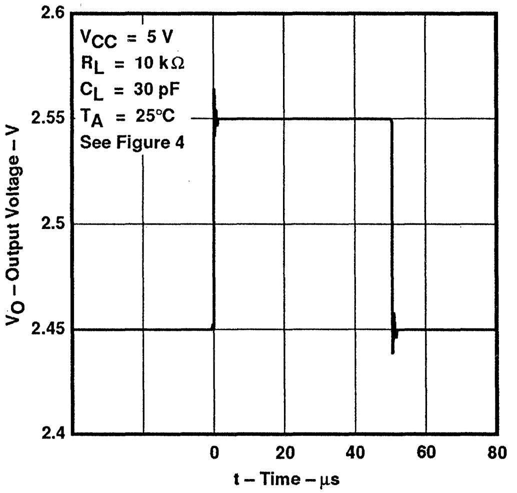


Figure 28

---

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS

VOLTAGE-FOLLOWER
LARGE-SIGNAL
PULSE RESPONSE

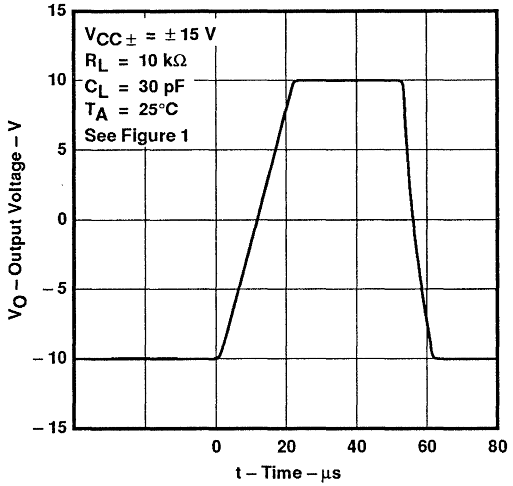


Figure 29

VOLTAGE-FOLLOWER
LARGE-SIGNAL
PULSE RESPONSE

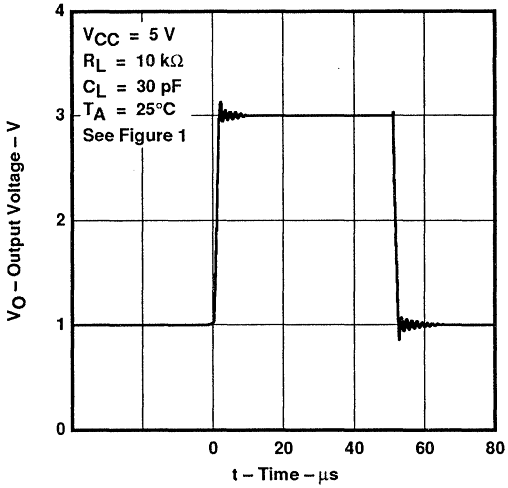


Figure 30

PEAK-TO-PEAK EQUIVALENT
INPUT NOISE VOLTAGE
0.1 TO 1 Hz

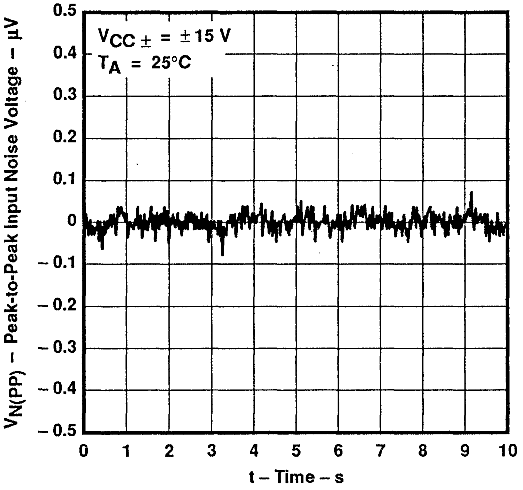


Figure 31

PEAK-TO-PEAK EQUIVALENT
INPUT NOISE VOLTAGE
0.1 TO 10 Hz

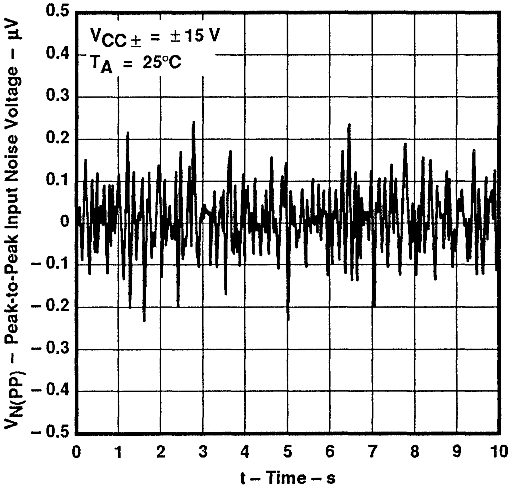


Figure 32

TYPICAL CHARACTERISTICS†

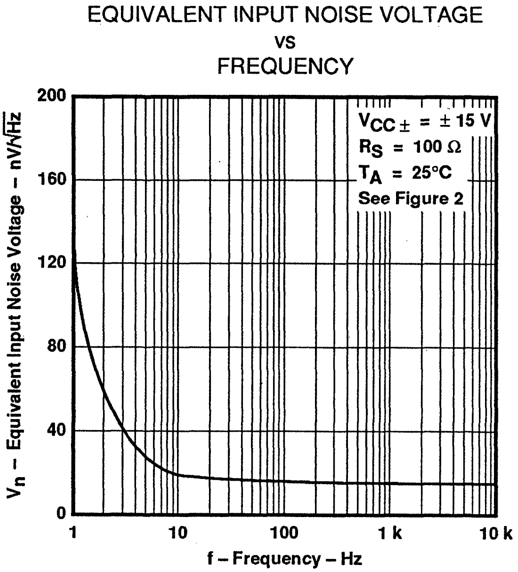


Figure 33

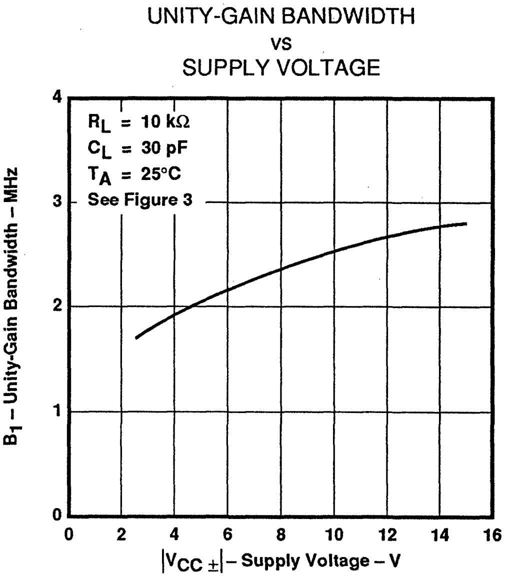


Figure 34

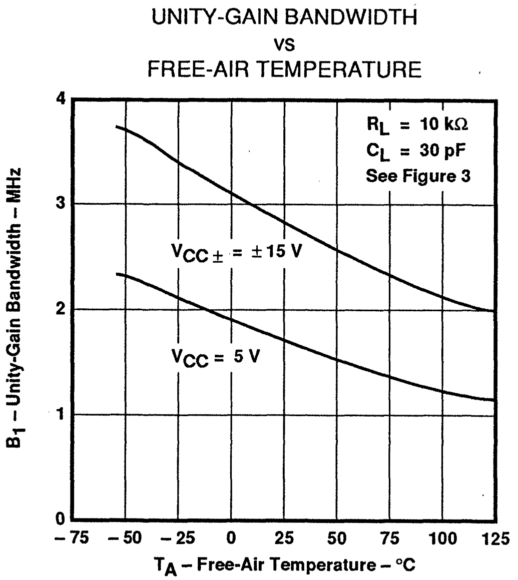


Figure 35

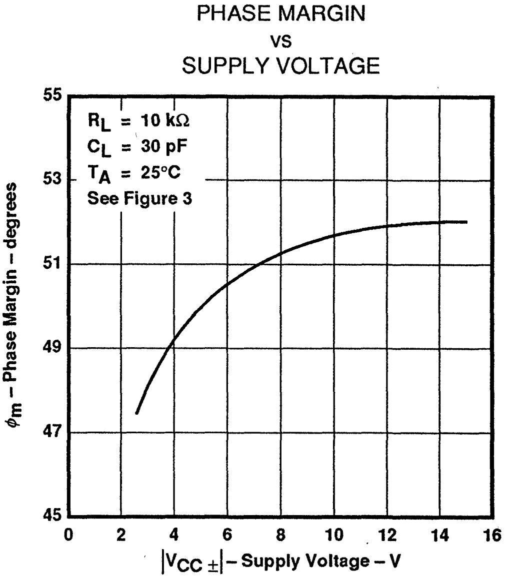


Figure 36

---

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

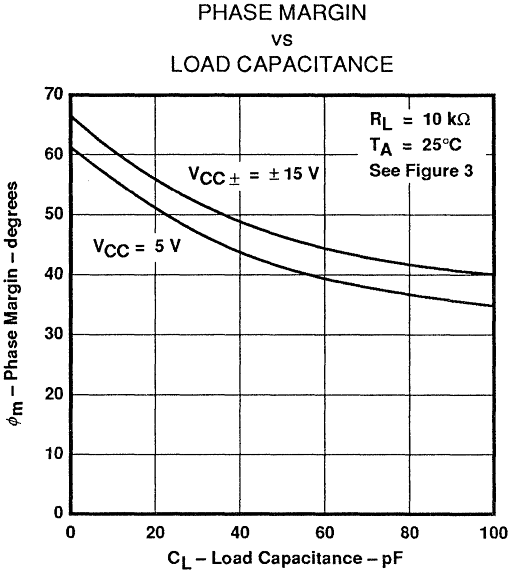


Figure 37

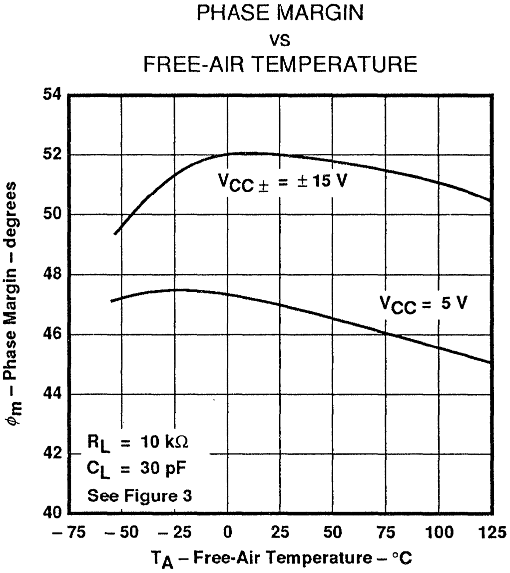


Figure 38

---

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

APPLICATION INFORMATION

voltage-follower applications

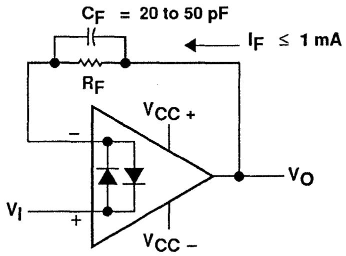


Figure 39. Voltage Follower

The TLE2022 circuitry includes input protection diodes to limit the voltage across the input transistors; however, no provision is made in the circuit to limit the current if these diodes are forward-biased. Note that this condition can occur when the device is operated in the voltage-follower configuration and driven with a fast, large-signal pulse. It is recommended that a feedback resistor be used to limit the current to a maximum of 1 mA to prevent degradation of the device. Also, remember that this feedback resistor will form a pole with the input capacitance of the device. For feedback resistor values greater than 10 kΩ, this pole will degrade the amplifier's phase margin. This problem can be alleviated by adding a capacitor (20 pF to 50 pF) in parallel with the feedback resistor (see Figure 39).

input characteristics

The input of any unused amplifiers should be tied to ground to avoid possible oscillation.

TLE2024, TLE2024A, TLE2024B, TLE2024Y EXCALIBUR HIGH-SPEED LOW-POWER PRECISION QUAD OPERATIONAL AMPLIFIERS

D3265, MAY 1989 – REVISED OCTOBER 1991

available features

- Supply Current . . . 1 mA Max
- High Unity-Gain Bandwidth . . . 2.8 MHz Typ
- High Slew Rate . . . 0.45 V/µs Min
- Supply Current Change Over Military Temp Range . . . 50 µA Typ
- Specified for Both 5 V/Gnd and ± 15 V Operation
- Phase-Reversal Protection
- High Open-Loop Gain . . . 7 V/µV (137 dB) Typ
- Low Offset Voltage . . . 500 µV Max
- Offset Voltage Drift With Time 0.005 µV/mo Typ
- Low Input Bias Current . . . 50 nA Max
- Low Noise Voltage . . . 19 nV/√Hz Typ at f = 10 Hz

description

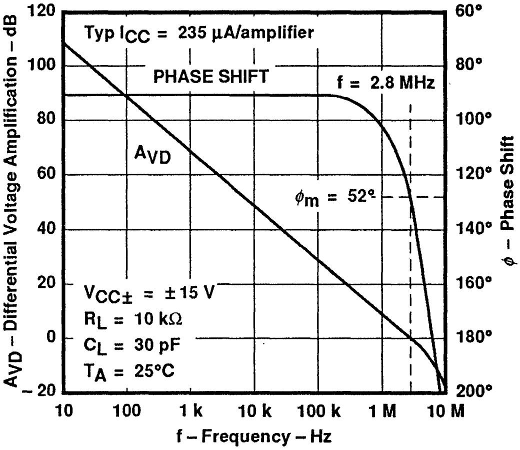
The TLE2024, TLE2024A, TLE2024B, and TLE2024Y devices are precision, high-speed, low-power quad operational amplifiers using Texas Instruments patent-pending Excalibur process. These devices combine the best features of the OP421 with highly improved slew rate, unity-gain bandwidth, and input offset voltage.

The complementary bipolar Excalibur process utilizes isolated vertical P-N-P transistors that yield dramatic improvement in unity-gain bandwidth and slew rate over similar devices.

The addition of a patent-pending bias circuit in conjunction with this process results in extremely stable parameters with both time and temperature. This means that a "precision" device remains a precision device even with changes in temperature and over years of use.

This combination of excellent dc performance with a common-mode input voltage range that includes

LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION and PHASE SHIFT vs FREQUENCY



AVAILABLE OPTIONS

T$_A$	V$_{IO}$ max AT 25°C	PACKAGE				CHIP FORM (Y)
		SMALL OUTLINE (DW)	CHIP CARRIER (FK)	CERAMIC DIP (J)	PLASTIC DIP (N)	
0°C to 70°C	500 µV 750 µV 1000 µV	TLE2024BCDW TLE2024ACDW TLE2024CDW			TLE2024BCN TLE2024ACN TLE2024CN	TLE2024Y
– 40°C to 85°C	500 µV 750 µV 1000 µV	TLE2024BIDW TLE2024AIDW TLE2024IDW			TLE2024BIN TLE2024AIN TLE2024IN	
– 55°C to 125°C	500 µV 750 µV 1000 µV	TLE2024BMDW TLE2024AMDW TLE2024MDW	TLE2024AMFK TLE2024MFK	TLE2024BMJ TLE2024AMJ TLE2024MJ	TLE2024BMN TLE2024AMN TLE2024MN	

The D package is available taped and reeled. Add the suffix R (e.g., TLE2024CDWR). Chips are tested at 25°C.

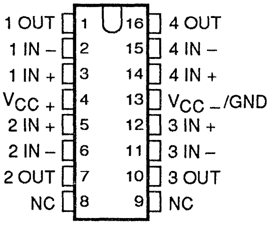
description (continued)

the negative rail makes these devices the ideal choice for low-level signal conditioning applications in either single-supply or split-supply configurations. In addition, these devices offer phase-reversal protection circuitry that eliminates an unexpected change in output states when one of the inputs goes below the negative supply rail.

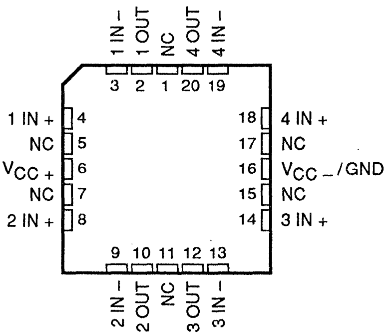
A variety of available packaging options includes small-outline and chip carrier versions for high-density systems applications.

The C-suffix devices are characterized for operation from 0°C to 70°C. The I-suffix devices are characterized for operation from −40°C to 85°C. The M-suffix devices are characterized for operation over the full military temperature range of −55°C to 125°C.

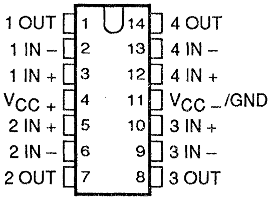
DW PACKAGE
(TOP VIEW)



FK PACKAGE
(TOP VIEW)



J or N PACKAGE
(TOP VIEW)

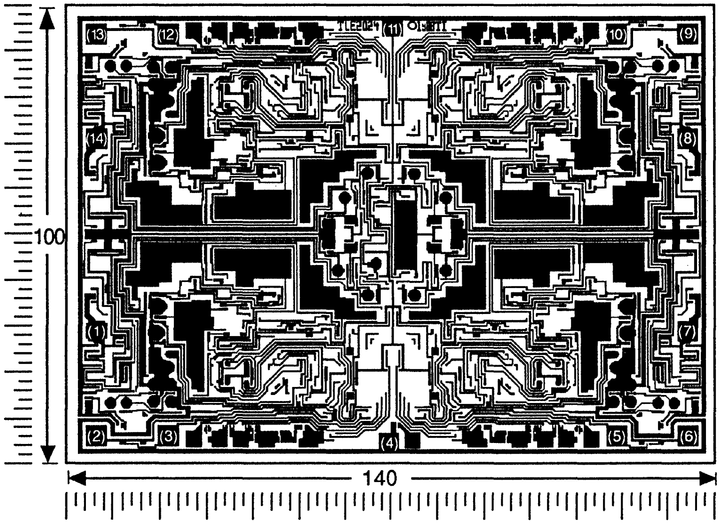


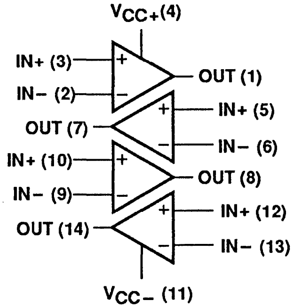
NC – No internal connection

chip information

These chips, properly assembled, display characteristics similar to the TLE2024. Thermal compression or ultrasonic bonding may be used on the doped aluminum bonding pads. Chips may be mounted with conductive epoxy or a gold-silicon preform.

BONDING PAD ASSIGNMENTS





CHIP THICKNESS:
15 TYPICAL

BONDING PADS:
4 X 4 MINIMUM

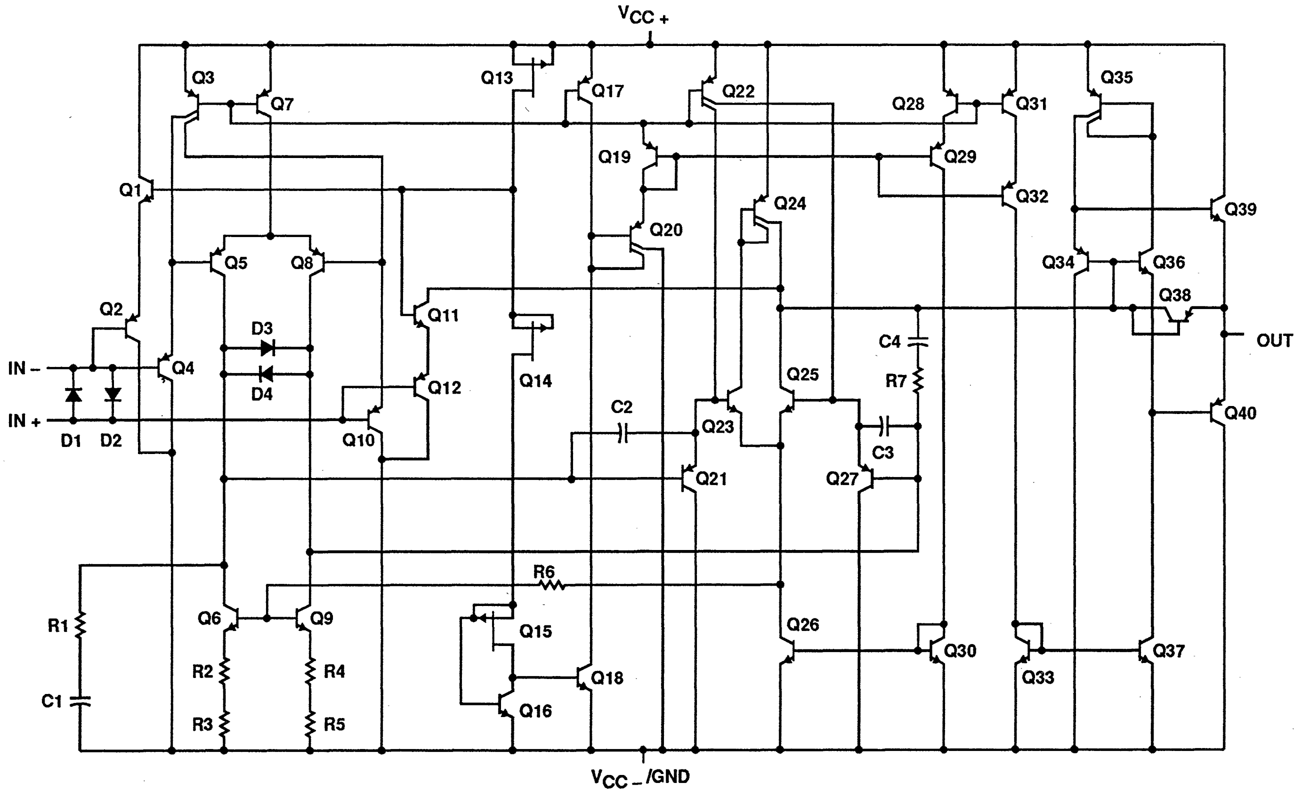
T_J max = 150°C

TOLERANCES
ARE ±10%

ALL DIMENSIONS
ARE IN MILS

PIN (11) INTERNALLY
CONNECTED TO
BACKSIDE OF CHIP

equivalent schematic (each amplifier)



Component count: Diodes — 16 Capacitors — 16
Resistors — 28 Transistors — 160

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC+} (see Note 1)	20 V
Supply voltage, V_{CC-} (see Note 1)	−20 V
Differential input voltage (see Note 2)	±0.6 V
Input voltage , V_I (any input, see Note 1)	$V_{CC\pm}$
Input current, I_I (each input)	±1 mA
Output current, I_O (each output)	±40 mA
Total current into V_{CC+} terminal	80 mA
Total current out of V_{CC-} terminal	80 mA
Duration of short-circuit current at (or below) 25°C (see Note 3)	unlimited
Continuous total dissipation	See Dissipation Rating Table
Operating free-air temperature range, T_A: C-suffix	0°C to 70°C
I-suffix	−40°C to 85°C
M-suffix	−55°C to 125°C
Storage temperature range	−65°C to 150°C
Case temperature for 60 seconds: FK package	260°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: DW or N package	260°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: J package	300°C

NOTES: 1. All voltage values, except differential voltages, are with respect to the midpoint between V_{CC+} and V_{CC-}.

2. Differential voltages are at the noninverting input with respect to the inverting input. Excessive current will flow if a differential input voltage in excess of approximately ±600 mV is applied between the inputs unless some limiting resistance is used.

3. The output may be shorted to either supply. Temperature and/or supply voltages must be limited to ensure that the maximum dissipation rating is not exceeded.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING	$T_A = 125°C$ POWER RATING
DW	1025 mW	8.2 mW/°C	656 mW	533 mW	205 mW
FK	1375 mW	11.0 mW/°C	880 mW	715 mW	275 mW
J	1375 mW	11.0 mW/°C	880 mW	715 mW	275 mW
N	1150 mW	9.2 mW/°C	736 mW	598 mW	230 mW

recommended operating conditions

		C-SUFFIX			I-SUFFIX			M-SUFFIX			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, $V_{CC\pm}$		± 2		± 20	± 2		± 20	± 2		± 20	V
Common-mode input voltage, V_{IC}	$V_{CC} = 5\ V$	0		3.5	0		3.2	0		3.2	V
	$V_{CC\pm} = \pm 15\ V$	– 15		13.5	– 15		13.2	– 15		13.2	
Operating free-air temperature, T_A		0		70	– 40		85	– 55		125	°C

electrical characteristics at specified free-air temperature, V_{CC} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A†	TLE2024C			TLE2024AC			TLE2024BC			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_{IC} = 0, R_S = 50 Ω	25°C			1100			850			600	µV
			Full range			1300			1050			800	
α_{VIO}	Temperature coefficient of input offset voltage		Full range		2			2			2		µV/°C
	Input offset voltage long-term drift (see Note 4)		25°C		0.005			0.005			0.005		µV/mo
I_{IO}	Input offset current		25°C		0.6	6		0.5	5		0.4	4	nA
			Full range			6			5			4	
I_{IB}	Input bias current		25°C		45	60		40	55		35	50	nA
			Full range			65			60			55	
V_{ICR}	Common-mode input voltage range	R_S = 50 Ω	25°C	0 to 3.5	−0.3 to 4		0 to 3.5	−0.3 to 4		0 to 3.5	−0.3 to 4		V
			Full range	0 to 3.5			0 to 3.5			0 to 3.5			
V_{OH}	High-level output voltage	R_L = 10 kΩ	25°C	3.9	4.2		3.9	4.2		4	4.3		V
			Full range	3.7			3.7			3.8			
V_{OL}	Low-level output voltage		25°C		0.7	0.8		0.7	0.8		0.7	0.8	V
			Full range			0.95			0.95			0.95	
A_{VD}	Large-signal differential voltage amplification	V_O = 1.4 V to 4 V, R_L = 10 kΩ	25°C	0.2	1.5		0.3	1.5		0.4	1.5		V/µV
			Full range	0.1			0.1			0.1			
CMRR	Common-mode rejection ratio	V_{IC} = V_{ICR} min, R_S = 50 Ω	25°C	80	90		82	92		85	95		dB
			Full range	80			82			85			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC} / \Delta V_{IO}$)	V_{CC} = 5 V to 30 V	25°C	98	112		100	115		103	117		dB
			Full range	93			95			98			
I_{CC}	Supply current	V_O = 2.5 V, No load	25°C		800	1200		800	1200		800	1200	µA
			Full range			1200			1200			1200	
ΔI_{CC}	Supply current change over operating temperature range		Full range		15			15			15		µA

†Full range is 0°C to 70°C.

NOTE 4: Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at T_A = 150°C extrapolated to T_A = 25°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

electrical characteristics at specified free-air temperature, $V_{CC\pm} = \pm 15$ V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A†	TLE2024C			TLE2024AC			TLE2024BC			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	$V_{IC} = 0$, $R_S = 50\ \Omega$	25°C			1000			750			500	µV
			Full range			1200			950			700	
α_{VIO}	Temperature coefficient of input offset voltage		Full range		2			2			2		µV/°C
	Input offset voltage long-term drift (see Note 4)		25°C		0.006			0.006			0.006		µV/mo
I_{IO}	Input offset current		25°C		0.6	6		0.5	5		0.4	4	nA
			Full range			6			5			4	
I_{IB}	Input bias current		25°C		50	60		45	55		40	50	nA
			Full range			65			60			55	
V_{ICR}	Common-mode input voltage range	$R_S = 50\ \Omega$	25°C	−15 to 13.5	−15.3 to 14		−15 to 13.5	−15.3 to 14		−15 to 13.5	−15.3 to 14		V
			Full range	−15 to 13.5			−15 to 13.5			−15 to 13.5			
V_{OM+}	Maximum positive peak output voltage swing	$R_L = 10\ k\Omega$	25°C	13.8	14.1		13.9	14.2		14	14.3		V
			Full range	13.7			13.8			13.9			
V_{OM-}	Maximum negative peak output voltage swing		25°C	−13.7	−14.1		−13.7	−14.1		−13.7	−14.1		V
			Full range	−13.6			−13.6			−13.6			
A_{VD}	Large-signal differential voltage amplification	$V_O = \pm 10$ V, $R_L = 10\ k\Omega$	25°C	0.4	2		0.8	4		1	7		V/µV
			Full range	0.4			0.8			1			
CMRR	Common-mode rejection ratio	$V_{IC} = V_{ICR}$ min, $R_S = 50\ \Omega$	25°C	92	102		94	105		97	108		dB
			Full range	88			90			93			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm} / \Delta V_{IO}$)	$V_{CC\pm} = \pm 2.5$ V to ± 15 V	25°C	98	112		100	115		103	117		dB
			Full range	93			95			98			
I_{CC}	Supply current	$V_O = 0$, No load	25°C		1050	1400		1050	1400		1050	1400	µA
			Full range			1400			1400			1400	
ΔI_{CC}	Supply current change over operating temperature range		Full range		20			20			20		µA

†Full range is 0°C to 70°C.

NOTE 4: Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at $T_A = 150°C$ extrapolated to $T_A = 25°C$ using the Arrhenius equation and assuming an activation energy of 0.96 eV.

operating characteristics at V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	TLE2024C			TLE2024AC			TLE2024BC			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
SR	Slew rate at unity gain	V_O = 1 V to 3 V, See Figure 1		0.5			0.5			0.5		V/µs
V_n	Equivalent input noise voltage (see Figure 2)	f = 10 Hz		21	50		21	50		21	50	nV/√Hz
		f = 1 kHz		17	30		17	30		17	30	
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 to 1 Hz		0.16			0.16			0.16		µV
		f = 0.1 to 10 Hz		0.47			0.47			0.47		
I_n	Equivalent input noise current			0.1			0.1			0.1		pA/√Hz
B_1	Unity-gain bandwidth	See Figure 3		1.7			1.7			1.7		MHz
ϕ_m	Phase margin at unity gain	See Figure 3		47°			47°			47°		

operating characteristics at specified free-air temperature, $V_{CC\pm}$ = ± 15 V

PARAMETER		TEST CONDITIONS	T_A†	TLE2024C			TLE2024AC			TLE2024BC			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
SR	Slew rate at unity gain	V_O = ± 10 V, See Figure 1	25°C	0.45	0.7		0.45	0.7		0.45	0.7		V/µs
			Full range	0.45			0.45			0.45			
V_n	Equivalent input noise voltage (see Figure 2)	f = 10 Hz	25°C		19	50		19	50		19	50	nV/√Hz
		f = 1 kHz	25°C		15	30		15	30		15	30	
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 to 1 Hz	25°C		0.16			0.16			0.16		µV
		f = 0.1 to 10 Hz	25°C		0.47			0.47			0.47		
I_n	Equivalent input noise current		25°C		0.1			0.1			0.1		pA/√Hz
B_1	Unity-gain bandwidth	See Figure 3	25°C		2.8			2.8			2.8		MHz
ϕ_m	Phase margin at unity gain	See Figure 3	25°C		52°			52°			52°		

†Full range is 0°C to 70°C.

electrical characteristics at specified free-air temperature, V_{CC} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A†	TLE2024I			TLE2024AI			TLE2024BI			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_{IC} = 0, R_S = 50 Ω	25°C			1100			850			600	µV
			Full range			1300			1050			800	
α_{VIO}	Temperature coefficient of input offset voltage		Full range		2			2			2		µV/°C
	Input offset voltage long-term drift (see Note 4)		25°C		0.005			0.005			0.005		µV/mo
I_{IO}	Input offset current		25°C		0.6	6		0.5	5		0.4	4	nA
			Full range			7			6			5	
I_{IB}	Input bias current		25°C		45	60		40	55		35	50	nA
			Full range			70			65			60	
V_{ICR}	Common-mode input voltage range	R_S = 50 Ω	25°C	0 to 3.5	−0.3 to 4		0 to 3.5	−0.3 to 4		0 to 3.5	−0.3 to 4		V
			Full range	0 to 3.2			0 to 3.2			0 to 3.2			
V_{OM+}	Maximum positive peak output voltage swing	R_L = 10 kΩ	25°C	3.9	4.2		3.9	4.2		4	4.3		V
			Full range	3.7			3.7			3.8			
V_{OM-}	Maximum negative peak output voltage swing		25°C		0.7	0.8		0.7	0.8		0.7	0.8	V
			Full range			0.95			0.95			0.95	
A_{VD}	Large-signal differential voltage amplification	V_O = ± 10 V, R_L = 10 kΩ	25°C	0.2	1.5		0.3	1.5		0.4	1.5		V/µV
			Full range	0.1			0.1			0.1			
CMRR	Common-mode rejection ratio	V_{IC} = V_{ICR} min, R_S = 50 Ω	25°C	80	90		82	92		85	95		dB
			Full range	80			82			85			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm} / \Delta V_{IO}$)	$V_{CC\pm}$ = ± 2.5 V to ± 15 V	25°C	98	112		100	115		103	117		dB
			Full range	93			95			98			
I_{CC}	Supply current	V_O = 0, No load	25°C		800	1200		800	1200		800	1200	µA
			Full range			1200			1200			1200	
ΔI_{CC}	Supply current change over operating temperature range		Full range		30			30			30		µA

†Full range is – 40°C to 85°C.

NOTE 4: Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at T_A = 150°C extrapolated to T_A = 25°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

electrical characteristics at specified free-air temperature, $V_{CC\pm} = \pm 15$ V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A†	TLE2024I			TLE2024AI			TLE2024BI			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	$V_{IC} = 0$, $R_S = 50\ \Omega$	25°C			1000			750			500	µV
			Full range			1200			950			700	
α_{VIO}	Temperature coefficient of input offset voltage		Full range		2			2			2		µV/°C
	Input offset voltage long-term drift (see Note 4)		25°C		0.006			0.006			0.006		µV/mo
I_{IO}	Input offset current		25°C		0.6	6		0.5	5		0.4	4	nA
			Full range			7			6			5	
I_{IB}	Input bias current		25°C		50	60		45	55		40	50	nA
			Full range			70			65			60	
V_{ICR}	Common-mode input voltage range	$R_S = 50\ \Omega$	25°C	– 15 to 13.5	– 15.3 to 14		– 15 to 13.5	– 15.3 to 14		– 15 to 13.5	– 15.3 to 14		V
			Full range	– 15 to 13.2			– 15 to 13.2			– 15 to 13.2			
V_{OM+}	Maximum positive peak output voltage swing	$R_L = 10\ k\Omega$	25°C	13.8	14.1		13.9	14.2		14	14.3		V
			Full range	13.7			13.7			13.8			
V_{OM-}	Maximum negative peak output voltage swing		25°C	– 13.7	– 14.1		– 13.7	– 14.1		– 13.7	– 14.1		V
			Full range	– 13.6			– 13.6			– 13.6			
A_{VD}	Large-signal differential voltage amplification	$V_O = \pm 10$ V, $R_L = 10\ k\Omega$	25°C	0.4	2		0.8	4		1	7		V/µV
			Full range	0.4			0.8			1			
CMRR	Common-mode rejection ratio	$V_{IC} = V_{ICR}$ min, $R_S = 50\ \Omega$	25°C	92	102		94	105		97	108		dB
			Full range	88			90			93			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm} / \Delta V_{IO}$)	$V_{CC\pm} = \pm 2.5$ V to ± 15 V	25°C	98	112		100	115		103	117		dB
			Full range	93			95			98			
I_{CC}	Supply current	$V_O = 0$, No load	25°C		1050	1400		1050	1400		1050	1400	µA
			Full range			1400			1400			1400	
ΔI_{CC}	Supply current change over operating temperature range		Full range		50			50			50		µA

†Full range is – 40°C to 85°C.

NOTE 4: Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at $T_A = 150°C$ extrapolated to $T_A = 25°C$ using the Arrhenius equation and assuming an activation energy of 0.96 eV.

operating characteristics at V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	TLE2024I			TLE2024AI			TLE2024BI			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
SR	Slew rate at unity gain	V_O = 1 V to 3 V, See Figure 1		0.5			0.5			0.5		V/μs
V_n	Equivalent input noise voltage (see Figure 2)	f = 10 Hz		21	50		21	50		21	50	nV/√Hz
		f = 1 kHz		17	30		17	30		17	30	
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 to 1 Hz		0.16			0.16			0.16		μV
		f = 0.1 to 10 Hz		0.47			0.47			0.47		
I_n	Equivalent input noise current			0.1			0.1			0.1		pA/√Hz
B_1	Unity-gain bandwidth	See Figure 3		1.7			1.7			1.7		MHz
ϕ_m	Phase margin at unity gain	See Figure 3		47°			47°			47°		

operating characteristics at specified free-air temperature, $V_{CC\pm}$ = ±15 V

PARAMETER		TEST CONDITIONS	T_A†	TLE2024I			TLE2024AI			TLE2024BI			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
SR	Slew rate at unity gain	V_O = ±10 V, See Figure 1	25°C	0.45	0.7		0.45	0.7		0.45	0.7		V/μs
			Full range	0.42			0.42			0.42			
V_n	Equivalent input noise voltage (see Figure 2)	f = 10 Hz	25°C		19	50		19	50		19	50	nV/√Hz
		f = 1 kHz	25°C		15	30		15	30		15	30	
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 to 1 Hz	25°C		0.16			0.16			0.16		μV
		f = 0.1 to 10 Hz	25°C		0.47			0.47			0.47		
I_n	Equivalent input noise current		25°C		0.1			0.1			0.1		pA/√Hz
B_1	Unity-gain bandwidth	See Figure 3	25°C		2.8			2.8			2.8		MHz
ϕ_m	Phase margin at unity gain	See Figure 3	25°C		52°			52°			52°		

†Full range is – 40°C to 85°C.

electrical characteristics at specified free-air temperature, V_{CC} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A†	TLE2024M			TLE2024AM			TLE2024BM			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_{IC} = 0, R_S = 50 Ω	25°C			1100			850			600	µV
			Full range			1300			1050			800	
α_{VIO}	Temperature coefficient of input offset voltage		Full range		2			2			2		µV/°C
	Input offset voltage long-term drift (see Note 4)		25°C		0.005			0.005			0.005		µV/mo
I_{IO}	Input offset current		25°C		0.6	6		0.5	5		0.4	4	nA
			Full range			10			9			8	
I_{IB}	Input bias current		25°C		45	60		40	55		35	50	nA
			Full range			80			75			70	
V_{ICR}	Common-mode input voltage range	R_S = 50 Ω	25°C	0 to 3.5	−0.3 to 4		0 to 3.5	−0.3 to 4		0 to 3.5	−0.3 to 4		V
			Full range	0 to 3.2			0 to 3.2			0 to 3.2			
V_{OM+}	Maximum positive peak output voltage swing	R_L = 10 kΩ	25°C	3.9	4.2		3.9	4.2		4	4.3		V
			Full range	3.7			3.7			3.8			
V_{OM-}	Maximum negative peak output voltage swing		25°C		0.7	0.8		0.7	0.8		0.7	0.8	V
			Full range			0.95			0.95			0.95	
A_{VD}	Large-signal differential voltage amplification	V_O = ± 10 V, R_L = 10 kΩ	25°C	0.2	1.5		0.3	1.5		0.4	1.5		V/µV
			Full range	0.1			0.1			0.1			
CMRR	Common-mode rejection ratio	V_{IC} = V_{ICR} min, R_S = 50 Ω	25°C	80	90		82	92		85	95		dB
			Full range	80			82			85			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm} / \Delta V_{IO}$)	$V_{CC\pm}$ = ± 2.5 V to ± 15 V	25°C	98	112		100	115		103	117		dB
			Full range	93			95			98			
I_{CC}	Supply current	V_O = 0, No load	25°C		800	1200		800	1200		800	1200	µA
			Full range			1200			1200			1200	
ΔI_{CC}	Supply current change over operating temperature range		Full range		50			50			50		µA

†Full range is – 55°C to 125°C.

NOTE 4: Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at T_A = 150°C extrapolated to T_A = 25°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

electrical characteristics at specified free-air temperature, $V_{CC\pm} = \pm 15$ V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A†	TLE2024M			TLE2024AM			TLE2024BM			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	$V_{IC} = 0$, $R_S = 50\ \Omega$	25°C			1000			750			500	µV
			Full range			1200			950			700	
α_{VIO}	Temperature coefficient of input offset voltage		Full range		2			2			2		µV/°C
	Input offset voltage long-term drift (see Note 4)		25°C		0.006			0.006			0.006		µV/mo
I_{IO}	Input offset current		25°C		0.6	6		0.5	5		0.4	4	nA
			Full range			10			9			8	
I_{IB}	Input bias current		25°C		50	60		45	55		40	50	nA
			Full range			80			75			70	
V_{ICR}	Common-mode input voltage range	$R_S = 50\ \Omega$	25°C	–15 to 13.5	–15.3 to 14		–15 to 13.5	–15.3 to 14		–15 to 13.5	–15.3 to 14		V
			Full range	–15 to 13.2			–15 to 13.2			–15 to 13.2			
V_{OM+}	Maximum positive peak output voltage swing	$R_L = 10\ k\Omega$	25°C	13.8	14.1		13.9	14.2		14	14.3		V
			Full range	13.7			13.7			13.8			
V_{OM-}	Maximum negative peak output voltage swing		25°C	–13.7	–14.1		–13.7	–14.1		–13.7	–14.1		V
			Full range	–13.6			–13.6			–13.6			
A_{VD}	Large-signal differential voltage amplification	$V_O = \pm 10$ V, $R_L = 10\ k\Omega$	25°C	0.4	2		0.8	4		1	7		V/µV
			Full range	0.4			0.8			1			
CMRR	Common-mode rejection ratio	$V_{IC} = V_{ICR}$ min, $R_S = 50\ \Omega$	25°C	92	102		94	105		97	108		dB
			Full range	88			90			93			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm} / \Delta V_{IO}$)	$V_{CC\pm} = \pm 2.5$ V to ± 15 V	25°C	98	112		100	115		103	117		dB
			Full range	93			95			98			
I_{CC}	Supply current	$V_O = 0$, No load	25°C		1050	1400		1050	1400		1050	1400	µA
			Full range			1400			1400			1400	
ΔI_{CC}	Supply current change over operating temperature range		Full range		85			85			85		µA

† Full range is – 55°C to 125°C.

NOTE 4: Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at $T_A = 150°C$ extrapolated to $T_A = 25°C$ using the Arrhenius equation and assuming an activation energy of 0.96 eV.

operating characteristics at V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	TLE2024M			TLE2024AM			TLE2024BM			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
SR	Slew rate at unity gain	V_O = 1 V to 3 V, See Figure 1		0.5			0.5			0.5		V/μs
V_n	Equivalent input noise voltage (see Figure 2)	f = 10 Hz		21			21			21		nV/√Hz
		f = 1 kHz		17			17			17		
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 to 1 Hz		0.16			0.16			0.16		μV
		f = 0.1 to 10 Hz		0.47			0.47			0.47		
I_n	Equivalent input noise current			0.1			0.1			0.1		pA/√Hz
B_1	Unity-gain bandwidth	See Figure 3		1.7			1.7			1.7		MHz
ϕ_m	Phase margin at unity gain	See Figure 3		47°			47°			47°		

operating characteristics at specified free-air temperature, $V_{CC\pm}$ = ± 15 V

PARAMETER		TEST CONDITIONS	T_A†	TLE2024M			TLE2024AM			TLE2024BM			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
SR	Slew rate at unity gain	V_O = ± 10 V, See Figure 1	25°C	0.45	0.7		0.45	0.7		0.45	0.7		V/μs
			Full range	0.4			0.4			0.4			
V_n	Equivalent input noise voltage (see Figure 2)	f = 10 Hz	25°C		19			19			19		nV/√Hz
		f = 1 kHz	25°C		15			15			15		
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 to 1 Hz	25°C		0.16			0.16			0.16		μV
		f = 0.1 to 10 Hz	25°C		0.47			0.47			0.47		
I_n	Equivalent input noise current		25°C		0.1			0.1			0.1		pA/√Hz
B_1	Unity-gain bandwidth	See Figure 3	25°C		2.8			2.8			2.8		MHz
ϕ_m	Phase margin at unity gain	See Figure 3	25°C		52°			52°			52°		

†Full range is – 55°C to 125°C.

electrical characteristics, V_{CC} = 5 V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	V_{IC} = 0, R_S = 50 Ω		250	1100	µV
	Input offset voltage long-term drift (see Note 4)			0.005		µV/mo
I_{IO}	Input offset current			0.6	6	nA
I_{IB}	Input bias current			45	60	nA
V_{ICR}	Common-mode input voltage range	R_S = 50 Ω	0 to 3.5	−0.3 to 4		V
V_{OH}	Maximum high-level output voltage	R_L = 10 kΩ	3.9	4.2		V
V_{OL}	Maximum low-level output voltage			0.7	0.8	V
A_{VD}	Large-signal differential voltage amplification	V_O = 1.4 V to 4 V, R_L = 10 kΩ	0.2	1.5		V/µV
CMRR	Common-mode rejection ratio	$V_{IC} = V_{ICR}$min, R_S = 50 Ω	80	90		dB
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC}/\Delta V_{IO}$)	V_{CC} = 5 V to 30 V	98	112		dB
I_{CC}	Supply current	V_O = 2.5 V, No load		800	1200	µA

NOTE 4: Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at T_A = 150°C extrapolated to T_A = 25°C using the Arrhenius equation and assuming and activation energy of 0.96 eV.

operating characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain	V_O = 1 V to 3 V, See Figure 1		0.5		V/µs
V_n	Equivalent input noise voltage (see Figure 2)	f = 10 Hz		21	50	nV/√Hz
		f = 1 kHz		17	30	
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 to 1 Hz		0.16		µV
		f = 0.1 to 10 Hz		0.47		
I_n	Equivalent input noise current			0.1		pA/√Hz
B_1	Unity-gain bandwidth	See Figure 3		1.7		MHz
ϕ_m	Phase margin at unity gain	See Figure 3		47°		

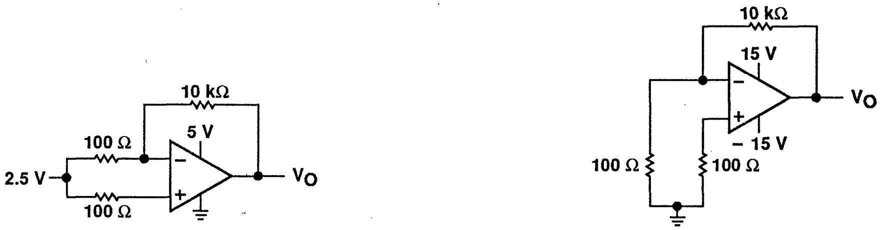
PARAMETER MEASUREMENT INFORMATION

NOTE A: C_L includes fixture capacitance.

(a) SINGLE SUPPLY

(b) SPLIT SUPPLY

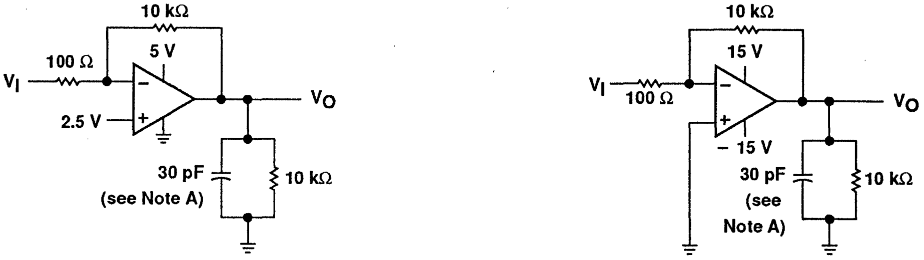
Figure 1. Slew Rate Test Circuit



(a) SINGLE SUPPLY

(b) SPLIT SUPPLY

Figure 2. Noise Voltage Test Circuit



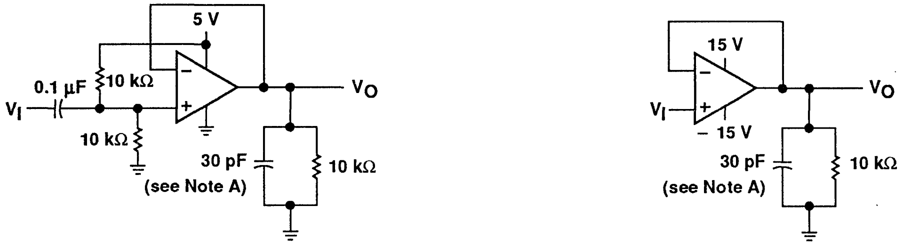
NOTE A: C_L includes fixture capacitance.

(a) SINGLE SUPPLY

(b) SPLIT SUPPLY

Figure 3. Unity-Gain Bandwidth and Phase Margin Test Circuit

PARAMETER MEASUREMENT INFORMATION



NOTE A: C_L includes fixture capacitance.

(a) SINGLE SUPPLY

(b) SPLIT SUPPLY

Figure 4. Small-Signal Pulse Response Test Circuit

typical values

Typical values presented in this data sheet represent the median (50% point) of device parametric performance.

TYPICAL CHARACTERISTICS

table of graphs

			FIGURE
V_{IO}	Input offset voltage	Distribution	5
I_{IB}	Input bias current	vs Common-mode voltage	6
		vs Temperature	7
I_I	Input current	vs Differential input voltage	8
V_{OM}	Maximum peak output voltage	vs Output current	9
		vs Temperature	10
V_{OH}	High-level output voltage	vs High-level output current	11
		vs Temperature	12
V_{OL}	Low-level output voltage	vs Low-level output current	13
		vs Temperature	14
$V_{O(PP)}$	Maximum peak-to-peak output voltage swing	vs Frequency	15, 16
A_{VD}	Differential voltage amplification	vs Frequency	17
		vs Temperature	18
I_{OS}	Short-circuit output current	vs Supply voltage	19, 21
		vs Temperature	20, 22
I_{CC}	Supply current	vs Supply voltage	23
		vs Temperature	24
CMRR	Common-mode rejection ratio	vs Frequency	25
SR	Slew rate	vs Temperature	26
	Pulse response	Small-signal	27, 28
		Large-signal	29, 30
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	0.1 to 1 Hz	31
		0.1 to 10 Hz	32
V_n	Equivalent input noise voltage	vs Frequency	33
B_1	Unity-gain bandwidth	vs Supply voltage	34
		vs Temperature	35
ϕ_m	Phase margin	vs Supply voltage	36
		vs Capacitive load	37
		vs Temperature	38
	Phase shift	vs Frequency	17

TYPICAL CHARACTERISTICS†

TLE2024
DISTRIBUTION OF
INPUT OFFSET VOLTAGE

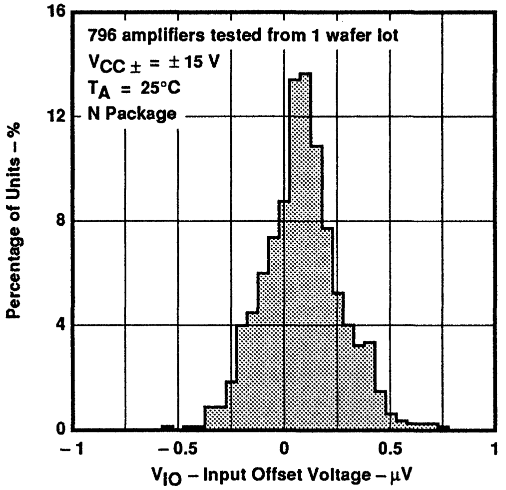


Figure 5

TLE2024B
INPUT BIAS CURRENT
vs
COMMON-MODE INPUT VOLTAGE

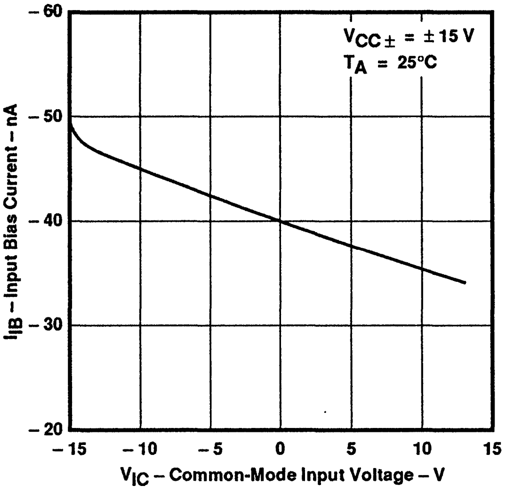


Figure 6

TLE2024B
INPUT BIAS CURRENT
vs
FREE-AIR TEMPERATURE

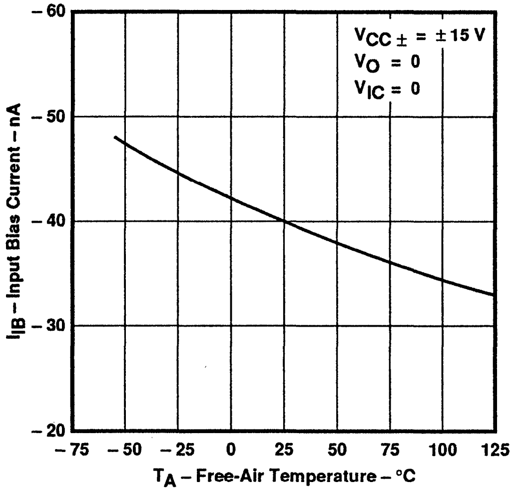


Figure 7

INPUT CURRENT
vs
DIFFERENTIAL INPUT VOLTAGE

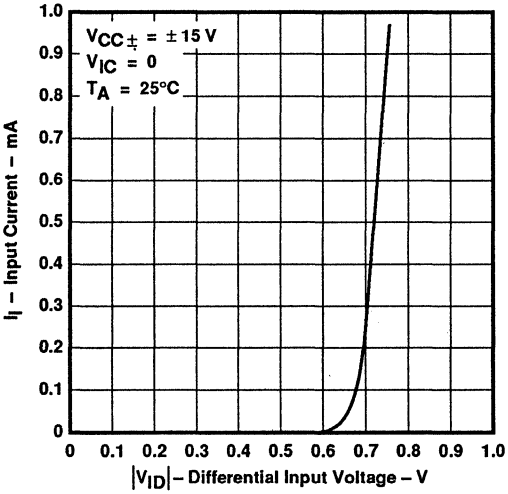


Figure 8

---

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS[†]

TLE2024B
MAXIMUM PEAK OUTPUT VOLTAGE
vs
OUTPUT CURRENT

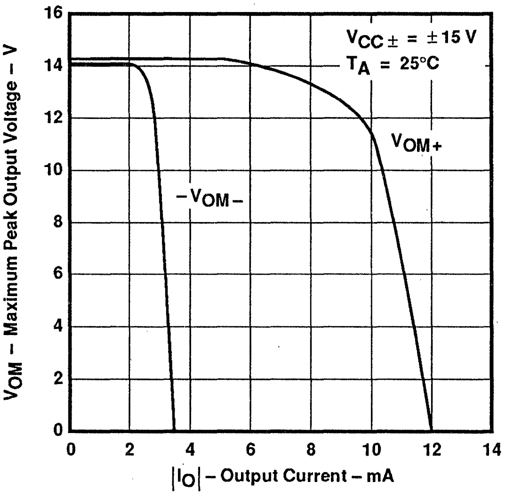


Figure 9

TLE2024B
MAXIMUM PEAK OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

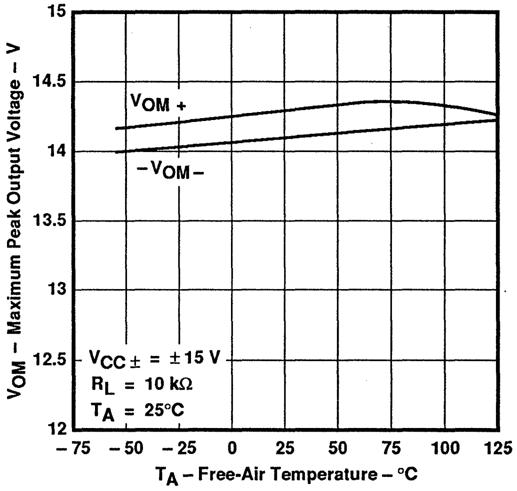


Figure 10

TLE2024B
HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

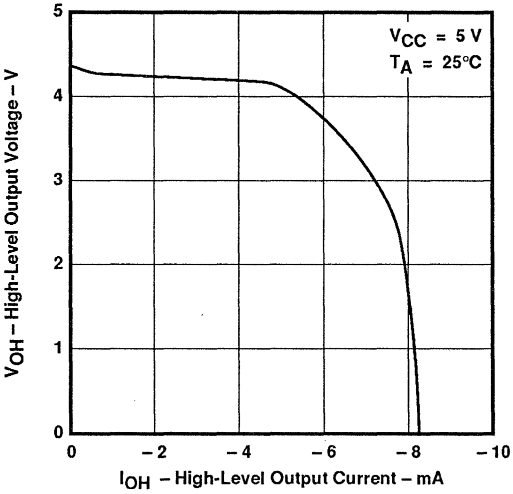


Figure 11

TLE2024B
HIGH-LEVEL OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

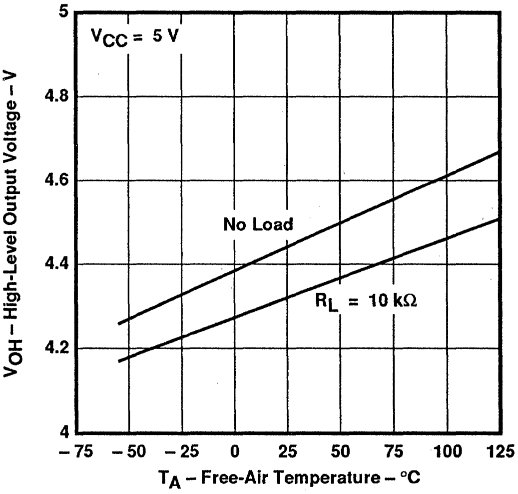


Figure 12

[†] Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

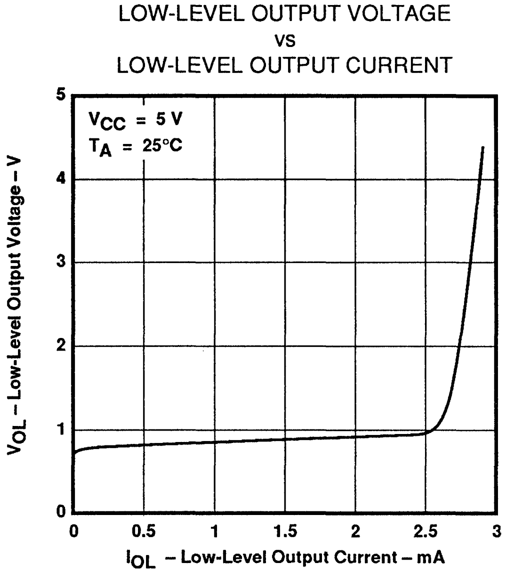


Figure 13

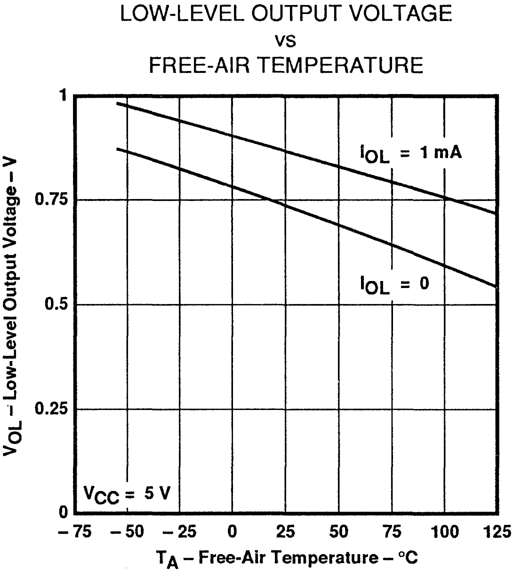


Figure 14

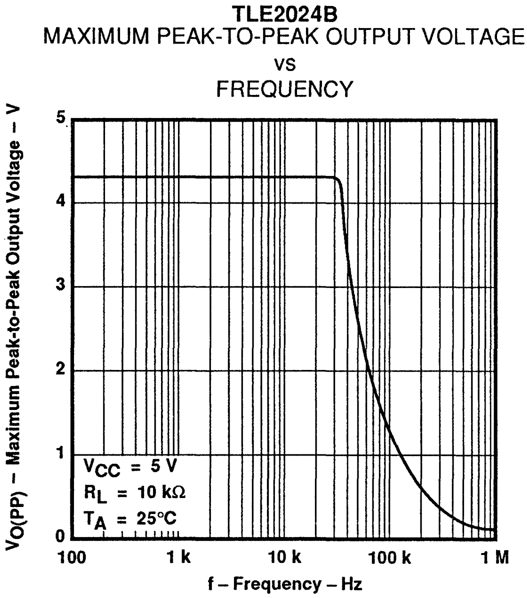


Figure 15

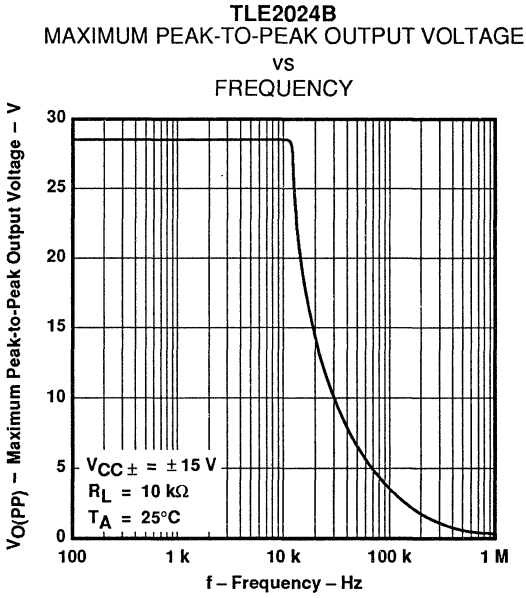


Figure 16

---

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

TLE2024
LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION and PHASE SHIFT
vs
FREQUENCY

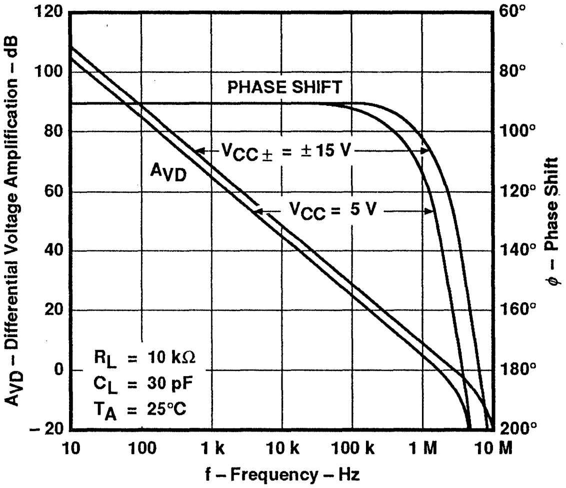


Figure 17

TLE2024B
LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION
vs
FREE-AIR TEMPERATURE

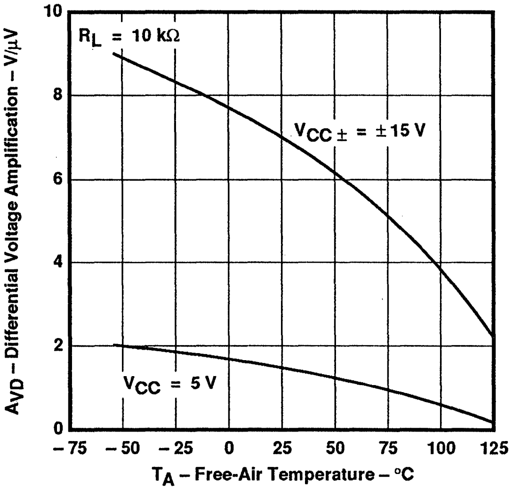


Figure 18

SHORT-CIRCUIT OUTPUT CURRENT
vs
SUPPLY VOLTAGE

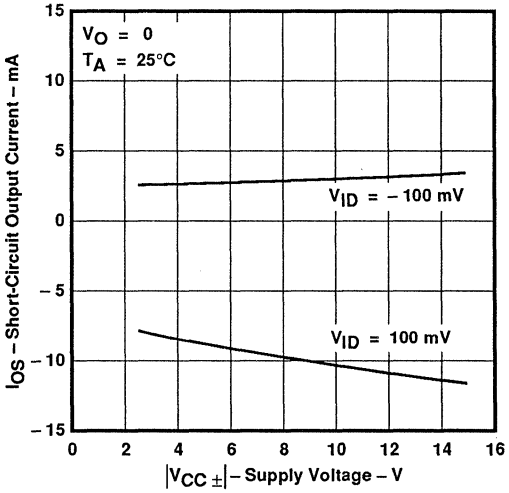


Figure 19

SHORT-CIRCUIT OUTPUT CURRENT
vs
FREE-AIR TEMPERATURE

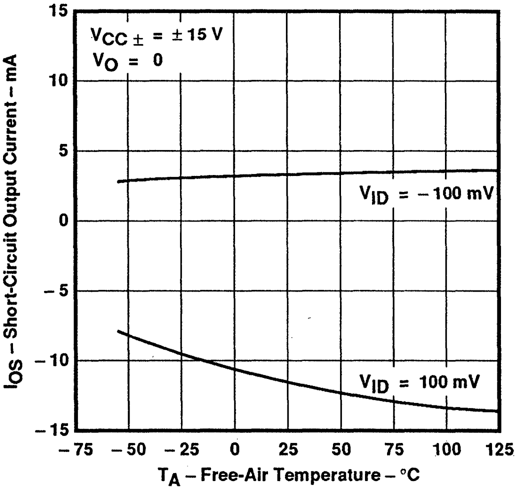


Figure 20

---

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

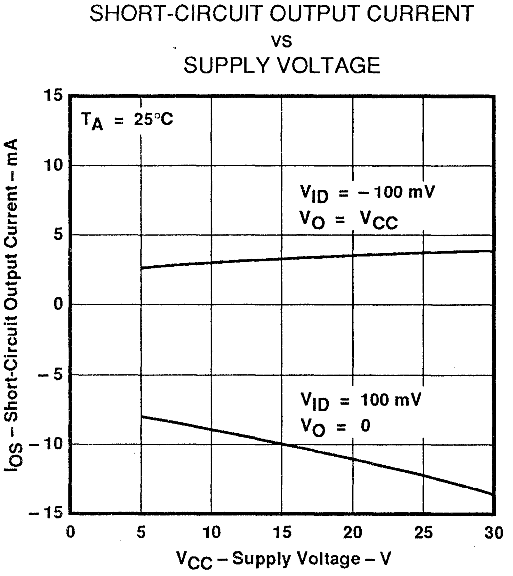


Figure 21

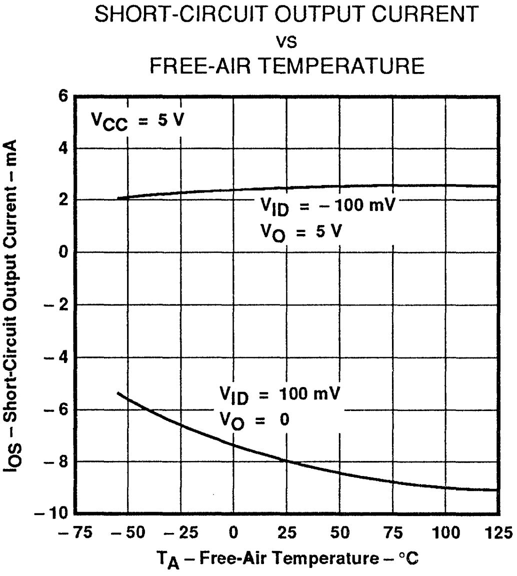


Figure 22

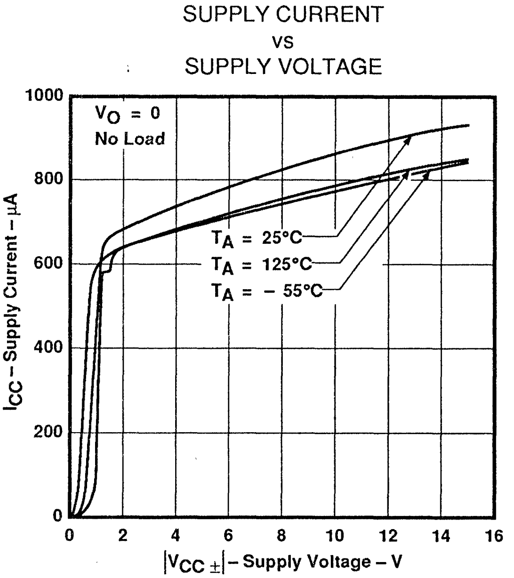


Figure 23

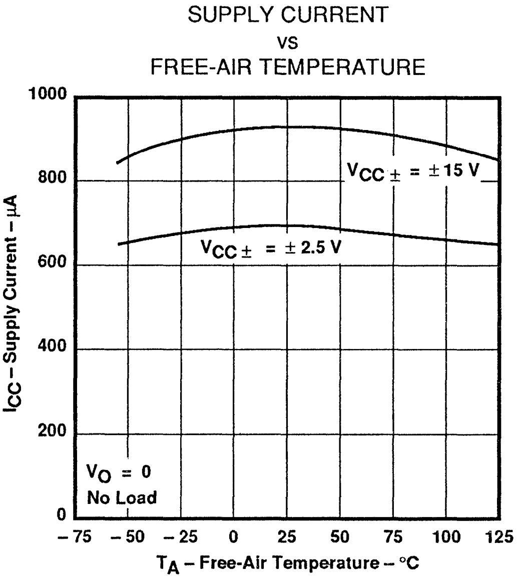


Figure 24

---

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

TLE2024B
COMMON-MODE REJECTION RATIO
vs
FREQUENCY

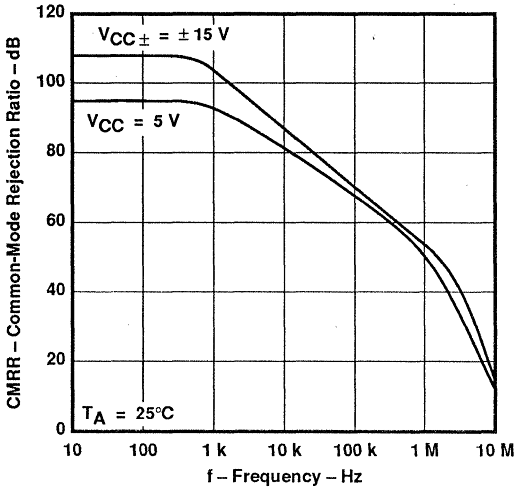


Figure 25

SLEW RATE
vs
FREE-AIR TEMPERATURE

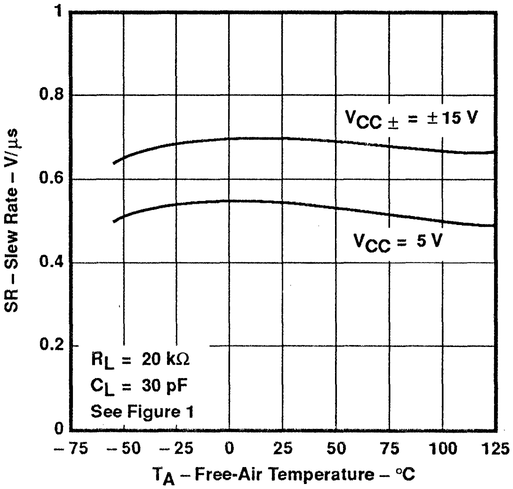


Figure 26

VOLTAGE-FOLLOWER
SMALL-SIGNAL
PULSE RESPONSE

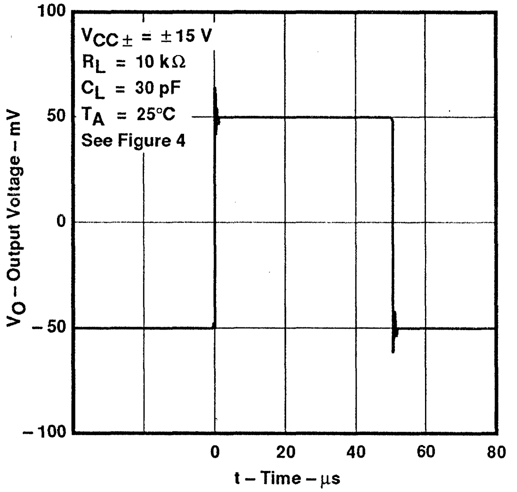


Figure 27

VOLTAGE-FOLLOWER
SMALL-SIGNAL
PULSE RESPONSE

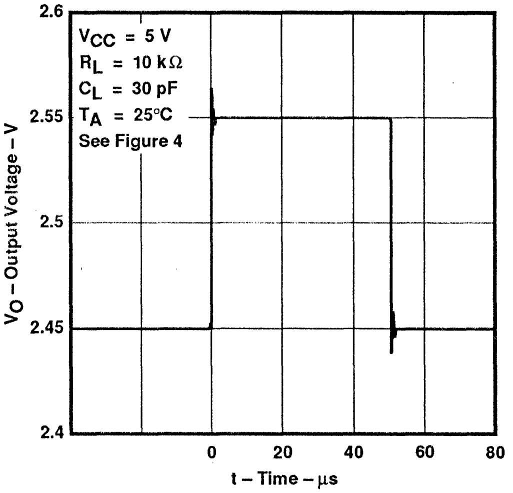


Figure 28

---

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS

VOLTAGE-FOLLOWER
LARGE-SIGNAL
PULSE RESPONSE

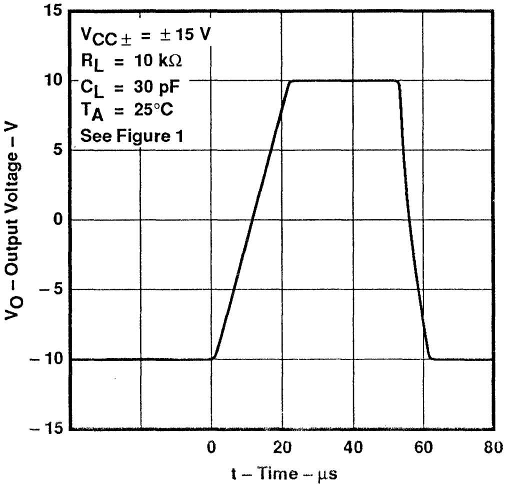


Figure 29

VOLTAGE-FOLLOWER
LARGE-SIGNAL
PULSE RESPONSE

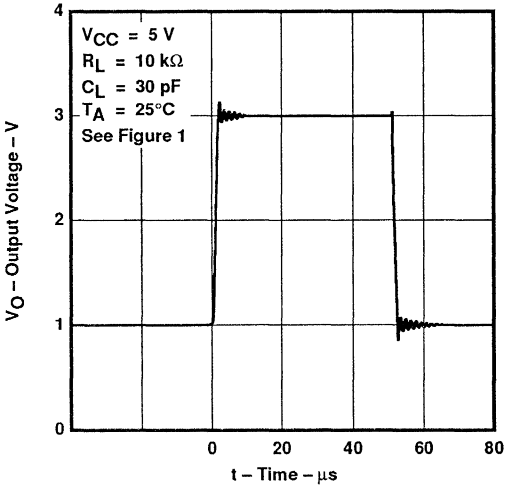


Figure 30

PEAK-TO-PEAK EQUIVALENT
INPUT NOISE VOLTAGE
0.1 TO 1 Hz

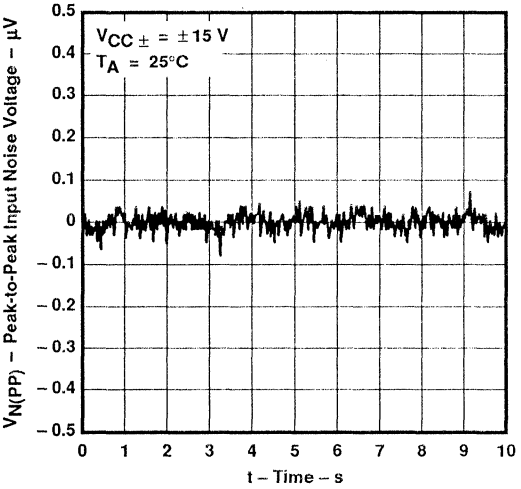


Figure 31

PEAK-TO-PEAK EQUIVALENT
INPUT NOISE VOLTAGE
0.1 TO 10 Hz

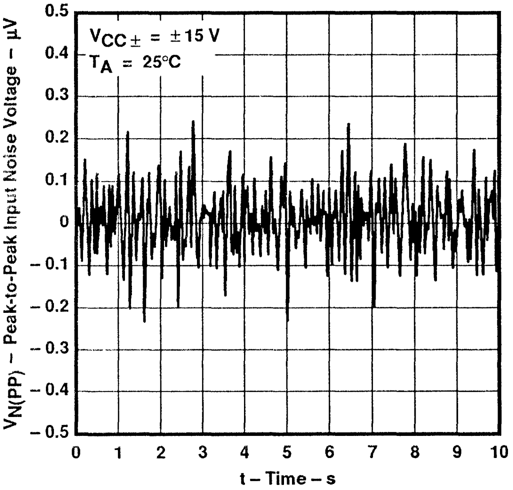


Figure 32

TYPICAL CHARACTERISTICS†

EQUIVALENT INPUT NOISE VOLTAGE
vs
FREQUENCY

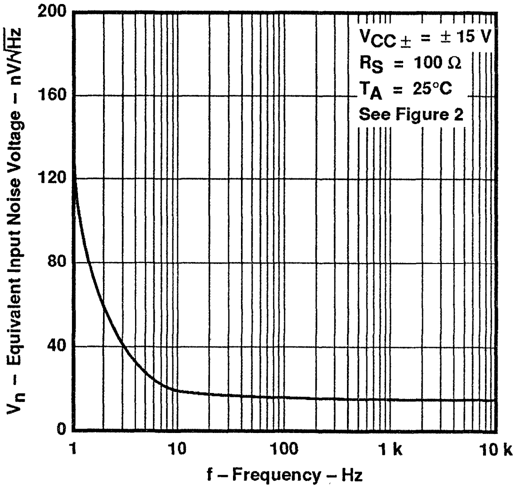


Figure 33

UNITY-GAIN BANDWIDTH
vs
SUPPLY VOLTAGE

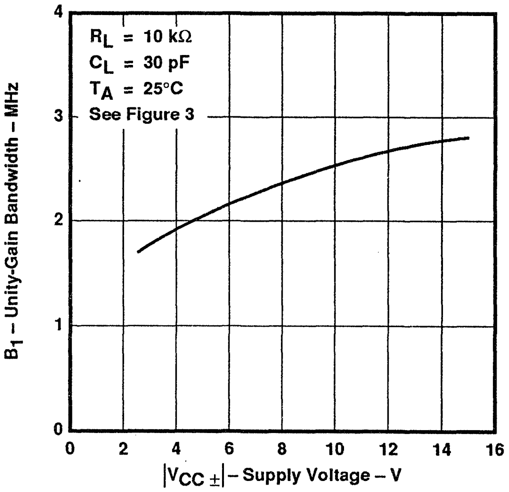


Figure 34

UNITY-GAIN BANDWIDTH
vs
FREE-AIR TEMPERATURE

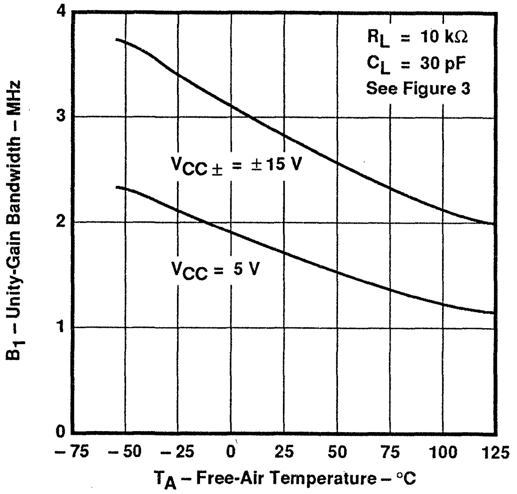


Figure 35

PHASE MARGIN
vs
SUPPLY VOLTAGE

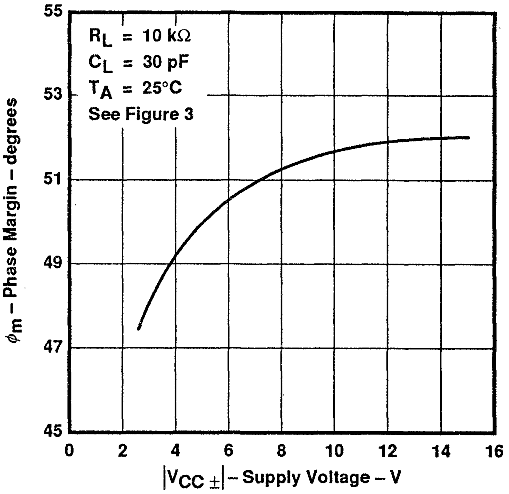


Figure 36

---

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

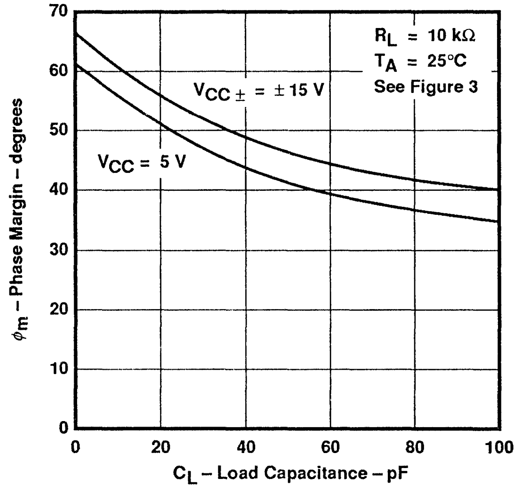

PHASE MARGIN
vs
LOAD CAPACITANCE

Figure 37

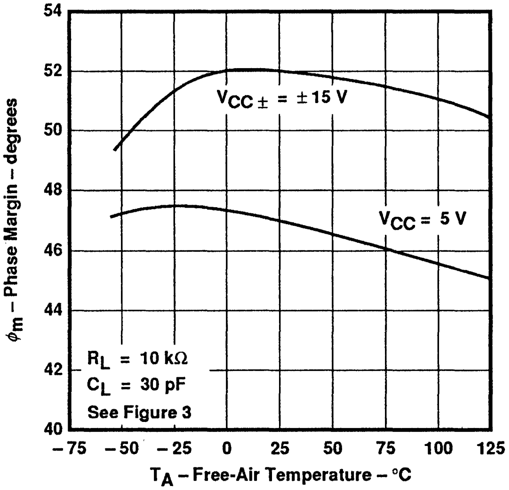

PHASE MARGIN
vs
FREE-AIR TEMPERATURE

Figure 38

---

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

APPLICATION INFORMATION

voltage-follower applications

The TLE2024 circuitry includes input protection diodes to limit the voltage across the input transistors; however, no provision is made in the circuit to limit the current if these diodes are forward-biased. Note that this condition can occur when the device is operated in the voltage-follower configuration and driven with a fast, large-signal pulse. It is recommended that a feedback resistor be used to limit the current to a maximum of 1 mA to prevent degradation of the device. Also, remember that this feedback resistor will form a pole with the input capacitance of the device. For feedback resistor values greater than 10 kΩ, this pole will degrade the amplifier's phase margin. This problem can be alleviated by adding a capacitor (20 pF to 50 pF) in parallel with the feedback resistor (see Figure 39).

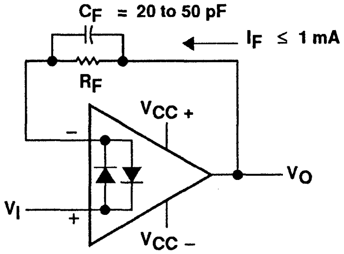


Figure 39. Voltage Follower

input characteristics

The input of any unused amplifiers should be tied to ground to avoid possible oscillation.

TLE2027, TLE2027A
EXCALIBUR LOW-NOISE HIGH-SPEED PRECISION OPERATIONAL AMPLIFIERS

D3440, MAY 1990 – REVISED APRIL 1991

available features

- **Outstanding Combination of DC Precision and AC Performance:**
  - **Unity-Gain Bandwidth . . . 15 MHz Typ**
  - **V_n. . . . 3.3 nV/√Hz at f = 10 Hz Typ, 2.5 nV/√Hz at f = 1 kHz Typ**
  - **V_{IO} . . . 25 μV Max**
  - **A_{VD}. . . 45 V/μV Typ, With R_L = 2 kΩ, 19 V/μV Typ, With R_L = 600 Ω**
- **Available in Standard-Pinout Small-Outline Package**
- **Output Features Saturation Recovery Circuitry**
- **Macromodels and Statistical Information**

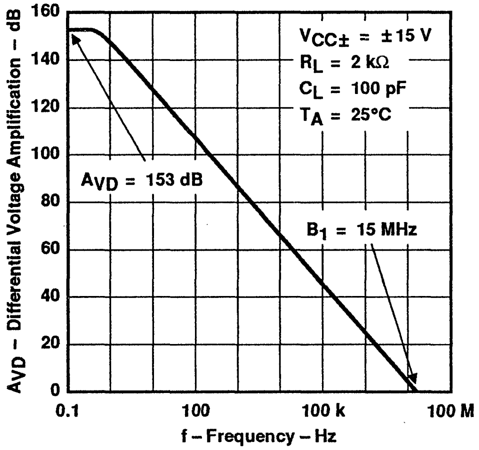
description

The TLE2027 and TLE2027A contain innovative circuit design expertise and high-quality process control techniques to produce a level of ac performance and dc precision previously unavailable in single operational amplifiers. Manufactured using Texas Instruments state-of-the-art Excalibur process, these devices allow upgrades to systems that use lower-precision devices.

In the area of dc precision, the TLE2027 and TLE2027A offer maximum offset voltages of 100 μV and 25 μV, respectively, common-mode rejection ratio of 131 dB (typ), supply voltage rejection ratio of 144 dB (typ), and dc gain of 45 V/μV (typ).

Ac performance is highlighted by a typical unity-gain bandwidth specification of 15 MHz, 55° of phase margin, and noise voltage specifications of 3.3 nV/√Hz and 2.5 nV/√Hz at frequencies of 10 Hz and 1 kHz, respectively.

LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION vs FREQUENCY



Both the TLE2027 and TLE2027A are available in a wide variety of packages, including the industry-standard 8-pin small-outline version for high-density system applications. The C-suffix devices are characterized for operation from 0°C to 70°C. The I-suffix devices are characterized for operation from −40°C to 105°C. The M-suffix devices are characterized for operation over the full military temperature range of −55°C to 125°C.

AVAILABLE OPTIONS

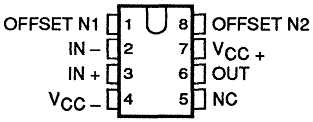
T_A	V_{IO} max AT 25°C	PACKAGE				
		SMALL-OUTLINE (D)	CHIP CARRIER (FK)	CERAMIC DIP (JG)	METAL CAN (L)	PLASTIC DIP (P)
0°C to 70°C	25 μV	TLE2027ACD	——	——	——	TLE2027ACP
	100 μV	TLE2027CD	——	——	——	TLE2027CP
– 40°C to 105°C	25 μV	TLE2027AID	——	——	——	TLE2027AIP
	100 μV	TLE2027ID	——	——	——	TLE2027IP
– 55°C to 125°C	25 μV	TLE2027AMD	TLE2027AMFK	TLE2027AMJG	TLE2027AML	TLE2027AMP
	100 μV	TLE2027MD	TLE2027MFK	TLE2027MJG	TLE2027ML	TLE2027MP

D packages are available taped and reeled. Add "R" suffix to device type, (e.g., TLE2027ACDR).

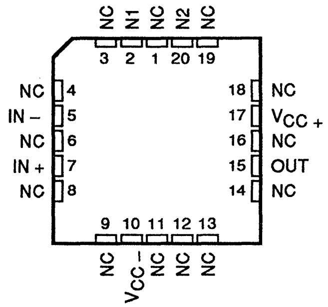
TEXAS INSTRUMENTS
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

On products compliant to MIL-STD-883, Class B, all parameters are tested unless otherwise noted. On all other products, production processing does not necessarily include testing of all parameters.

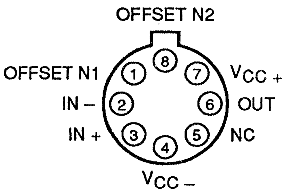
D, JG, OR P PACKAGE
(TOP VIEW)



FK PACKAGE
(TOP VIEW)



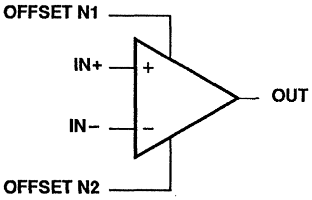
L PACKAGE
(TOP VIEW)



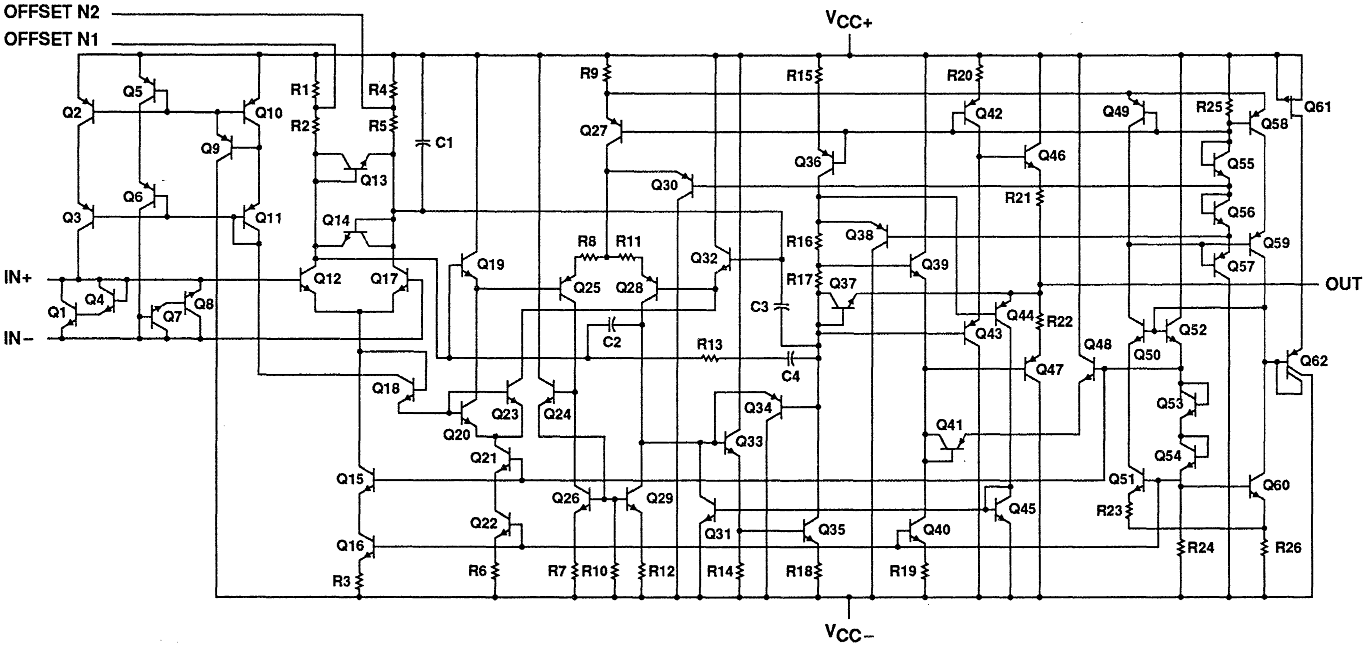
Pin 4 of the L package is in electrical contact with the case.

NC – No internal connection

symbol



equivalent schematic



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC+} (see Note 1)	22 V
Supply voltage, V_{CC-}	−22 V
Differential input voltage (see Note 2)	±1.2 V
Input voltage range, V_I (any input)	$V_{CC\pm}$
Input current, I_I (each input)	±1 mA
Output current, I_O	±50 mA
Total current into V_{CC+} terminal	50 mA
Total current out of V_{CC-} terminal	50 mA
Duration of short-circuit current at (or below) 25°C (see Note 3)	unlimited
Continuous total dissipation	See Dissipation Rating Table
Operating free-air temperature range, T_A: C-suffix	0°C to 70°C
I-suffix	−40°C to 105°C
M-suffix	−55°C to 125°C
Storage temperature range	−65°C to 150°C
Case temperature for 60 seconds: FK package	260°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D or P package	260°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: JG or L package	300°C

NOTES: 1. All voltage values, except differential voltages, are with respect to the midpoint between V_{CC+} and V_{CC-}.
2. Differential voltages are at the noninverting input with respect to the inverting input. Excessive current will flow if a differential input voltage in excess of approximately ±1.2 V is applied between the inputs unless some limiting resistance is used.
3. The output may be shorted to either supply. Temperature and/or supply voltages must be limited to ensure that the maximum dissipation rating is not exceeded.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 105°C$ POWER RATING	$T_A = 125°C$ POWER RATING
D	725 mW	5.8 mW/°C	464 mW	261 mW	145 mW
FK	1375 mW	11.0 mW/°C	880 mW	495 mW	275 mW
JG	1050 mW	8.4 mW/°C	672 mW	378 mW	210 mW
L	650 mW	5.2 mW/°C	416 mW	234 mW	130 mW
P	1000 mW	8.0 mW/°C	640 mW	360 mW	200 mW

recommended operating conditions

		C-SUFFIX		I-SUFFIX		M-SUFFIX		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
Supply voltage, $V_{CC\pm}$		± 4	± 22	± 4	± 22	± 4	± 22	V
Common-mode input voltage, V_{IC}	T_A = 25°C	− 11	11	− 11	11	− 11	11	V
	T_A = Full range	− 10.5	10.5	− 10.4	10.4	− 10.2	10.2	
Operating free-air temperature, T_A		0	70	− 40	105	− 55	125	°C

electrical characteristics at specified free-air temperature, $V_{CC\pm}$ = ±15 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A†	TLE2027C			TLE2027AC			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_{IC} = 0, R_S = 50 Ω	25°C		20	100		10	25	μV
			Full range			145			70	
α_{VIO}	Temperature coefficient of input offset voltage		Full range		0.4	1		0.2	1	μV/°C
	Input offset voltage long-term drift (see Note 4)		25°C		0.006	1		0.006	1	μV/mo
I_{IO}	Input offset current		25°C		6	90		6	90	nA
			Full range			150			150	
I_{IB}	Input bias current		25°C		15	90		15	90	nA
			Full range			150			150	
V_{ICR}	Common-mode input voltage range	R_S = 50 Ω	25°C	− 11 to 11	− 13 to 13		− 11 to 11	− 13 to 13		V
			Full range	− 10.5 to 10.5			− 10.5 to 10.5			
V_{OM+}	Maximum positive peak output voltage swing	R_L = 600 Ω	25°C	10.5			10.5			V
			Full range	10			10			
		R_L = 2 kΩ	25°C	12			12			
			Full range	11			11			
V_{OM-}	Maximum negative peak output voltage swing	R_L = 600 Ω	25°C	− 10.5	− 13		−10.5	−13		V
			Full range	− 10			− 10			
		R_L = 2 kΩ	25°C	− 12	− 13.5		− 12	−13.5		
			Full range	− 11			− 11			
A_{VD}	Large-signal differential voltage amplification	V_O = ± 11 V, R_L = 2 kΩ	25°C	5	45		10	45		V/μV
		V_O = ± 10 V, R_L = 2 kΩ	Full range	2			4			
		V_O = ± 10 V, R_L = 1 kΩ	25°C	3.5	38		8	38		
			Full range	1			2.5			
		V_O = ± 10 V, R_L = 600 Ω	25°C	2	19		5	19		
			Full range	0.5			2			
c_i	Input capacitance		25°C		8			8		pF
z_o	Open-loop output impedance	I_O = 0	25°C		50			50		Ω
CMRR	Common-mode rejection ratio	V_{IC} = V_{ICR} min, R_S = 50 Ω	25°C	100	131		117	131		dB
			Full range	98			114			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm} / \Delta V_{IO}$)	$V_{CC\pm}$ = ± 4 V to ± 18 V, R_S = 50 Ω	25°C	94	144		110	144		dB
		$V_{CC\pm}$ = ± 4 V to ± 18 V, R_S = 50 Ω	Full range	92			106			
I_{CC}	Supply current	V_O = 0, No Load	25°C		3.8	5.3		3.8	4.7	mA
			Full range			5.6			4.8	

†Full range is 0°C to 70°C.

NOTE 4: Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at T_A = 150°C extrapolated to T_A = 25°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

operating characteristics at specified free-air temperature, $V_{CC\pm} = \pm 15$ V

PARAMETER		TEST CONDITIONS	T_A†	TLE2027C			TLE2027AC			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
SR	Slew rate at unity gain	$R_L = 2$ kΩ, $C_L = 100$ pF, See Figure 1	25°C	1.7	2.8		1.7	2.8		V/μs
			Full range	1.2			1.2			
V_n	Equivalent input noise voltage (see Figure 2)	$R_S = 100$ Ω, f = 10 Hz	25°C		3.3	8		3.3	4.5	nV/√Hz
		$R_S = 100$ Ω, f = 1 kHz			2.5	4.5		2.5	3.8	
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 10 Hz	25°C		50	250		50	130	nV
I_n	Equivalent input noise current	f = 10 Hz	25°C		1.5	4		1.5	4	pA/√Hz
		f = 1 kHz			0.4	0.6		0.4	0.6	
THD	Total harmonic distortion	$V_O = \pm 10$ V, $A_{VD} = 1$, See Note 5	25°C		< 0.002%			< 0.002%		
B_1	Unity-gain bandwidth (see Figure 3)	$R_L = 2$ kΩ, $C_L = 100$ pF	25°C	7	13		9	13		MHz
B_{OM}	Maximum output-swing bandwidth	$R_L = 2$ kΩ	25°C		30			30		kHz
ϕ_m	Phase margin at unity gain (see Figure 3)	$R_L = 2$ kΩ, $C_L = 100$ pF	25°C		55°			55°		

†Full range is 0°C to 70°C.

NOTE 5: Measured distortion of the source used in the analysis was 0.002%.

electrical characteristics at specified free-air temperature, $V_{CC\pm}$ = ±15 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A†	TLE2027I			TLE2027AI			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_{IC} = 0, R_S = 50 Ω	25°C		20	100		10	25	μV
			Full range			180			105	
α_{VIO}	Temperature coefficient of input offset voltage		Full range		0.4	1		0.2	1	μV/°C
	Input offset voltage long-term drift (see Note 4)		25°C		0.006	1		0.006	1	μV/mo
I_{IO}	Input offset current		25°C		6	90		6	90	nA
			Full range			150			150	
I_{IB}	Input bias current		25°C		15	90		15	90	nA
			Full range			150			150	
V_{ICR}	Common-mode input voltage range	R_S = 50 Ω	25°C	−11 to 11	−13 to 13		−11 to 11	−13 to 13		V
			Full range	−10.4 to 10.4			−10.4 to 10.4			
V_{OM+}	Maximum positive peak output voltage swing	R_L = 600 Ω	25°C	10.5			10.5			V
			Full range	10			10			
		R_L = 2 kΩ	25°C	12			12			
			Full range	11			11			
V_{OM-}	Maximum negative peak output voltage swing	R_L = 600 Ω	25°C	−10.5	−13		−10.5	−13		V
			Full range	−10			−10			
		R_L = 2 kΩ	25°C	−12	−13.5		−12	−13.5		
			Full range	−11			−11			
A_{VD}	Large-signal differential voltage amplification	V_O = ±11 V, R_L = 2 kΩ	25°C	5	45		10	45		V/μV
		V_O = ±10 V, R_L = 2 kΩ	Full range	2			3.5			
		V_O = ±10 V, R_L = 1 kΩ	25°C	3.5	38		8	38		
			Full range	1			2.2			
		V_O = ±10 V, R_L = 600 Ω	25°C	2	19		5	19		
			Full range	0.5			1.1			
c_i	Input capacitance		25°C		8			8		pF
z_o	Open-loop output impedance	I_O = 0	25°C		50			50		Ω
CMRR	Common-mode rejection ratio	V_{IC} = V_{ICR} min, R_S = 50 Ω	25°C	100	131		117	131		dB
			Full range	96			113			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm} / \Delta V_{IO}$)	$V_{CC\pm}$ = ±4 V to ±18 V, R_S = 50 Ω	25°C	94	144		110	144		dB
		$V_{CC\pm}$ = ±4 V to ±18 V, R_S = 50 Ω	Full range	90			105			
I_{CC}	Supply current	V_O = 0, No Load	25°C		3.8	5.3		3.8	4.7	mA
			Full range			5.6			4.9	

†Full range is −40°C to 105°C.

NOTE 4: Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at T_A = 150°C extrapolated to T_A = 25°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

operating characteristics at specified free-air temperature, $V_{CC\pm}$ = ±15 V

PARAMETER		TEST CONDITIONS	T_A†	TLE2027I			TLE2027AI			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
SR	Slew rate at unity gain	R_L = 2 kΩ, C_L = 100 pF, See Figure 1	25°C	1.7	2.8		1.7	2.8		V/μs
			Full range	1.1			1.1			
V_n	Equivalent input noise voltage (see Figure 2)	R_S = 100 Ω, f = 10 Hz	25°C		3.3	8		3.3	4.5	nV/√Hz
		R_S = 100 Ω, f = 1 kHz			2.5	4.5		2.5	3.8	
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 10 Hz	25°C		50	250		50	130	nV
I_n	Equivalent input noise current	f = 10 Hz	25°C		1.5	4		1.5	4	pA/√Hz
		f = 1 kHz			0.4	0.6		0.4	0.6	
THD	Total harmonic distortion	V_O = ±10 V, A_{VD} = 1, See Note 5	25°C		< 0.002%			< 0.002%		
B_1	Unity-gain bandwidth (see Figure 3)	R_L = 2 kΩ, C_L = 100 pF	25°C	7	13		9	13		MHz
B_{OM}	Maximum output-swing bandwidth	R_L = 2 kΩ	25°C		30			30		kHz
ϕ_m	Phase margin at unity gain (see Figure 3)	R_L = 2 kΩ, C_L = 100 pF	25°C		55°			55°		

†Full range is −40°C to 105°C.

NOTE 5: Measured distortion of the source used in the analysis was 0.002%.

electrical characteristics at specified free-air temperature, $V_{CC\pm} = \pm 15$ V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A†	TLE2027M			TLE2027AM			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	$V_{IC} = 0$, $R_S = 50\ \Omega$	25°C		20	100		10	25	µV
			Full range			200			105	
α_{VIO}	Temperature coefficient of input offset voltage		Full range		0.4	1*		0.2	1*	µV/°C
	Input offset voltage long-term drift (see Note 4)		25°C		0.006	1*		0.006	1*	µV/mo
I_{IO}	Input offset current		25°C		6	90		6	90	nA
			Full range			150			150	
I_{IB}	Input bias current		25°C		15	90		15	90	nA
			Full range			150			150	
V_{ICR}	Common-mode input voltage range	$R_S = 50\ \Omega$	25°C	− 11 to 11	− 13 to 13		− 11 to 11	− 13 to 13		V
			Full range	− 10.3 to 10.3			− 10.4 to 10.4			
V_{OM+}	Maximum positive peak output voltage swing	$R_L = 600\ \Omega$	25°C	10.5			10.5			V
			Full range	10			10			
		$R_L = 2\ k\Omega$	25°C	12			12			
			Full range	11			11			
V_{OM-}	Maximum negative peak output voltage swing	$R_L = 600\ \Omega$	25°C	− 10.5	− 13		− 10.5	− 13		V
			Full range	− 10			− 10			
		$R_L = 2\ k\Omega$	25°C	− 12	− 13.5		− 12	− 13.5		
			Full range	− 11			− 11			
A_{VD}	Large-signal differential voltage amplification	$V_O = \pm 11$ V, $R_L = 2\ k\Omega$	25°C	5	45		10	45		V/µV
		$V_O = \pm 10$ V, $R_L = 2\ k\Omega$	Full range	2.5			3.5			
		$V_O = \pm 10$ V, $R_L = 1\ k\Omega$	25°C	3.5	38		8	38		
			Full range	1.8			2.2			
		$V_O = \pm 10$ V, $R_L = 600\ \Omega$	25°C	2	19		5	19		
c_i	Input capacitance		25°C		8			8		pF
z_o	Open-loop output impedance	$I_O = 0$	25°C		50			50		Ω
CMRR	Common-mode rejection ratio	$V_{IC} = V_{ICR}$ min, $R_S = 50\ \Omega$	25°C	100	131		117	131		dB
			Full range	96			113			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm} / \Delta V_{IO}$)	$V_{CC\pm} = \pm 4$ V to ± 18 V, $R_S = 50\ \Omega$	25°C	94	144		110	144		dB
		$V_{CC\pm} = \pm 4$ V to ± 18 V, $R_S = 50\ \Omega$	Full range	90			105			
I_{CC}	Supply current	$V_O = 0$, No Load	25°C		3.8	5.3		3.8	4.7	mA
			Full range			5.6			5	

*On products compliant to MIL-STD-883, Class B, this parameter is not production tested.

†Full range is −55°C to 125°C.

NOTE 4: Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at $T_A = 150°C$ extrapolated to $T_A = 25°C$ using the Arrhenius equation and assuming an activation energy of 0.96 eV.

operating characteristics, $V_{CC\pm} = \pm 15$ V, $T_A = 25°C$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A†	TLE2027M			TLE2027AM			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
SR	Slew rate at unity gain	$R_L = 2$ kΩ, $C_L = 100$ pF, See Figure 1	25°C	1.7	2.8		1.7	2.8		V/µs
			Full range	1			1			
V_n	Equivalent input noise voltage (see Figure 2)	$R_S = 100$ Ω, f = 10 Hz	25°C		3.3	8*		3.3	4.5*	nV/√Hz
		$R_S = 100$ Ω, f = 1 kHz			2.5	4.5*		2.5	3.8*	
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 10 Hz	25°C		50	250*		50	130*	nV
I_n	Equivalent input noise current	f = 10 Hz	25°C		1.5	4*		1.5	4*	pA/√Hz
		f = 1 kHz			0.4	0.6*		0.4	0.6*	
THD	Total harmonic distortion	$V_O = \pm 10$ V, $A_{VD} = 1$, See Note 5	25°C		< 0.002%			< 0.002%		
B_1	Unity-gain bandwidth (see Figure 3)	$R_L = 2$ kΩ, $C_L = 100$ pF	25°C	7*	13		9*	13		MHz
B_{OM}	Maximum output-swing bandwidth	$R_L = 2$ kΩ	25°C		30			30		kHz
ϕ_m	Phase margin at unity gain (see Figure 3)	$R_L = 2$ kΩ, $C_L = 100$ pF	25°C		55°			55°		

*On products compliant to MIL-STD-883, Class B, this parameter is not production tested.

†Full range is −55°C to 125°C.

NOTE 5: Measured distortion of the source used in the analysis was 0.002%.

PARAMETER MEASUREMENT INFORMATION

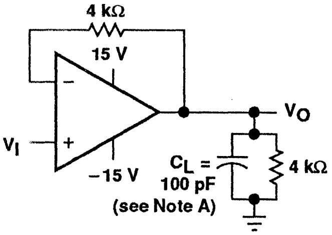


Figure 1. Slew Rate Test Circuit

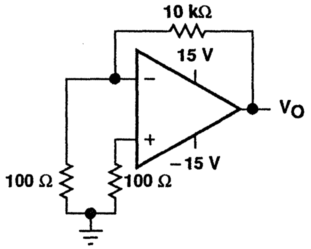


Figure 2. Noise Voltage Test Circuit

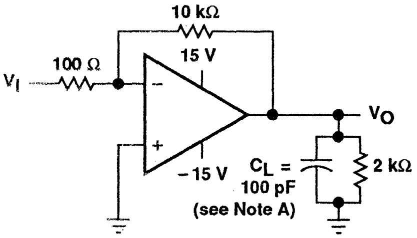


Figure 3. Unity-Gain Bandwidth and Phase Margin Test Circuit

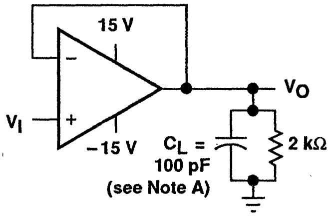


Figure 4. Small-Signal Pulse Response Test Circuit

NOTE A: C_L includes fixture capacitance.

PARAMETER MEASUREMENT INFORMATION

typical values

Typical values as presented in this data sheet represent the median (50% point) of device parametric performance.

initial estimates of parameter distributions

In the on-going program of improving data sheets and supplying more information to our customer, Texas Instruments has added an estimate of not only the "typical" values but also the spread around these values. These are in the form of distribution bars that show the 95% (upper) points and the 5% (lower) points from our characterization of the initial wafer lots of this new device type (see Figure 5). The distribution bars are shown at the points where data was actually collected. The 95% and 5% points are used instead of ±3 sigma since some of the distributions are not true Gaussian distributions.

The number of units tested and the number of different wafer lots used are on all of the graphs where distribution bars are shown. As noted in Figure 5, there were a total of 835 units from 2 wafer lots. In this case, there is a very good estimate for the within-lot variability and a possibly poor estimate of the lot-to-lot variability. This will always be the case on newly released products since there will only be data available from a few wafer lots.

The distribution bars are not intended to replace the minimum and maximum limits in the electrical tables. Each distribution bar represents 90% of the total units tested at a specific temperature. While 10% of the units tested fell outside any given distribution bar, this should not be interpreted to mean that the same individual devices fell outside every distribution bar.

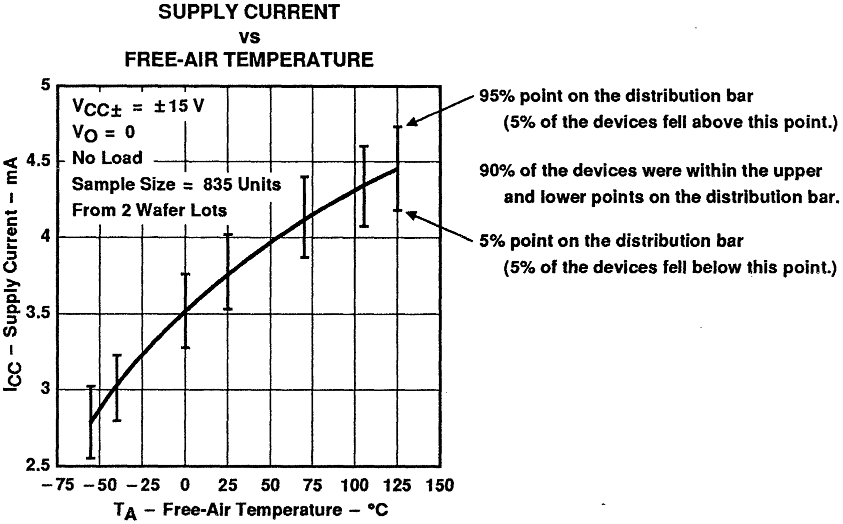


Figure 5. Sample Graph with Distribution Bars

TYPICAL CHARACTERISTICS

table of graphs

			FIGURE
V_{IO}	Input offset voltage	Distribution	6
ΔV_{IO}	Input offset voltage change	vs Time after power on	7, 8
I_{IO}	Input offset current	vs Temperature	9
I_{IB}	Input bias current	vs Common-mode input voltage vs Temperature	10 11
I_I	Input current	vs Differential input voltage	12
$V_{O(PP)}$	Maximum peak-to-peak output voltage	vs Frequency	13
V_{OM}	Maximum peak output voltage	vs Load resistance vs Temperature	14, 15 16, 17
A_{VD}	Large-signal differential voltage amplification	vs Supply voltage vs Load resistance vs Frequency vs Temperature	18 20 19, 21 22
z_o	Output impedance	vs Frequency	23
CMRR	Common-mode rejection ratio	vs Frequency	24
k_{SVR}	Supply voltage rejection ratio	vs Frequency	25
I_{OS}	Short-circuit output current	vs Supply voltage vs Time vs Temperature	26, 27 28, 29 30, 31
I_{CC}	Supply current	vs Supply voltage vs Temperature	32 33
	Pulse response	Small-signal Large-signal	34 35
V_n	Equivalent input noise voltage	vs Frequency	36
	Noise voltage (referred to input)	0.1 to 10 Hz	37
B_1	Unity-gain-bandwidth	vs Supply voltage vs Load capacitance	38 39
SR	Slew rate	vs Temperature	40
ϕ_m	Phase margin	vs Supply voltage vs Load capacitance vs Temperature	41 42 43
ϕ	Phase shift	vs Frequency	19, 21

TYPICAL CHARACTERISTICS†

TLE2027
DISTRIBUTION OF
INPUT OFFSET VOLTAGE

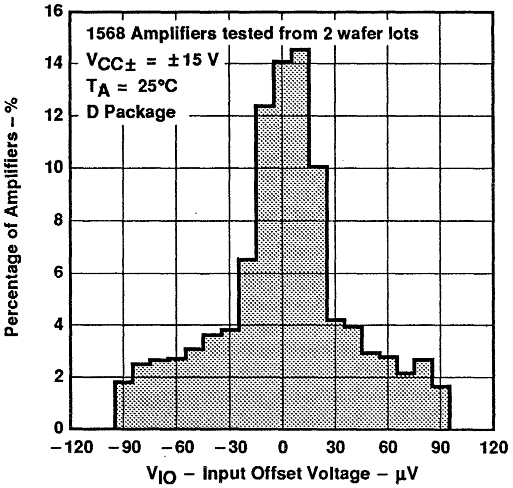


Figure 6

INPUT OFFSET VOLTAGE CHANGE
vs
TIME AFTER POWER ON

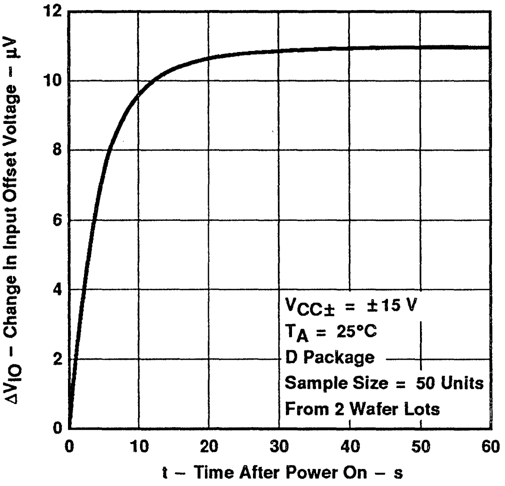


Figure 7

INPUT OFFSET VOLTAGE CHANGE
vs
TIME AFTER POWER ON

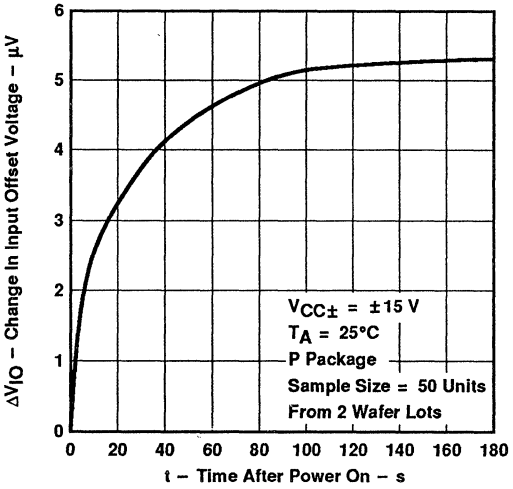


Figure 8

INPUT OFFSET CURRENT
vs
FREE-AIR TEMPERATURE

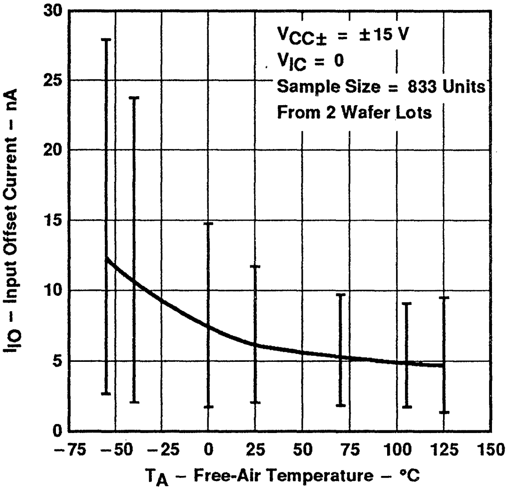


Figure 9

---

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

INPUT BIAS CURRENT vs COMMON-MODE INPUT VOLTAGE

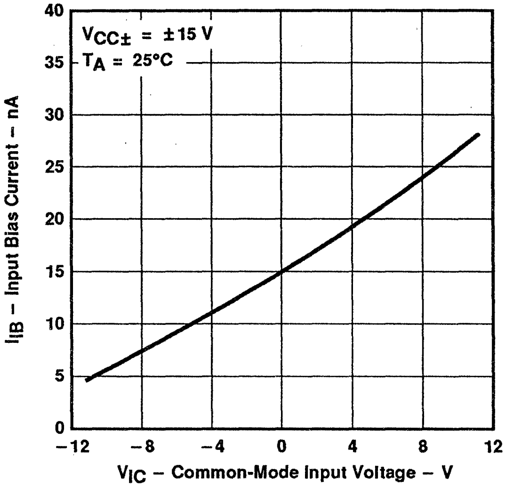


Figure 10

INPUT BIAS CURRENT vs FREE-AIR TEMPERATURE

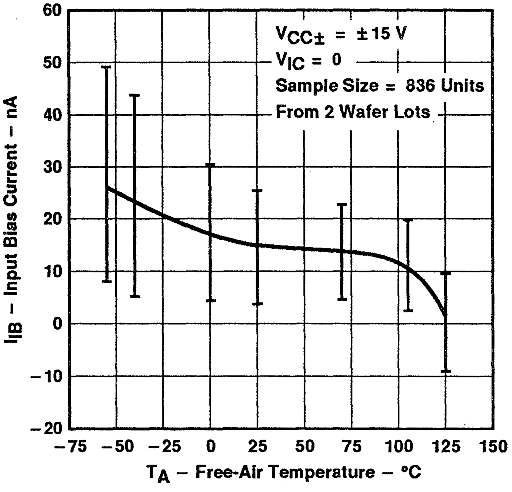


Figure 11

INPUT CURRENT vs DIFFERENTIAL INPUT VOLTAGE

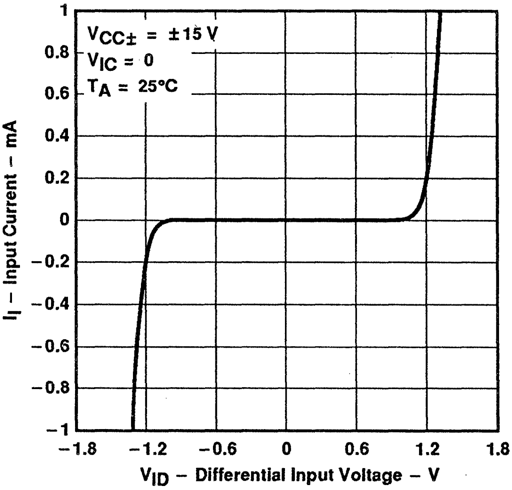


Figure 12

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE vs FREQUENCY

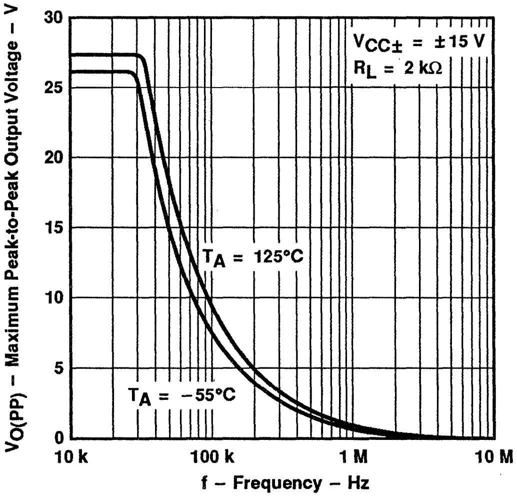


Figure 13

---

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

MAXIMUM POSITIVE PEAK OUTPUT VOLTAGE vs LOAD RESISTANCE

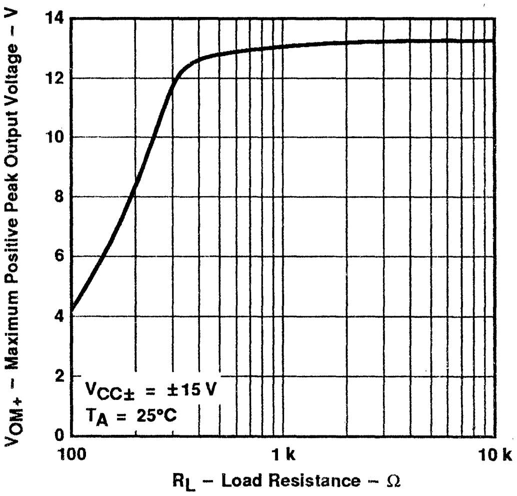


Figure 14

MAXIMUM NEGATIVE PEAK OUTPUT VOLTAGE vs LOAD RESISTANCE

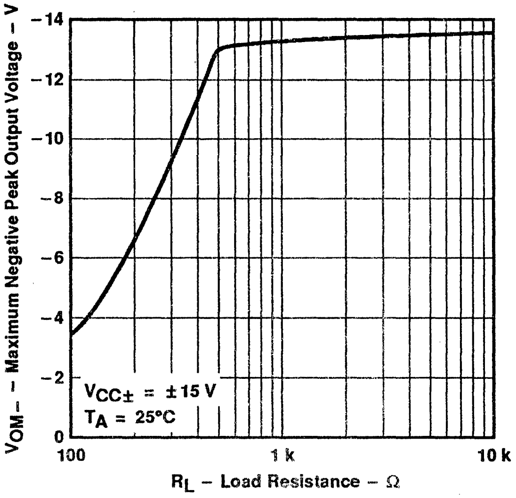


Figure 15

MAXIMUM POSITIVE PEAK OUTPUT VOLTAGE vs FREE-AIR TEMPERATURE

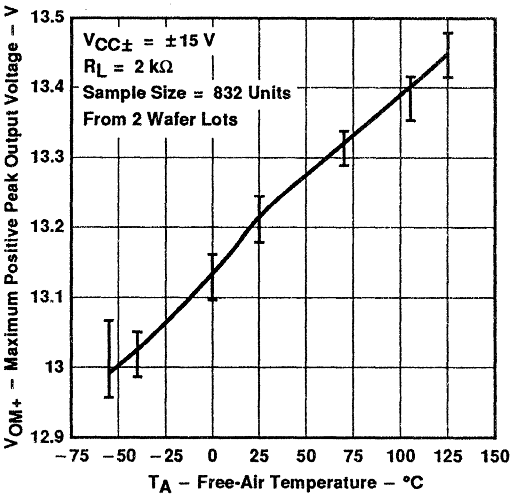


Figure 16

MAXIMUM NEGATIVE PEAK OUTPUT VOLTAGE vs FREE-AIR TEMPERATURE

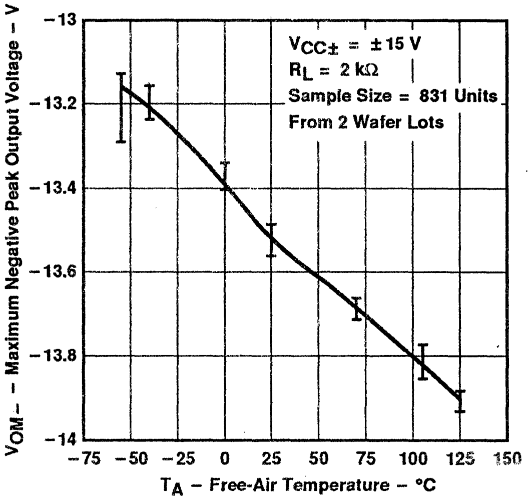


Figure 17

---

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS

LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION vs SUPPLY VOLTAGE

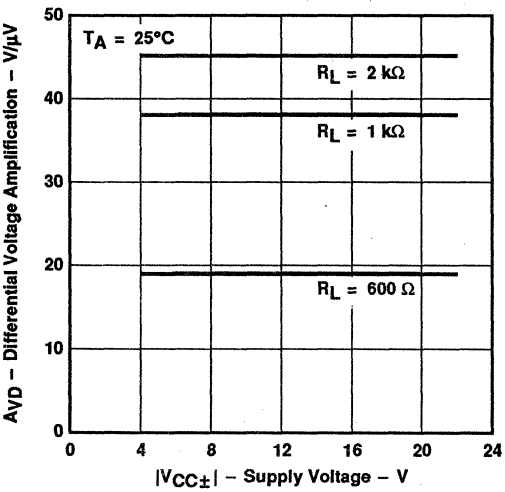


Figure 18

LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION AND PHASE SHIFT vs FREQUENCY

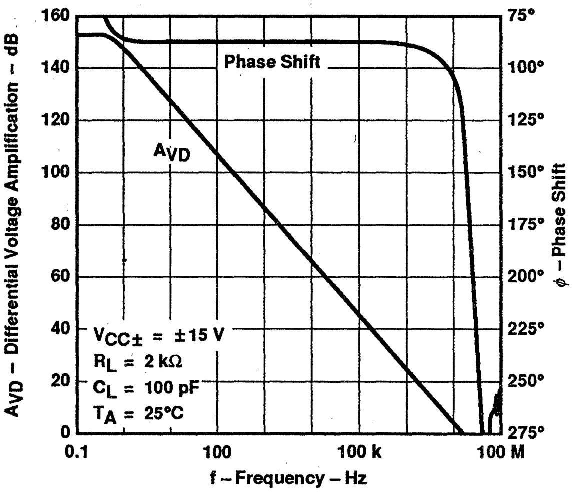


Figure 19

LARGE-SIGNAL VOLTAGE AMPLIFICATION vs LOAD RESISTANCE

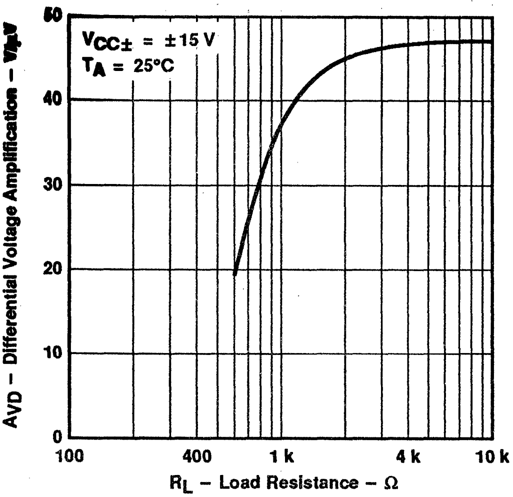


Figure 20

LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION AND PHASE SHIFT vs FREQUENCY

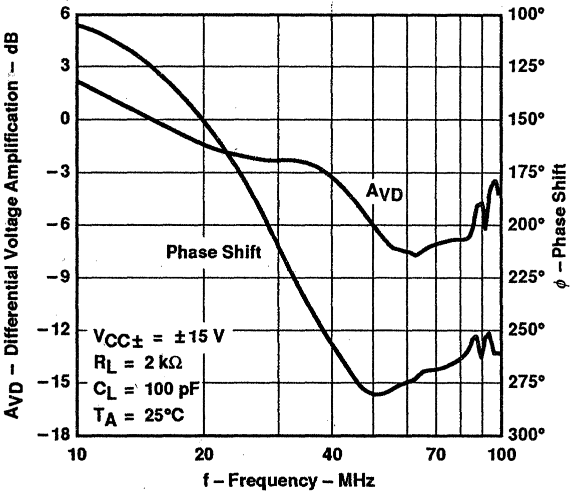


Figure 21

TYPICAL CHARACTERISTICS†

LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION vs FREE-AIR TEMPERATURE

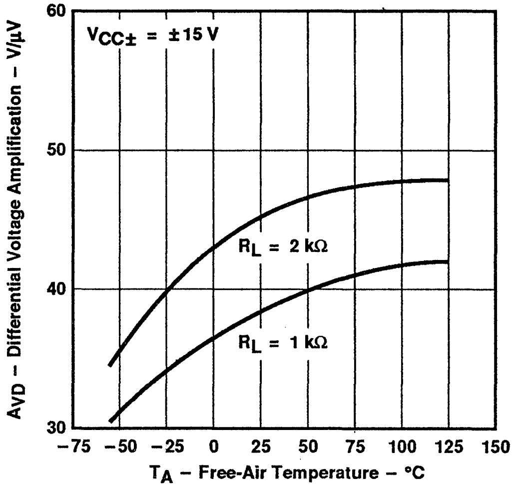


Figure 22

OUTPUT IMPEDANCE vs FREQUENCY

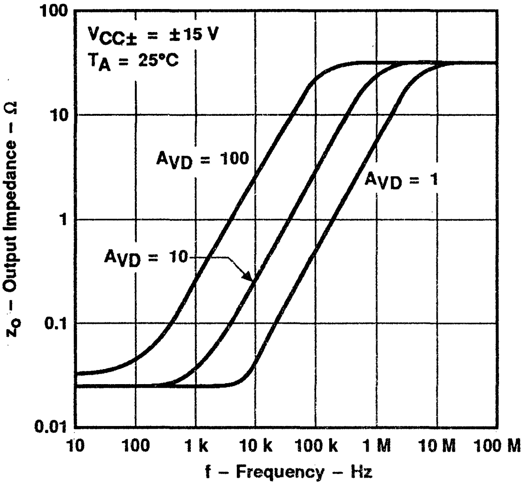


Figure 23

COMMON-MODE REJECTION RATIO vs FREQUENCY

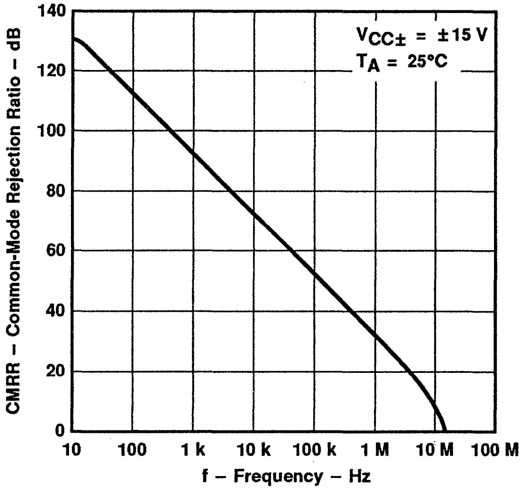


Figure 24

SUPPLY VOLTAGE REJECTION RATIO vs FREQUENCY

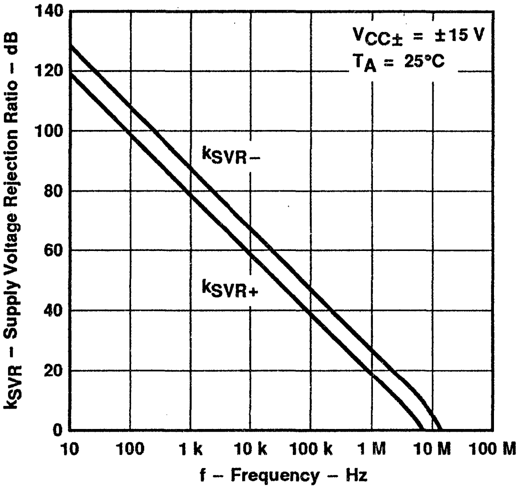


Figure 25

---

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS

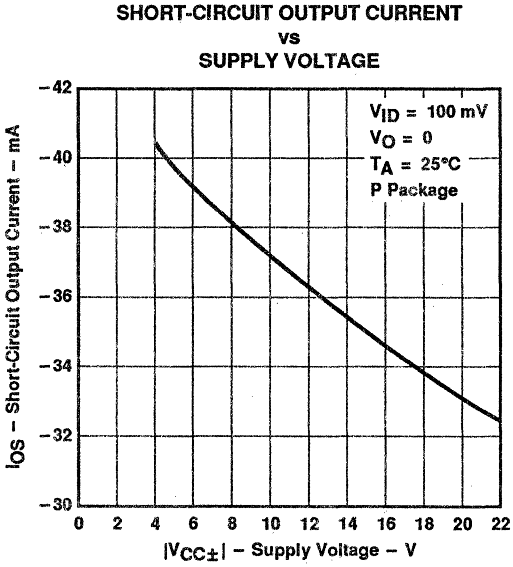


Figure 26

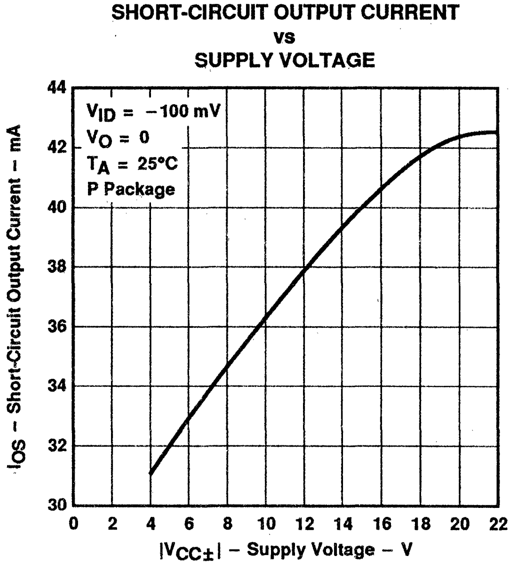


Figure 27

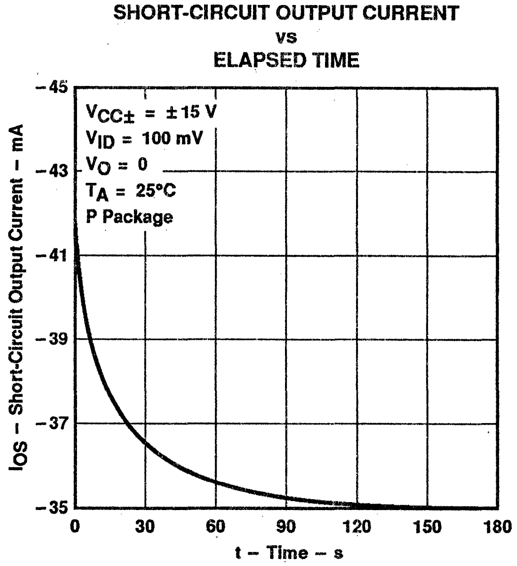


Figure 28

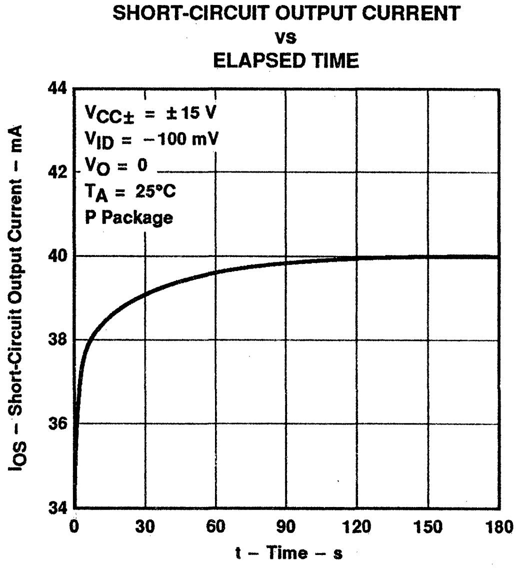


Figure 29

TYPICAL CHARACTERISTICS†

SHORT-CIRCUIT OUTPUT CURRENT vs FREE-AIR TEMPERATURE

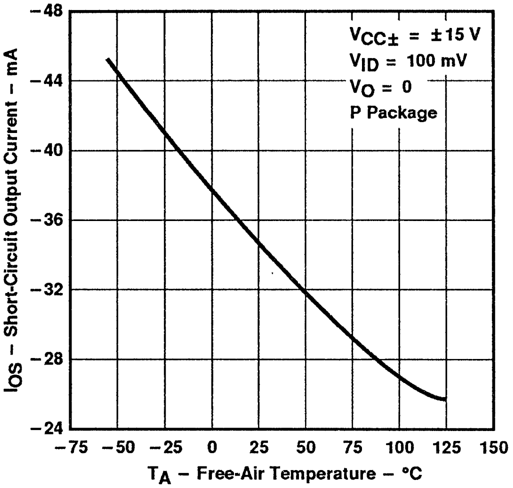


Figure 30

SHORT-CIRCUIT OUTPUT CURRENT vs FREE-AIR TEMPERATURE

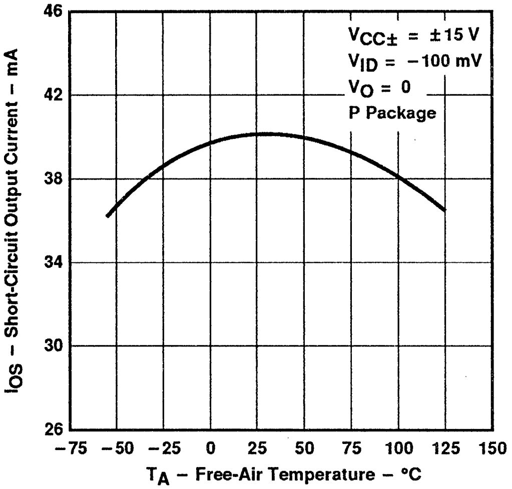


Figure 31

SUPPLY CURRENT vs SUPPLY VOLTAGE

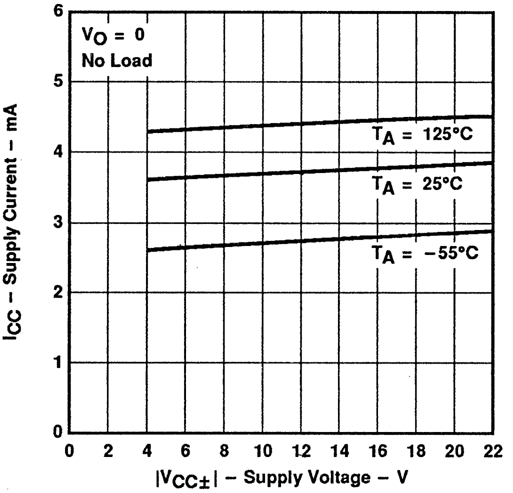


Figure 32

SUPPLY CURRENT vs FREE-AIR TEMPERATURE

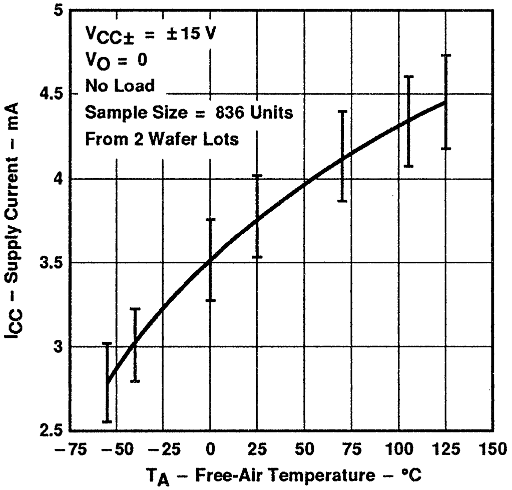


Figure 33

---

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS

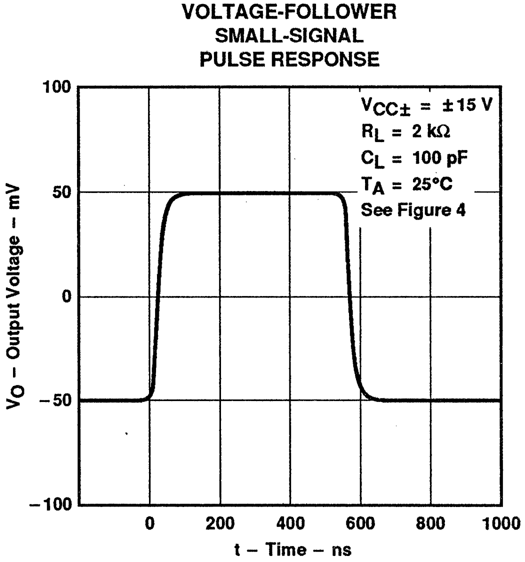


Figure 34

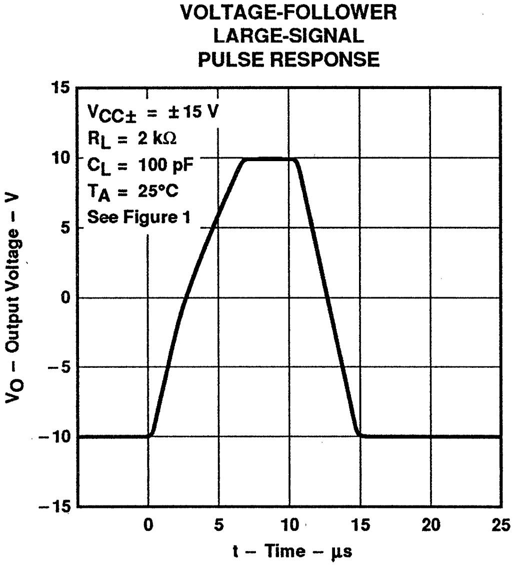


Figure 35

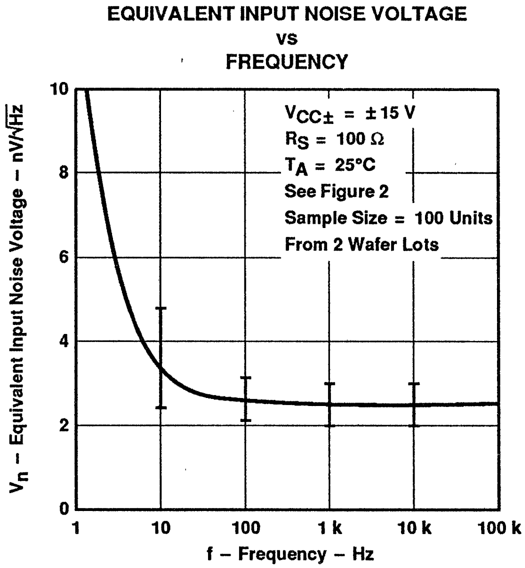


Figure 36

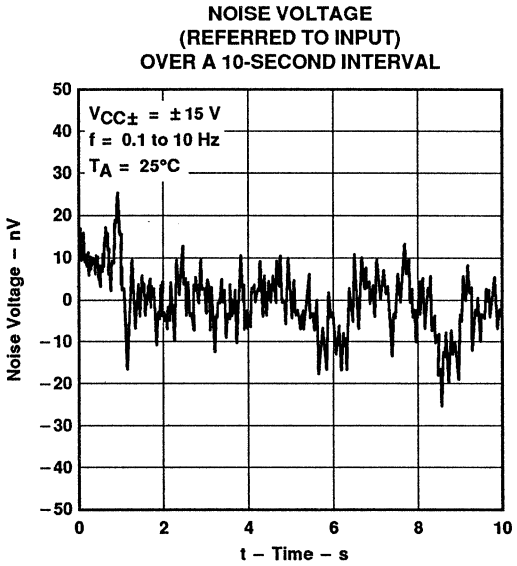


Figure 37

TYPICAL CHARACTERISTICS†

UNITY-GAIN BANDWIDTH
vs
SUPPLY VOLTAGE

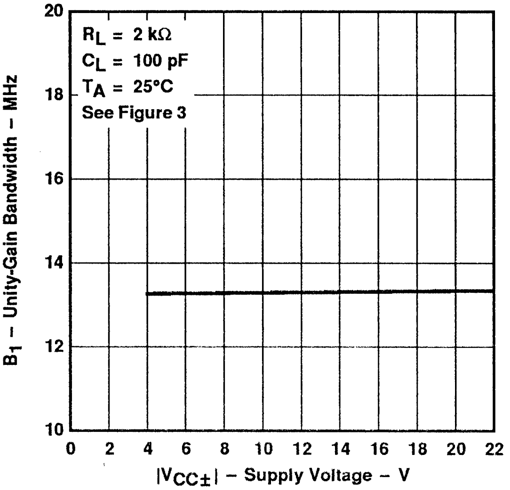


Figure 38

UNITY-GAIN BANDWIDTH
vs
LOAD CAPACITANCE

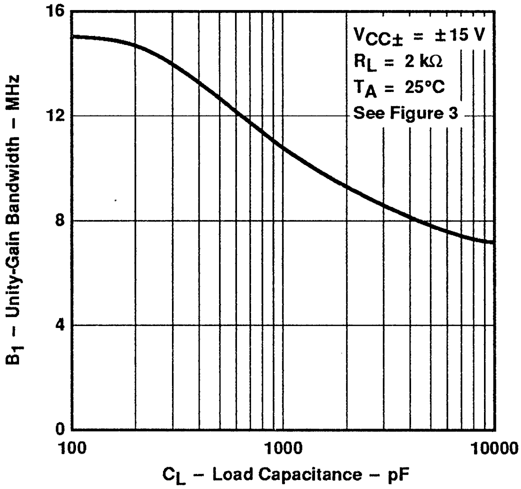


Figure 39

SLEW RATE
vs
FREE-AIR TEMPERATURE

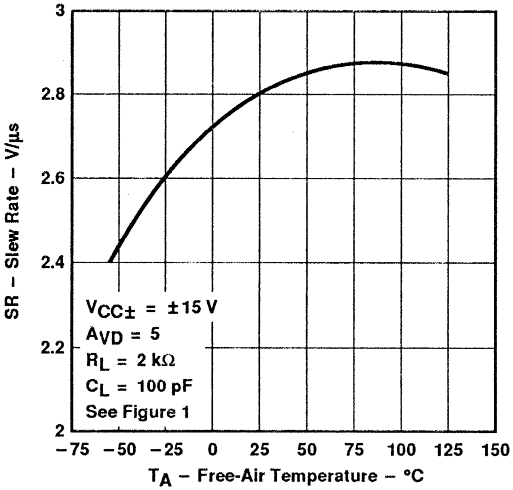


Figure 40

PHASE MARGIN
vs
SUPPLY VOLTAGE

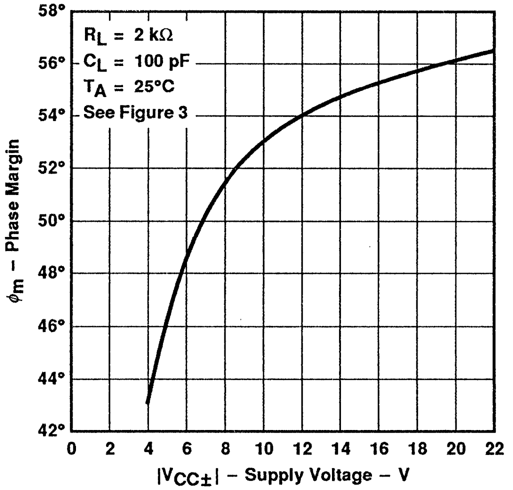


Figure 41

---

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

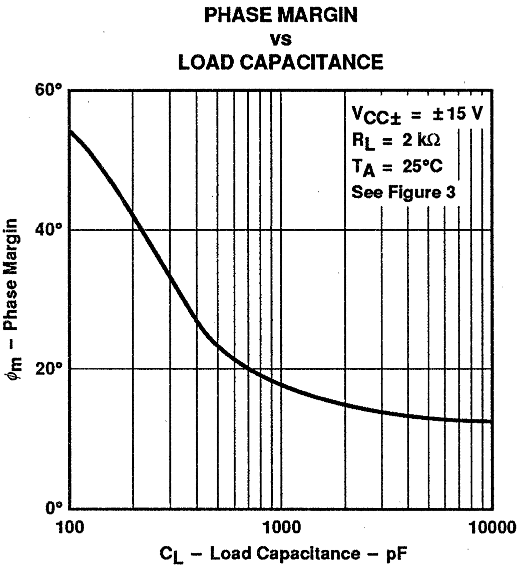


Figure 42

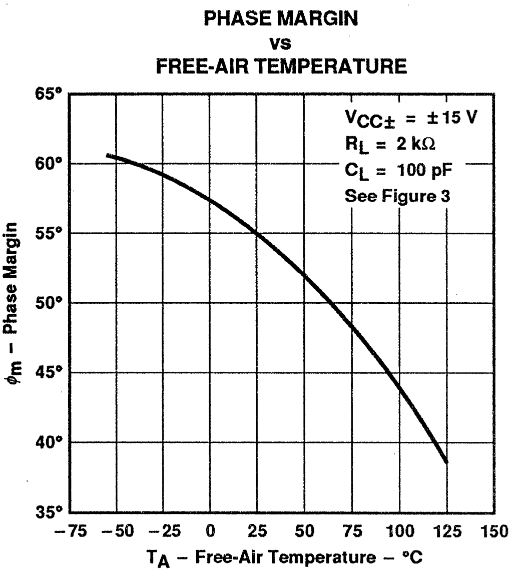


Figure 43

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

APPLICATION INFORMATION

macromodel information

Macromodel information provided was derived using *PSpice® Parts*™ model generation software. The Boyle macromodel (see Note 6) and subcircuit in Figures 44 and 45 were generated using the TLE2027 typical electrical and operating characteristics at 25°C. Using this information, output simulations of the following key parameters can be generated to a tolerance of 20% (in most cases):

- Maximum positive output voltage swing
- Maximum negative output voltage swing
- Slew rate
- Quiescent power dissipation
- Input bias current
- Open-loop voltage amplification
- Gain-bandwidth product
- Common-mode rejection ratio
- Phase margin
- DC output resistance
- AC output resistance
- Short-circuit output current limit

NOTE 6: G. R. Boyle, B. M. Cohn, D. O. Pederson, and J. E. Solomon, "Macromodeling of Integrated Circuit Operational Amplifiers", *IEEE Journal of Solid-State Circuits*, SC-9, 353 (1974).

APPLICATION INFORMATION

macromodel information (continued)

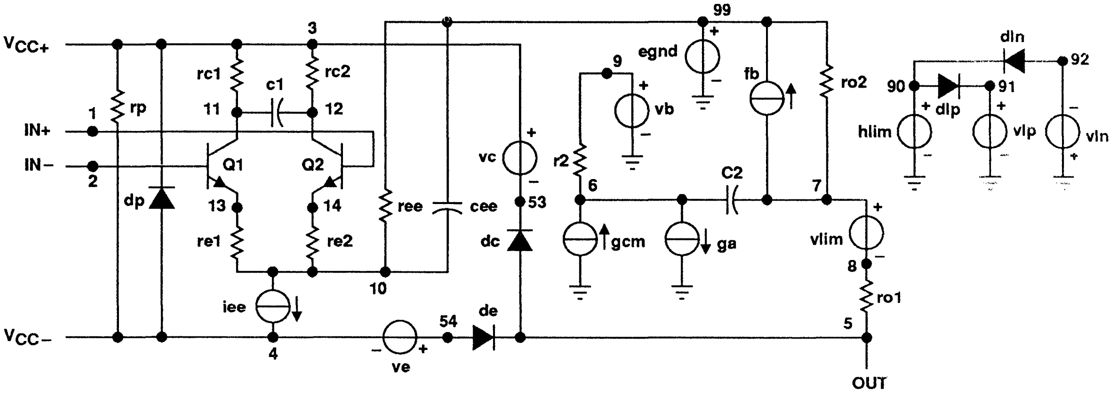


Figure 44. Boyle Macromodel

```
.subckt TLE2027  1 2 3 4 5
*
  c1   11 12 4.003E-12
  c2    6  7 20.00E-12
  dc    5 53 dx
  de   54  5 dx
  dlp  90 91 dx
  dln  92 90 dx
  dp    4  3 dx
  egnd 99  0 poly(2)  (3,0)  (4,0)  0 .5 .5
  fb    7 99 poly(5) vb vc ve vlp vln 0 954.8E6 -1E9 1E9 1E9 -1E9
  ga    6  0 11 12 2.062E-3
  gcm   0  6 10 99 531.3E-12
  iee  10  4 dc 56.01E-6
  hlim 90  0 vlim 1K
  q1   11  2 13 qx
  q2   12  1 14 qx
  r2    6  9 100.0E3
  rc1   3 11 530.5
  rc2   3 12 530.5
  re1  13 10 -393.2
  re2  14 10 -393.2
  ree  10 99 3.571E6
  ro1   8  5 25
  ro2   7 99 25
  rp    3  4 8.013E3
  vb    9  0 dc 0
  vc    3 53 dc 2.400
  ve   54  4 dc 2.100
  vlim  7  8 dc 0
  vlp  91  0 dc 40
  vln   0 92 dc 40
.model dx D(Is=800.0E-18)
.model qx NPN(Is=800.0E-18 Bf=7.000E3)
.ends
```

Figure 45. Macromodel Subcircuit

APPLICATION INFORMATION

voltage-follower applications

The TLE2027 circuitry includes input protection diodes to limit the voltage across the input transistors; however, no provision is made in the circuit to limit the current if these diodes are forward-biased. Note that this condition can occur when the device is operated in the voltage-follower configuration and driven with a fast, large-signal pulse. It is recommended that a feedback resistor be used to limit the current to a maximum of 1 mA to prevent degradation of the device. Also, remember that this feedback resistor will form a pole with the input capacitance of the device. For feedback resistor values greater than 10 kΩ, this pole will degrade the amplifier's phase margin. This problem can be alleviated by adding a capacitor (20 pF to 50 pF) in parallel with the feedback resistor (see Figure 46).

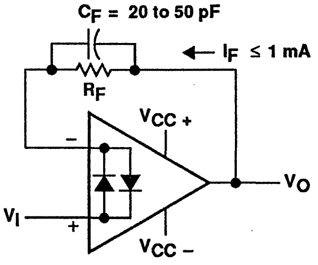


Figure 46. Voltage-Follower

input offset voltage nulling

The TLE2027 series offers external null pins that can be used to further reduce the input offset voltage. The circuits of Figure 47 can be connected as shown if the feature is desired. If external nulling is not needed, the null pins may be left disconnected.

(a) Standard Adjustment

(b) Adjustment with Improved Sensitivity

Figure 47. Input Offset Voltage Nulling Circuits

TLE2037, TLE2037A
EXCALIBUR LOW-NOISE HIGH-SPEED PRECISION DECOMPENSATED OPERATIONAL AMPLIFIERS

D3454, MAY 1990 – REVISED APRIL 1991

available features

- **Outstanding Combination of DC Precision and AC Performance:**
  Gain-Bandwidth Product . . . 80 MHz Typ
  V . . . 3.3 nV/√Hz at f = 10 Hz Typ,
  2.5 nV/√Hz at f = 1 kHz Typ
  V_{IO} . . . 25 μV Max
  A_{VD} . . . 45 V/μV Typ, With R_L = 2 kΩ,
  19 V/μV Typ, With R_L = 600 Ω
- **Available in Standard-Pinout Small-Outline Package**
- **Output Features Saturation Recovery Circuitry**
- **Macromodels and Statistical Information Included**

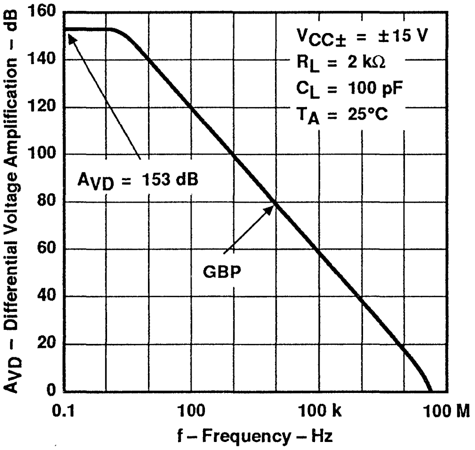
description

The TLE2037 and TLE2037A combine innovative circuit design expertise and high-quality process control techniques to produce a level of ac performance and dc precision previously unavailable in single operational amplifiers. Using the Texas Instruments state-of-the-art Excalibur process, these devices allow upgrades to systems that use lower-precision devices.

The TLE2037 and TLE2037A are decompensated versions of the TLE2027 and TLE2027A and are stable to a close-loop gain of 5. In the area of dc precision, these parts offer maximum offset voltages of 100 μV and 25 μV, respectively, common-mode rejection ratio of 131 dB (typ), supply voltage rejection ratio of 144 dB (typ), and dc gain of 45 V/μV (typ).

The ac performance is highlighted by a typical gain-bandwidth product specification of 80 MHz, 50° of phase margin, and noise voltage specifications of 3.3 nV/√Hz and 2.5 nV/√Hz at frequencies of 10 Hz and 1 kHz, respectively.

LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION vs FREQUENCY



Both the TLE2037 and TLE2037A are available in a wide variety of packages, including the industry-standard 8-pin small-outline version for high-density system applications. The C-suffix devices are characterized for operation from 0°C to 70°C. The I-suffix devices are characterized for operation from −40°C to 105°C. The M-suffix devices are characterized for operation over the full military temperature range of −55°C to 125°C.

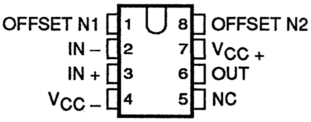
AVAILABLE OPTIONS

T_A	V_{IO} max AT 25°C	PACKAGE				
		SMALL-OUTLINE (D)	CHIP CARRIER (FK)	CERAMIC DIP (JG)	METAL CAN (L)	PLASTIC DIP (P)
0°C to 70°C	25 μV	TLE2037ACD	——	——	——	TLE2037ACP
	100 μV	TLE2037CD	——	——	——	TLE2037CP
– 40°C to 105°C	25 μV	TLE2037AID	——	——	——	TLE2037AIP
	100 μV	TLE2037ID	——	——	——	TLE2037IP
– 55°C to 125°C	25 μV	TLE2037AMD	TLE2037AMFK	TLE2037AMJG	TLE2037AML	TLE2037AMP
	100 μV	TLE2037MD	TLE2037MFK	TLE2037MJG	TLE2037ML	TLE2037MP

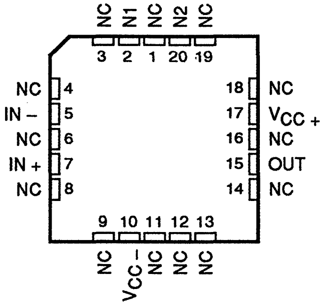
D packages are available taped and reeled. Add “R” suffix to device type, (e.g., TLE2037ACDR).

TEXAS INSTRUMENTS
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

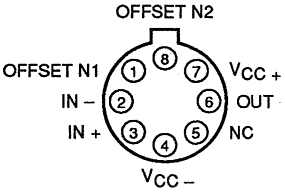
D, JG, OR P PACKAGE
(TOP VIEW)



FK PACKAGE
(TOP VIEW)



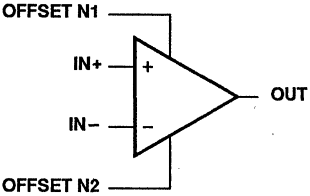
L PACKAGE
(TOP VIEW)



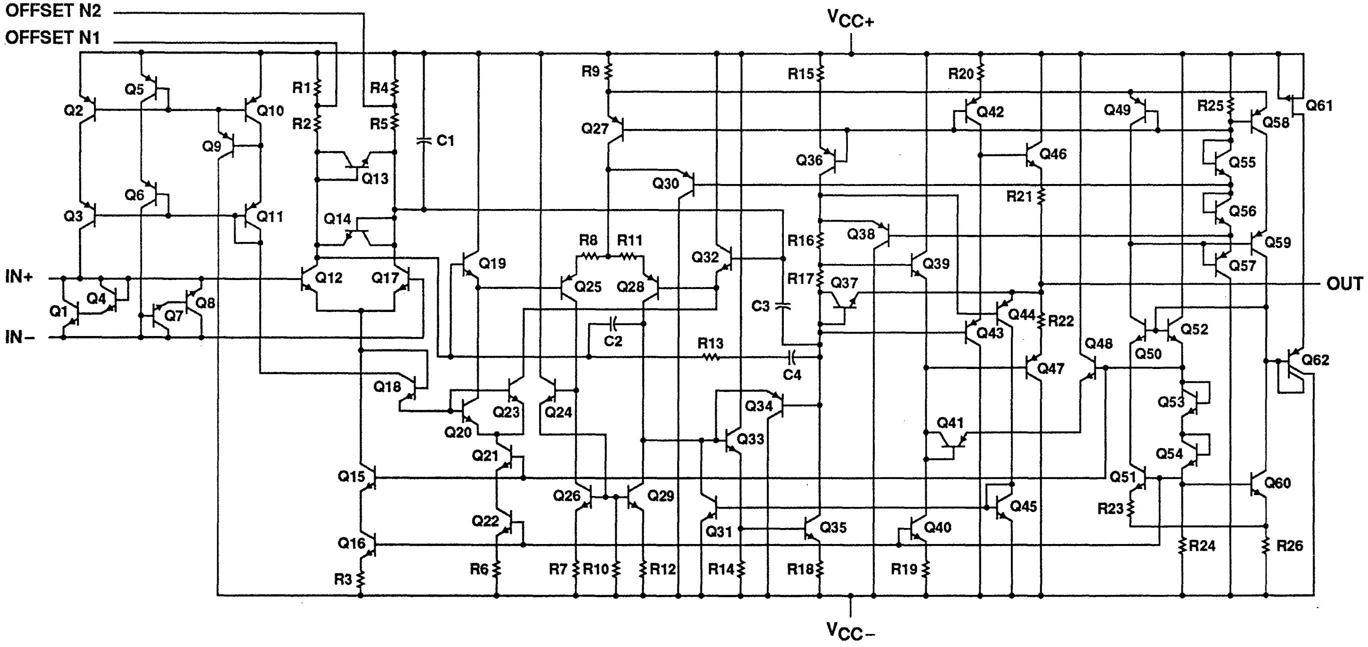
Pin 4 of the L package is in electrical contact with the case.

NC – No internal connection

symbol



equivalent schematic



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC+} (see Note 1)	22 V
Supply voltage, V_{CC-}	−22 V
Differential input voltage (see Note 2)	±1.2 V
Input voltage range, V_I (any input)	$V_{CC\pm}$
Input current, I_I (each input)	±1 mA
Output current, I_O	±50 mA
Total current into V_{CC+} terminal	50 mA
Total current out of V_{CC-} terminal	50 mA
Duration of short-circuit current at (or below) 25°C (see Note 3)	unlimited
Continuous total dissipation	See Dissipation Rating Table
Operating free-air temperature range, T_A: C-suffix	0°C to 70°C
I-suffix	−40°C to 105°C
M-suffix	−55°C to 125°C
Storage temperature range	−65°C to 150°C
Case temperature for 60 seconds: FK package	260°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D or P package	260°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: JG or L package	300°C

NOTES: 1. All voltage values, except differential voltages, are with respect to the midpoint between V_{CC+} and V_{CC-}.

2. Differential voltages are at the noninverting input with respect to the inverting input. Excessive current will flow if a differential input voltage in excess of approximately ±1.2 V is applied between the inputs unless some limiting resistance is used.

3. The output may be shorted to either supply. Temperature and/or supply voltages must be limited to ensure that the maximum dissipation rating is not exceeded.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 105°C$ POWER RATING	$T_A = 125°C$ POWER RATING
D	725 mW	5.8 mW/°C	464 mW	261 mW	145 mW
FK	1375 mW	11.0 mW/°C	880 mW	495 mW	275 mW
JG	1050 mW	8.4 mW/°C	672 mW	378 mW	210 mW
L	650 mW	5.2 mW/°C	416 mW	234 mW	130 mW
P	1000 mW	8.0 mW/°C	640 mW	360 mW	200 mW

recommended operating conditions

		C-SUFFIX		I-SUFFIX		M-SUFFIX		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
Supply voltage, $V_{CC\pm}$		± 4	± 22	± 4	± 22	± 4	± 22	V
Common-mode input voltage, V_{IC}	T_A = 25°C	− 11	11	− 11	11	− 11	11	V
	T_A = Full range	− 10.5	10.5	− 10.4	10.4	− 10.2	10.2	
Operating free-air temperature, T_A		0	70	− 40	105	− 55	125	°C

electrical characteristics at specified free-air temperature, $V_{CC\pm}$ = ±15 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A†	TLE2037C			TLE2037AC			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_{IC} = 0, R_S = 50 Ω	25°C		20	100		10	25	µV
			Full range			145			70	
α_{VIO}	Temperature coefficient of input offset voltage		Full range		0.4	1		0.2	1	µV/°C
	Input offset voltage long-term drift (see Note 4)		25°C		0.006	1		0.006	1	µV/mo
I_{IO}	Input offset current		25°C		6	90		6	90	nA
			Full range			150			150	
I_{IB}	Input bias current		25°C		15	90		15	90	nA
			Full range			150			150	
V_{ICR}	Common-mode input voltage range	R_S = 50 Ω	25°C	− 11 to 11	− 13 to 13		− 11 to 11	− 13 to 13		V
			Full range	− 10.5 to 10.5			− 10.5 to 10.5			
V_{OM+}	Maximum positive peak output voltage swing	R_L = 600 Ω	25°C	10.5	12.9		10.5	12.9		V
			Full range	10			10			
		R_L = 2 kΩ	25°C	12	13.2		12	13.2		
			Full range	11			11			
V_{OM-}	Maximum negative peak output voltage swing	R_L = 600 Ω	25°C	− 10.5	− 13		− 10.5	− 13		V
			Full range	− 10			− 10			
		R_L = 2 kΩ	25°C	− 12	− 13.5		− 12	− 13.5		
			Full range	− 11			− 11			
A_{VD}	Large-signal differential voltage amplification	V_O = ± 11 V, R_L = 2 kΩ	25°C	5	45		10	45		V/µV
		V_O = ± 10 V, R_L = 2 kΩ	Full range	2			4			
		V_O = ± 10 V, R_L = 1 kΩ	25°C	3.5	38		8	38		
			Full range	1			2.5			
		V_O = ± 10 V, R_L = 600 Ω	25°C	2	19		5	19		
			Full range	0.5			2			
c_i	Input capacitance		25°C		8			8		pF
z_o	Open-loop output impedance	I_O = 0	25°C		50			50		Ω
CMRR	Common-mode rejection ratio	V_{IC} = V_{ICR} min, R_S = 50 Ω	25°C	100	131		117	131		dB
			Full range	98			114			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm} / \Delta V_{IO}$)	$V_{CC\pm}$ = ± 4 V to ± 18 V, R_S = 50 Ω	25°C	94	144		110	144		dB
		$V_{CC\pm}$ = ± 4 V to ± 18 V, R_S = 50 Ω	Full range	92			106			
I_{CC}	Supply current	V_O = 0, No Load	25°C		3.8	5.3		3.8	4.7	mA
			Full range			5.6			4.8	

†Full range is 0°C to 70°C.

NOTE 4: Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at T_A = 150°C extrapolated to T_A = 25°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

operating characteristics at specified free-air temperature, $V_{CC\pm} = \pm 15$ V

PARAMETER		TEST CONDITIONS	T_A†	TLE2037C			TLE2037AC			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
SR	Slew rate	$A_{VD} = 5$, $R_L = 2$ kΩ, $C_L = 100$ pF, See Figure 1	25°C	6	7.5		6	7.5		V/µs
			Full range	5			5			
V_n	Equivalent input noise voltage (see Figure 2)	$R_S = 100$ Ω, f = 10 Hz	25°C		3.3	8		3.3	4.5	nV/√Hz
		$R_S = 100$ Ω, f = 1 kHz			2.5	4.5		2.5	3.8	
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 10 Hz	25°C		50	250		50	130	nV
I_n	Equivalent input noise current	f = 10 Hz	25°C		1.5	4		1.5	4	pA/√Hz
		f = 1 kHz			0.4	0.6		0.4	0.6	
THD	Total harmonic distortion	$V_O = \pm 10$ V, $A_{VD} = 5$, See Note 5	25°C		< 0.002%			< 0.002%		
	Gain-bandwidth product	f = 100 kHz, $R_L = 2$ kΩ, $C_L = 100$ pF	25°C	50	76		50	76		MHz
B_{OM}	Maximum output-swing bandwidth	$R_L = 2$ kΩ	25°C		80			80		kHz
ϕ_m	Phase margin	$R_L = 2$ kΩ, $C_L = 100$ pF	25°C		50°			50°		

†Full range is 0°C to 70°C.

NOTE 5: Measured distortion of the source used in the analysis was 0.002%.

electrical characteristics at specified free-air temperature, $V_{CC\pm}$ = ±15 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A†	TLE2037I			TLE2037AI			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_{IC} = 0, R_S = 50 Ω	25°C		20	100		10	25	μV
			Full range			180			105	
α_{VIO}	Temperature coefficient of input offset voltage		Full range		0.4	1		0.2	1	μV/°C
	Input offset voltage long-term drift (see Note 4)		25°C		0.006	1		0.006	1	μV/mo
I_{IO}	Input offset current		25°C		6	90		6	90	nA
			Full range			150			150	
I_{IB}	Input bias current		25°C		15	90		15	90	nA
			Full range			150			150	
V_{ICR}	Common-mode input voltage range	R_S = 50 Ω	25°C	−11 to 11	−13 to 13		−11 to 11	−13 to 13		V
			Full range	−10.4 to 10.4			−10.4 to 10.4			
V_{OM+}	Maximum positive peak output voltage swing	R_L = 600 Ω	25°C	10.5	12.9		10.5	12.9		V
			Full range	10			10			
		R_L = 2 kΩ	25°C	12	13.2		12	13.2		
			Full range	11			11			
V_{OM-}	Maximum negative peak output voltage swing	R_L = 600 Ω	25°C	−10.5	−13		−10.5	−13		V
			Full range	−10			−10			
		R_L = 2 kΩ	25°C	−12	−13.5		−12	−13.5		
			Full range	−11			−11			
A_{VD}	Large-signal differential voltage amplification	V_O = ±11 V, R_L = 2 kΩ	25°C	5	45		10	45		V/μV
		V_O = ±10 V, R_L = 2 kΩ	Full range	2.5			3.5			
		V_O = ±10 V, R_L = 1 kΩ	25°C	3.5	38		8	38		
			Full range	1.8			2.2			
		V_O = ±10 V, R_L = 600 Ω	25°C	2	19		5	19		
			Full range	0.5			1.1			
c_i	Input capacitance		25°C		8			8		pF
z_o	Open-loop output impedance	I_O = 0	25°C		50			50		Ω
CMRR	Common-mode rejection ratio	V_{IC} = V_{ICR} min, R_S = 50 Ω	25°C	100	131		117	131		dB
			Full range	96			113			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm}/\Delta V_{IO}$)	$V_{CC\pm}$ = ±4 V to ±18 V, R_S = 50 Ω	25°C	94	144		110	144		dB
		$V_{CC\pm}$ = ±4 V to ±18 V, R_S = 50 Ω	Full range	90			105			
I_{CC}	Supply current	V_O = 0, No Load	25°C		3.8	5.3		3.8	4.7	mA
			Full range			5.6			4.9	

†Full range is −40°C to 105°C.

NOTE 4: Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at T_A = 150°C extrapolated to T_A = 25°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

operating characteristics at specified free-air temperature, $V_{CC\pm} = \pm 15$ V

PARAMETER		TEST CONDITIONS	T_A†	TLE2037I			TLE2037AI			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
SR	Slew rate	A_{VD} = 5, R_L = 2 kΩ, C_L = 100 pF, See Figure 1	25°C	6	7.5		6	7.5		V/μs
			Full range	4.7			4.7			
V_n	Equivalent input noise voltage (see Figure 2)	R_S = 100 Ω, f = 10 Hz	25°C		3.3	8		3.3	4.5	nV/√Hz
		R_S = 100 Ω, f = 1 kHz			2.5	4.5		2.5	3.8	
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 10 Hz	25°C		50	250		50	130	nV
I_n	Equivalent input noise current	f = 10 Hz	25°C		1.5	4		1.5	4	pA/√Hz
		f = 1 kHz			0.4	0.6		0.4	0.6	
THD	Total harmonic distortion	V_O = ± 10 V, A_{VD} = 5, See Note 5	25°C		< 0.002%			< 0.002%		
	Gain-bandwidth product	f = 100 kHz, R_L = 2 kΩ, C_L = 100 pF	25°C	50	76		50	76		MHz
B_{OM}	Maximum output-swing bandwidth	R_L = 2 kΩ	25°C		80			80		kHz
ϕ_m	Phase margin	R_L = 2 kΩ, C_L = 100 pF	25°C		50°			50°		

†Full range is – 40°C to 105°C.
NOTE 5: Measured distortion of the source used in the analysis was 0.002%.

electrical characteristics at specified free-air temperature, $V_{CC\pm} = \pm 15$ V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A†	TLE2037M			TLE2037AM			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	$V_{IC} = 0$, $R_S = 50\ \Omega$	25°C		20	100		10	25	μV
			Full range			200			105	
α_{VIO}	Temperature coefficient of input offset voltage		Full range		0.4	1*		0.2	1*	μV/°C
	Input offset voltage long-term drift (see Note 4)		25°C		0.006	1		0.006	1	μV/mo
I_{IO}	Input offset current		25°C		6	90		6	90	nA
			Full range			150			150	
I_{IB}	Input bias current		25°C		15	90		15	90	nA
			Full range			150			150	
V_{ICR}	Common-mode input voltage range	$R_S = 50\ \Omega$	25°C	−11 to 11	−13 to 13		−11 to 11	−13 to 13		V
			Full range	−10.3 to 10.3			−10.4 to 10.4			
V_{OM+}	Maximum positive peak output voltage swing	$R_L = 600\ \Omega$	25°C	10.5	12.9		10.5	12.9		V
			Full range	10			10			
		$R_L = 2\ k\Omega$	25°C	12	13.2		12	13.2		
			Full range	11			11			
V_{OM-}	Maximum negative peak output voltage swing	$R_L = 600\ \Omega$	25°C	−10.5	−13		−10.5	−13		V
			Full range	−10			−10			
		$R_L = 2\ k\Omega$	25°C	−12	−13.5		−12	−13.5		
			Full range	−11			−11			
A_{VD}	Large-signal differential voltage amplification	$V_O = \pm 11$ V, $R_L = 2\ k\Omega$	25°C	5	45		10	45		V/μV
		$V_O = \pm 10$ V, $R_L = 2\ k\Omega$	Full range	2.5			3.5			
		$V_O = \pm 10$ V, $R_L = 1\ k\Omega$	25°C	3.5	38		8	38		
			Full range	1.8			2.2			
		$V_O = \pm 10$ V, $R_L = 600\ \Omega$	25°C	2	19		5	19		
c_i	Input capacitance		25°C		8			8		pF
z_o	Open-loop output impedance	$I_O = 0$	25°C		50			50		Ω
CMRR	Common-mode rejection ratio	$V_{IC} = V_{ICR}$ min, $R_S = 50\ \Omega$	25°C	100	131		117	131		dB
			Full range	96			113			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm} / \Delta V_{IO}$)	$V_{CC\pm} = \pm 4$ V to ± 18 V, $R_S = 50\ \Omega$	25°C	94	144		110	144		dB
		$V_{CC\pm} = \pm 4$ V to ± 18 V, $R_S = 50\ \Omega$	Full range	90			105			
I_{CC}	Supply current	$V_O = 0$, No Load	25°C		3.8	5.3		3.8	4.7	mA
			Full range			5.6			5	

*On products compliant to MIL-STD-883, Class B, this parameter is not production tested.

†Full range is −55°C to 125°C.

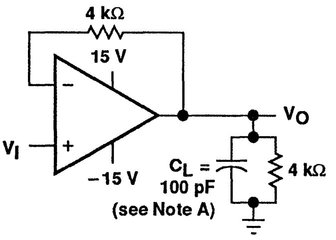
NOTE 4: Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at $T_A = 150°C$ extrapolated to $T_A = 25°C$ using the Arrhenius equation and assuming an activation energy of 0.96 eV.

operating characteristics at specified free-air temperature, $V_{CC\pm}$ = ±15 V

PARAMETER		TEST CONDITIONS	T_A†	TLE2037M			TLE2037AM			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
SR	Slew rate	A_{VD} = 5, R_L = 2 kΩ, C_L = 100 pF, See Figure 1	25°C	6*	7.5		6*	7.5		V/µs
			Full range	4.4*			4.4*			
V_n	Equivalent input noise voltage (see Figure 2)	R_S = 100 Ω, f = 10 Hz	25°C		3.3	8*		3.3	4.5*	nV/√Hz
		R_S = 100 Ω, f = 1 kHz			2.5	4.5*		2.5	3.8*	
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 10 Hz	25°C		50	250*		50	130*	nV
I_n	Equivalent input noise current	f = 10 Hz	25°C		1.5	4*		1.5	4*	pA/√Hz
		f = 1 kHz			0.4	0.6*		0.4	0.6*	
THD	Total harmonic distortion	V_O = ±10 V, A_{VD} = 5, See Note 5	25°C	< 0.002%			< 0.002%			
	Gain-bandwidth product	f = 100 kHz, R_L = 2 kΩ, C_L = 100 pF	25°C	50	76		50	76		MHz
B_{OM}	Maximum output-swing bandwidth	R_L = 2 kΩ	25°C		80			80		kHz
ϕ_m	Phase margin	R_L = 2 kΩ, C_L = 100 pF	25°C	50°			50°			

*On products compliant to MIL-STD-883, Class B, this parameter is not production tested.
†Full range is – 55°C to 125°C.
NOTE 5: Measured distortion of the source used in the analysis was 0.002%.

PARAMETER MEASUREMENT INFORMATION



NOTE A: C_L includes fixture capacitance.

Figure 1. Slew Rate Test Circuit

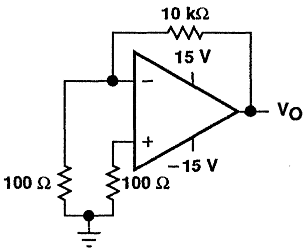


Figure 2. Noise Voltage Test Circuit

PARAMETER MEASUREMENT INFORMATION

typical values

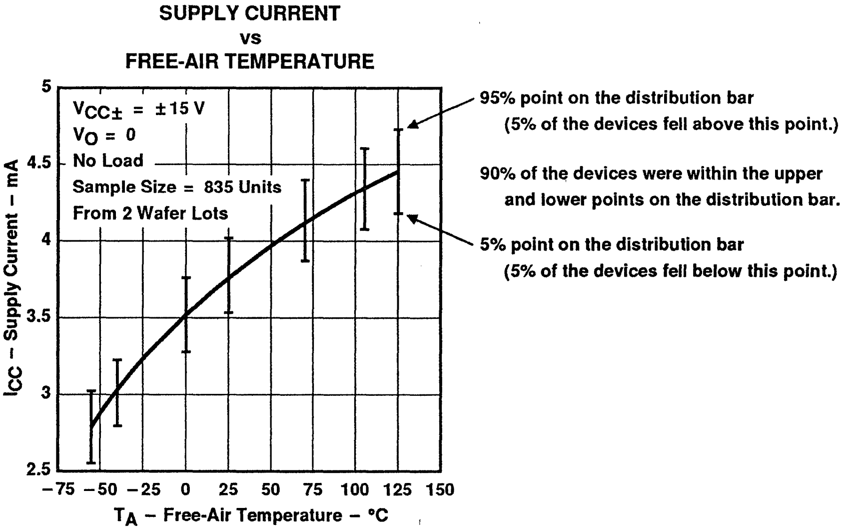
Typical values as presented in this data sheet represent the median (50% point) of device parametric performance.

initial estimates of parameter distributions

In the on-going program of improving data sheets and supplying more information to our customer, Texas Instruments has added an estimate of not only the "typical" values but also the spread around these values. These are in the form of distribution bars that show the 95% (upper) points and the 5% (lower) points from our characterization of the initial wafer lots of this new device type (see Figure 3). The distribution bars are shown at the points where data was actually collected. The 95% and 5% points are used instead of ±3 sigma since some of the distributions are not true Gaussian distributions.

The number of units tested and the number of different wafer lots used are on all of the graphs where distribution bars are shown. As noted in Figure 3, there were a total of 835 units from 2 wafer lots. In this case, there is a very good estimate for the within-lot variability and a possibly poor estimate of the lot-to-lot variability. This will always be the case on newly released products, since there will only be data available from a few wafer lots.

The distribution bars are not intended to replace the minimum and maximum limits in the electrical tables. Each distribution bar represents 90% of the total units tested at a specific temperature. And, while 10% of the units tested fell outside any given distribution bar, this should not be interpreted to mean that the same individual devices fell outside every distribution bar.



95% point on the distribution bar
(5% of the devices fell above this point.)

90% of the devices were within the upper and lower points on the distribution bar.

5% point on the distribution bar
(5% of the devices fell below this point.)

Figure 3. Sample Graph with Distribution Bars

TYPICAL CHARACTERISTICS

table of graphs

			FIGURE
V_{IO}	Input offset voltage	Distribution	4
ΔV_{IO}	Input offset voltage change	vs Time after power on	5, 6
I_{IO}	Input offset current	vs Temperature	7
I_{IB}	Input bias current	vs Common-mode input voltage	8
		vs Temperature	9
I_I	Input current	vs Differential input voltage	10
$V_{O(PP)}$	Maximum peak-to-peak output voltage	vs Frequency	11
V_{OM}	Maximum peak output voltage	vs Load resistance	12, 13
		vs Temperature	14, 15
A_{VD}	Large-signal differential voltage amplification	vs Supply voltage	16
		vs Load resistance	18
		vs Frequency	17, 19
		vs Temperature	20
z_o	Output impedance	vs Frequency	21
CMRR	Common-mode rejection ratio	vs Frequency	22
k_{SVR}	Supply voltage rejection ratio	vs Frequency	23
I_{OS}	Short-circuit output current	vs Supply voltage	24, 25
		vs Time	26, 27
		vs Temperature	28, 29
I_{CC}	Supply current	vs Supply voltage	30
		vs Temperature	31
	Pulse response	Small-signal	32
		Large-signal	33
V_n	Equivalent input noise voltage	vs Frequency	34
	Noise voltage (referred to input)	0.1 to 10 Hz	35
	Gain-bandwidth product	vs Supply voltage	36
		vs Load capacitance	37
SR	Slew rate	vs Temperature	38
ϕ_m	Phase margin	vs Supply voltage	39
		vs Load capacitance	40
		vs Temperature	41
ϕ	Phase shift	vs Frequency	17, 19

TYPICAL CHARACTERISTICS†

TLE2037
DISTRIBUTION OF
INPUT OFFSET VOLTAGE

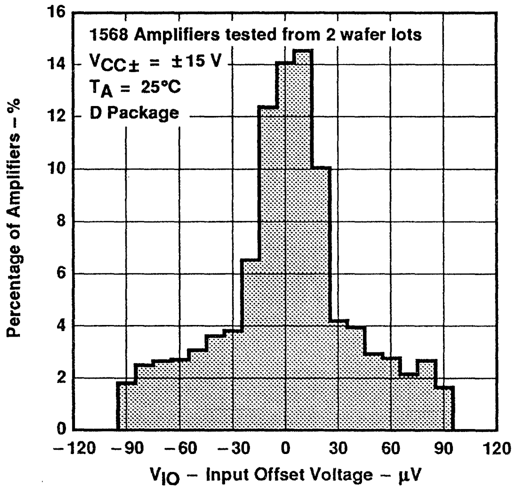


Figure 4

INPUT OFFSET VOLTAGE CHANGE
vs
TIME AFTER POWER ON

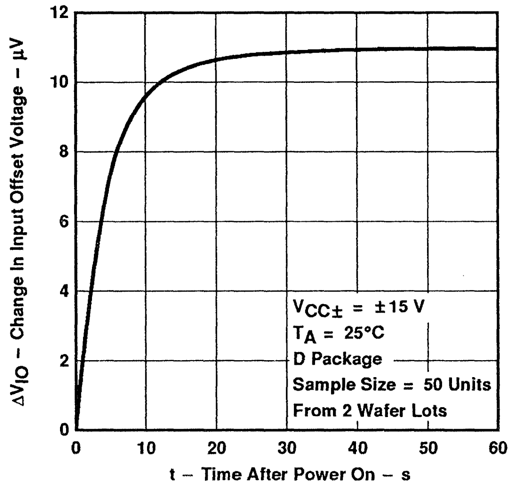


Figure 5

INPUT OFFSET VOLTAGE CHANGE
vs
TIME AFTER POWER ON

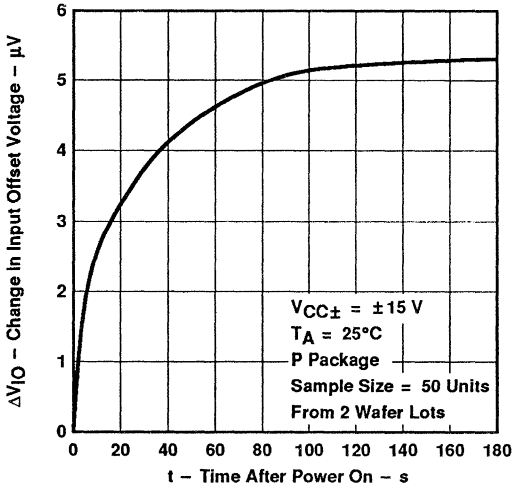


Figure 6

INPUT OFFSET CURRENT
vs
FREE-AIR TEMPERATURE

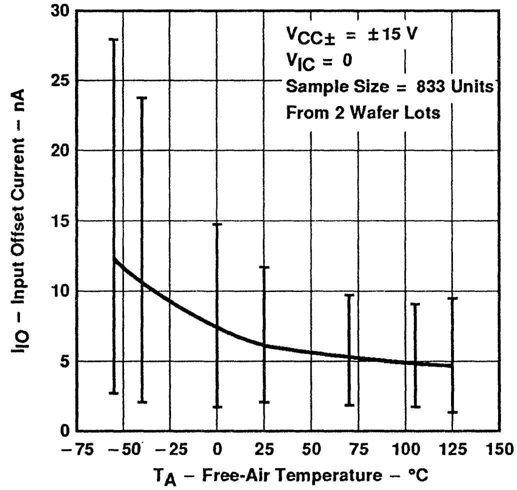
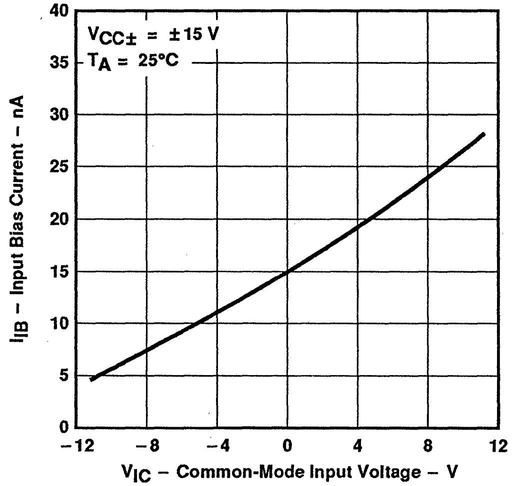


Figure 7

---

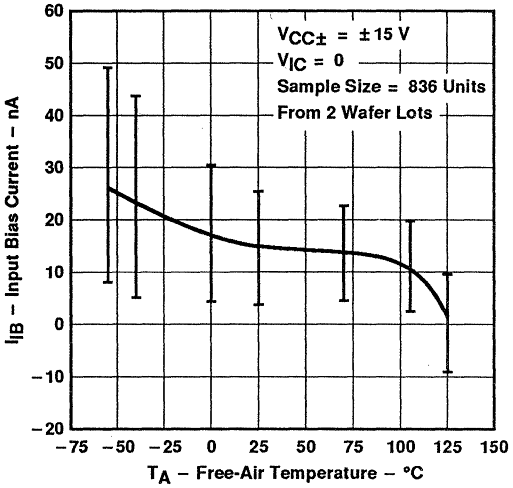
† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†



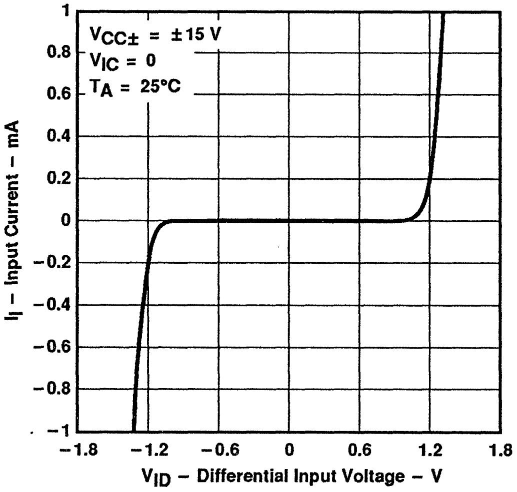
INPUT BIAS CURRENT vs COMMON-MODE INPUT VOLTAGE

Figure 8



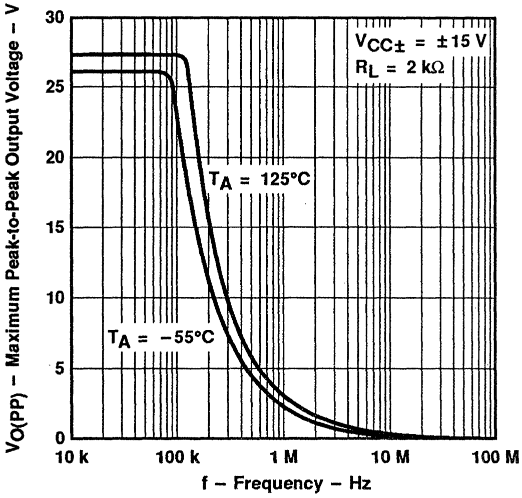
INPUT BIAS CURRENT vs FREE-AIR TEMPERATURE

Figure 9



INPUT CURRENT vs DIFFERENTIAL INPUT VOLTAGE

Figure 10



MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE vs FREQUENCY

Figure 11

---

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

MAXIMUM POSITIVE PEAK OUTPUT VOLTAGE vs LOAD RESISTANCE

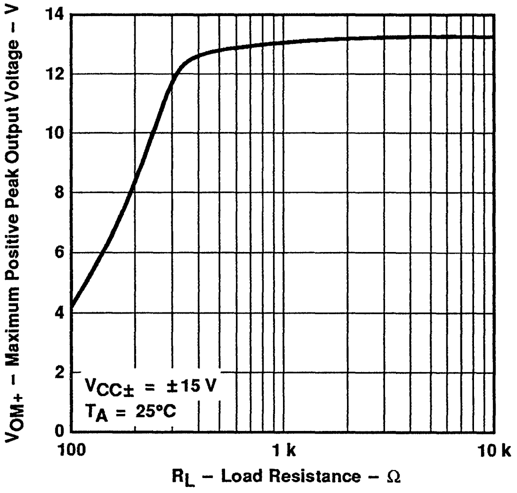


Figure 12

MAXIMUM NEGATIVE PEAK OUTPUT VOLTAGE vs LOAD RESISTANCE

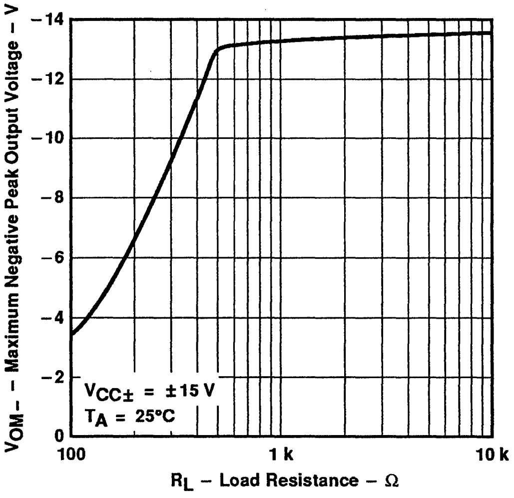


Figure 13

MAXIMUM POSITIVE PEAK OUTPUT VOLTAGE vs FREE-AIR TEMPERATURE

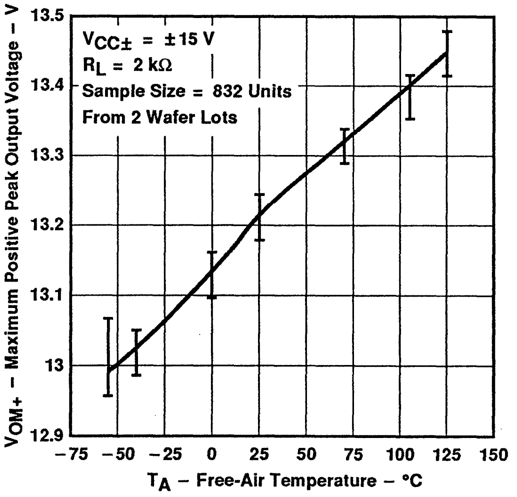


Figure 14

MAXIMUM NEGATIVE PEAK OUTPUT VOLTAGE vs FREE-AIR TEMPERATURE

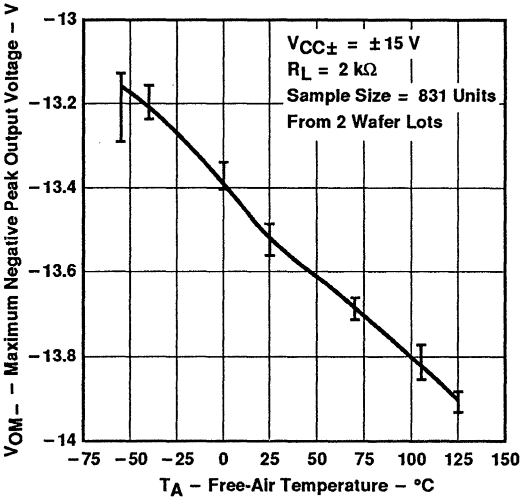


Figure 15

---

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS

LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION vs SUPPLY VOLTAGE

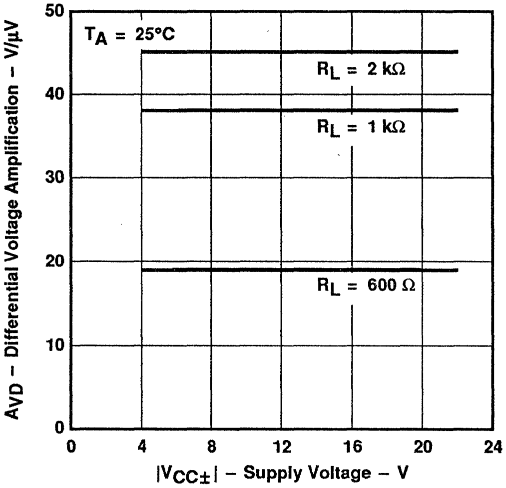


Figure 16

LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION AND PHASE SHIFT vs FREQUENCY

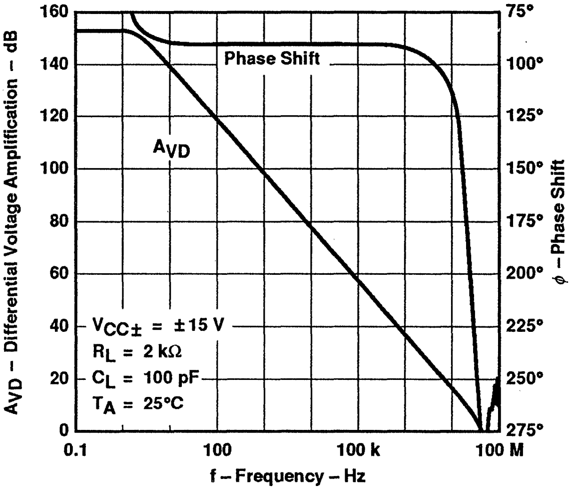


Figure 17

LARGE-SIGNAL VOLTAGE AMPLIFICATION vs LOAD RESISTANCE

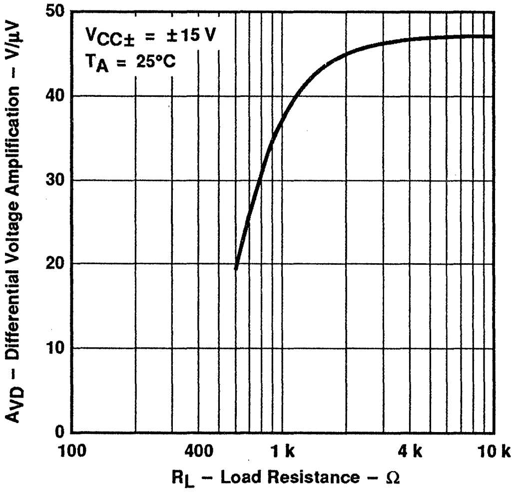


Figure 18

LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION AND PHASE SHIFT vs FREQUENCY

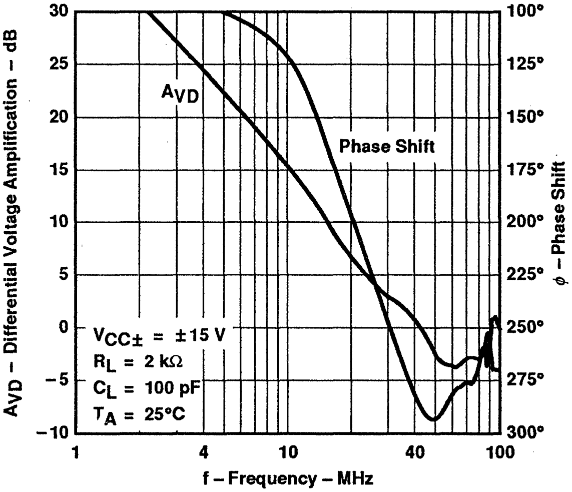


Figure 19

TYPICAL CHARACTERISTICS†

LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION vs FREE-AIR TEMPERATURE

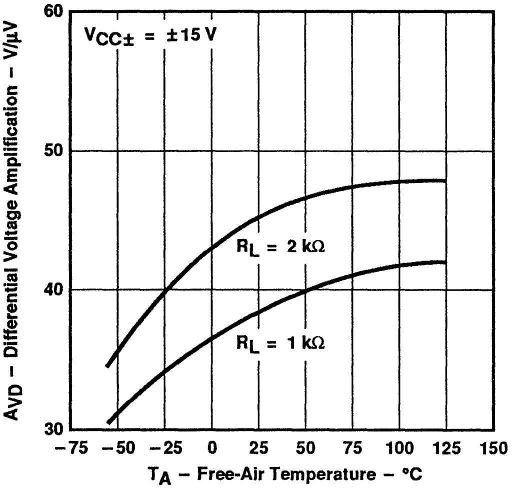


Figure 20

OUTPUT IMPEDANCE vs FREQUENCY

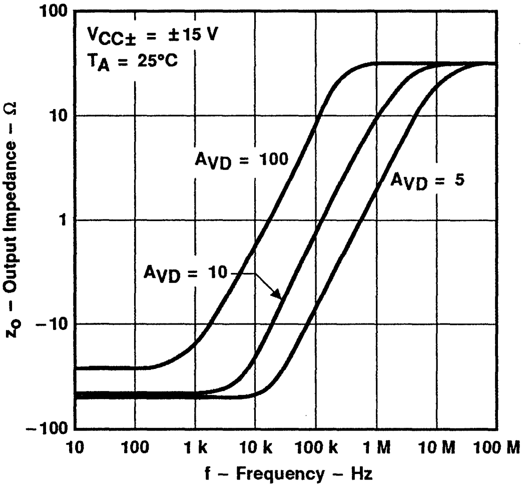


Figure 21

COMMON-MODE REJECTION RATIO vs FREQUENCY

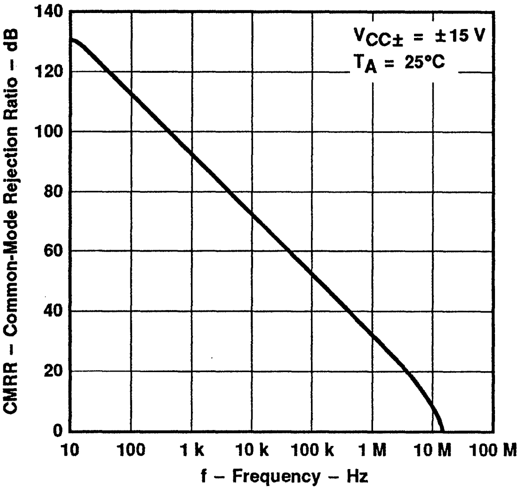


Figure 22

SUPPLY VOLTAGE REJECTION RATIO vs FREQUENCY

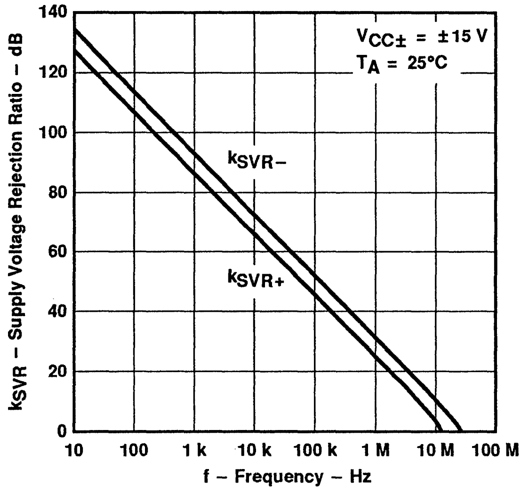


Figure 23

---

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS

SHORT-CIRCUIT OUTPUT CURRENT vs SUPPLY VOLTAGE

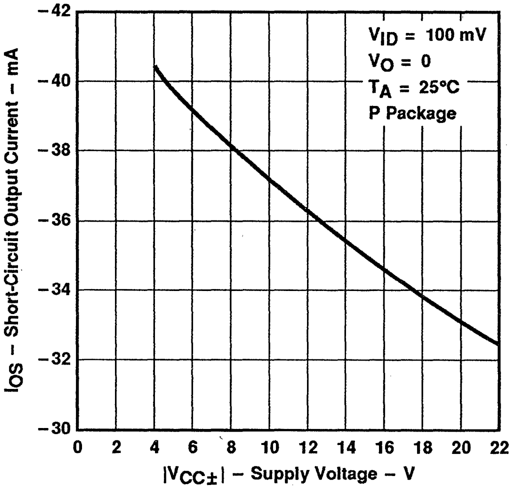


Figure 24

SHORT-CIRCUIT OUTPUT CURRENT vs SUPPLY VOLTAGE

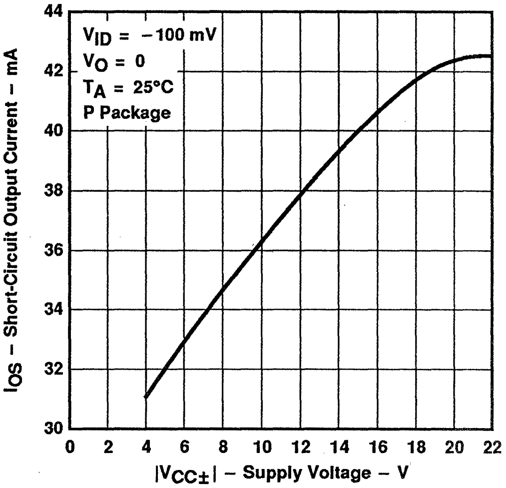


Figure 25

SHORT-CIRCUIT OUTPUT CURRENT vs ELAPSED TIME

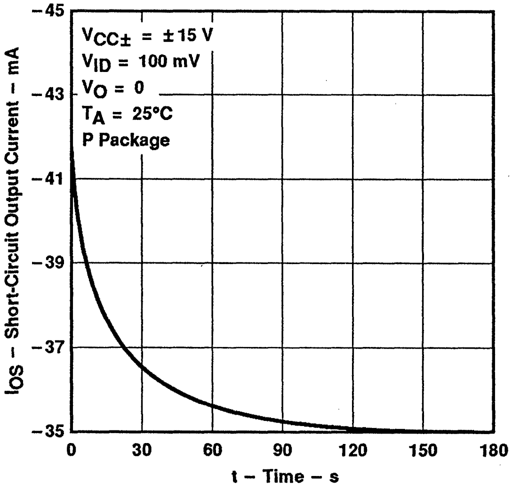


Figure 26

SHORT-CIRCUIT OUTPUT CURRENT vs ELAPSED TIME

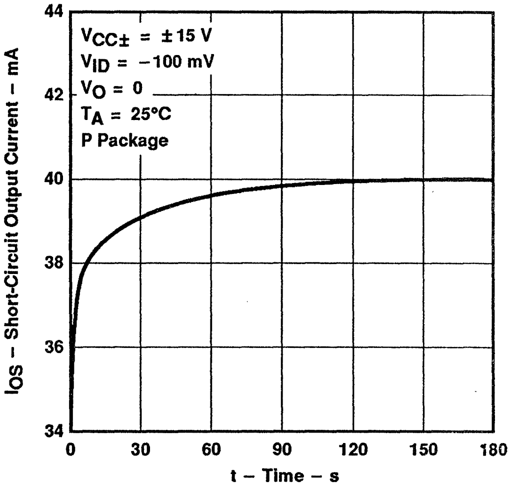


Figure 27

TYPICAL CHARACTERISTICS†

SHORT-CIRCUIT OUTPUT CURRENT vs FREE-AIR TEMPERATURE

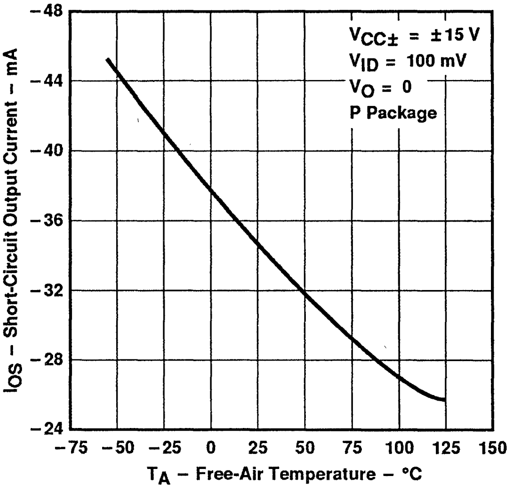


Figure 28

SHORT-CIRCUIT OUTPUT CURRENT vs FREE-AIR TEMPERATURE

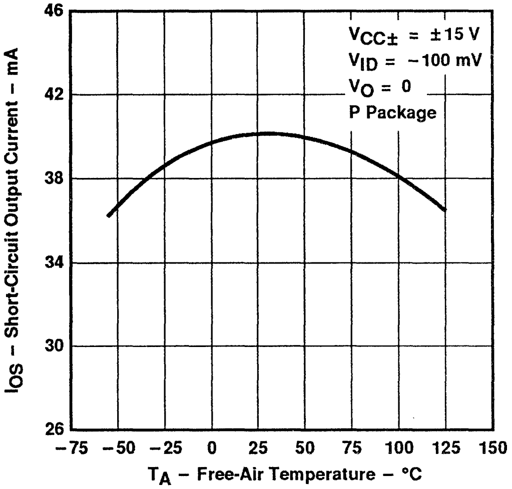


Figure 29

SUPPLY CURRENT vs SUPPLY VOLTAGE

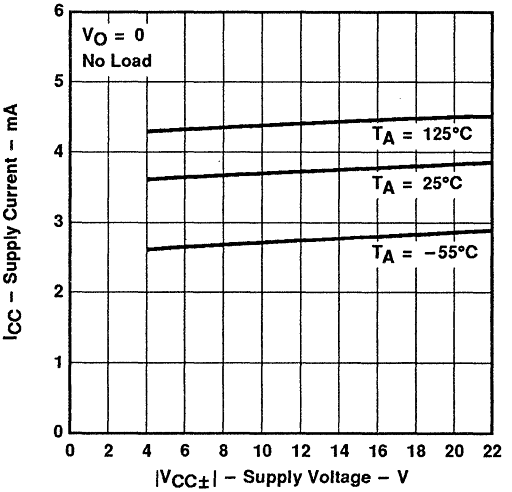


Figure 30

SUPPLY CURRENT vs FREE-AIR TEMPERATURE

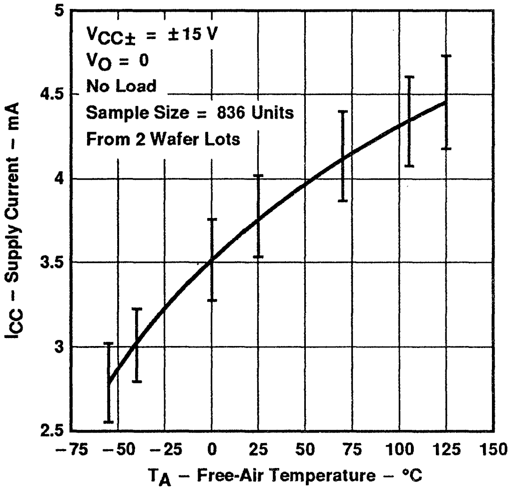


Figure 31

---

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS

SMALL-SIGNAL
PULSE RESPONSE

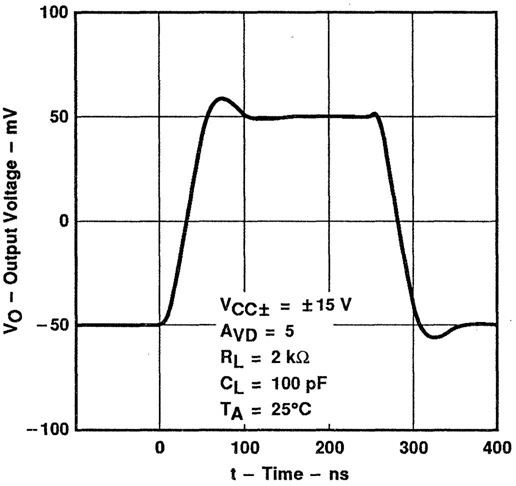


Figure 32

LARGE-SIGNAL
PULSE RESPONSE

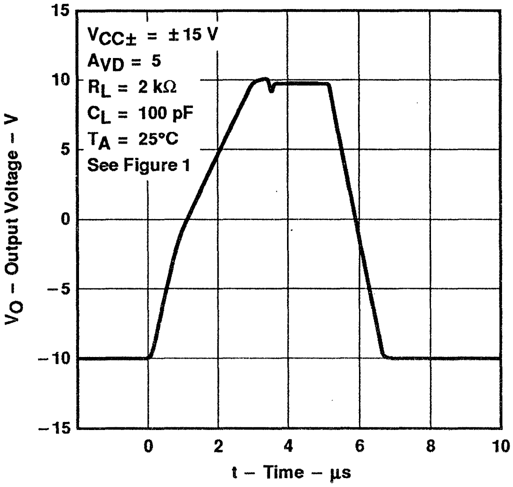


Figure 33

EQUIVALENT INPUT NOISE VOLTAGE
vs
FREQUENCY

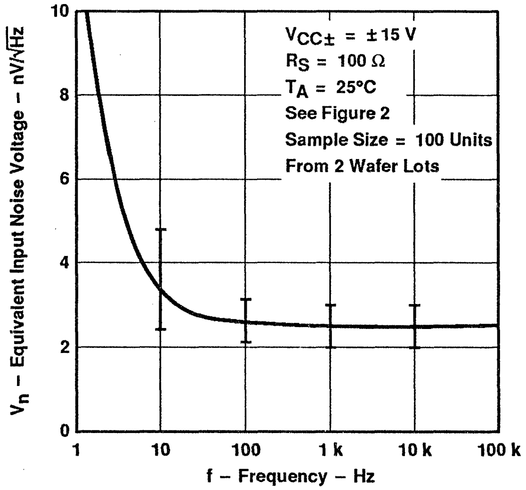


Figure 34

NOISE VOLTAGE
(REFERRED TO INPUT)
OVER A 10-SECOND INTERVAL

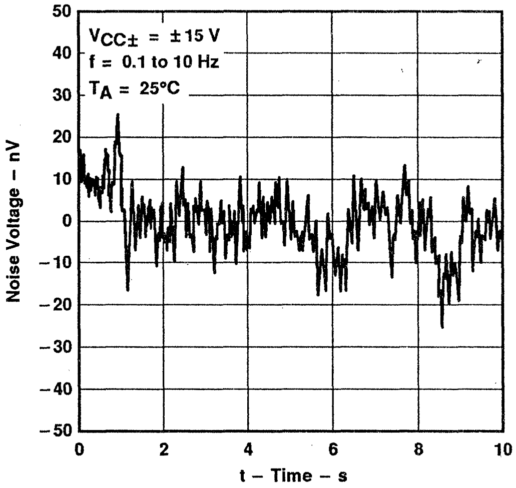


Figure 35

TYPICAL CHARACTERISTICS†

GAIN-BANDWITH PRODUCT vs SUPPLY VOLTAGE

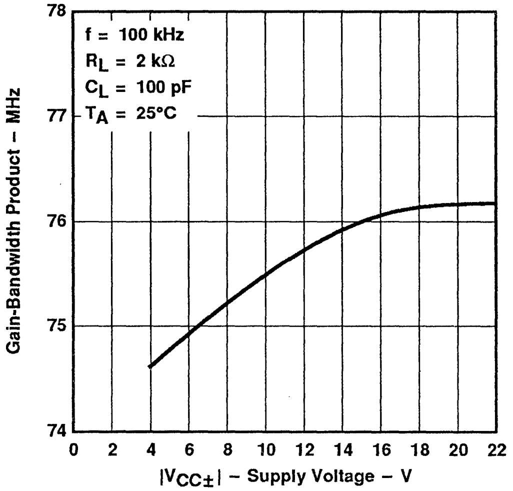


Figure 36

GAIN-BANDWIDTH PRODUCT vs LOAD CAPACITANCE

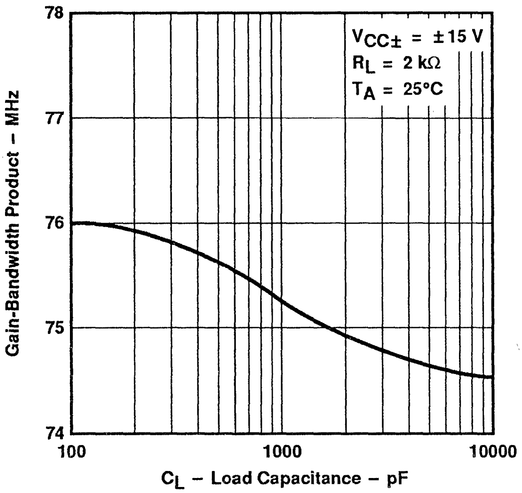


Figure 37

SLEW RATE vs FREE-AIR TEMPERATURE

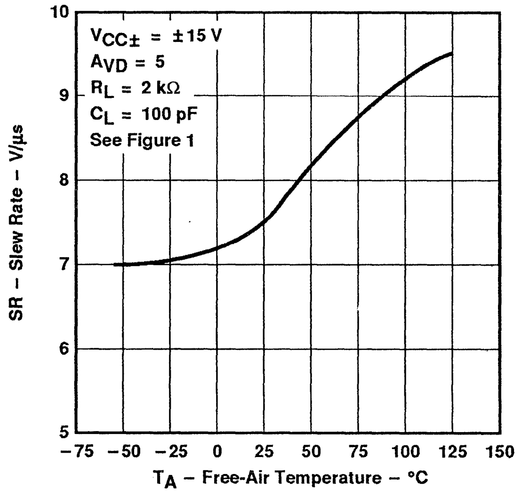


Figure 38

PHASE MARGIN vs SUPPLY VOLTAGE

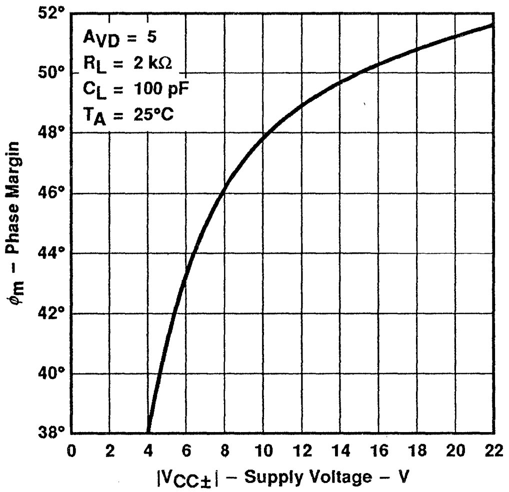


Figure 39

---

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

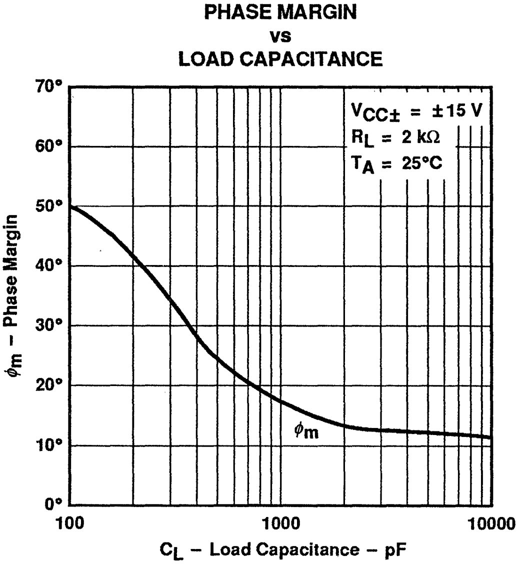


Figure 40

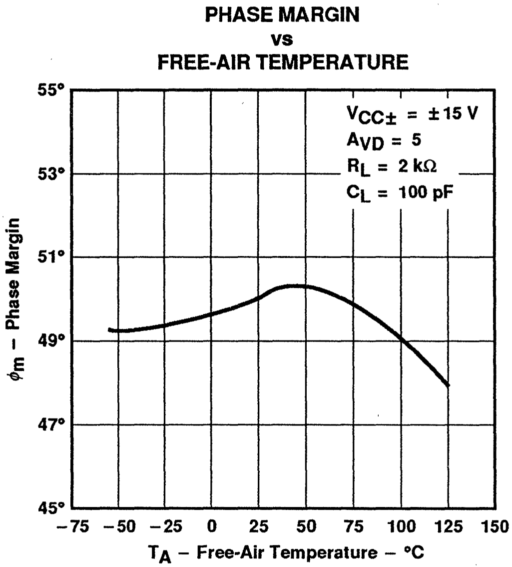


Figure 41

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

APPLICATION INFORMATION

macromodel information

Macromodel information provided was derived using *PSpice® Parts™* model generation software. The Boyle macromodel (see Note 6) and subcircuit in Figures 42 and 43 were generated using the TLE2037 typical electrical and operating characteristics at 25°C. Using this information, output simulations of the following key parameters can be generated to a tolerance of 20% (in most cases):

- Maximum positive output voltage swing
- Maximum negative output voltage swing
- Slew rate
- Quiescent power dissipation
- Input bias current
- Open-loop voltage amplification
- Gain-bandwidth product
- Common-mode rejection ratio
- Phase margin
- DC output resistance
- AC output resistance
- Short-circuit output current limit

NOTE 6: G. R. Boyle, B. M. Cohn, D. O. Pederson, and J. E. Solomon, "Macromodeling of Integrated Circuit Operational Amplifiers", *IEEE Journal of Solid-State Circuits*, SC-9, 353 (1974).

PSpice is a registered trademark of MicroSim Corporation.
Parts is a trademark of MicroSim Corporation.

APPLICATION INFORMATION

macromodel information (continued)

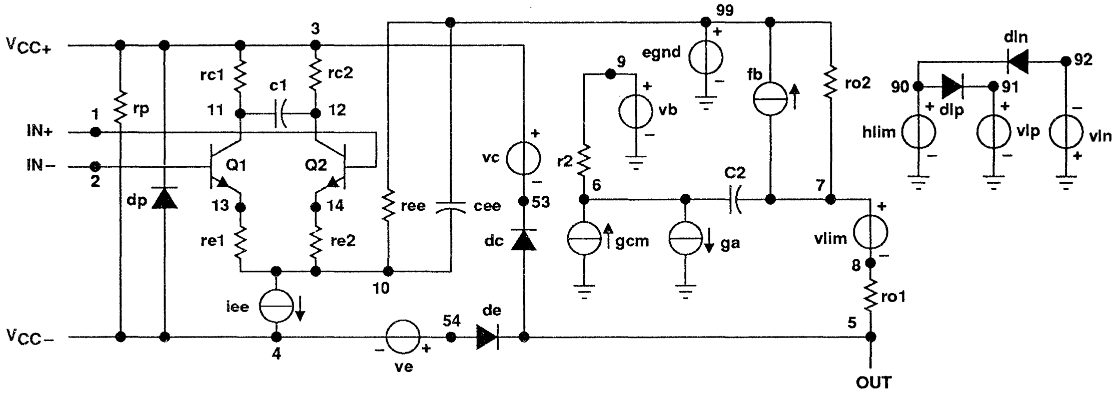


Figure 42. Boyle Macromodel

```
.subckt TLE2037  1 2 3 4 5
*
  c1    11 12 14.74E-12
  c2     6  7 7.500E-12
  dc     5 53 dx
  de    54  5 dx
  dlp   90 91 dx
  dln   92 90 dx
  dp     4  3 dx
  egnd  99  0 poly(2)  (3,0)  (4,0)  0 .5 .5
  fb     7 99 poly(5) vb vc ve vlp vln 0 923.4E6 -800E6 800E6 800E6 -800E6
  ga     6  0 11 12 2.121E-3
  gcm    0  6 10 99 597.7E-12
  iee   10  4 dc 56.26E-6
  hlim  90  0 vlim 1K
  q1    11  2 13 qx
  q2    12  1 14 qx
  r2     6  9 100.0E3
  rc1    3 11 471.5
  rc2    3 12 471.5
  re1   13 10 -448
  re2   14 10 -448
  ree   10 99 3.555E6
  ro1    8  5 25
  ro2    7 99 25
  rp     3  4 8.013E3
  vb     9  0 dc 0
  vc     3 53 dc 2.400
  ve    54  4 dc 2.100
  vlim   7  8 dc 0
  vlp   91  0 dc 40
  vln    0 92 dc 40
.model dx D(Is=800.0E-18)
.model qx NPN(Is=800.0E-18 Bf=7.031E3)
.ends
```

Figure 43. Macromodel Subcircuit

APPLICATION INFORMATION

input offset voltage nulling

The TLE2037 series offers external null pins that can be used to further reduce the input offset voltage. The circuit of Figure 44 can be connected as shown if the feature is desired. If external nulling is not needed, the null pins may be left disconnected.

(a) Standard Adjustment

(b) Adjustment with Improved Sensitivity

Figure 44. Input Offset Voltage Nulling Circuits

TLE2061, TLE2061A, TLE2061B, TLE2061Y
EXCALIBUR JFET-INPUT HIGH-OUTPUT-DRIVE µPOWER OPERATIONAL AMPLIFIERS

D3345, OCTOBER 1989 – REVISED NOVEMBER 1991

available features

- **Excellent Output Drive Capability**
  V_O = ± 2.5 V Min at R_L = 100 Ω, $V_{CC\pm}$ = ± 5 V
  V_O = ± 12.5 V Min at R_L = 600 Ω, $V_{CC\pm}$ = ± 15 V
- **Low Supply Current . . . 280 µA Typ**
- **High Unity-Gain Bandwidth . . . 2.1 MHz Typ**
- **High Slew Rate . . . 3.4 V/µs Typ**
- **Macromodels Included**
- **Wide Operating Supply Voltage Range $V_{CC\pm}$ = ± 3.5 V to ± 20 V**
- **High Open-Loop Gain . . . 280 V/mV Typ**
- **Low Offset Voltage . . . 500 µV Max**
- **Low Offset Voltage Drift With Time 0.04 µV/mo Typ**
- **Low Input Bias Current . . . 5 pA Typ**

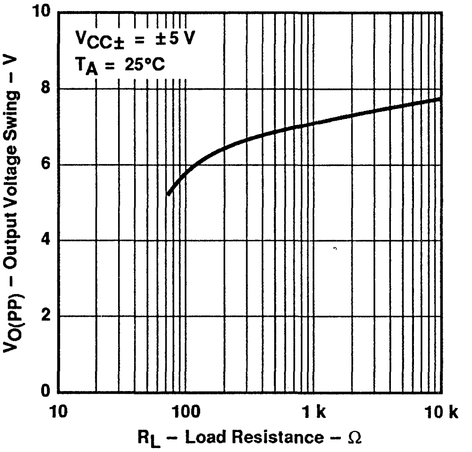
description

The TLE2061, TLE2061A, and TLE2061B are JFET-input, high-output drive, micropower precision operational amplifiers manufactured using Texas Instruments Excalibur process. These devices combine outstanding output drive capability with low-power consumption, excellent dc precision, and wide bandwidth.

In addition to maintaining the traditional JFET advantages of fast slew rates and low input bias and offset currents, the Excalibur process offers outstanding parametric stability over time and temperature. This results in a "precision" device remaining precise even with changes in temperature and over years of use.

The TLE2061, TLE2061A, and TLE2061B are ideal choices for any application requiring excellent dc precision, high output drive, wide bandwidth, and low power consumption.

MAXIMUM PEAK-TO-PEAK
OUTPUT VOLTAGE SWING
vs
LOAD RESISTANCE



A variety of available package options includes small-outline and chip-carrier versions for high-density system applications.

AVAILABLE OPTIONS

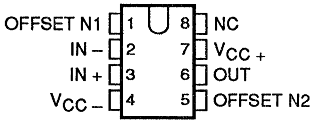
T_A	V_{IO} max AT 25°C	PACKAGE						CHIP FORM (Y)
		SMALL OUTLINE (D)	SSOP (DB)	CHIP CARRIER (FK)	CERAMIC DIP (JG)	PLASTIC DIP (P)	TSSOP (PW)	
0°C	500 µV	——	——	——	——	——	——	——
to	1.5 µV	TLE2061ACD	——	——	——	TLE2061ACP	——	——
70°C	3 mV	TLE2061CD	TLE2061CDBLE	——	——	TLE2061CP	TLE2061CPWLE	TLE2061Y
– 40°C	500 µV	——	——	——	——	——	——	——
to	1.5 µV	TLE2061AID	——	——	——	TLE2061AIP	——	——
85°C	3 mV	TLE2061ID	——	——	——	TLE2061IP	——	——
– 55°C	500 µV	——	——	——	——	——	——	——
to	1.5 µV	TLE2061AMD	——	TLE2061AMFK	TLE2061AMJG	TLE2061AMP	——	——
125°C	3 mV	TLE2061MD	——	TLE2061MFK	TLE2061MJG	TLE2061MP	——	——

D packages are available taped and reeled. Add "R" suffix to device type, (e.g., TLE2061ACDR).The DB and PW packages are only available left-end taped and reeled. Chips are tested at 25°C.

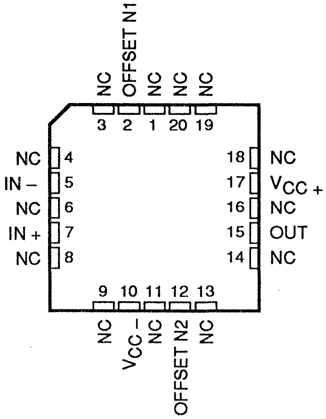
description (continued)

The C-suffix devices are characterized for operation from 0°C to 70°C. The I-suffix devices are characterized for operation from −40°C to 85°C. The M-suffix devices are characterized for operation over the full military temperature range of −55°C to 125°C.

D, DB, JG, P, or PW PACKAGE
(TOP VIEW)



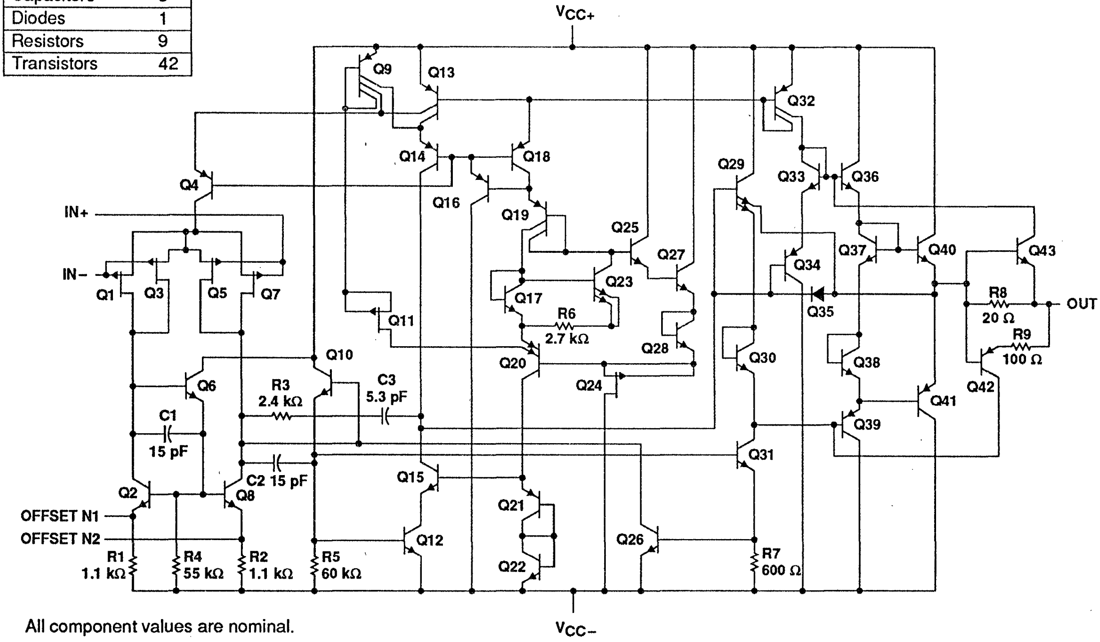
FK PACKAGE
(TOP VIEW)



NC – No internal connection

equivalent schematic

ACTUAL DEVICE COMPONENT COUNT	
Capacitors	3
Diodes	1
Resistors	9
Transistors	42

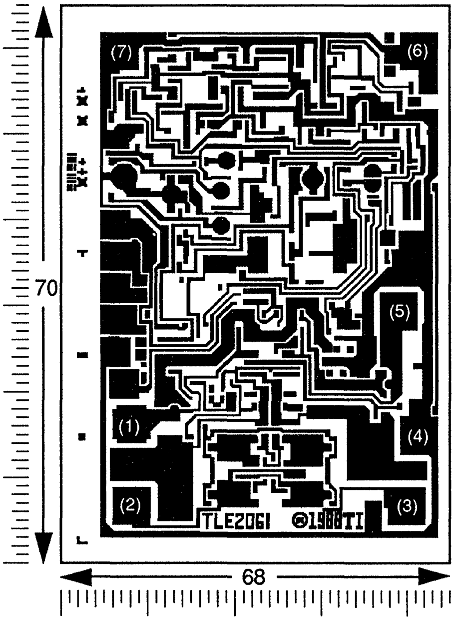


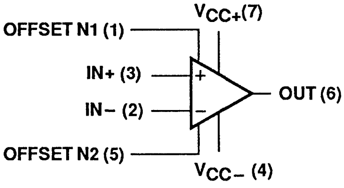
All component values are nominal.

chip information

These chips, properly assembled, display characteristics similar to the TLE2061. Thermal compression or ultrasonic bonding may be used on the doped aluminum bonding pads. Chips may be mounted with conductive epoxy or a gold-silicon preform.

BONDING PAD ASSIGNMENTS





CHIP THICKNESS:
15 TYPICAL

BONDING PADS:
4 X 4 MINIMUM

T_J max = 150°C

TOLERANCES
ARE ± 10%

ALL DIMENSIONS
ARE IN MILS

PIN (4) INTERNALLY CONNECTED
TO BACKSIDE OF CHIP

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC+} (see Note 1)	22 V
Supply voltage, V_{CC-}	−22 V
Differential input voltage (see Note 2)	±44 V
Input voltage, V_I (any input)	$\pm V_{CC}$
Input current, I_I (each input)	±1 mA
Output current, I_O	±80 mA
Total current into V_{CC+} terminal	80 mA
Total current out of V_{CC-} terminal	−80 mA
Duration of short-circuit current at (or below) 25°C (see Note 3)	unlimited
Continuous total dissipation	See Dissipation Rating Table
Operating free-air temperature range, T_A: C-suffix	0°C to 70°C
I-suffix	−40°C to 85°C
M-suffix	−55°C to 125°C
Storage temperature range	−65°C to 150°C
Case temperature for 60 seconds: FK package	260°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D, DB, P or PW package	260°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: JG package	300°C

NOTES: 1. All voltage values, except differential voltages, are with respect to the midpoint between V_{CC+} and V_{CC-}.
2. Differential voltages are at the noninverting input with respect to the inverting input.
3. The output may be shorted to either supply. Temperature and/or supply voltages must be limited to ensure that the maximum dissipation rating is not exceeded.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING	$T_A = 125°C$ POWER RATING
D	725 mW	5.8 mW/°C	464 mW	377 mW	145 mW
DB	525 mW	4.2 mW/°C	336 mW	273 mW	———
FK	1375 mW	11.0 mW/°C	880 mW	715 mW	275 mW
JG	1050 mW	8.4 mW/°C	672 mW	546 mW	210 mW
P	1000 mW	8.0 mW/°C	640 mW	520 mW	200 mW
PW	525 mW	4.2 mW/°C	336 mW	273 mW	———

recommended operating conditions

		C-SUFFIX		I-SUFFIX		M-SUFFIX		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
Supply voltage, $V_{CC\pm}$		±3.5	±20	±3.5	±20	± 3.5	±20	V
Common-mode input voltage, V_{IC}	$V_{CC\pm} = \pm 5$ V	−1.6	4	−1.6	4	−1.6	4	V
	$V_{CC\pm} = \pm 15$ V	−11	13	−11	13	−11	13	
	$V_{CC\pm} = \pm 20$ V	−15	16.5	−15	16.5	−15	16.5	
Operating free-air temperature, T_A		0	70	− 40	85	−55	125	°C

electrical characteristics at specified free-air temperature, $V_{CC\pm} = \pm 5$ V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A	MIN	TYP	MAX	UNIT
V_{IO} Input offset voltage	TLE2061C	$V_{IC} = 0$, $R_S = 50\ \Omega$	25°C		0.8	3.1	mV
			Full range			4	
	TLE2061AC		25°C		0.6	2.6	
			Full range			3.5	
	TLE2061BC		25°C		0.5	1.9	
			Full range			2.4	
α_{VIO} Temperature coefficient of input offset voltage			Full range		6		µV/°C
Input offset voltage long-term drift (see Note 4)			25°C		0.04		µV/mo
I_{IO} Input offset current			25°C		1		pA
			Full range			0.8	nA
I_{IB} Input bias current			25°C		3		pA
			Full range			2	nA
V_{ICR} Common-mode input voltage range			25°C	−1.6 to 4	−2 to 6		V
			Full range	−1.6 to 4			V
V_{OM+} Maximum positive peak output voltage swing		$R_L = 10\ k\Omega$	25°C	3.5	3.7		V
			Full range	3.3			
		$R_L = 100\ \Omega$	25°C	2.5	3.1		
			Full range	2			
V_{OM-} Maximum negative peak output voltage swing		$R_L = 10\ k\Omega$	25°C	−3.7	−3.9		V
			Full range	−3.3			
		$R_L = 100\ \Omega$	25°C	−2.5	−2.7		
			Full range	−2			
A_{VD} Large-signal differential voltage amplification		$V_O = \pm 2.8$ V, $R_L = 10\ k\Omega$	25°C	15	80		V/mV
			Full range	2			
		$V_O = 0$ to 2 V, $R_L = 100\ \Omega$	25°C	0.75	45		
			Full range	0.5			
		$V_O = 0$ to −2 V, $R_L = 100\ \Omega$	25°C	0.5	3		
			Full range	0.25			
r_i Input resistance			25°C		10^{12}		Ω
c_i Input capacitance			25°C		4		pF
z_o Open-loop output impedance		$I_O = 0$	25°C		280		Ω
CMRR Common-mode rejection ratio		$R_S = 50\ \Omega$, $V_{IC} = V_{ICR}$ min	25°C	65	82		dB
			Full range	65			
k_{SVR} Supply-voltage rejection ratio ($\Delta V_{CC\pm} / \Delta V_{IO}$)		$V_{CC\pm} = \pm 5$ V to ± 20 V, $R_S = 50\ \Omega$	25°C	75	93		dB
			Full range	75			
I_{CC} Supply current		$V_O = 0$, No load	25°C		280	325	µA
			Full range			350	
ΔI_{CC} Supply current change over operating temperature range			Full range		29		µA

†Full range is 0°C to 70°C.

NOTE 4: Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at $T_A = 150°C$ extrapolated to $T_A = 25°C$ using the Arrhenius equation and assuming an activation energy of 0.96 eV.

operating characteristics at specified free-air temperature, $V_{CC\pm} = \pm 5$ V

PARAMETER		TEST CONDITIONS		T_A	MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain (see Figure 1)	R_L = 10 kΩ,	C_L = 100 pF	25°C	2.2	3.4		V/µs
				Full range	2.1			
V_n	Equivalent input noise voltage (see Figure 2)	f = 10 Hz,	R_S = 100 Ω	25°C		59	100	nV/√Hz
		f = 1 kHz,	R_S = 100 Ω	25°C		43	60	
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 10 Hz		25°C		1.1		µV
I_n	Equivalent input noise current	f = 1 kHz		25°C		1		fA/√Hz
THD	Total harmonic distortion	A_{VD} = 2, $V_{O(PP)}$ = 2 V,	f = 10 kHz, R_L = 10 kΩ	25°C		0.025%		
B_1	Unity-gain bandwidth (see Figure 3)	R_L = 10 kΩ,	C_L = 100 pF	25°C		1.8		MHz
		R_L = 100 Ω,	C_L = 100 pF	25°C		1.3		
	Settling time	0.1%		25°C		5		µs
		0.01%		25°C		10		
B_{OM}	Maximum-output-swing bandwidth	A_{VD} = 1,	R_L = 10 kΩ	25°C		140		kHz
ϕ_m	Phase margin at unity gain (see Figure 3)	R_L = 10 kΩ,	C_L = 100 pF	25°C		58°		
		R_L = 100 Ω,	C_L = 100 pF	25°C		75°		

† Full range is 0°C to 70°C.

electrical characteristics at specified free-air temperature, $V_{CC\pm} = \pm 15$ V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A	MIN	TYP	MAX	UNIT
V_{IO} Input offset voltage	TLE2061C	$V_{IC} = 0$, $R_S = 50\ \Omega$	25°C		0.6	3	mV
			Full range			3.9	
	TLE2061AC		25°C		0.5	1.5	
			Full range			2.5	
	TLE2061BC		25°C		0.3	0.5	
			Full range			1	
α_{VIO} Temperature coefficient of input offset voltage			Full range		6		µV/°C
Input offset voltage long-term drift (see Note 4)			25°C		0.04		µV/mo
I_{IO} Input offset current			25°C		2		pA
			Full range			1	nA
I_{IB} Input bias current			25°C		4		pA
			Full range			3	nA
V_{ICR} Common-mode input voltage range			25°C	−11 to 13	−12 to 16		V
			Full range	−11 to 13			V
V_{OM+} Maximum positive peak output voltage swing		$R_L = 10\ k\Omega$	25°C	13.2	13.7		V
			Full range	13			
		$R_L = 600\ \Omega$	25°C	12.5	13.2		
			Full range	12			
V_{OM-} Maximum negative peak output voltage swing		$R_L = 10\ k\Omega$	25°C	−13.2	−13.7		V
			Full range	−13			
		$R_L = 600\ \Omega$	25°C	−12.5	−13		
			Full range	−12			
A_{VD} Large-signal differential voltage amplification		$V_O = \pm 10$ V, $R_L = 10\ k\Omega$	25°C	30	230		V/mV
			Full range	20			
		$V_O = 0$ to 8 V, $R_L = 600\ \Omega$	25°C	25	100		
			Full range	10			
		$V_O = 0$ to −8 V, $R_L = 600\ \Omega$	25°C	3	25		
			Full range	1			
r_i Input resistance			25°C		10^{12}		Ω
c_i Input capacitance			25°C		4		pF
z_o Open-loop output impedance		$I_O = 0$	25°C		280		Ω
CMRR Common-mode rejection ratio		$R_S = 50\ \Omega$, $V_{IC} = V_{ICR}$ min	25°C	72	90		dB
			Full range	70			
k_{SVR} Supply-voltage rejection ratio ($\Delta V_{CC\pm} / \Delta V_{IO}$)		$V_{CC\pm} = \pm 5$ V to ± 15 V, $R_S = 50\ \Omega$	25°C	75	93		dB
			Full range	75			
I_{CC} Supply current		$V_O = 0$, No load	25°C		290	350	µA
			Full range			375	
ΔI_{CC} Supply current change over operating temperature range			Full range		34		µA

†Full range is 0°C to 70°C.

NOTE 4: Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at $T_A = 150°C$ extrapolated to $T_A = 25°C$ using the Arrhenius equation and assuming an activation energy of 0.96 eV.

operating characteristics at specified free-air temperature, $V_{CC\pm} = \pm 15$ V

PARAMETER		TEST CONDITIONS		T_A	MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain (see Figure 1)	$R_L = 10$ kΩ,	$C_L = 100$ pF	25°C	2.6	3.4		V/µs
				Full range	2.5			
V_n	Equivalent input noise voltage (see Figure 2)	f = 10 Hz,	$R_S = 100$ Ω	25°C		70	100	nV/√Hz
		f = 1 kHz,	$R_S = 100$ Ω	25°C		40	60	
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 10 Hz		25°C		1.1		µV
I_n	Equivalent input noise current	f = 1 kHz		25°C		1.1		fA/√Hz
THD	Total harmonic distortion	$A_{VD} = 2$, $V_{O(PP)} = 2$ V,	f = 10 kHz, $R_L = 10$ kΩ	25°C		0.025%		
B_1	Unity-gain bandwidth (see Figure 3)	$R_L = 10$ kΩ,	$C_L = 100$ pF	25°C		2		MHz
		$R_L = 600$ Ω,	$C_L = 100$ pF	25°C		1.5		
	Settling time	0.1%		25°C		5		µs
		0.01%		25°C		10		
B_{OM}	Maximum-output-swing bandwidth	$A_{VD} = 1$,	$R_L = 10$ kΩ	25°C		40		kHz
ϕ_m	Phase margin at unity gain (see Figure 3)	$R_L = 10$ kΩ,	$C_L = 100$ pF	25°C		60°		
		$R_L = 600$ Ω,	$C_L = 100$ pF	25°C		70°		

†Full range is 0°C to 70°C.

electrical characteristics at specified free-air temperature, $V_{CC\pm}$ = ±20 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS	T_A	MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	TLE2061C	V_{IC} = 0, R_S = 50 Ω	25°C		0.6	3	mV
				Full range			3.9	
		TLE2061AC		25°C		0.6	1.6	
				Full range			2.5	
		TLE2061BC		25°C		0.3	0.5	
				Full range			1	
α_{VIO}	Temperature coefficient of input offset voltage			Full range		6		μV/°C
	Input offset voltage long-term drift (see Note 4)			25°C		0.04		μV/mo
I_{IO}	Input offset current			25°C		3		pA
				Full range			1	nA
I_{IB}	Input bias current			25°C		5		pA
				Full range			3	nA
V_{ICR}	Common-mode input voltage range			25°C	−15 to 16.5	−17 to 21		V
				Full range	−15 to 16.5			V
V_{OM+}	Maximum positive peak output voltage swing		R_L = 10 kΩ	25°C	18.2	18.7		V
				Full range	18			
			R_L = 600 Ω	25°C	15	18.1		
				Full range	12			
V_{OM-}	Maximum negative peak output voltage swing		R_L = 10 kΩ	25°C	−18.2	−18.7		V
				Full range	−18			
			R_L = 600 Ω	25°C	−15	−18		
				Full range	−12			
A_{VD}	Large-signal differential voltage amplification		V_O = ±15 V, R_L = 10 kΩ	25°C	30	280		V/mV
				Full range	20			
			V_O = 0 to 10 V, R_L = 600 Ω	25°C	25	80		
				Full range	10			
			V_O = 0 to −10 V, R_L = 600 Ω	25°C	3	20		
				Full range	1			
r_i	Input resistance			25°C		10^{12}		Ω
c_i	Input capacitance			25°C		4		pF
z_o	Open-loop output impedance		I_O = 0	25°C		280		Ω
CMRR	Common-mode rejection ratio		R_S = 50 Ω, V_{IC} = V_{ICR} min	25°C	75	91		dB
				Full range	70			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm} / \Delta V_{IO}$)		$V_{CC\pm}$ = ±5 V to ±20 V, R_S = 50 Ω	25°C	75	93		dB
				Full range	70			
I_{CC}	Supply current		V_O = 0, No load	25°C		300	375	μA
				Full range			400	
ΔI_{CC}	Supply current change over operating temperature range			Full range		18		μA

†Full range is 0°C to 70°C.

NOTE 4: Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at T_A = 150°C extrapolated to T_A = 25°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

operating characteristics at specified free-air temperature, $V_{CC\pm}$ = ±20 V

PARAMETER		TEST CONDITIONS		T_A	MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain (see Figure 1)	R_L = 10 kΩ,	C_L = 100 pF	25°C	2.8	3.4		V/μs
				Full range	2.5			
V_n	Equivalent input noise voltage (see Figure 2)	f = 10 Hz,	R_S = 100 Ω	25°C		75	100	nV/√Hz
		f = 1 kHz,	R_S = 100 Ω	25°C		40	60	
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 10 Hz		25°C		1.1		μV
I_n	Equivalent input noise current	f = 1 kHz		25°C		1.3		fA/√Hz
THD	Total harmonic distortion	A_{VD} = 2, $V_{O(PP)}$ = 2 V,	f = 10 kHz, R_L = 10 kΩ	25°C		0.025%		
B_1	Unity-gain bandwidth (see Figure 3)	R_L = 10 kΩ,	C_L = 100 pF	25°C		2.1		MHz
		R_L = 600 Ω,	C_L = 100 pF	25°C		1.6		
	Settling time	0.1%		25°C		5		μs
		0.01%		25°C		10		
B_{OM}	Maximum-output-swing bandwidth	A_{VD} = 1,	R_L = 10 kΩ	25°C		28		kHz
ϕ_m	Phase margin at unity gain (see Figure 3)	R_L = 10 kΩ,	C_L = 100 pF	25°C		60°		
		R_L = 600 Ω,	C_L = 100 pF	25°C		70°		

†Full range is 0°C to 70°C.

electrical characteristics at specified free-air temperature, $V_{CC\pm} = \pm 5$ V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A	MIN	TYP	MAX	UNIT
V_{IO} Input offset voltage	TLE2061I	V_{IC} = 0, R_S = 50 Ω	25°C		0.8	3.1	mV
			Full range			4.4	
	TLE2061AI		25°C		0.6	2.6	
			Full range			3.9	
	TLE2061BI		25°C		0.5	1.9	
			Full range			2.7	
α_{VIO} Temperature coefficient of input offset voltage			Full range		6		μV/°C
Input offset voltage long-term drift (see Note 4)			25°C		0.04		μV/mo
I_{IO} Input offset current			25°C		1		pA
			Full range			2	nA
I_{IB} Input bias current			25°C		3		pA
			Full range			4	nA
V_{ICR} Common-mode input voltage range			25°C	− 1.6 to 4	− 2 to 6		V
			Full range	− 1.6 to 4			V
V_{OM+} Maximum positive peak output voltage swing		R_L = 10 kΩ	25°C	3.5	3.7		V
			Full range	3.1			
		R_L = 100 Ω	25°C	2.5	3.1		
			Full range	2			
V_{OM-} Maximum negative peak output voltage swing		R_L = 10 kΩ	25°C	− 3.7	− 3.9		V
			Full range	− 3.1			
		R_L = 100 Ω	25°C	− 2.5	− 2.7		
			Full range	− 2			
A_{VD} Large-signal differential voltage amplification		V_O = ± 2.8 V, R_L = 10 kΩ	25°C	15	80		V/mV
			Full range	2			
		V_O = 0 to 2 V, R_L = 100 Ω	25°C	0.75	45		
			Full range	0.5			
		V_O = 0 to − 2 V, R_L = 100 Ω	25°C	0.5	3		
			Full range	0.25			
r_i Input resistance			25°C		10^{12}		Ω
c_i Input capacitance			25°C		4		pF
z_o Open-loop output impedance		I_O = 0	25°C		280		Ω
CMRR Common-mode rejection ratio		R_S = 50 Ω, V_{IC} = V_{ICR} min	25°C	65	82		dB
			Full range	65			
k_{SVR} Supply-voltage rejection ratio ($\Delta V_{CC\pm} / \Delta V_{IO}$)		$V_{CC\pm}$ = ± 5 V to ± 20 V, R_S = 50 Ω	25°C	75	93		dB
			Full range	65			
I_{CC} Supply current		V_O = 0, No load	25°C		280	325	μA
			Full range			350	
ΔI_{CC} Supply current change over operating temperature range			Full range		29		μA

†Full range is − 40°C to 85°C.

NOTE 4: Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at T_A = 150°C extrapolated to T_A = 25°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

operating characteristics at specified free-air temperature, $V_{CC\pm} = \pm 5$ V

PARAMETER		TEST CONDITIONS		T_A	MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain (see Figure 1)	R_L = 10 kΩ,	C_L = 100 pF	25°C	2.2	3.4		V/µs
				Full range	1.7			
V_n	Equivalent input noise voltage (see Figure 2)	f = 10 Hz,	R_S = 100 Ω	25°C		59	100	nV/√Hz
		f = 1 kHz,	R_S = 100 Ω	25°C		43	60	
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 10 Hz		25°C		1.1		µV
I_n	Equivalent input noise current	f = 1 kHz		25°C		1		fA/√Hz
THD	Total harmonic distortion	A_{VD} = 2, $V_{O(PP)}$ = 2 V,	f = 10 kHz, R_L = 10 kΩ	25°C		0.025%		
B_1	Unity-gain bandwidth (see Figure 3)	R_L = 10 kΩ,	C_L = 100 pF	25°C		1.8		MHz
		R_L = 100 Ω,	C_L = 100 pF	25°C		1.3		
	Settling time	0.1%		25°C		5		µs
		0.01%		25°C		10		
B_{OM}	Maximum-output-swing bandwidth	A_{VD} = 1,	R_L = 10 kΩ	25°C		140		kHz
ϕ_m	Phase margin at unity gain (see Figure 3)	R_L = 10 kΩ,	C_L = 100 pF	25°C		58°		
		R_L = 100 Ω,	C_L = 100 pF	25°C		75°		

†Full range is – 40°C to 85°C.

electrical characteristics at specified free-air temperature, $V_{CC\pm} = \pm 15$ V (unless otherwise noted)

PARAMETER			TEST CONDITIONS	T_A	MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	TLE2061I	$V_{IC} = 0$, $R_S = 50\ \Omega$	25°C		0.6	3	mV
				Full range			4.3	
		TLE2061AI		25°C		0.5	1.5	
				Full range			2.9	
		TLE2061BI		25°C		0.3	0.5	
				Full range			1.3	
α_{VIO}	Temperature coefficient of input offset voltage			Full range		6		μV/°C
	Input offset voltage long-term drift (see Note 4)			25°C		0.04		μV/mo
I_{IO}	Input offset current			25°C		2		pA
				Full range			3	nA
I_{IB}	Input bias current			25°C		4		pA
				Full range			5	nA
V_{ICR}	Common-mode input voltage range			25°C	− 11 to 13	− 12 to 16		V
				Full range	− 11 to 13			V
V_{OM+}	Maximum positive peak output voltage swing		$R_L = 10\ k\Omega$	25°C	13.2	13.7		V
				Full range	13			
			$R_L = 600\ \Omega$	25°C	12.5	13.2		
				Full range	12			
V_{OM-}	Maximum negative peak output voltage swing		$R_L = 10\ k\Omega$	25°C	− 13.2	− 13.7		V
				Full range	− 13			
			$R_L = 600\ \Omega$	25°C	− 12.5	− 13		
				Full range	− 12			
A_{VD}	Large-signal differential voltage amplification		$V_O = \pm 10$ V, $R_L = 10\ k\Omega$	25°C	30	230		V/mV
				Full range	20			
			$V_O = 0$ to 8 V, $R_L = 600\ \Omega$	25°C	25	100		
				Full range	10			
			$V_O = 0$ to − 8 V, $R_L = 600\ \Omega$	25°C	3	25		
				Full range	1			
r_i	Input resistance			25°C		10^{12}		Ω
c_i	Input capacitance			25°C		4		pF
z_o	Open-loop output impedance		$I_O = 0$	25°C		280		Ω
CMRR	Common-mode rejection ratio		$R_S = 50\ \Omega$, $V_{IC} = V_{ICR}$ min	25°C	72	90		dB
				Full range	65			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm} / \Delta V_{IO}$)		$V_{CC\pm} = \pm 5$ V to ± 15 V, $R_S = 50\ \Omega$	25°C	75	93		dB
				Full range	65			
I_{CC}	Supply current		$V_O = 0$, No load	25°C		290	350	μA
				Full range			375	
ΔI_{CC}	Supply current change over operating temperature range			Full range		34		μA

† Full range is − 40°C to 85°C.

NOTE 4: Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at $T_A = 150°C$ extrapolated to $T_A = 25°C$ using the Arrhenius equation and assuming an activation energy of 0.96 eV.

operating characteristics at specified free-air temperature, $V_{CC\pm} = \pm 15$ V

PARAMETER		TEST CONDITIONS		T_A	MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain (see Figure 1)	R_L = 10 kΩ,	C_L = 100 pF	25°C	2.6	3.4		V/μs
				Full range	2.1			
V_n	Equivalent input noise voltage (see Figure 2)	f = 10 Hz,	R_S = 100 Ω	25°C		70	100	nV/√Hz
		f = 1 kHz,	R_S = 100 Ω	25°C		40	60	
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 10 Hz		25°C		1.1		μV
I_n	Equivalent input noise current	f = 1 kHz		25°C		1.1		fA/√Hz
THD	Total harmonic distortion	A_{VD} = 2, $V_{O(PP)}$ = 2 V,	f = 10 kHz, R_L = 10 kΩ	25°C		0.025%		
B_1	Unity-gain bandwidth (see Figure 3)	R_L = 10 kΩ,	C_L = 100 pF	25°C		2		MHz
		R_L = 600 Ω,	C_L = 100 pF	25°C		1.5		
	Settling time	0.1%		25°C		5		μs
		0.01%		25°C		10		
B_{OM}	Maximum-output-swing bandwidth	A_{VD} = 1,	R_L = 10 kΩ	25°C		40		kHz
ϕ_m	Phase margin at unity gain (see Figure 3)	R_L = 10 kΩ,	C_L = 100 pF	25°C		60°		
		R_L = 600 Ω,	C_L = 100 pF	25°C		70°		

†Full range is – 40°C to 85°C.

electrical characteristics at specified free-air temperature, $V_{CC\pm} = \pm 20$ V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A	MIN	TYP	MAX	UNIT
V_{IO} Input offset voltage	TLE2061I	$V_{IC} = 0$, $R_S = 50\ \Omega$	25°C		0.6	3	mV
			Full range			4.3	
	TLE2061AI		25°C		0.6	1.6	
			Full range			2.9	
	TLE2061BI		25°C		0.3	0.5	
			Full range			1.3	
α_{VIO} Temperature coefficient of input offset voltage			Full range		6		μV/°C
Input offset voltage long-term drift (see Note 4)			25°C		0.04		μV/mo
I_{IO} Input offset current			25°C		3		pA
			Full range			3	nA
I_{IB} Input bias current			25°C		5		pA
			Full range			5	nA
V_{ICR} Common-mode input voltage range			25°C	– 15 to 16.5	– 17 to 21		V
			Full range	– 15 to 16.5			V
V_{OM+} Maximum positive peak output voltage swing		$R_L = 10\ k\Omega$	25°C	18.2	18.7		V
			Full range	18			
		$R_L = 600\ \Omega$	25°C	15	18.1		
			Full range	12			
V_{OM-} Maximum negative peak output voltage swing		$R_L = 10\ k\Omega$	25°C	– 18.2	– 18.7		V
			Full range	– 18			
		$R_L = 600\ \Omega$	25°C	– 15	– 18		
			Full range	– 12			
A_{VD} Large-signal differential voltage amplification		$V_O = \pm 15$ V, $R_L = 10\ k\Omega$	25°C	30	280		V/mV
			Full range	20			
		$V_O = 0$ to 10 V, $R_L = 600\ \Omega$	25°C	25	80		
			Full range	10			
		$V_O = 0$ to – 10 V, $R_L = 600\ \Omega$	25°C	3	20		
			Full range	1			
r_i Input resistance			25°C		10^{12}		Ω
c_i Input capacitance			25°C		4		pF
z_o Open-loop output impedance		$I_O = 0$	25°C		280		Ω
CMRR Common-mode rejection ratio		$R_S = 50\ \Omega$, $V_{IC} = V_{ICR}$ min	25°C	75	91		dB
			Full range	65			
k_{SVR} Supply-voltage rejection ratio ($\Delta V_{CC\pm} / \Delta V_{IO}$)		$V_{CC\pm} = \pm 5$ V to ± 20 V, $R_S = 50\ \Omega$	25°C	75	93		dB
			Full range	65			
I_{CC} Supply current		$V_O = 0$, No load	25°C		300	375	μA
			Full range			400	
ΔI_{CC} Supply current change over operating temperature range			Full range		36		μA

†Full range is – 40°C to 85°C.

NOTE 4: Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at $T_A = 150°C$ extrapolated to $T_A = 25°C$ using the Arrhenius equation and assuming an activation energy of 0.96 eV.

operating characteristics at specified free-air temperature, $V_{CC\pm} = \pm 20$ V

PARAMETER		TEST CONDITIONS		T_A	MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain (see Figure 1)	R_L = 10 kΩ,	C_L = 100 pF	25°C	2.8	3.4		V/μs
				Full range	2.1			
V_n	Equivalent input noise voltage (see Figure 2)	f = 10 Hz,	R_S = 100 Ω	25°C		75	100	nV/√Hz
		f = 1 kHz,	R_S = 100 Ω	25°C		40	60	
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 10 Hz		25°C		1.1		μV
I_n	Equivalent input noise current	f = 1 kHz		25°C		1.3		fA/√Hz
THD	Total harmonic distortion	A_{VD} = 2, $V_{O(PP)}$ = 2 V,	f = 10 kHz, R_L = 10 kΩ	25°C		0.025%		
B_1	Unity-gain bandwidth (see Figure 3)	R_L = 10 kΩ,	C_L = 100 pF	25°C		2.1		MHz
		R_L = 600 Ω,	C_L = 100 pF	25°C		1.6		
	Settling time	0.1%		25°C		5		μs
		0.01%		25°C		10		
B_{OM}	Maximum-output-swing bandwidth	A_{VD} = 1,	R_L = 10 kΩ	25°C		28		kHz
ϕ_m	Phase margin at unity gain (see Figure 3)	R_L = 10 kΩ,	C_L = 100 pF	25°C		60°		
		R_L = 600 Ω,	C_L = 100 pF	25°C		70°		

†Full range is – 40°C to 85°C.

electrical characteristics at specified free-air temperature, $V_{CC\pm} = \pm 5$ V (unless otherwise noted)

PARAMETER			TEST CONDITIONS	T_A	MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	TLE2061M	$V_{IC} = 0$, $R_S = 50\ \Omega$	25°C		0.8	3.1	mV
				Full range			6	
		TLE2061AM		25°C		0.6	2.6	
				Full range			4.6	
		TLE2061BM		25°C		0.5	1.9	
				Full range			3.1	
α_{VIO}	Temperature coefficient of input offset voltage			Full range		6		µV/°C
	Input offset voltage long-term drift (see Note 4)			25°C		0.04		µV/mo
I_{IO}	Input offset current			25°C		1		pA
				Full range			15	nA
I_{IB}	Input bias current			25°C		3		pA
				Full range			30	nA
V_{ICR}	Common-mode input voltage range			25°C	− 1.6 to 4	− 2 to 6		V
				Full range	− 1.6 to 4			V
V_{OM+}	Maximum positive peak output voltage swing		$R_L = 10\ k\Omega$	25°C	3.5	3.7		V
				Full range	3			
			$R_L = 600\ \Omega$	25°C	2.5	3.6		
				Full range	2			
			$R_L = 100\ \Omega$	25°C	2.5	3.1		
				Full range	2			
V_{OM-}	Maximum negative peak output voltage swing		$R_L = 10\ k\Omega$	25°C	− 3.5	− 3.9		V
				Full range	− 3			
		FK, and JG packages	$R_L = 600\ \Omega$	25°C	− 2.5	− 3.5		
				Full range	− 2			
		D and P packages	$R_L = 100\ \Omega$	25°C	− 2.5	− 2.7		
				Full range	− 2			
A_{VD}	Large-signal differential voltage amplification		$V_O = \pm 2.8$ V, $R_L = 10\ k\Omega$	25°C	15	80		V/mV
				Full range	2			
		FK, and JG packages	$V_O = 0$ to 2.5 V, $R_L = 600\ \Omega$	25°C	1	65		
				Full range	0.5			
			$V_O = 0$ to − 2.5 V, $R_L = 600\ \Omega$	25°C	1	16		
				Full range	0.5			
		D and P packages	$V_O = 0$ to 2 V, $R_L = 100\ \Omega$	25°C	0.75	45		
				Full range	0.5			
			$V_O = 0$ to − 2 V, $R_L = 100\ \Omega$	25°C	0.5	3		
				Full range	0.25			

† Full range is − 55°C to 125°C.

NOTE 4: Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at T_A = 150°C extrapolated to T_A = 25°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

electrical characteristics at specified free-air temperature, $V_{CC\pm}$ = ±5 V (unless otherwise noted) (continued)

PARAMETER		TEST CONDITIONS	T_A†	MIN	TYP	MAX	UNIT
r_i	Input resistance		25°C		10^{12}		Ω
c_i	Input capacitance		25°C		4		pF
z_o	Open-loop output impedance	$I_O = 0$	25°C		280		Ω
CMRR	Common-mode rejection ratio	R_S = 50 Ω, $V_{IC} = V_{ICR}$ min	25°C	65	82		dB
			Full range	60			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm} / \Delta V_{IO}$)	$V_{CC\pm}$ = ±5 V to ±20 V, R_S = 50 Ω	25°C	75	93		dB
			Full range	65			
I_{CC}	Supply current	$V_O = 0$, No load	25°C		280	325	μA
			Full range			350	
ΔI_{CC}	Supply current change over operating temperature range		Full range		39		μA

†Full range is – 55°C to 125°C.

operating characteristics at specified free-air temperature, $V_{CC\pm}$ = ±5 V

PARAMETER		TEST CONDITIONS		T_A	MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain (see Figure 1)	R_L = 10 kΩ,	C_L = 100 pF	25°C		3.4		V/μs
V_n	Equivalent input noise voltage (see Figure 2)	f = 10 Hz,	R_S = 100 Ω	25°C		59		nV/√Hz
		f = 1 kHz,	R_S = 100 Ω	25°C		43		
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 10 Hz		25°C		1.1		μV
I_n	Equivalent input noise current	f = 1 kHz		25°C		1		fA/√Hz
THD	Total harmonic distortion	A_{VD} = 2, $V_{O(PP)}$ = 2 V,	f = 10 kHz, R_L = 10 kΩ	25°C		0.025%		
B_1	Unity-gain bandwidth (see Figure 3)	R_L = 10 kΩ,	C_L = 100 pF	25°C		1.8		MHz
		R_L = 600 Ω,	C_L = 100 pF	25°C		1.3		
	Settling time	0.1%		25°C		5		μs
		0.01%		25°C		10		
B_{OM}	Maximum-output-swing bandwidth	A_{VD} = 1,	R_L = 10 kΩ	25°C		140		kHz
ϕ_m	Phase margin at unity gain (see Figure 3)	R_L = 10 kΩ,	C_L = 100 pF	25°C		58°		
		R_L = 600 Ω,	C_L = 100 pF	25°C		75°		

electrical characteristics at specified free-air temperature, $V_{CC\pm} = \pm 15$ V (unless otherwise noted)

PARAMETER			TEST CONDITIONS	T_A	MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	TLE2061M	$V_{IC} = 0$, $R_S = 50\ \Omega$	25°C		0.6	3	mV
				Full range			6	
		TLE2061AM		25°C		0.5	1.5	
				Full range			3.6	
		TLE2061BM		25°C		0.3	0.5	
				Full range			1.7	
α_{VIO}	Temperature coefficient of input offset voltage			Full range		6		µV/°C
	Input offset voltage long-term drift (see Note 4)			25°C		0.04		µV/mo
I_{IO}	Input offset current			25°C		2		pA
				Full range			20	nA
I_{IB}	Input bias current			25°C		4		pA
				Full range			40	nA
V_{ICR}	Common-mode input voltage range			25°C	− 11 to 13	− 12 to 16		V
				Full range	− 11 to 13			V
V_{OM+}	Maximum positive peak output voltage swing		$R_L = 10\ k\Omega$	25°C	13	13.7		V
				Full range	12.5			
			$R_L = 600\ \Omega$	25°C	12.5	13.2		
				Full range	12			
V_{OM-}	Maximum negative peak output voltage swing		$R_L = 10\ k\Omega$	25°C	− 13	− 13.7		V
				Full range	− 12.5			
			$R_L = 600\ \Omega$	25°C	− 12.5	− 13		
				Full range	− 12			
A_{VD}	Large-signal differential voltage amplification		$V_O = \pm 10$ V, $R_L = 10\ k\Omega$	25°C	30	230		V/mV
				Full range	20			
			$V_O = 0$ to 8 V, $R_L = 600\ \Omega$	25°C	25	100		
				Full range	7			
			$V_O = 0$ to − 8 V, $R_L = 600\ \Omega$	25°C	3	25		
				Full range	1			
r_i	Input resistance			25°C		10^{12}		Ω
c_i	Input capacitance			25°C		4		pF
z_o	Open-loop output impedance		$I_O = 0$	25°C		280		Ω
CMRR	Common-mode rejection ratio		$R_S = 50\ \Omega$, $V_{IC} = V_{ICR}$ min	25°C	72	90		dB
				Full range	65			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm} / \Delta V_{IO}$)		$V_{CC\pm} = \pm 5$ V to ± 15 V, $R_S = 50\ \Omega$	25°C	75	93		dB
				Full range	65			
I_{CC}	Supply current		$V_O = 0$, No load	25°C		290	350	µA
				Full range			375	
ΔI_{CC}	Supply current change over operating temperature range			Full range		46		µA

†Full range is – 55°C to 125°C.

NOTE 4: Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at $T_A = 150°C$ extrapolated to $T_A = 25°C$ using the Arrhenius equation and assuming an activation energy of 0.96 eV.

operating characteristics at specified free-air temperature, $V_{CC\pm} = \pm 15$ V

PARAMETER		TEST CONDITIONS		T_A	MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain (see Figure 1)	R_L = 10 kΩ,	C_L = 100 pF	25°C	2	3.4		V/μs
				Full range	1.8			
V_n	Equivalent input noise voltage (see Figure 2)	f = 10 Hz,	R_S = 100 Ω	25°C		70		nV/√Hz
		f = 1 kHz,	R_S = 100 Ω	25°C		40		
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 10 Hz		25°C		1.1		μV
I_n	Equivalent input noise current	f = 1 kHz		25°C		1.1		fA/√Hz
THD	Total harmonic distortion	A_{VD} = 2, $V_{O(PP)}$ = 2 V,	f = 10 kHz, R_L = 10 kΩ	25°C		0.025%		
B_1	Unity-gain bandwidth (see Figure 3)	R_L = 10 kΩ,	C_L = 100 pF	25°C		2		MHz
		R_L = 600 Ω,	C_L = 100 pF	25°C		1.5		
	Settling time	0.1%		25°C		5		μs
		0.01%		25°C		10		
B_{OM}	Maximum-output-swing bandwidth	A_{VD} = 1,	R_L = 10 kΩ	25°C		40		kHz
ϕ_m	Phase margin at unity gain (see Figure 3)	R_L = 10 kΩ,	C_L = 100 pF	25°C		60°		
		R_L = 600 Ω,	C_L = 100 pF	25°C		70°		

† Full range is – 55°C to 125°C.

electrical characteristics at specified free-air temperature, $V_{CC\pm} = \pm 20$ V (unless otherwise noted)

PARAMETER			TEST CONDITIONS	T_A	MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	TLE2061M	$V_{IC} = 0$, $R_S = 50\ \Omega$	25°C		0.6	3	mV
				Full range			6	
		TLE2061AM		25°C		0.6	1.6	
				Full range			3.6	
		TLE2061BM		25°C		0.3	0.5	
				Full range			1.7	
α_{VIO}	Temperature coefficient of input offset voltage			Full range		6		μV/°C
	Input offset voltage long-term drift (see Note 4)			25°C		0.04		μV/mo
I_{IO}	Input offset current			25°C		3		pA
				Full range			20	nA
I_{IB}	Input bias current			25°C		5		pA
				Full range			40	nA
V_{ICR}	Common-mode input voltage range			25°C	−15 to 16.5	−17 to 21		V
				Full range	−15 to 16.5			V
V_{OM+}	Maximum positive peak output voltage swing		$R_L = 10\ k\Omega$	25°C	18	18.7		V
				Full range	17.5			
			$R_L = 600\ \Omega$	25°C	15	18.1		
				Full range	12			
V_{OM-}	Maximum negative peak output voltage swing		$R_L = 10\ k\Omega$	25°C	−18	−18.7		V
				Full range	−17.5			
			$R_L = 600\ \Omega$	25°C	−15	−18		
				Full range	−12			
A_{VD}	Large-signal differential voltage amplification		$V_O = \pm 15$ V, $R_L = 10\ k\Omega$	25°C	30	280		V/mV
				Full range	20			
			$V_O = 0$ to 10 V, $R_L = 600\ \Omega$	25°C	25	80		
				Full range	10			
			$V_O = 0$ to -10 V, $R_L = 600\ \Omega$	25°C	3	20		
				Full range	1			
r_i	Input resistance			25°C		10^{12}		Ω
c_i	Input capacitance			25°C		4		pF
z_o	Open-loop output impedance		$I_O = 0$	25°C		280		Ω
CMRR	Common-mode rejection ratio		$R_S = 50\ \Omega$, $V_{IC} = V_{ICR}$ min	25°C	75	91		dB
				Full range	65			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm} / \Delta V_{IO}$)		$V_{CC\pm} = \pm 5$ V to ± 20 V, $R_S = 50\ \Omega$	25°C	75	93		dB
				Full range	65			
I_{CC}	Supply current		$V_O = 0$, No load	25°C		300	375	μA
				Full range			400	
ΔI_{CC}	Supply current change over operating temperature range			Full range		50		μA

† Full range is −55°C to 125°C.

NOTE 4: Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at $T_A = 150°C$ extrapolated to $T_A = 25°C$ using the Arrhenius equation and assuming an activation energy of 0.96 eV.

operating characteristics at specified free-air temperature, $V_{CC\pm} = \pm 20$ V

PARAMETER		TEST CONDITIONS		T_A	MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain (see Figure 1)	$R_L = 10\ k\Omega$,	$C_L = 100$ pF	25°C		3.4		V/μs
V_n	Equivalent input noise voltage (see Figure 2)	f = 10 Hz,	$R_S = 100\ \Omega$	25°C		75		nV/√Hz
		f = 1 kHz,	$R_S = 100\ \Omega$	25°C		40		
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 10 Hz		25°C		1.1		μV
I_n	Equivalent input noise current	f = 1 kHz		25°C		1.3		fA/√Hz
THD	Total harmonic distortion	$A_{VD} = 2$, $V_{O(PP)} = 2$ V,	f = 10 kHz, $R_L = 10\ k\Omega$	25°C		0.025%		
B_1	Unity-gain bandwidth (see Figure 3)	$R_L = 10\ k\Omega$,	$C_L = 100$ pF	25°C		2.1		MHz
		$R_L = 600\ \Omega$,	$C_L = 100$ pF	25°C		1.6		
	Settling time	0.1%		25°C		5		μs
		0.01%		25°C		10		
B_{OM}	Maximum-output-swing bandwidth	$A_{VD} = 1$,	$R_L = 10\ k\Omega$	25°C		28		kHz
ϕ_m	Phase margin at unity gain (see Figure 3)	$R_L = 10\ k\Omega$,	$C_L = 100$ pF	25°C		60°		
		$R_L = 600\ \Omega$,	$C_L = 100$ pF	25°C		70°		

electrical characteristics at $V_{CC\pm}$ = ±15 V, T_A = 25°C (unless otherwise noted)

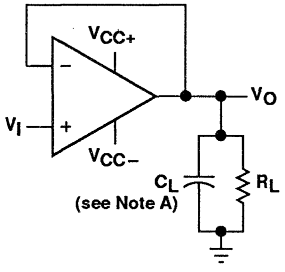
PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	$V_{IC} = 0$,	$R_S = 50\ \Omega$		0.6	3	mV
$\propto V_{io}$	Input offset voltage long-term drift (see Note 4)				0.04		μV/mo
I_{IO}	Input offset current				2		pA
I_{IB}	Input bias current				4		pA
V_{ICR}	Common-mode input voltage range			−11 to 13	−12 to 16		V
V_{OM+}	Maximum positive peak output voltage swing	$R_L = 10\ k\Omega$		13.2	13.7		V
		$R_L = 600\ \Omega$		12.5	13.2		
V_{OM-}	Maximum negative peak output voltage swing	$R_L = 10\ k\Omega$		−13.2	−13.7		V
		$R_L = 600\ \Omega$		−12.5	−13		
A_{VD}	Large-signal differential voltage amplification	$V_O = \pm 10$ V,	$R_L = 10\ k\Omega$	30	230		V/mV
		$V_O = 0$ to 8 V,	$R_L = 600\ \Omega$	25	100		
		$V_O = 0$ to −8 V,	$R_L = 600\ \Omega$	3	25		
r_i	Input resistance				10^{12}		Ω
c_i	Input capacitance				4		pF
z_o	Open-loop ouput impedance	$I_O = 0$			280		Ω
CMRR	Common-mode rejection ratio	$R_S = 50\ \Omega$,	$V_{IC} = V_{ICR}$min	72	90		dB
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC}/\Delta V_{IO}$)	$V_{CC\pm} = \pm 5$ V to ±15 V, $R_S = 50\ \Omega$		75	93		dB
I_{CC}	Supply current	$V_O = 0$,	No load		290	350	μA

NOTE 4: Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at T_A = 150°C extrapolated to T_A = 25°C using the Arrhenius equation and assuming and activation energy of 0.96 eV.

operating characteristics at $V_{CC\pm}$ = ±15 V, T_A = 25°C

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain	$R_L = 10\ k\Omega$,	$C_L = 100$ pF	2.6	3.4		V/μs
V_n	Equivalent input noise voltage (see Figure 2)	f = 10 Hz,	$R_S = 100\ \Omega$		70		nV/√Hz
		f = 1 kHz,	$R_S = 100\ \Omega$		40		
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 10 Hz			1.1		μV
I_n	Equivalent input noise current	f = 1 Hz			1.1		fA/√Hz
THD	Total harmonic distortion	$A_{VD} = 2$, $V_{O(PP)} = 2$ V,	f = 10 kHz, $R_L = 10\ k\Omega$		0.025%		
B_1	Unity gain-bandwidth (see Figure 3)	$R_L = 10\ k\Omega$,	$C_L = 100$ pF		2		MHz
		$R_L = 600\ \Omega$,	$C_L = 100$ pF		1.5		
	Settling time	0.1%			5		μs
		0.01%			10		
B_{OM}	Maximum-output-swing bandwidth	$A_{VD} = 1$,	$R_L = 10\ k\Omega$		40		kHz
ϕ_m	Phase margin at unity gain (see Figure 3)	$R_L = 10\ k\Omega$,	$C_L = 100$ pF		60°		
		$R_L = 600\ \Omega$,	$C_L = 100$ pF		70°		

PARAMETER MEASUREMENT INFORMATION



NOTE A: C_L includes fixture capacitance.

Figure 1. Slew Rate Test Circuit

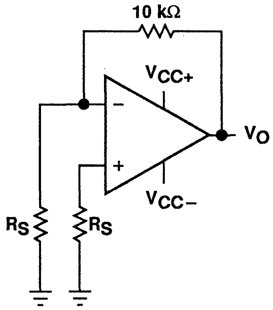
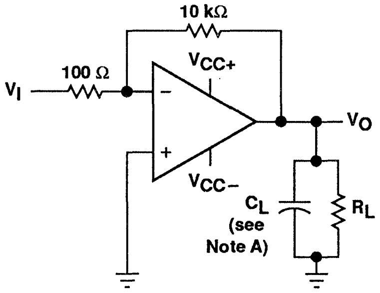


Figure 2. Noise Voltage Test Circuit



NOTE A: C_L includes fixture capacitance.

Figure 3. Unity-Gain Bandwidth and Phase Margin Test Circuit

typical values

Typical values as presented in this data sheet represent the median (50% point) of device parametric performance.

input bias and offset current

At the picoamp bias current level typical of the TLE2061, TLE2061A, and TLE2061B, accurate measurement of the bias current becomes difficult. Not only does this measurement require a picoammeter, but test socket leakages can easily exceed the actual device bias currents. To accurately measure these small currents, Texas Instruments uses a two-step process. The socket leakage is measured using picoammeters with bias voltages applied but with no device in the socket. The device is then inserted into the socket and a second test that measures both the socket leakage and the device input bias current is performed. The two measurements are then subtracted algebraically to determine the bias current of the device.

TYPICAL CHARACTERISTICS

table of graphs

			FIGURE
V_{IO}	Input offset voltage	Distribution	4
I_{IB}	Input bias current	vs Common-mode voltage vs Temperature	5 6
I_{IO}	Input offset current	vs Temperature	6
V_{ICR}	Common-mode input voltage range limits	vs Temperature	7
V_{OM}	Maximum peak output voltage swing	vs Output current vs Supply voltage	8, 9 10, 11, 12
$V_{O(PP)}$	Maximum peak-to-peak output voltage	vs Frequency	13, 14, 15
A_{VD}	Differential voltage amplification	vs Frequency vs Temperature	16 17
I_{OS}	Short-circuit output current	vs Time vs Temperature	18 19
z_o	Output impedance	vs Frequency	20
CMRR	Common-mode rejection ratio	vs Frequency	21
I_{CC}	Supply current	vs Supply voltage vs Temperature	22 23
	Pulse response	Small-signal Large-signal	24, 25 26, 27
	Noise voltage (referred to input)	0.1 to 10 Hz	28
V_n	Equivalent input noise voltage	vs Frequency	29
THD	Total harmonic distortion	vs Frequency	30, 31
B_1	Unity-gain bandwidth	vs Supply voltage vs Temperature	32 33
ϕ_m	Phase margin	vs Supply voltage vs Load capacitance vs Temperature	34 35 36
	Phase shift	vs Frequency	16

TYPICAL CHARACTERISTICS[†]

TLE2061
DISTRIBUTION OF
INPUT OFFSET VOLTAGE

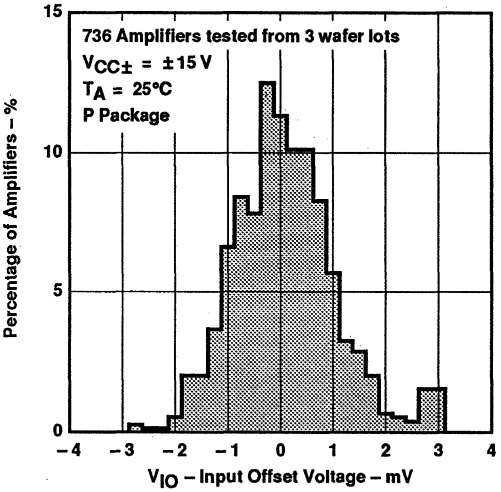


Figure 4

INPUT BIAS CURRENT
vs
COMMON-MODE INPUT VOLTAGE

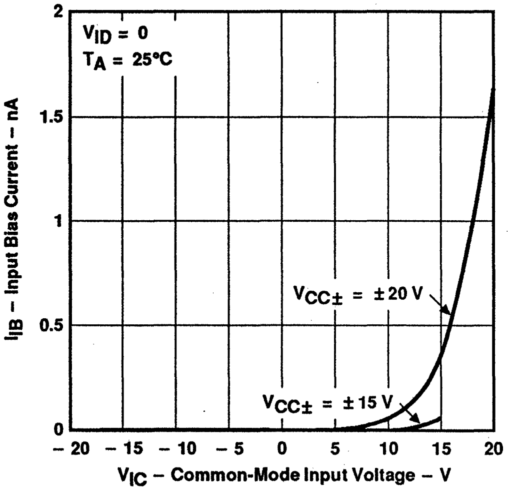


Figure 5

INPUT BIAS CURRENT
and INPUT OFFSET CURRENT
vs
FREE-AIR TEMPERATURE

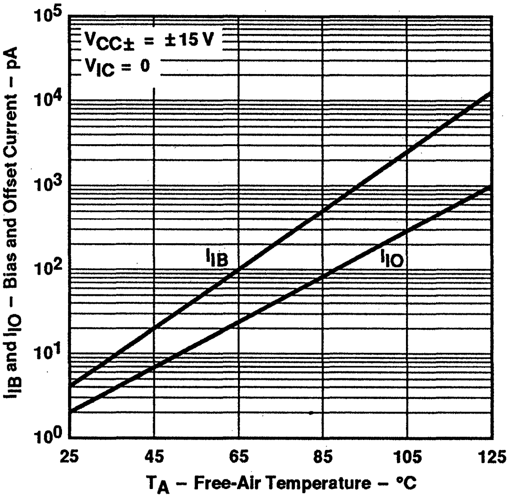


Figure 6

COMMON-MODE
INPUT VOLTAGE RANGE LIMITS
vs
FREE-AIR TEMPERATURE

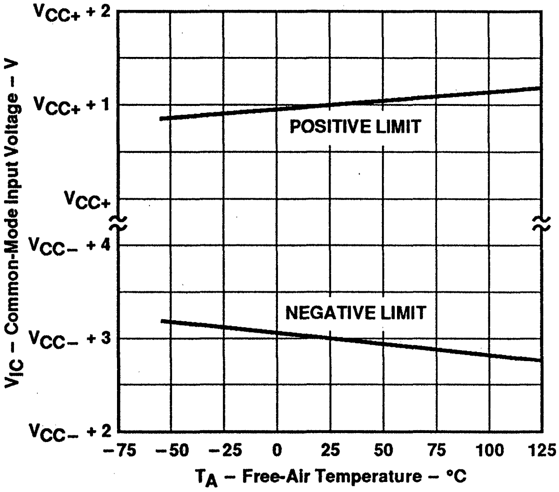


Figure 7

[†] Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS

MAXIMUM POSITIVE PEAK OUTPUT VOLTAGE vs OUTPUT CURRENT

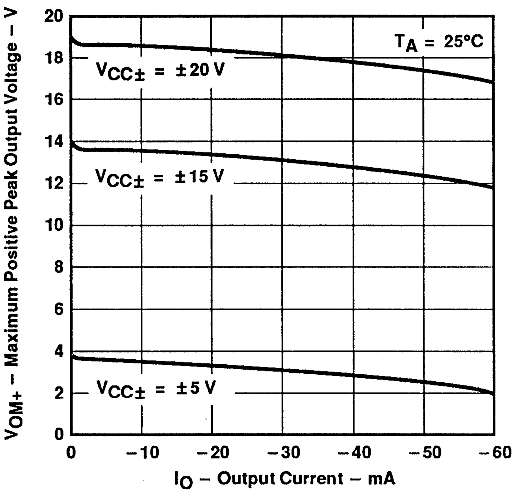


Figure 8

MAXIMUM NEGATIVE PEAK OUTPUT VOLTAGE vs OUTPUT CURRENT

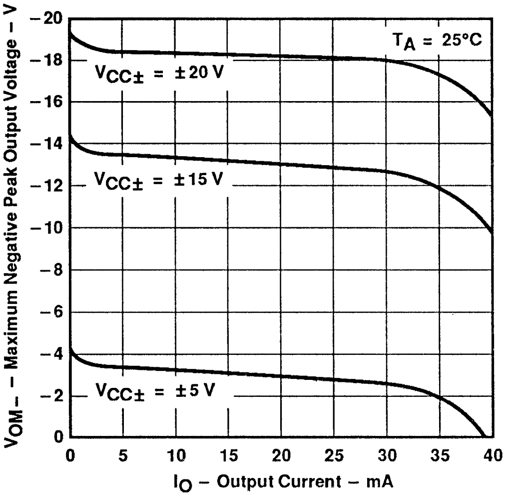


Figure 9

MAXIMUM PEAK OUTPUT VOLTAGE vs SUPPLY VOLTAGE

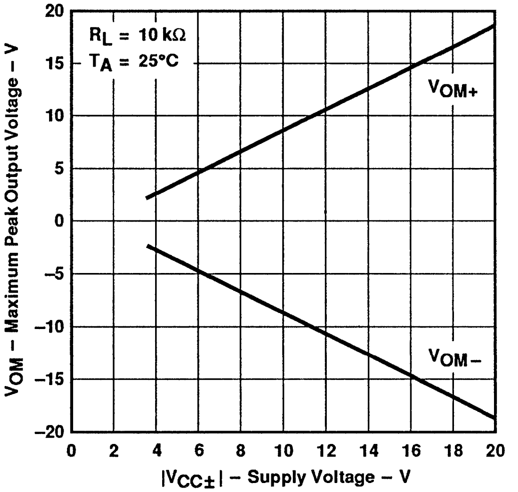


Figure 10

MAXIMUM PEAK OUTPUT VOLTAGE vs SUPPLY VOLTAGE

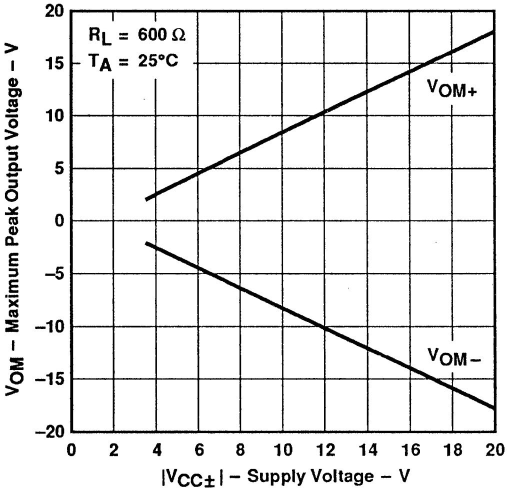


Figure 11

TYPICAL CHARACTERISTICS

MAXIMUM PEAK OUTPUT VOLTAGE vs SUPPLY VOLTAGE

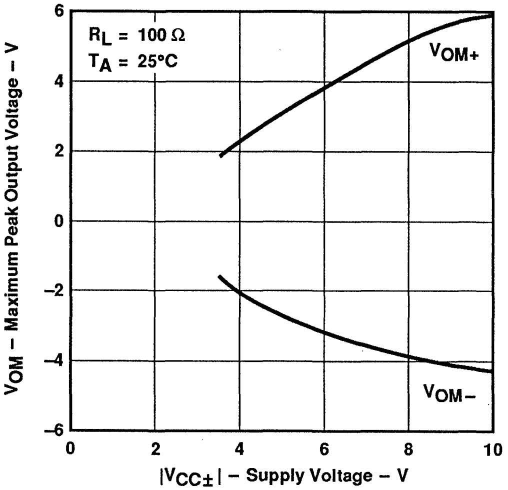


Figure 12

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE vs FREQUENCY

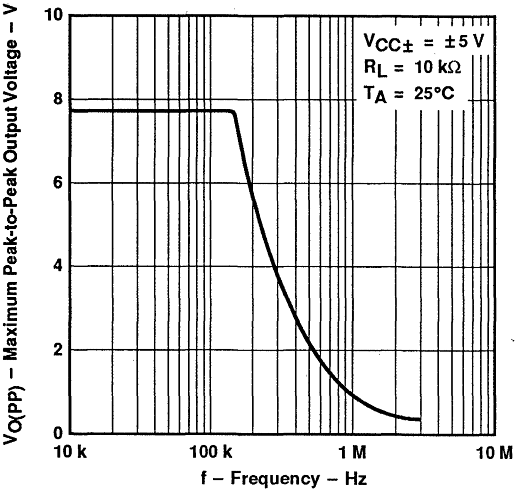


Figure 13

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE vs FREQUENCY

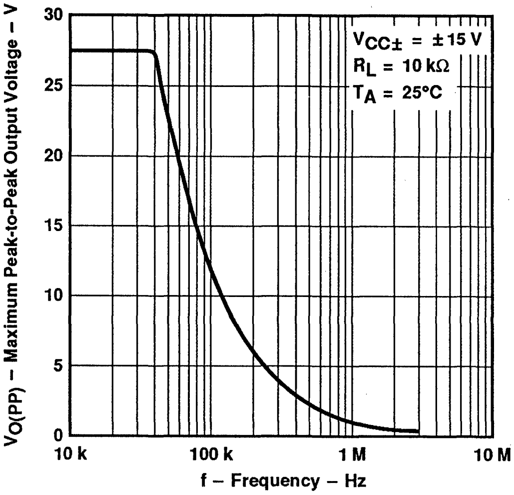


Figure 14

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE vs FREQUENCY

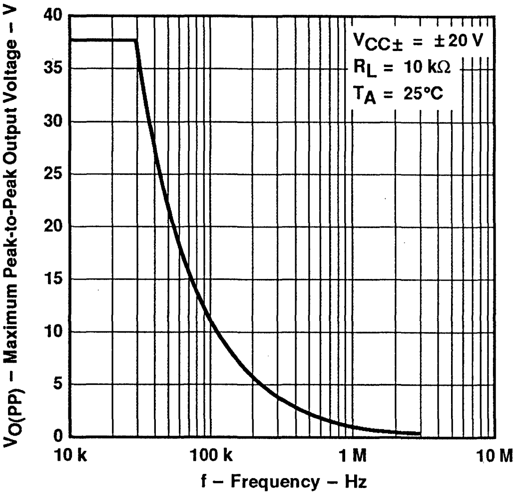


Figure 15

TYPICAL CHARACTERISTICS†

LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION and PHASE SHIFT
vs
FREQUENCY

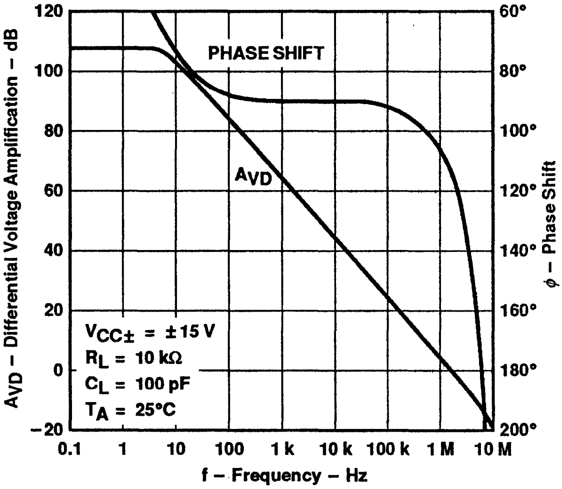


Figure 16

LARGE-SIGNAL VOLTAGE AMPLIFICATION
vs
FREE-AIR TEMPERATURE

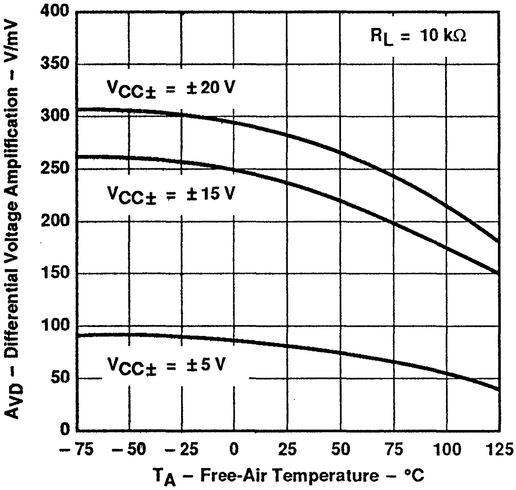


Figure 17

SHORT-CIRCUIT OUTPUT CURRENT
vs
ELAPSED TIME

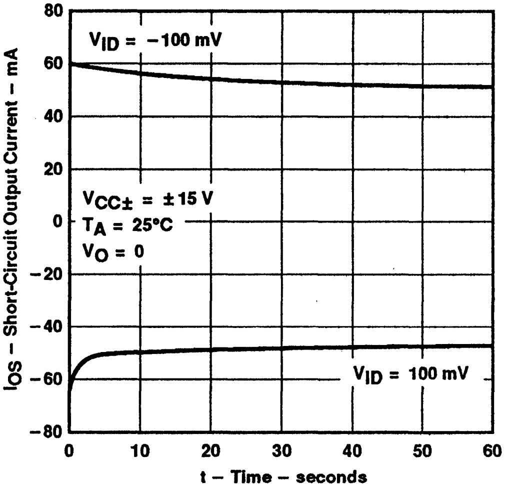


Figure 18

SHORT-CIRCUIT OUTPUT CURRENT
vs
FREE-AIR TEMPERATURE

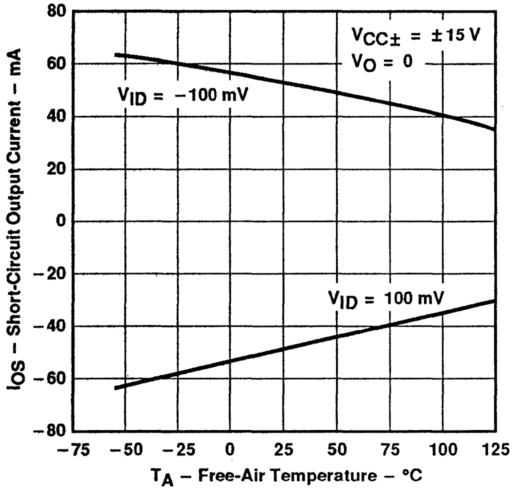


Figure 19

---

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS[†]

OUTPUT IMPEDANCE
vs
FREQUENCY

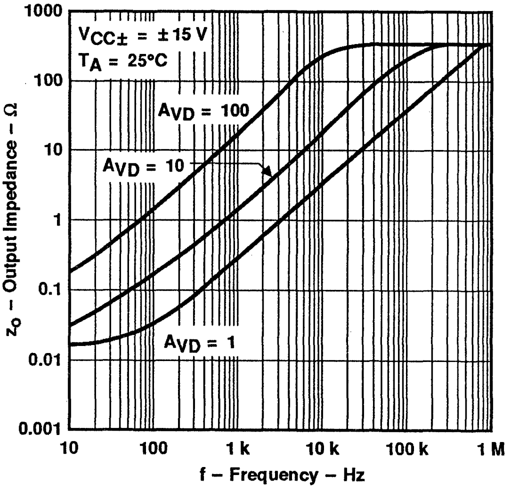


Figure 20

COMMON-MODE REJECTION RATIO
vs
FREQUENCY

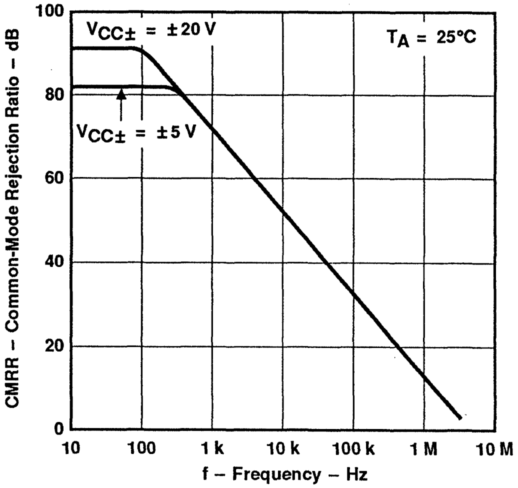


Figure 21

SUPPLY CURRENT
vs
SUPPLY VOLTAGE

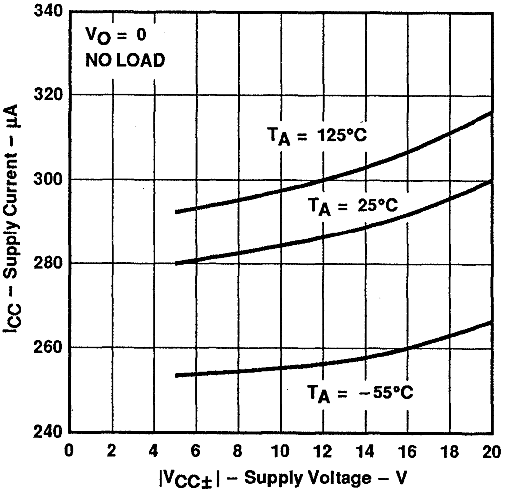


Figure 22

SUPPLY CURRENT
vs
FREE-AIR TEMPERATURE

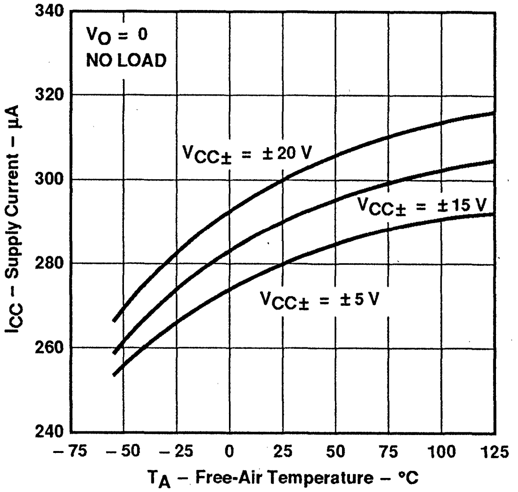


Figure 23

[†] Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS

VOLTAGE-FOLLOWER
SMALL-SIGNAL
PULSE RESPONSE

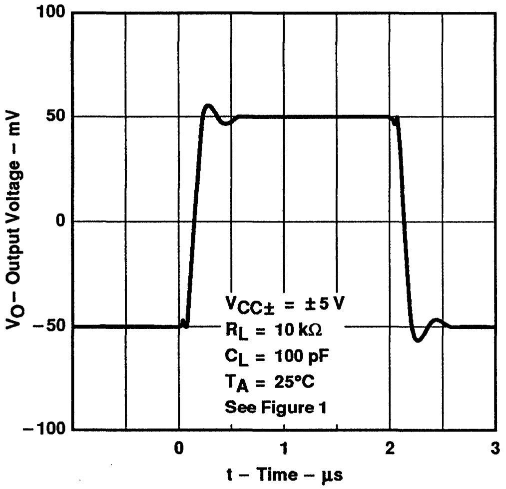


Figure 24

VOLTAGE-FOLLOWER
SMALL-SIGNAL
PULSE RESPONSE

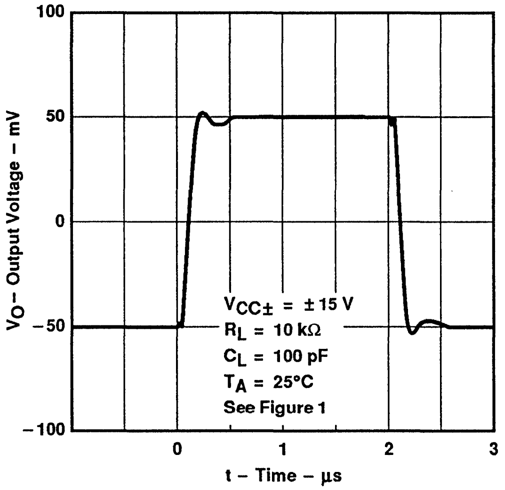


Figure 25

VOLTAGE-FOLLOWER
LARGE-SIGNAL
PULSE RESPONSE

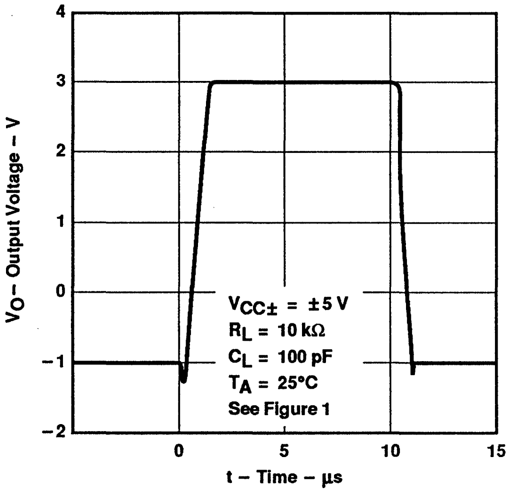


Figure 26

VOLTAGE-FOLLOWER
LARGE-SIGNAL
PULSE RESPONSE

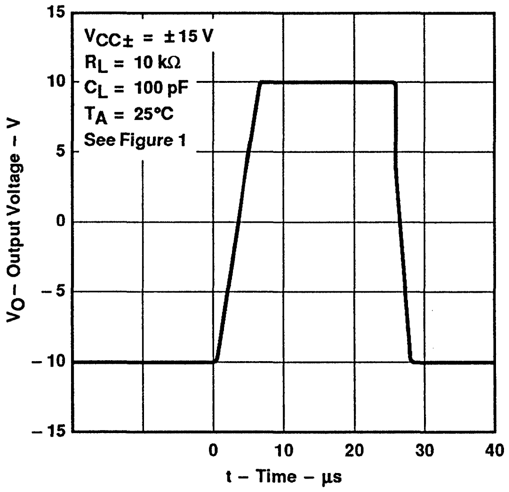


Figure 27

TYPICAL CHARACTERISTICS

NOISE VOLTAGE
(REFERRED TO INPUT)
OVER A 10-SECOND INTERVAL

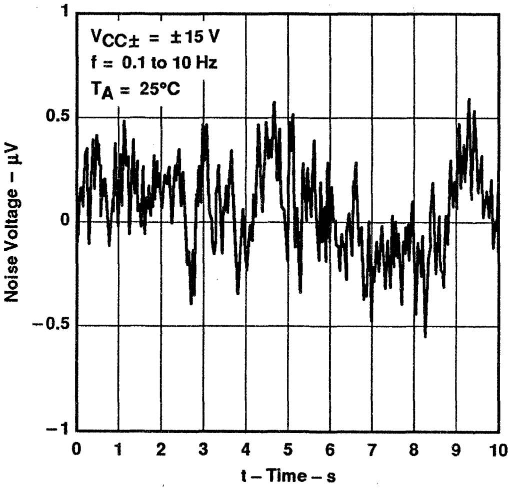


Figure 28

EQUIVALENT INPUT NOISE VOLTAGE
vs
FREQUENCY

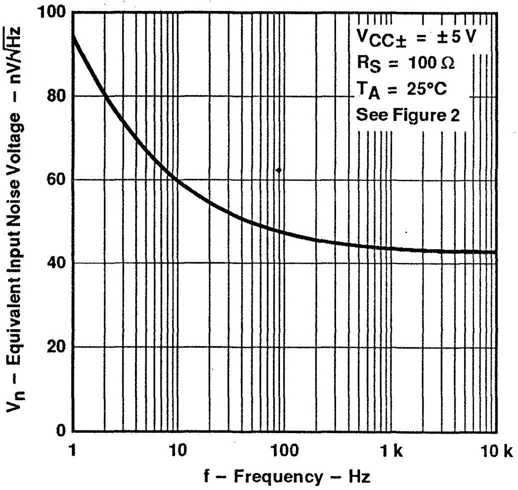


Figure 29

TOTAL HARMONIC DISTORTION
vs
FREQUENCY

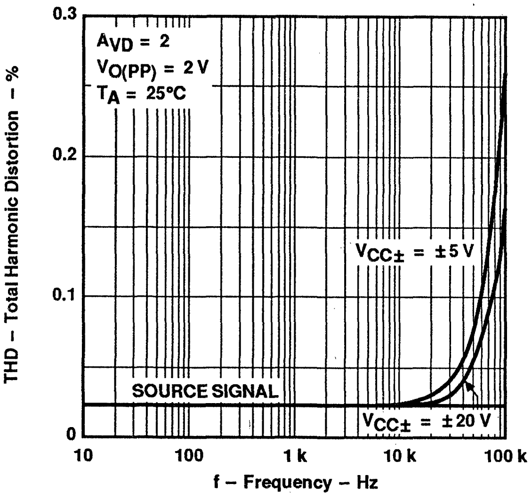


Figure 30

TOTAL HARMONIC DISTORTION
vs
FREQUENCY

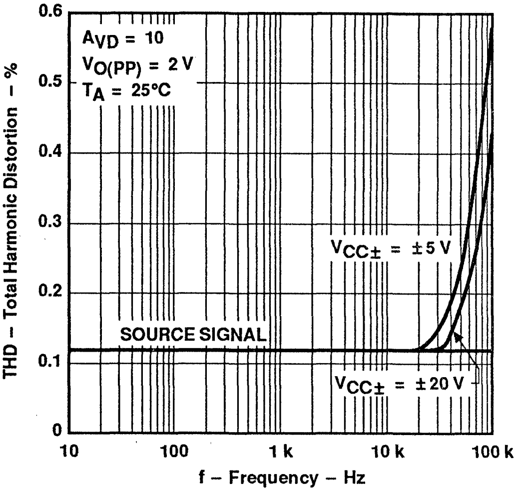


Figure 31

TYPICAL CHARACTERISTICS†

UNITY-GAIN BANDWIDTH
vs
SUPPLY VOLTAGE

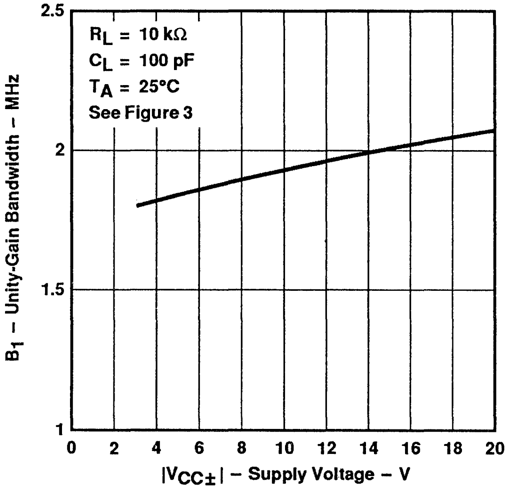


Figure 32

UNITY-GAIN BANDWIDTH
vs
FREE-AIR TEMPERATURE

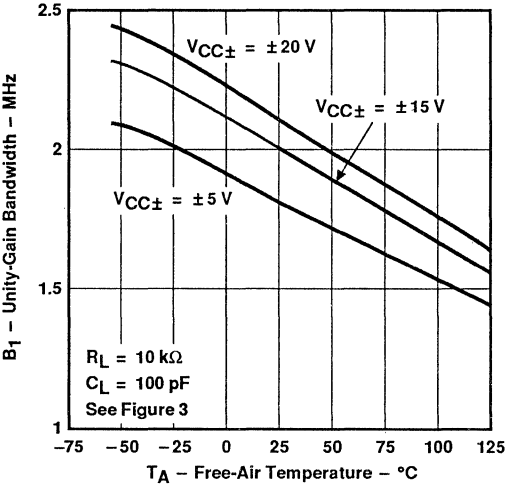


Figure 33

PHASE MARGIN
vs
SUPPLY VOLTAGE

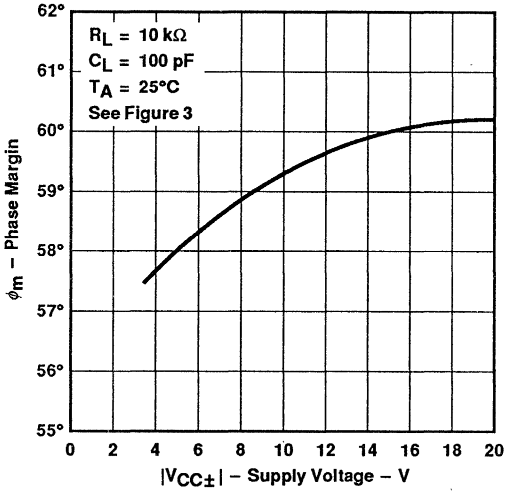


Figure 34

PHASE MARGIN
vs
LOAD CAPACITANCE

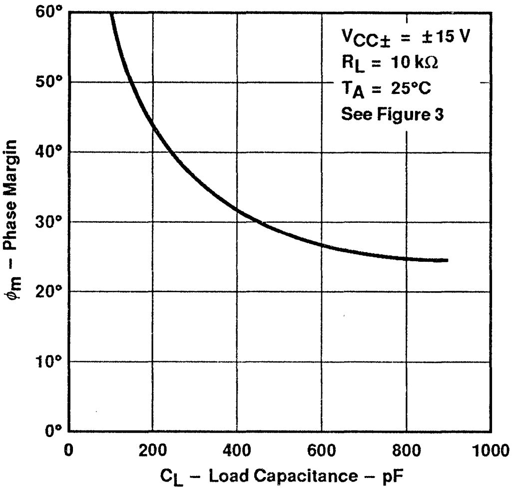


Figure 35

---

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

PHASE MARGIN vs FREE-AIR TEMPERATURE

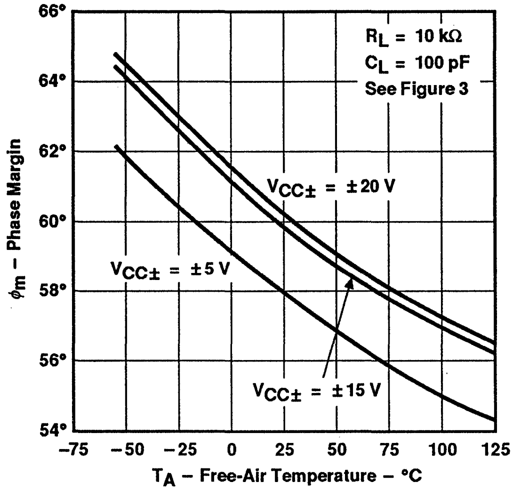


Figure 36

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

APPLICATION INFORMATION

macromodel information

Macromodel information provided was derived using *PSpice*™ *Parts*™ model generation software. The Boyle macromodel (see Note 5) and subcircuit in Figure 37 were generated using the TLE2061 typical electrical and operating characteristics at 25°C. Using this information, output simulations of the following key parameters can be generated to a tolerance of 20% (in most cases):

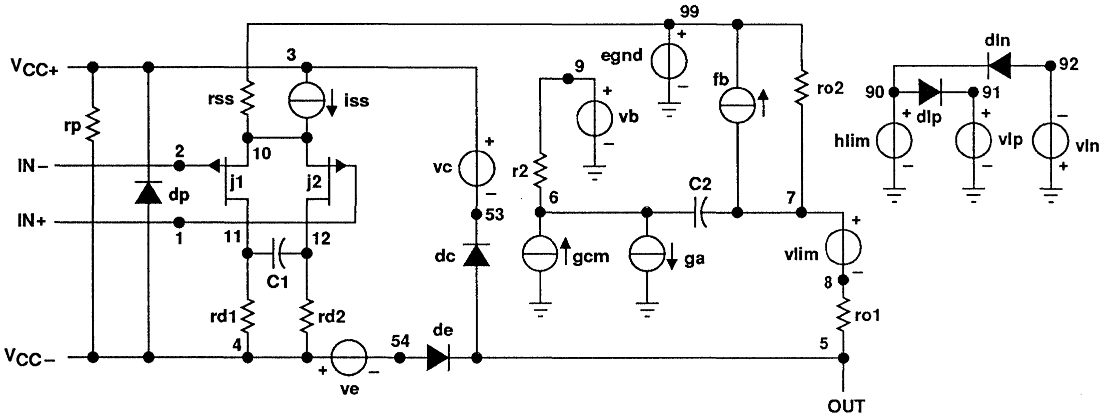
- Maximum positive output voltage swing
- Maximum negative output voltage swing
- Slew rate
- Quiescent power dissipation
- Input bias current
- Open-loop voltage amplification
- Unity gain frequency
- Common-mode rejection ratio
- Phase margin
- dc output resistance
- ac output resistance
- Short-circuit output current limit

NOTE 5: G. R. Boyle, B. M. Cohn, D. O. Pederson, and J. E. Solomon, "Macromodeling of Integrated Circuit Operational Amplifiers", IEEE Journal of Solid-State Circuits, SC-9, 353 (1974).

Parts is a trademark of MicroSim Corporation.
PSpice is a trademark of MicroSim Corporation.

APPLICATION INFORMATION

macromodel information (continued)



```
.subckt TLE2061  1 2 3 4 5
  c1    11 12 1.457E-12
  c2     6  7 15.00E-12
  dc     5 53 dx
  de    54  5 dx
  dlp   90 91 dx
  dln   92 90 dx
  dp     4  3 dx
  egnd 99   0 poly(2)  (3,0)  (4,0)  0 .5 .5
  fb     7 99 poly(5)  vb vc ve vlp vln 0 4.357E6 -4E6 4E6 4E6 -4E6
  ga     6  0 11 12 188.5E-6
  gcm    0  6 10 99 3.352E-9
  iss    3 10 dc 51.00E-6
  hlim 90   0 vlim 1K
  j1    11  2 10 jx
  j2    12  1 10 jx
  r2     6  9 100.0E3
  rd1    4 11 5.305E3
  rd2    4 12 5.305E3
  ro1    8  5 280
  ro2    7 99 280
  rp     3  4 113.2E3
  rss   10 99 3.922E6
  vb     9  0 dc 0
  vc     3 53 dc 2
  ve    54  4 dc 2
  vlim   7  8 dc 0
  vlp   91  0 dc 50
  vln    0 92 dc 50
.model dx D(Is=800.0E-18)
.model jx PJF(Is=2.000E-12 Beta=423E-6 Vto=-1)
.ends
```

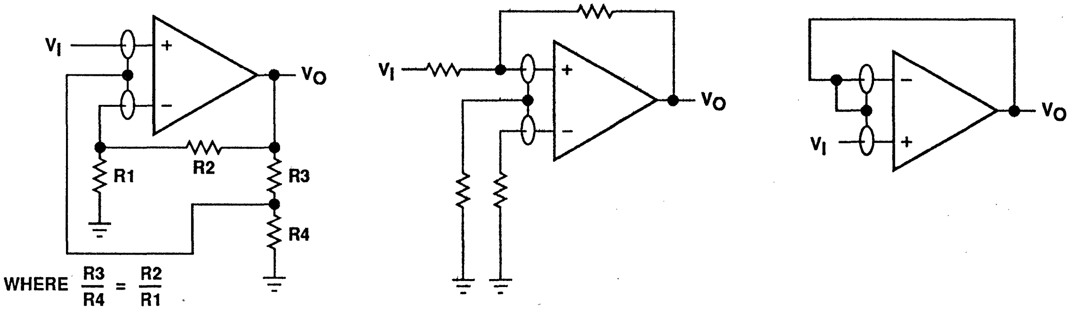
Figure 37. Boyle Macromodel and Subcircuit

APPLICATION INFORMATION

input characteristics

The TLE2061, TLE2061A, and TLE2061B are specified with a minimum and a maximum input voltage that, if exceeded at either input, could cause the device to malfunction.

Because of the extremely high input impedance and resulting low bias current requirements, the TLE2061, TLE2061A, and TLE2061B are well suited for low-level signal processing; however, leakage currents on printed circuit boards and sockets can easily exceed bias current requirements and cause degradation in system performance. It is a good practice to include guard rings around inputs (see Figure 38). These guards should be driven from a low-impedance source at the same voltage level as the common-mode input.



WHERE $\frac{R3}{R4} = \frac{R2}{R1}$

Figure 38. Use of Guard Rings

input offset voltage nulling

The TLE2061 series offers external null pins that can be used to further reduce the input offset voltage. The circuit of Figure 39 can be connected as shown if the feature is desired. If external nulling is not needed, the null pins may be left disconnected.

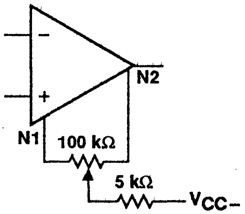


Figure 39. Input Offset Voltage Nulling

TLE2062, TLE2062A, TLE2062B, TLE2062Y
EXCALIBUR JFET-INPUT HIGH-OUTPUT-DRIVE µPOWER DUAL OPERATIONAL AMPLIFIERS

D3346, OCTOBER 1989 – REVISED NOVEMBER 1991

available features

- Excellent Output Drive Capability
  V_O = ± 2.5 V Min at R_L = 100 Ω,
  $V_{CC\pm}$ = ± 5 V
  V_O = ± 12.5 V Min at R_L = 600 Ω,
  $V_{CC\pm}$ = ± 15 V
- Low Supply Current . . . 280 µA Typ Per Amplifier
- High Unity-Gain Bandwidth . . . 2.1 MHz Typ
- High Slew Rate . . . 3.4 V/µs Typ
- Macromodels Included
- Wide Operating Supply Voltage Range
  $V_{CC\pm}$ = ± 3.5 V to ± 20 V
- High Open-Loop Gain . . . 280 V/mV Typ
- Low Offset Voltage . . . 1 mV Max
- Low Offset Voltage Drift With Time
  0.04 µV/mo Typ
- Low Input Bias Current . . . 5 pA Typ

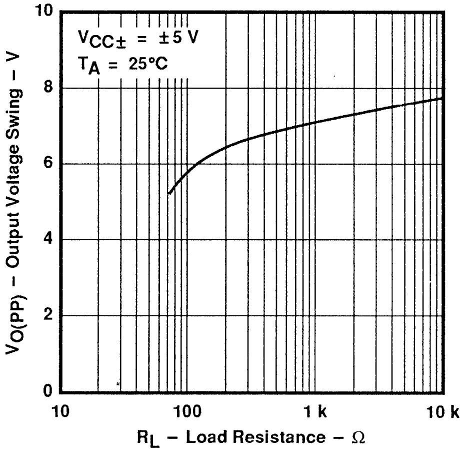
description

The TLE2062, TLE2062A, and TLE2062B are JFET-input, low-power, precision dual operational amplifiers manufactured using Texas Instruments Excalibur process. These devices combine outstanding output drive capability with low power consumption, excellent dc precision, and wide bandwidth.

In addition to maintaining the traditional JFET advantages of fast slew rates and low input bias and offset currents, the Excalibur process offers outstanding parametric stability over time and temperature. This results in a “precision” device remaining precise even with changes in temperature and over years of use.

The TLE2062, TLE2062A, and TLE2062B are ideal choices for any application requiring excellent dc precision, high output drive, wide bandwidth, and low power consumption.

MAXIMUM PEAK-TO-PEAK
OUTPUT VOLTAGE SWING
vs
LOAD RESISTANCE



AVAILABLE OPTIONS

T_A	V_{IO} max AT 25°C	PACKAGE SMALL OUTLINE (D)	CHIP CARRIER (FK)	CERAMIC DIP (JG)	PLASTIC DIP (P)	CHIP FORM (Y)
0°C	1 mV	——	——	——	——	TLE2062Y
to	2 mV	TLE2062ACD	——	——	TLE2062ACP	
70°C	4 mV	TLE2062CD	——	——	TLE2062CP	
– 40°C	1 mV	——	——	——	——	
to	2 mV	TLE2062AID	——	——	TLE2062AIP	
85°C	4 mV	TLE2062ID	——	——	TLE2062IP	
– 55°C	1 mV	——	——	——	——	
to	2 mV	TLE2062AMD	TLE2062AMFK	TLE2062AMJG	TLE2062AMP	
125°C	4 mV	TLE2062MD	TLE2062MFK	TLE2062MJG	TLE2062MP	

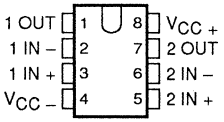
D packages are available taped and reeled. Add “R” suffix to device type (e.g., TLE2062ACDR). Chips are tested at 25°C.

description (continued)

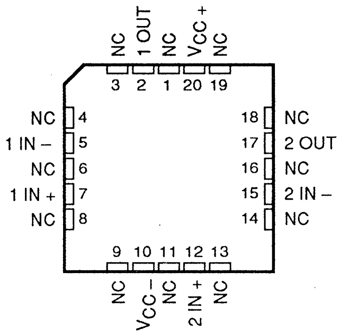
A variety of available package options includes small-outline and chip carrier versions for high-density system applications.

The C-suffix devices are characterized for operation from 0°C to 70°C. The I-suffix devices are characterized for operation from −40°C to 85°C. The M-suffix devices are characterized for operation over the full military temperature range of −55°C to 125°C.

D, JG, OR P PACKAGE
(TOP VIEW)



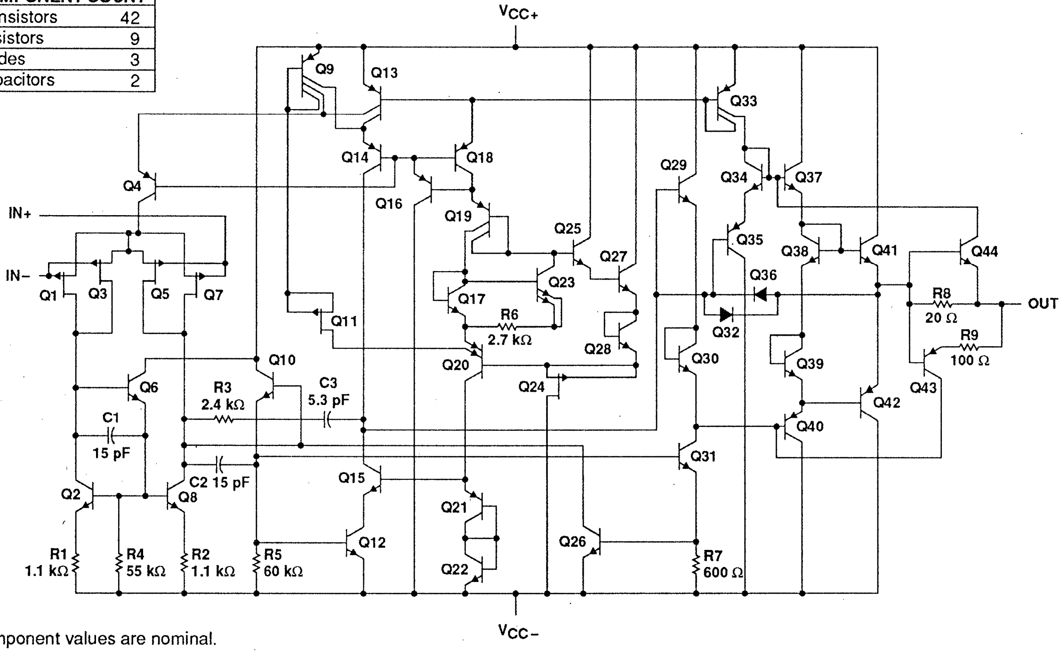
FK PACKAGE
(TOP VIEW)



NC – No internal connection

equivalent schematic (each channel)

ACTUAL DEVICE COMPONENT COUNT	
Transistors	42
Resistors	9
Diodes	3
Capacitors	2

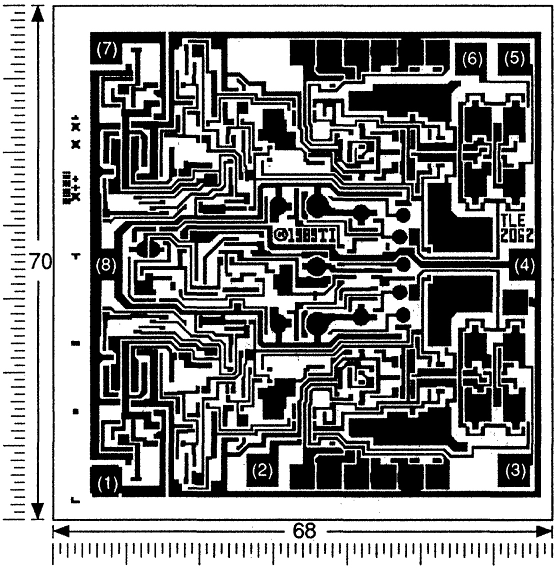


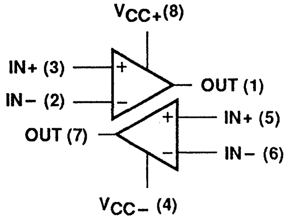
Component values are nominal.

chip information

These chips, properly assembled, display characteristics similar to the TLE2062. Thermal compression or ultrasonic bonding may be used on the doped aluminum bonding pads. Chips may be mounted with conductive epoxy or a gold-silicon preform.

BONDING PAD ASSIGNMENTS





CHIP THICKNESS:
15 TYPICAL

BONDING PADS:
4 X 4 MINIMUM

T_J max = 150°C

TOLERANCES
ARE ± 10%

ALL DIMENSIONS
ARE IN MILS

PIN (4) INTERNALLY
CONNECTED TO
BACKSIDE OF CHIP

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC+} (see Note 1)	22 V
Supply voltage, V_{CC-}	−22 V
Differential input voltage (see Note 2)	±44 V
Input voltage, V_I (any input)	$V_{CC\pm}$
Input current, I_I (each input)	±1 mA
Output current, I_O (each output)	±80 mA
Total current into V_{CC+} terminal	80 mA
Total current out of V_{CC-} terminal	80 mA
Duration of short-circuit current at (or below) 25°C (see Note 3)	unlimited
Continuous total dissipation	See Dissipation Rating Table
Operating free-air temperature range, T_A: C-suffix	0°C to 70°C
I-suffix	−40°C to 85°C
M-suffix	−55°C to 125°C
Storage temperature range	−65°C to 150°C
Case temperature for 60 seconds: FK package	260°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D or P package	260°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: JG package	300°C

NOTES: 1. All voltage values, except differential voltages, are with respect to the midpoint between V_{CC+} and V_{CC-}.
2. Differential voltages are at the noninverting input with respect to the inverting input.
3. The output may be shorted to either supply. Temperature and/or supply voltages must be limited to ensure that the maximum dissipation rating is not exceeded.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR ABOVE T_A = 25°C	T_A = 70°C POWER RATING	T_A = 85°C POWER RATING	T_A = 125°C POWER RATING
D	725 mW	5.8 mW/°C	464 mW	377 mW	145 mW
FK	1375 mW	11 mW/°C	880 mW	715 mW	275 mW
JG	1050 mW	8.4 mW/°C	672 mW	546 mW	210 mW
P	1000 mW	8 mW/°C	640 mW	520 mW	200 mW

recommended operating conditions

		C-SUFFIX		I-SUFFIX		M-SUFFIX		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
Supply voltage, $V_{CC\pm}$		± 3.5	± 20	± 3.5	± 20	± 3.5	± 20	V
Common-mode input voltage, V_{IC}	$V_{CC\pm}$ = ± 5 V	− 1.6	4	− 1.6	4	− 1.6	4	V
	$V_{CC\pm}$ = ± 15 V	− 11	13	− 11	13	− 11	13	
	$V_{CC\pm}$ = ± 20 V	− 15	16.5	− 15	16.5	− 15	16.5	
Operating free-air temperature, T_A		0	70	− 40	85	− 55	125	°C

electrical characteristics at specified free-air temperature, $V_{CC\pm}$ = ±5 V (unless otherwise noted)

			TEST CONDITIONS	T_A†	MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	TLE2062C	V_{IC} = 0, R_S = 50 Ω	25°C		1	5	mV
				Full range			5.9	
		TLE2062AC		25°C		0.9	4	
				Full range			4.9	
		TLE2062BC		25°C		0.7	3	
				Full range			3.9	
αV_{IO}	Temperature coefficient of input offset voltage			Full range		6		μV/°C
	Input offset voltage long-term drift (see Note 4)			25°C		0.04		μV/mo
I_{IO}	Input offset current			25°C		1		pA
				Full range			0.8	nA
I_{IB}	Input bias current			25°C		3		pA
				Full range			2	nA
V_{ICR}	Common-mode input voltage range			25°C	− 1.6 to 4	− 2 to 6		V
				Full range	− 1.6 to 4			V
V_{OM+}	Maximum positive peak output voltage swing		R_L = 10 kΩ	25°C	3.5	3.7		V
				Full range	3.3			
			R_L = 100 Ω	25°C	2.5	3.1		
				Full range	2			
V_{OM-}	Maximum negative peak output voltage swing		R_L = 10 kΩ	25°C	− 3.7	− 3.9		V
				Full range	− 3.3			
			R_L = 100 Ω	25°C	− 2.5	− 2.7		
				Full range	− 2			
A_{VD}	Large-signal differential voltage amplification		V_O = ± 2.8 V, R_L = 10 kΩ	25°C	15	80		V/mV
				Full range	2			
			V_O = 0 to 2 V, R_L = 100 Ω	25°C	0.75	45		
				Full range	0.5			
			V_O = 0 to − 2 V, R_L = 100 Ω	25°C	0.5	3		
				Full range	0.25			
r_i	Input resistance			25°C		10^{12}		Ω
c_i	Input capacitance			25°C		4		pF
z_o	Open-loop output impedance		I_O = 0	25°C		560		Ω
CMRR	Common-mode rejection ratio		R_S = 50 Ω, V_{IC} = V_{ICR} min	25°C	65	82		dB
				Full range	65			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm}/\Delta V_{IO}$)		$V_{CC\pm}$ = ±5 V to ± 20 V, R_S = 50 Ω	25°C	75	93		dB
				Full range	75			
I_{CC}	Supply current		V_O = 0, No load	25°C		560	620	μA
				Full range			635	
ΔI_{CC}	Supply current change over operating temperature range			Full range		26		μA

†Full range is 0°C to 70°C.

NOTE 4: Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at T_A = 150°C extrapolated to T_A = 25°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

operating characteristics at specified free-air temperature, $V_{CC\pm} = \pm 5$ V

PARAMETER		TEST CONDITIONS		T_A†	MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain (see Figure 1)	R_L = 10 kΩ,	C_L = 100 pF	25°C	2.2	3.4		V/μs
				Full range	2.1			
V_n	Equivalent input noise voltage (see Figure 2)	f = 10 Hz,	R_S = 100 Ω	25°C		59	100	nV/√Hz
		f = 1 kHz,	R_S = 100 Ω	25°C		43	60	
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 10 Hz		25°C		1.1		μV
I_n	Equivalent input noise current	f = 1 kHz		25°C		1		fA/√Hz
THD	Total harmonic distortion	A_{VD} = 2, $V_{O(PP)}$ = 2 V,	f = 10 kHz, R_L = 10 kΩ	25°C		0.025%		
B_1	Unity-gain bandwidth (see Figure 3)	R_L = 10 kΩ,	C_L = 100 pF	25°C		1.8		MHz
		R_L = 100 Ω,	C_L = 100 pF	25°C		1.3		
	Settling time	0.1%		25°C		5		μs
		0.01%		25°C		10		
B_{OM}	Maximum-output-swing bandwidth	A_{VD} = 1,	R_L = 10 kΩ	25°C		140		kHz
ϕ_m	Phase margin at unity gain (see Figure 3)	R_L = 10 kΩ,	C_L = 100 pF	25°C		58°		
		R_L = 100 Ω,	C_L = 100 pF	25°C		75°		

†Full range is 0°C to 70°C.

electrical characteristics at specified free-air temperature, $V_{CC\pm} = \pm 15$ V (unless otherwise noted)

			TEST CONDITIONS	T_A†	MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	TLE2062C	$V_{IC} = 0$, $R_S = 50\ \Omega$	25°C		0.9	4	mV
				Full range			4.9	
		TLE2062AC		25°C		0.8	2	
				Full range			2.9	
		TLE2062BC		25°C		0.5	1	
				Full range			1.9	
αV_{IO}	Temperature coefficient of input offset voltage			Full range		6		μV/°C
	Input offset voltage long-term drift (see Note 4)			25°C		0.04		μV/mo
I_{IO}	Input offset current			25°C		2		pA
				Full range			1	nA
I_{IB}	Input bias current			25°C		4		pA
				Full range			3	nA
V_{ICR}	Common-mode input voltage range			25°C	− 11 to 13	− 12 to 16		V
				Full range	− 11 to 13			V
V_{OM+}	Maximum positive peak output voltage swing		$R_L = 10\ k\Omega$	25°C	13.2	13.7		V
				Full range	13			
			$R_L = 600\ \Omega$	25°C	12.5	13.2		
				Full range	12			
V_{OM-}	Maximum negative peak output voltage swing		$R_L = 10\ k\Omega$	25°C	− 13.2	− 13.7		V
				Full range	− 13			
			$R_L = 600\ \Omega$	25°C	− 12.5	− 13		
				Full range	− 12			
A_{VD}	Large-signal differential voltage amplification		$V_O = \pm 10$ V, $R_L = 10\ k\Omega$	25°C	30	230		V/mV
				Full range	20			
			$V_O = 0$ to 8 V, $R_L = 600\ \Omega$	25°C	25	100		
				Full range	10			
			$V_O = 0$ to − 8 V, $R_L = 600\ \Omega$	25°C	3	25		
				Full range	1			
r_i	Input resistance			25°C		10^{12}		Ω
c_i	Input capacitance			25°C		4		pF
z_o	Open-loop output impedance		$I_O = 0$	25°C		560		Ω
CMRR	Common-mode rejection ratio		$R_S = 50\ \Omega$, $V_{IC} = V_{ICR}$ min	25°C	72	90		dB
				Full range	70			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm}/\Delta V_{IO}$)		$V_{CC\pm} = \pm 5$ V to ± 15 V, $R_S = 50\ \Omega$	25°C	75	93		dB
				Full range	75			
I_{CC}	Supply current		$V_O = 0$, No load	25°C		625	690	μA
				Full range			715	
ΔI_{CC}	Supply current change over operating temperature range			Full range		36		μA

†Full range is 0°C to 70°C.

NOTE 4: Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at $T_A = 150°C$ extrapolated to $T_A = 25°C$ using the Arrhenius equation and assuming an activation energy of 0.96 eV.

operating characteristics at specified free-air temperature, $V_{CC\pm} = \pm 15$ V

PARAMETER		TEST CONDITIONS	T_A†	MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain (see Figure 1)	R_L = 10 kΩ, C_L = 100 pF	25°C	2.6	3.4		V/µs
			Full range	2.5			
V_n	Equivalent input noise voltage (see Figure 2)	f = 10 Hz, R_S = 100 Ω	25°C		70	100	nV/√Hz
		f = 1 kHz, R_S = 100 Ω	25°C		40	60	
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 10 Hz	25°C		1.1		µV
I_n	Equivalent input noise current	f = 1 kHz	25°C		1.1		fA/√Hz
THD	Total harmonic distortion	A_{VD} = 2, f = 10 kHz, $V_{O(PP)}$ = 2 V, R_L = 10 kΩ	25°C		0.025%		
B_1	Unity-gain bandwidth (see Figure 3)	R_L = 10 kΩ, C_L = 100 pF	25°C		2		MHz
		R_L = 600 Ω, C_L = 100 pF	25°C		1.5		
	Settling time	0.1%	25°C		5		µs
		0.01%	25°C		10		
B_{OM}	Maximum-output-swing bandwidth	A_{VD} = 1, R_L = 10 kΩ	25°C		40		kHz
ϕ_m	Phase margin at unity gain (see Figure 3)	R_L = 10 kΩ, C_L = 100 pF	25°C		60°		
		R_L = 600 Ω, C_L = 100 pF	25°C		70°		

†Full range is 0°C to 70°C.

electrical characteristics at specified free-air temperature, $V_{CC\pm} = \pm 20$ V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A†	MIN	TYP	MAX	UNIT
V_{IO} Input offset voltage	TLE2062C	$V_{IC} = 0$, $R_S = 50\ \Omega$	25°C		0.9	4	mV
			Full range			4.9	
	TLE2062AC		25°C		0.8	2.6	
			Full range			3.5	
	TLE2062BC		25°C		0.5	1.7	
			Full range			2.6	
αV_{IO} Temperature coefficient of input offset voltage			Full range		6		µV/°C
Input offset voltage long-term drift (see Note 4)			25°C		0.04		µV/mo
I_{IO} Input offset current			25°C		3		pA
			Full range			1	nA
I_{IB} Input bias current			25°C		5		pA
			Full range			3	nA
V_{ICR} Common-mode input voltage range			25°C	− 15 to 16.5	− 17 to 21		V
			Full range	− 15 to 16.5			V
V_{OM+} Maximum positive peak output voltage swing		$R_L = 10\ k\Omega$	25°C	18.2	18.7		V
			Full range	18			
		$R_L = 600\ \Omega$	25°C	15	18.1		
			Full range	12			
V_{OM-} Maximum negative peak output voltage swing		$R_L = 10\ k\Omega$	25°C	− 18.2	− 18.7		V
			Full range	− 18			
		$R_L = 600\ \Omega$	25°C	− 15	− 18		
			Full range	− 12			
A_{VD} Large-signal differential voltage amplification		$V_O = \pm 15$ V, $R_L = 10\ k\Omega$	25°C	30	280		V/mV
			Full range	20			
		$V_O = 0$ to 10 V, $R_L = 600\ \Omega$	25°C	25	80		
			Full range	10			
		$V_O = 0$ to − 10 V, $R_L = 600\ \Omega$	25°C	3	20		
			Full range	1			
r_i Input resistance			25°C		10^{12}		Ω
c_i Input capacitance			25°C		4		pF
z_o Open-loop output impedance		$I_O = 0$	25°C		560		Ω
CMRR Common-mode rejection ratio		$R_S = 50\ \Omega$, $V_{IC} = V_{ICR}$ min	25°C	75	91		dB
			Full range	70			
k_{SVR} Supply-voltage rejection ratio ($\Delta V_{CC\pm}/\Delta V_{IO}$)		$V_{CC\pm} = \pm 5$ V to ± 20 V, $R_S = 50\ \Omega$	25°C	75	93		dB
			Full range	70			
I_{CC} Supply current		$V_O = 0$, No load	25°C		660	730	µA
			Full range			750	
ΔI_{CC} Supply current change over operating temperature range			Full range		41		µA

†Full range is 0°C to 70°C.

NOTE 4: Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at $T_A = 150°C$ extrapolated to $T_A = 25°C$ using the Arrhenius equation and assuming an activation energy of 0.96 eV.

operating characteristics at specified free-air temperature, $V_{CC\pm}$ = ±20 V

PARAMETER		TEST CONDITIONS		T_A†	MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain (see Figure 1)	R_L = 10 kΩ,	C_L = 100 pF	25°C	2.8	3.4		V/μs
				Full range	2.5			
V_n	Equivalent input noise voltage (see Figure 2)	f = 10 Hz,	R_S = 100 Ω	25°C		75	100	nV/√Hz
		f = 1 kHz,	R_S = 100 Ω	25°C		40	60	
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 10 Hz		25°C		1.1		μV
I_n	Equivalent input noise current	f = 1 kHz		25°C		1.3		fA/√Hz
THD	Total harmonic distortion	A_{VD} = 2, $V_{O(PP)}$ = 2 V,	f = 10 kHz, R_L = 10 kΩ	25°C		0.025%		
B_1	Unity-gain bandwidth (see Figure 3)	R_L = 10 kΩ,	C_L = 100 pF	25°C		2.1		MHz
		R_L = 600 Ω,	C_L = 100 pF	25°C		1.6		
	Settling time	0.1%		25°C		5		μs
		0.01%		25°C		10		
B_{OM}	Maximum-output-swing bandwidth	A_{VD} = 1,	R_L = 10 kΩ	25°C		28		kHz
ϕ_m	Phase margin at unity gain (see Figure 3)	R_L = 10 kΩ,	C_L = 100 pF	25°C		60°		
		R_L = 600 Ω,	C_L = 100 pF	25°C		70°		

†Full range is 0°C to 70°C.

electrical characteristics at specified free-air temperature, $V_{CC\pm} = \pm 5$ V (unless otherwise noted)

			TEST CONDITIONS	T_A†	MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	TLE2062I	$V_{IC} = 0$, $R_S = 50\ \Omega$	25°C		1	5	mV
				Full range			6.3	
		TLE2062AI		25°C		0.9	4	
				Full range			5.3	
		TLE2062BI		25°C		0.7	3	
				Full range			4.3	
αV_{IO}	Temperature coefficient of input offset voltage			Full range		6		µV/°C
	Input offset voltage long-term drift (see Note 4)			25°C		0.04		µV/mo
I_{IO}	Input offset current			25°C		1		pA
				Full range			2	nA
I_{IB}	Input bias current			25°C		3		pA
				Full range			4	nA
V_{ICR}	Common-mode input voltage range			25°C	−1.6 to 4	−2 to 6		V
				Full range	−1.6 to 4			V
V_{OM+}	Maximum positive peak output voltage swing		$R_L = 10\ k\Omega$	25°C	3.5	3.7		V
				Full range	3.1			
			$R_L = 100\ \Omega$	25°C	2.5	3.1		
				Full range	2			
V_{OM-}	Maximum negative peak output voltage swing		$R_L = 10\ k\Omega$	25°C	−3.7	−3.9		V
				Full range	−3.1			
			$R_L = 100\ \Omega$	25°C	−2.5	−2.7		
				Full range	−2			
A_{VD}	Large-signal differential voltage amplification		$V_O = \pm 2.8$ V, $R_L = 10\ k\Omega$	25°C	15	80		V/mV
				Full range	2			
			$V_O = 0$ to 2 V, $R_L = 100\ \Omega$	25°C	0.75	45		
				Full range	0.5			
			$V_O = 0$ to −2 V, $R_L = 100\ \Omega$	25°C	0.5	3		
				Full range	0.25			
r_i	Input resistance			25°C		10^{12}		Ω
c_i	Input capacitance			25°C		4		pF
z_o	Open-loop output impedance		$I_O = 0$	25°C		560		Ω
CMRR	Common-mode rejection ratio		$R_S = 50\ \Omega$, $V_{IC} = V_{ICR}$ min	25°C	65	82		dB
				Full range	65			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm}/\Delta V_{IO}$)		$V_{CC\pm} = \pm 5$ V to ± 20 V, $R_S = 50\ \Omega$	25°C	75	93		dB
				Full range	65			
I_{CC}	Supply current		$V_O = 0$, No load	25°C		560	620	µA
				Full range			640	
ΔI_{CC}	Supply current change over operating temperature range			Full range		54		µA

†Full range is − 40°C to 85°C.

NOTE 4: Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at $T_A = 150$°C extrapolated to $T_A = 25$°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

operating characteristics at specified free-air temperature, $V_{CC\pm} = \pm 5$ V

PARAMETER		TEST CONDITIONS	T_A†	MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain (see Figure 1)	R_L = 10 kΩ, C_L = 100 pF	25°C	2.2	3.4		V/µs
			Full range	1.7			
V_n	Equivalent input noise voltage (see Figure 2)	f = 10 Hz, R_S = 100 Ω	25°C		59	100	nV/√Hz
		f = 1 kHz, R_S = 100 Ω	25°C		43	60	
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 10 Hz	25°C		1.1		µV
I_n	Equivalent input noise current	f = 1 kHz	25°C		1		fA/√Hz
THD	Total harmonic distortion	A_{VD} = 2, f = 10 kHz, $V_{O(PP)}$ = 2 V, R_L = 10 kΩ	25°C		0.025%		
B_1	Unity-gain bandwidth (see Figure 3)	R_L = 10 kΩ, C_L = 100 pF	25°C		1.8		MHz
		R_L = 100 Ω, C_L = 100 pF	25°C		1.3		
	Settling time	0.1%	25°C		5		µs
		0.01%	25°C		10		
B_{OM}	Maximum-output-swing bandwidth	A_{VD} = 1, R_L = 10 kΩ	25°C		140		kHz
ϕ_m	Phase margin at unity gain (see Figure 3)	R_L = 10 kΩ, C_L = 100 pF	25°C		58°		
		R_L = 100 Ω, C_L = 100 pF	25°C		75°		

† Full range is – 40°C to 85°C.

electrical characteristics at specified free-air temperature, $V_{CC\pm}$ = ±15 V (unless otherwise noted)

			TEST CONDITIONS	T_A†	MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	TLE2062I	V_{IC} = 0, R_S = 50 Ω	25°C		0.9	4	mV
				Full range			5.3	
		TLE2062AI		25°C		0.8	2	
				Full range			3.3	
		TLE2062BI		25°C		0.5	1	
				Full range			2.3	
αV_{IO}	Temperature coefficient of input offset voltage			Full range		6		µV/°C
	Input offset voltage long-term drift (see Note 4)			25°C		0.04		µV/mo
I_{IO}	Input offset current			25°C		2		pA
				Full range			3	nA
I_{IB}	Input bias current			25°C		4		pA
				Full range			5	nA
V_{ICR}	Common-mode input voltage range			25°C	− 11 to 13	− 12 to 16		V
				Full range	− 11 to 13			V
V_{OM+}	Maximum positive peak output voltage swing		R_L = 10 kΩ	25°C	13.2	13.7		V
				Full range	13			
			R_L = 600 Ω	25°C	12.5	13.2		
				Full range	12			
V_{OM-}	Maximum negative peak output voltage swing		R_L = 10 kΩ	25°C	− 13.2	− 13.7		V
				Full range	− 13			
			R_L = 600 Ω	25°C	− 12.5	− 13		
				Full range	− 12			
A_{VD}	Large-signal differential voltage amplification		V_O = ± 10 V, R_L = 10 kΩ	25°C	30	230		V/mV
				Full range	20			
			V_O = 0 to 8 V, R_L = 600 Ω	25°C	25	100		
				Full range	10			
			V_O = 0 to − 8 V, R_L = 600 Ω	25°C	3	25		
				Full range	1			
r_i	Input resistance			25°C		10^{12}		Ω
c_i	Input capacitance			25°C		4		pF
z_o	Open-loop output impedance		I_O = 0	25°C		560		Ω
CMRR	Common-mode rejection ratio		R_S = 50 Ω, V_{IC} = V_{ICR} min	25°C	72	90		dB
				Full range	65			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm}/\Delta V_{IO}$)		$V_{CC\pm}$ = ±5 V to ± 15 V, R_S = 50 Ω	25°C	75	93		dB
				Full range	65			
I_{CC}	Supply current		V_O = 0, No load	25°C		625	690	µA
				Full range			720	
ΔI_{CC}	Supply current change over operating temperature range			Full range		74		µA

†Full range is − 40°C to 85°C.

NOTE 4: Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at T_A = 150°C extrapolated to T_A = 25°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

operating characteristics at specified free-air temperature, $V_{CC\pm}$ = ±15 V

PARAMETER		TEST CONDITIONS		T_A†	MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain (see Figure 1)	R_L = 10 kΩ,	C_L = 100 pF	25°C	2.6	3.4		V/μs
				Full range	2.1			
V_n	Equivalent input noise voltage (see Figure 2)	f = 10 Hz,	R_S = 100 Ω	25°C		70	100	nV/√Hz
		f = 1 kHz,	R_S = 100 Ω	25°C		40	60	
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 10 Hz		25°C		1.1		μV
I_n	Equivalent input noise current	f = 1 kHz		25°C		1.1		fA/√Hz
THD	Total harmonic distortion	A_{VD} = 2, $V_{O(PP)}$ = 2 V,	f = 10 kHz, R_L = 10 kΩ	25°C		0.025%		
B_1	Unity-gain bandwidth (see Figure 3)	R_L = 10 kΩ,	C_L = 100 pF	25°C		2		MHz
		R_L = 600 Ω,	C_L = 100 pF	25°C		1.5		
	Settling time	0.1%		25°C		5		μs
		0.01%		25°C		10		
B_{OM}	Maximum-output-swing bandwidth	A_{VD} = 1,	R_L = 10 kΩ	25°C		40		kHz
ϕ_m	Phase margin at unity gain (see Figure 3)	R_L = 10 kΩ,	C_L = 100 pF	25°C		60°		
		R_L = 600 Ω,	C_L = 100 pF	25°C		70°		

† Full range is – 40°C to 85°C.

electrical characteristics at specified free-air temperature, $V_{CC\pm}$ = ±20 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A†	MIN	TYP	MAX	UNIT
V_{IO} Input offset voltage	TLE2062I	V_{IC} = 0, R_S = 50 Ω	25°C		0.9	4	mV
			Full range			5.3	
	TLE2062AI		25°C		0.8	2.6	
			Full range			3.9	
	TLE2062BI		25°C		0.5	1.7	
			Full range			3	
αV_{IO} Temperature coefficient of input offset voltage			Full range		6		µV/°C
Input offset voltage long-term drift (see Note 4)			25°C		0.04		µV/mo
I_{IO} Input offset current			25°C		3		pA
			Full range			3	nA
I_{IB} Input bias current			25°C		5		pA
			Full range			5	nA
V_{ICR} Common-mode input voltage range			25°C	−15 to 16.5	−17 to 21		V
			Full range	−15 to 16.5			V
V_{OM+} Maximum positive peak output voltage swing		R_L = 10 kΩ	25°C	18.2	18.7		V
			Full range	18			
		R_L = 600 Ω	25°C	15	18.1		
			Full range	12			
V_{OM-} Maximum negative peak output voltage swing		R_L = 10 kΩ	25°C	−18.2	−18.7		V
			Full range	−18			
		R_L = 600 Ω	25°C	−15	−18		
			Full range	−12			
A_{VD} Large-signal differential voltage amplification		V_O = ±15 V, R_L = 10 kΩ	25°C	30	280		V/mV
			Full range	20			
		V_O = 0 to 10 V, R_L = 600 Ω	25°C	25	80		
			Full range	10			
		V_O = 0 to −10 V, R_L = 600 Ω	25°C	3	20		
			Full range	1			
r_i Input resistance			25°C		10^{12}		Ω
c_i Input capacitance			25°C		4		pF
z_o Open-loop output impedance		I_O = 0	25°C		560		Ω
CMRR Common-mode rejection ratio		R_S = 50 Ω, V_{IC} = V_{ICR} min	25°C	75	91		dB
			Full range	65			
k_{SVR} Supply-voltage rejection ratio ($\Delta V_{CC\pm}/\Delta V_{IO}$)		$V_{CC\pm}$ = ±5 V to ±20 V, R_S = 50 Ω	25°C	75	93		dB
			Full range	65			
I_{CC} Supply current		V_O = 0, No load	25°C		660	730	µA
			Full range			755	
ΔI_{CC} Supply current change over operating temperature range			Full range		82		µA

† Full range is − 40°C to 85°C.

NOTE 4: Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at T_A = 150°C extrapolated to T_A = 25°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

operating characteristics at specified free-air temperature, $V_{CC\pm} = \pm 20$ V

PARAMETER		TEST CONDITIONS		T_A†	MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain (see Figure 1)	R_L = 10 kΩ,	C_L = 100 pF	25°C	2.8	3.4		V/μs
				Full range	2.1			
V_n	Equivalent input noise voltage (see Figure 2)	f = 10 Hz,	R_S = 100 Ω	25°C		75	100	nV/√Hz
		f = 1 kHz,	R_S = 100 Ω	25°C		40	60	
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 10 Hz		25°C		1.1		μV
I_n	Equivalent input noise current	f = 1 kHz		25°C		1.3		fA/√Hz
THD	Total harmonic distortion	A_{VD} = 2, $V_{O(PP)}$ = 2 V,	f = 10 kHz, R_L = 10 kΩ	25°C		0.025%		
B_1	Unity-gain bandwidth (see Figure 3)	R_L = 10 kΩ,	C_L = 100 pF	25°C		2.1		MHz
		R_L = 600 Ω,	C_L = 100 pF	25°C		1.6		
	Settling time	0.1%		25°C		5		μs
		0.01%		25°C		10		
B_{OM}	Maximum-output-swing bandwidth	A_{VD} = 1,	R_L = 10 kΩ	25°C		28		kHz
ϕ_m	Phase margin at unity gain (see Figure 3)	R_L = 10 kΩ,	C_L = 100 pF	25°C		60°		
		R_L = 600 Ω,	C_L = 100 pF	25°C		70°		

† Full range is – 40°C to 85°C.

electrical characteristics at specified free-air temperature, $V_{CC\pm}$ = ±5 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS	T_A†	MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	TLE2062M	V_{IC} = 0, R_S = 50 Ω	25°C		1	5	mV
				Full range			7	
		TLE2062AM		25°C		0.9	4	
				Full range			6	
		TLE2062BM		25°C		0.7	3	
				Full range			5	
α_{VIO}	Temperature coefficent of input offset voltage			Full range		6		µV/°C
	Input offset voltage long-term drift (see Note 4)			25°C		0.04		µV/mo
I_{IO}	Input offset current			25°C		1		pA
				Full range			15	nA
I_{IB}	Input bias current			25°C		3		pA
				Full range			30	nA
V_{ICR}	Common-mode input voltage range			25°C	− 1.6 to 4	− 2 to 6		V
				Full range	− 1.6 to 4			V
V_{OM+}	Maximum positive peak output voltage swing		R_L = 10 kΩ	25°C	3.5	3.7		V
				Full range	3			
		FK, and JG packages	R_L = 600 Ω	25°C	2.5	3.6		
				Full range	2			
		D and P packages	R_L = 100 Ω	25°C	2.5	3.1		
				Full range	2			
V_{OM-}	Maximum negative peak output voltage swing		R_L = 10 kΩ	25°C	− 3.5	− 3.9		V
				Full range	− 3			
		FK, and JG packages	R_L = 600 Ω	25°C	− 2.5	− 3.5		
				Full range	− 2			
		D and P packages	R_L = 100 Ω	25°C	− 2.5	− 2.7		
				Full range	− 2			
A_{VD}	Large-signal differential voltage amplification		V_O = ± 2.8 V, R_L = 10 kΩ	25°C	15	80		V/mV
				Full range	2			
		FK, and JG packages	V_O = 0 to 2.5 V, R_L = 600 Ω	25°C	1	65		
				Full range	0.5			
			V_O = 0 to − 2.5 V, R_L = 600 Ω	25°C	1	16		
				Full range	0.5			
		D and P packages	V_O = 0 to 2 V, R_L = 100 Ω	25°C	0.75	45		
				Full range	0.5			
			V_O = 0 to − 2 V, R_L = 100 Ω	25°C	0.5	3		
				Full range	0.25			

†Full range is – 55°C to 125°C.

NOTE 4: Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at T_A = 150°C extrapolated to T_A = 25°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

electrical characteristics at specified free-air temperature, $V_{CC\pm} = \pm 5$ V (unless otherwise noted) (continued)

PARAMETER		TEST CONDITIONS	T_A†	MIN	TYP	MAX	UNIT
r_i	Input resistance		25°C		10^{12}		Ω
c_i	Input capacitance		25°C		4		pF
z_o	Open-loop output impedance	$I_O = 0$	25°C		560		Ω
CMRR	Common-mode rejection ratio	$R_S = 50\ \Omega$, $V_{IC} = V_{ICR}$ min	25°C	65	82		dB
			Full range	60			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm} / \Delta V_{IO}$)	$V_{CC\pm} = \pm 5$ V to ± 20 V, $R_S = 50\ \Omega$	25°C	75	93		dB
			Full range	65			
I_{CC}	Supply current (two amplifiers)	$V_O = 0$, No load	25°C		560	620	µA
			Full range			650	
ΔI_{CC}	Supply current change over operating temperature range (two amplifiers)		Full range		72		µA

operating characteristics at specified free-air temperature, $V_{CC\pm} = \pm 5$ V

PARAMETER		TEST CONDITIONS		T_A†	MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain (see Figure 1)	$R_L = 10\ k\Omega$,	$C_L = 100$ pF	25°C		3.4		V/µs
				Full range				
V_n	Equivalent input noise voltage (see Figure 2)	f = 10 Hz,	$R_S = 100\ \Omega$	25°C		59		nV/√Hz
		f = 1 kHz,	$R_S = 100\ \Omega$	25°C		43		
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 10 Hz		25°C		1.1		µV
I_n	Equivalent input noise current	f = 1 kHz		25°C		1		fA/√Hz
THD	Total harmonic distortion	$A_{VD} = 2$, $V_{O(PP)} = 2$ V,	f = 10 kHz, $R_L = 10\ k\Omega$	25°C		0.025%		
B_1	Unity-gain bandwidth (see Figure 3)	$R_L = 10\ k\Omega$,	$C_L = 100$ pF	25°C		1.8		MHz
		$R_L = 600\ \Omega$,	$C_L = 100$ pF	25°C		1.3		
	Settling time	0.1%		25°C		5		µs
		0.01%		25°C		10		
B_{OM}	Maximum-output-swing bandwidth	$A_{VD} = 1$,	$R_L = 10\ k\Omega$	25°C		140		kHz
ϕ_m	Phase margin at unity gain (see Figure 3)	$R_L = 10\ k\Omega$,	$C_L = 100$ pF	25°C		58°		
		$R_L = 600\ \Omega$,	$C_L = 100$ pF	25°C		75°		

†Full range is – 55°C to 125°C.

electrical characteristics at specified free-air temperature, $V_{CC\pm} = \pm 15$ V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A†	MIN	TYP	MAX	UNIT
V_{IO} Input offset voltage	TLE2062M	$V_{IC} = 0$, $R_S = 50\ \Omega$	25°C		0.9	4	mV
			Full range			6	
	TLE2062AM		25°C		0.8	2	
			Full range			4	
	TLE2062BM		25°C		0.5	1	
			Full range			3	
αV_{IO} Temperature coefficient of input offset voltage			Full range		6		μV/°C
Input offset voltage long-term drift (see Note 4)			25°C		0.04		μV/mo
I_{IO} Input offset current			25°C		2		pA
			Full range			20	nA
I_{IB} Input bias current			25°C		4		pA
			Full range			40	nA
V_{ICR} Common-mode input voltage range			25°C	− 11 to 13	− 12 to 16		V
			Full range	− 11 to 13			V
V_{OM+} Maximum positive peak output voltage swing		$R_L = 10\ k\Omega$	25°C	13	13.7		V
			Full range	12.5			
		$R_L = 600\ \Omega$	25°C	12.5	13.2		
			Full range	11			
V_{OM-} Maximum negative peak output voltage swing		$R_L = 10\ k\Omega$	25°C	− 13	− 13.7		V
			Full range	− 12.5			
		$R_L = 600\ \Omega$	25°C	− 12.5	− 13		
			Full range	− 11			
A_{VD} Large-signal differential voltage amplification		$V_O = \pm 10$ V, $R_L = 10\ k\Omega$	25°C	30	230		V/mV
			Full range	20			
		$V_O = 0$ to 8 V, $R_L = 600\ \Omega$	25°C	25	100		
			Full range	7			
		$V_O = 0$ to − 8 V, $R_L = 600\ \Omega$	25°C	3	25		
			Full range	1			
r_i Input resistance			25°C		10^{12}		Ω
c_i Input capacitance			25°C		4		pF
z_o Open-loop output impedance		$I_O = 0$	25°C		560		Ω
CMRR Common-mode rejection ratio		$R_S = 50\ \Omega$, $V_{IC} = V_{ICR}$ min	25°C	72	90		dB
			Full range	65			
k_{SVR} Supply-voltage rejection ratio ($\Delta V_{CC\pm}/\Delta V_{IO}$)		$V_{CC\pm} = \pm 5$ V to ± 15 V, $R_S = 50\ \Omega$	25°C	75	93		dB
			Full range	65			
I_{CC} Supply current		$V_O = 0$, No load	25°C		625	690	μA
			Full range			730	
ΔI_{CC} Supply current change over operating temperature range			Full range		97		μA

† Full range is − 55°C to 125°C.

NOTE 4: Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at $T_A = 150°C$ extrapolated to $T_A = 25°C$ using the Arrhenius equation and assuming an activation energy of 0.96 eV.

operating characteristics at specified free-air temperature, $V_{CC\pm}$ = ±15 V

PARAMETER		TEST CONDITIONS		T_A†	MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain (see Figure 1)	R_L = 10 kΩ,	C_L = 100 pF	25°C	2	3.4		V/μs
				Full range	1.8			
V_n	Equivalent input noise voltage (see Figure 2)	f = 10 Hz,	R_S = 100 Ω	25°C		70		nV/√Hz
		f = 1 kHz,	R_S = 100 Ω	25°C		40		
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 10 Hz		25°C		1.1		μV
I_n	Equivalent input noise current	f = 1 kHz		25°C		1.1		fA/√Hz
THD	Total harmonic distortion	A_{VD} = 2, $V_{O(PP)}$ = 2 V,	f = 10 kHz, R_L = 10 kΩ	25°C		0.025%		
B_1	Unity-gain bandwidth (see Figure 3)	R_L = 10 kΩ,	C_L = 100 pF	25°C		2		MHz
		R_L = 600 Ω,	C_L = 100 pF	25°C		1.5		
	Settling time	0.1%		25°C		5		μs
		0.01%		25°C		10		
B_{OM}	Maximum-output-swing bandwidth	A_{VD} = 1,	R_L = 10 kΩ	25°C		40		kHz
ϕ_m	Phase margin at unity gain (see Figure 3)	R_L = 10 kΩ,	C_L = 100 pF	25°C		60°		
		R_L = 600 Ω,	C_L = 100 pF	25°C		70°		

†Full range is – 55°C to 125°C.

electrical characteristics at specified free-air temperature, $V_{CC\pm}$ = ±20 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS	T_A†	MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	TLE2062M	V_{IC} = 0, R_S = 50 Ω	25°C		0.9	4	mV
				Full range			6	
		TLE2062AM		25°C		0.8	2.6	
				Full range			4.6	
		TLE2062BM		25°C		0.5	1.7	
				Full range			3.7	
αV_{IO}	Temperature coefficient of input offset voltage			Full range		6		μV/°C
	Input offset voltage long-term drift (see Note 4)			25°C		0.04		μV/mo
I_{IO}	Input offset current			25°C		3		pA
				Full range			20	nA
I_{IB}	Input bias current			25°C		5		pA
				Full range			40	nA
V_{ICR}	Common-mode input voltage range			25°C	− 15 to 16.5	− 17 to 21		V
				Full range	− 15 to 16.5			V
V_{OM+}	Maximum positive peak output voltage swing		R_L = 10 kΩ	25°C	18	18.7		V
				Full range	17.5			
			R_L = 600 Ω	25°C	15	18.1		
				Full range	12			
V_{OM-}	Maximum negative peak output voltage swing		R_L = 10 kΩ	25°C	− 18	− 18.7		V
				Full range	− 17.5			
			R_L = 600 Ω	25°C	− 15	− 18		
				Full range	− 12			
A_{VD}	Large-signal differential voltage amplification		V_O = ± 15 V, R_L = 10 kΩ	25°C	30	280		V/mV
				Full range	20			
			V_O = 0 to 10 V, R_L = 600 Ω	25°C	25	80		
				Full range	10			
			V_O = 0 to − 10 V, R_L = 600 Ω	25°C	3	20		
				Full range	1			
r_i	Input resistance			25°C		10^{12}		Ω
c_i	Input capacitance			25°C		4		pF
z_o	Open-loop output impedance		I_O = 0	25°C		560		Ω
CMRR	Common-mode rejection ratio		R_S = 50 Ω, V_{IC} = V_{ICR} min	25°C	75	91		dB
				Full range	65			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm}/\Delta V_{IO}$)		$V_{CC\pm}$ = ±5 V to ± 20 V, R_S = 50 Ω	25°C	75	93		dB
				Full range	65			
I_{CC}	Supply current		V_O = 0, No load	25°C		660	730	μA
				Full range			770	
ΔI_{CC}	Supply current change over operating temperature range			Full range		106		μA

† Full range is − 55°C to 125°C.

NOTE 4: Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at T_A = 150°C extrapolated to T_A = 25°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

operating characteristics at specified free-air temperature, $V_{CC\pm} = \pm 20$ V

PARAMETER		TEST CONDITIONS		T_A†	MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain (see Figure 1)	R_L = 10 kΩ,	C_L = 100 pF	25°C		3.4		V/μs
				Full range				
V_n	Equivalent input noise voltage (see Figure 2)	f = 10 Hz,	R_S = 100 Ω	25°C		75		nV/√Hz
		f = 1 kHz,	R_S = 100 Ω	25°C		40		
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 10 Hz		25°C		1.1		μV
I_n	Equivalent input noise current	f = 1 kHz		25°C		1.3		fA/√Hz
THD	Total harmonic distortion	A_{VD} = 2, $V_{O(PP)}$ = 2 V,	f = 10 kHz, R_L = 10 kΩ	25°C		0.025%		
B_1	Unity-gain bandwidth (see Figure 3)	R_L = 10 kΩ,	C_L = 100 pF	25°C		2.1		MHz
		R_L = 600 Ω,	C_L = 100 pF	25°C		1.6		
	Settling time	0.1%		25°C		5		μs
		0.01%		25°C		10		
B_{OM}	Maximum-output-swing bandwidth	A_{VD} = 1,	R_L = 10 kΩ	25°C		28		kHz
ϕ_m	Phase margin at unity gain (see Figure 3)	R_L = 10 kΩ,	C_L = 100 pF	25°C		60°		
		R_L = 600 Ω,	C_L = 100 pF	25°C		70°		

†Full range is – 55°C to 125°C.

electrical characteristics at $V_{CC\pm}$ = ±15 V, T_A = 25°C (unless otherwise noted)

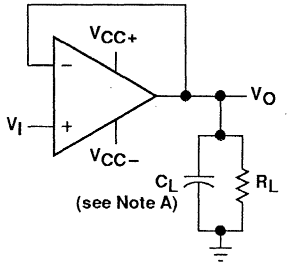
PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	V_{IC} = 0,	R_S = 50 Ω		0.9	4	mV
αV_{io}	Input offset voltage long-term drift (see Note 4)				0.04		µV/mo
I_{IO}	Input offset current				2		pA
I_{IB}	Input bias current				4		pA
V_{ICR}	Common-mode input voltage range			−11 to 13	−12 to 16		V
V_{OM+}	Maximum positive peak output voltage swing	R_L = 10 kΩ		13.2	13.7		V
		R_L = 600 Ω		12.5	13.2		
V_{OM-}	Maximum negative peak output voltage swing	R_L = 10 kΩ		−13.2	−13.7		V
		R_L = 600 Ω		−12.5	−13		
A_{VD}	Large-signal differential voltage amplification	V_O = ±10 V,	R_L = 10 kΩ	30	230		V/mV
		V_O = 0 to 8 V,	R_L = 600 Ω	25	100		
		V_O = 0 to −8 V,	R_L = 600 Ω	3	25		
r_i	Input resistance				10^{12}		Ω
c_i	Input capacitance				4		pF
z_o	Open-loop ouput impedance	I_O = 0			560		Ω
CMRR	Common-mode rejection ratio	R_S = 50 Ω,	$V_{IC} = V_{ICR}\min$	72	90		dB
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC}/\Delta V_{IO}$)	$V_{CC\pm}$ = ±5 V to ±15 V, R_S = 50 Ω		75	93		dB
I_{CC}	Supply current	V_O = 0,	No load		625	690	µA

NOTE 4: Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at T_A = 150°C extrapolated to T_A = 25°C using the Arrhenius equation and assuming and activation energy of 0.96 eV.

operating characteristics at $V_{CC\pm}$ = ±15 V, T_A = 25°C

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain	R_L = 10 kΩ,	C_L = 100 pF	2.6	3.4		V/µs
V_n	Equivalent input noise voltage (see Figure 2)	f = 10 Hz,	R_S = 100 Ω		70		nV/√Hz
		f = 1 kHz,	R_S = 100 Ω		40		
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 10 Hz			1.1		µV
I_n	Equivalent input noise current	f = 1 Hz			1.1		fA/√Hz
THD	Total harmonic distortion	A_{VD} = 2, $V_{O(PP)}$ = 2 V,	f = 10 kHz, R_L = 10 kΩ		0.025%		
B_1	Unity gain-bandwidth (see Figure 3)	R_L = 10 kΩ,	C_L = 100 pF		2		MHz
		R_L = 600 Ω,	C_L = 100 pF		1.5		
	Settling time	0.1%			5		µs
		0.01%			10		
B_{OM}	Maximum-output-swing bandwidth	A_{VD} = 1,	R_L = 10 kΩ		40		kHz
ϕ_m	Phase margin at unity gain (see Figure 3)	R_L = 10 kΩ,	C_L = 100 pF		60°		
		R_L = 600 Ω,	C_L = 100 pF		70°		

PARAMETER MEASUREMENT INFORMATION



NOTE A: C_L includes fixture capacitance.

Figure 1. Slew Rate Test Circuit

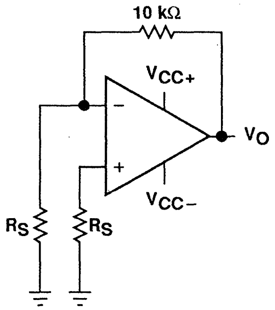
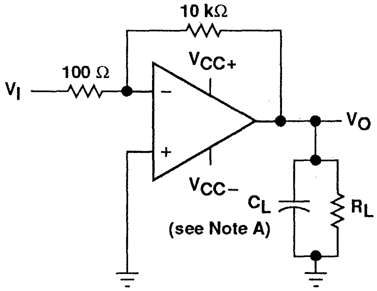


Figure 2. Noise Voltage Test Circuit



NOTE A: C_L includes fixture capacitance.

Figure 3. Unity-Gain Bandwidth and Phase Margin Test Circuit

typical values

Typical values as presented in this data sheet represent the median (50% point) of device parametric performance.

input bias and offset current

At the picoamp bias current level typical of the TLE2062, TLE2062A, and TLE2062B, accurate measurement of the bias current becomes difficult. Not only does this measurement require a picoammeter, but test socket leakages can easily exceed the actual device bias currents. To accurately measure these small currents, Texas Instruments uses a two-step process. The socket leakage is measured using picoammeters with bias voltages applied but with no device in the socket. The device is then inserted into the socket and a second test that measures both the socket leakage and the device input bias current is performed. The two measurements are then subtracted algebraically to determine the bias current of the device.

TYPICAL CHARACTERISTICS

table of graphs

			FIGURE
V_{IO}	Input offset voltage	Distribution	4
I_{IB}	Input bias current	vs Common-mode voltage	5
		vs Temperature	6
I_{IO}	Input offset current	vs Temperature	6
V_{ICR}	Common-mode input voltage range	vs Temperature	7
V_{OM}	Maximum peak output voltage swing	vs Output current	8, 9
		vs Supply voltage	10, 11, 12
$V_{O(PP)}$	Maximum peak-to-peak output voltage	vs Frequency	13, 14, 15
A_{VD}	Differential voltage amplification	vs Frequency	16
		vs Temperature	17
I_{OS}	Short-circuit output current	vs Time	18
		vs Temperature	19
z_o	Output impedance	vs Frequency	20
CMRR	Common-mode rejection ratio	vs Frequency	21
I_{CC}	Supply current	vs Supply voltage	22
		vs Temperature	23
	Pulse response	Small-signal	24, 25
		Large-signal	26, 27
	Noise voltage (referred to input)	0.1 to 10 Hz	28
V_n	Equivalent input noise voltage	vs Frequency	29
THD	Total harmonic distortion	vs Frequency	30, 31
B_1	Unity-gain bandwidth	vs Supply voltage	32
		vs Temperature	33
ϕ_m	Phase margin	vs Supply voltage	34
		vs Load capacitance	35
		vs Temperature	36
	Phase shift	vs Frequency	16

TYPICAL CHARACTERISTICS†

TLE2062
DISTRIBUTION OF
INPUT OFFSET VOLTAGE

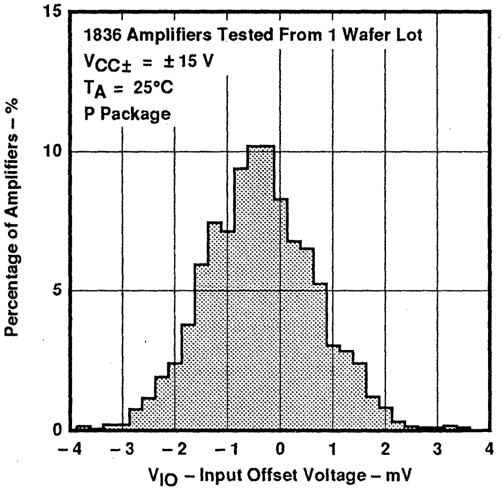


Figure 4

INPUT BIAS CURRENT
vs
COMMON-MODE INPUT VOLTAGE

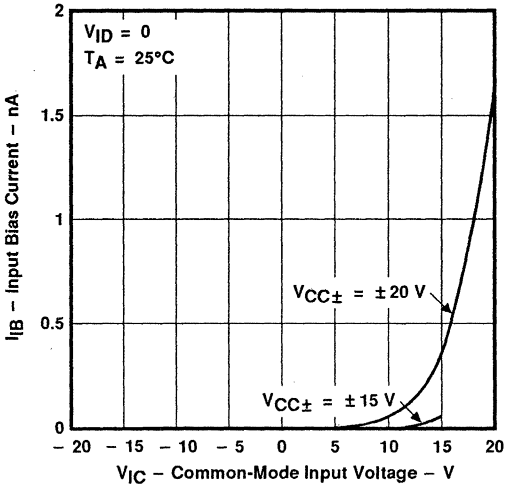


Figure 5

INPUT BIAS CURRENT
and INPUT OFFSET CURRENT
vs
FREE-AIR TEMPERATURE

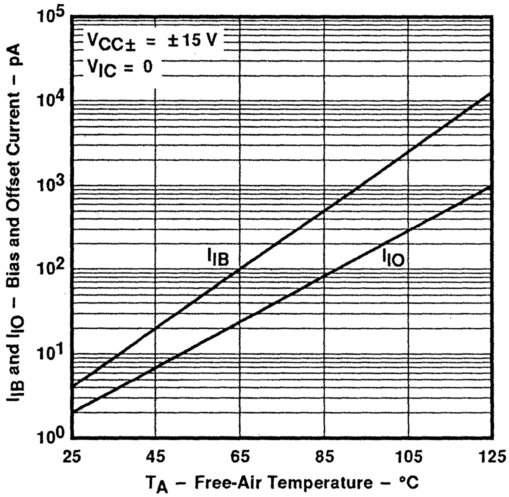


Figure 6

COMMON-MODE INPUT VOLTAGE RANGE
vs
FREE-AIR TEMPERATURE

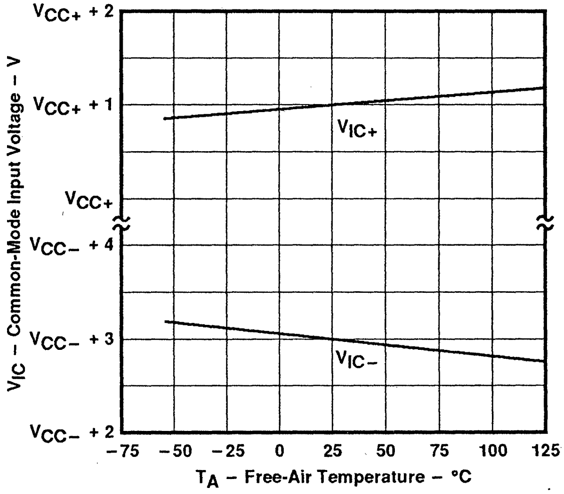


Figure 7

---

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS

MAXIMUM POSITIVE PEAK OUTPUT VOLTAGE vs OUTPUT CURRENT

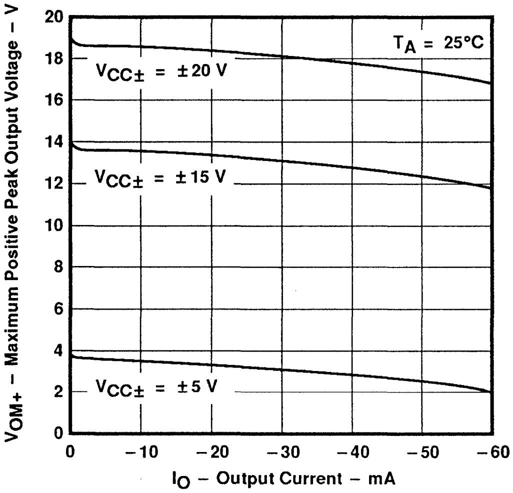


Figure 8

MAXIMUM NEGATIVE PEAK OUTPUT VOLTAGE vs OUTPUT CURRENT

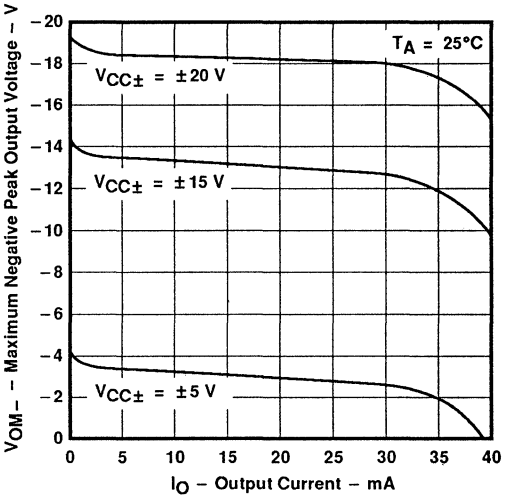


Figure 9

MAXIMUM PEAK OUTPUT VOLTAGE vs SUPPLY VOLTAGE

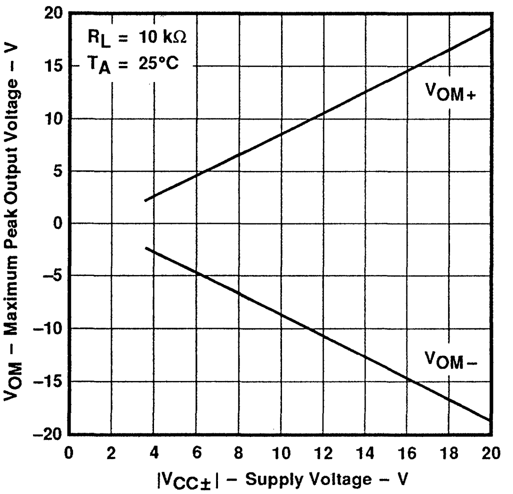


Figure 10

MAXIMUM PEAK OUTPUT VOLTAGE vs SUPPLY VOLTAGE

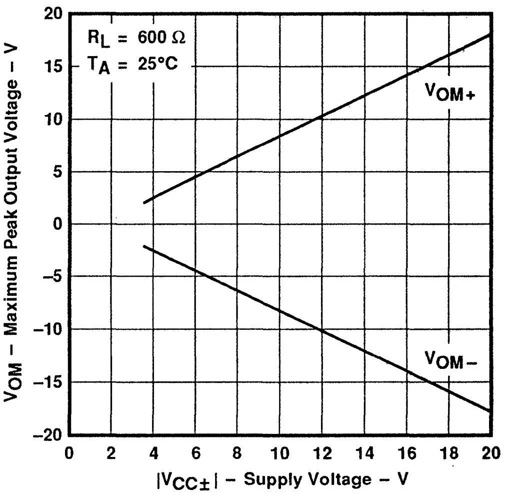


Figure 11

TYPICAL CHARACTERISTICS

MAXIMUM PEAK OUTPUT VOLTAGE
vs
SUPPLY VOLTAGE

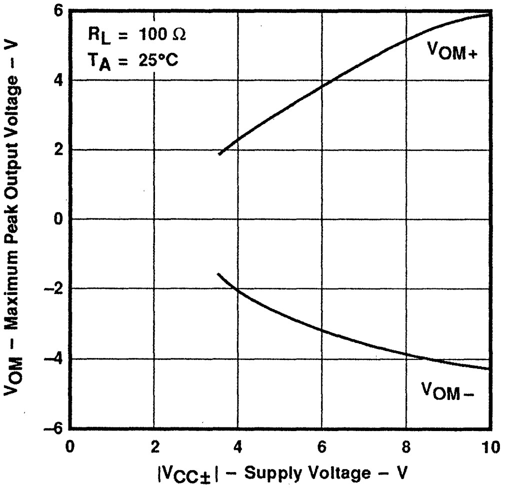


Figure 12

MAXIMUM PEAK-TO-PEAK
OUTPUT VOLTAGE
vs
FREQUENCY

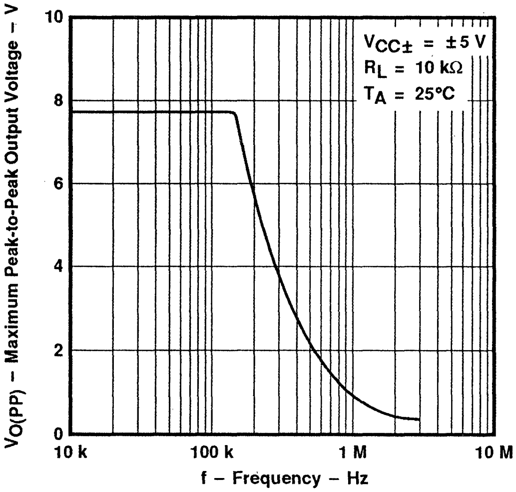


Figure 13

MAXIMUM PEAK-TO-PEAK
OUTPUT VOLTAGE
vs
FREQUENCY

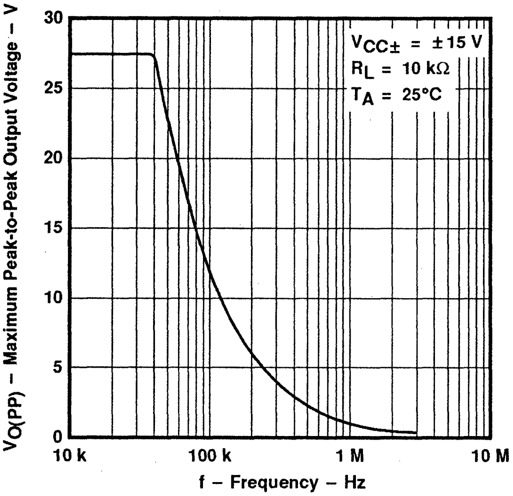


Figure 14

MAXIMUM PEAK-TO-PEAK
OUTPUT VOLTAGE
vs
FREQUENCY

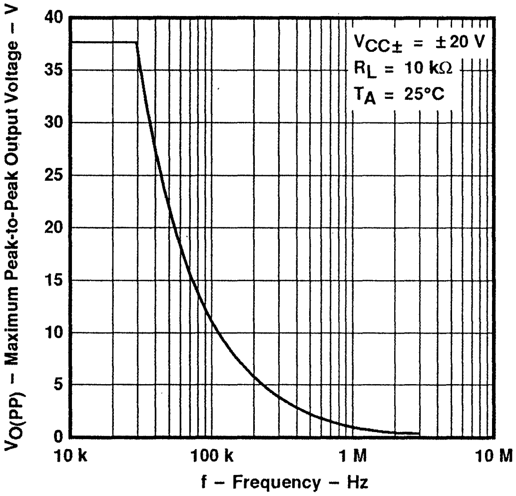


Figure 15

TYPICAL CHARACTERISTICS

LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION and PHASE SHIFT
vs
FREQUENCY

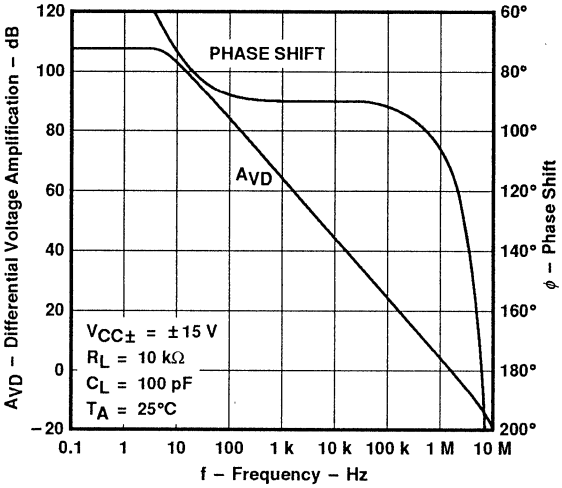


Figure 16

LARGE-SIGNAL VOLTAGE AMPLIFICATION
vs
FREE-AIR TEMPERATURE

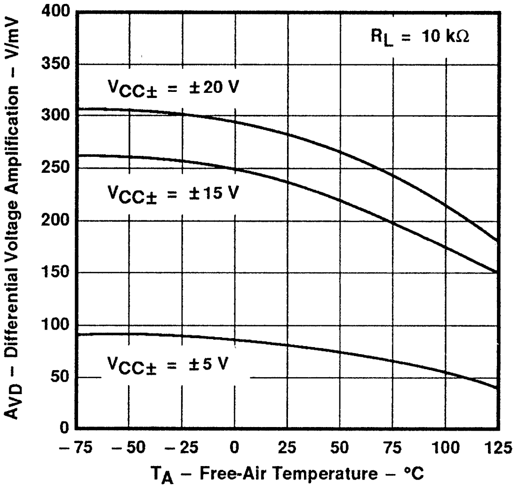


Figure 17

SHORT-CIRCUIT OUTPUT CURRENT
vs
ELAPSED TIME

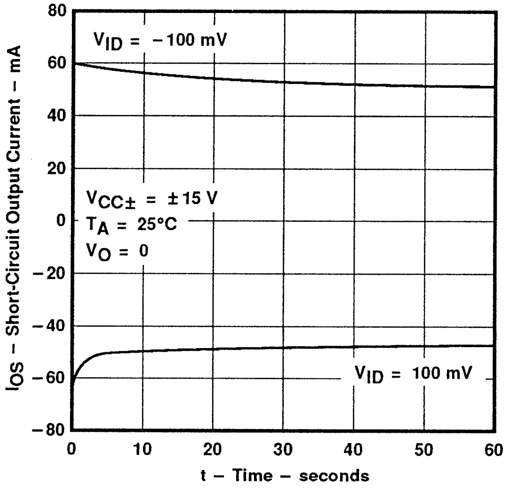


Figure 18

SHORT-CIRCUIT OUTPUT CURRENT
vs
FREE-AIR TEMPERATURE

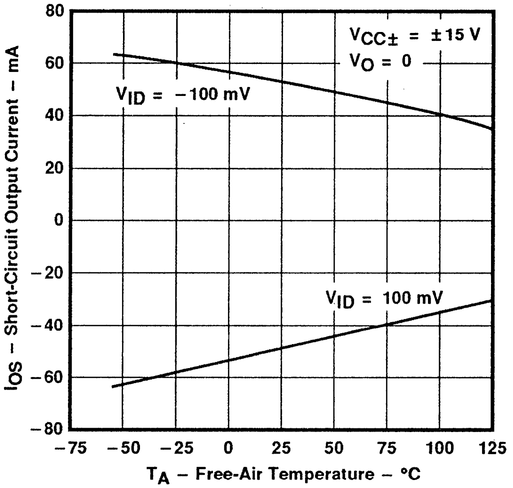


Figure 19

TYPICAL CHARACTERISTICS†

OUTPUT IMPEDANCE
vs
FREQUENCY

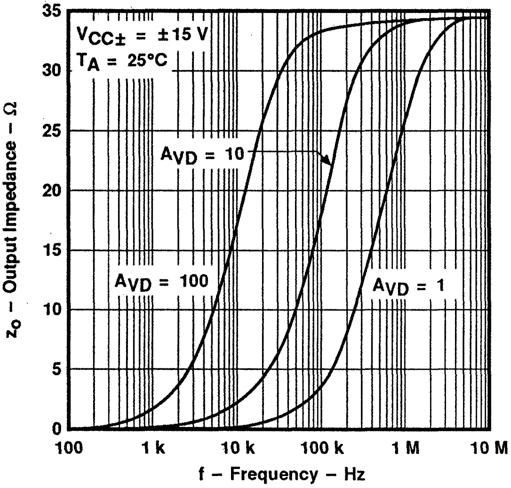


Figure 20

COMMON-MODE REJECTION RATIO
vs
FREQUENCY

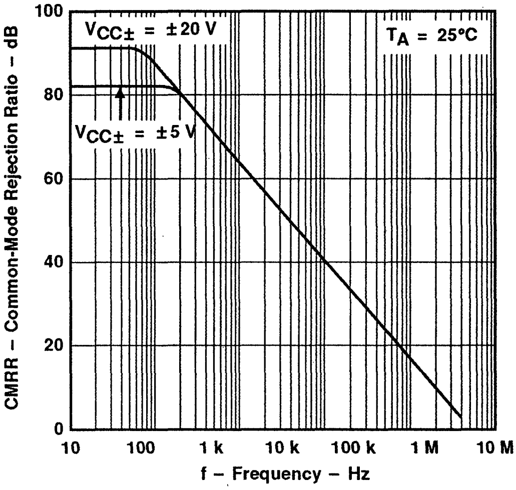


Figure 21

SUPPLY CURRENT
vs
SUPPLY VOLTAGE

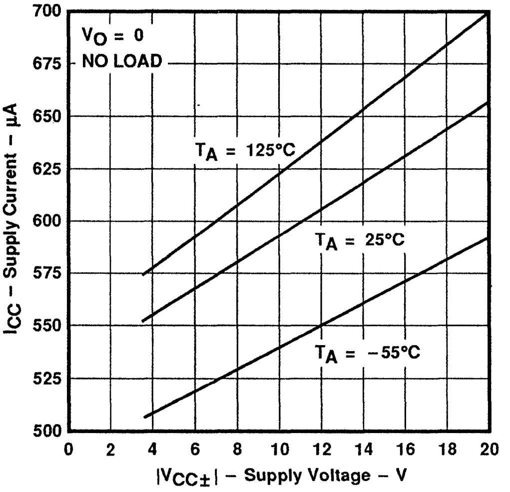


Figure 22

SUPPLY CURRENT
vs
FREE-AIR TEMPERATURE

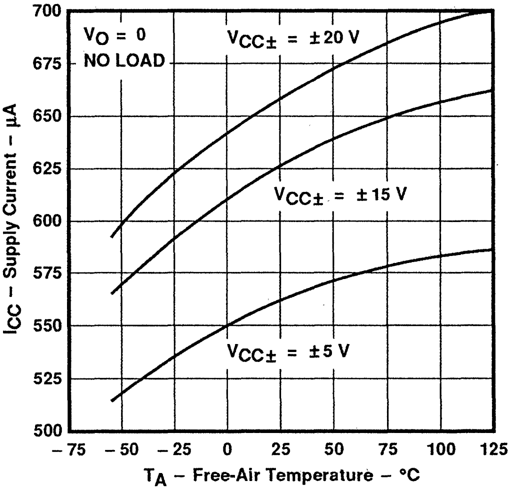


Figure 23

---

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS

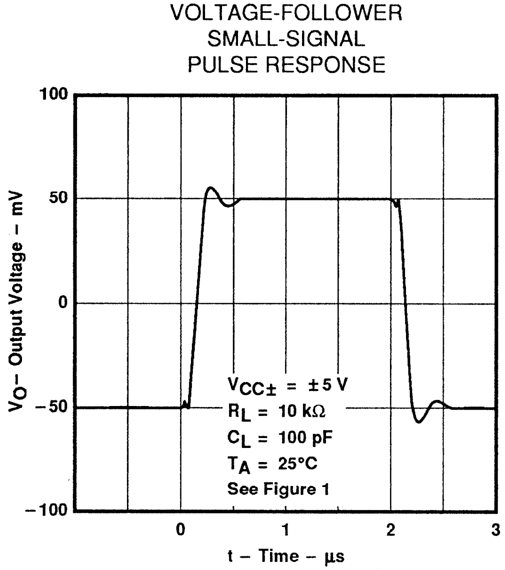


Figure 24

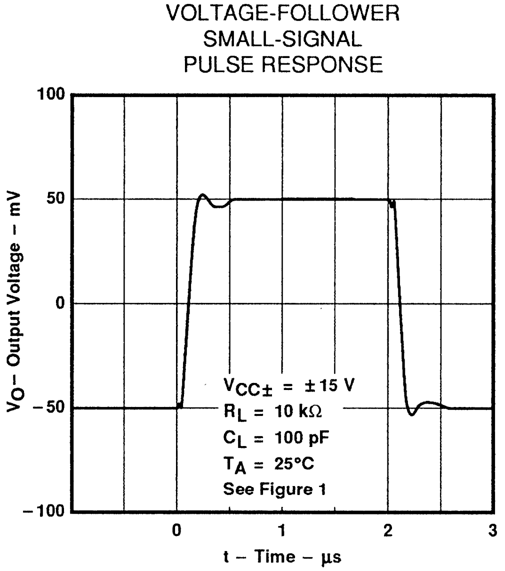


Figure 25

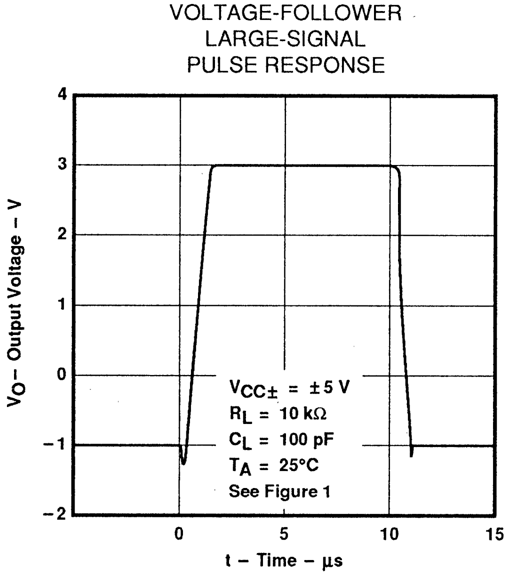


Figure 26

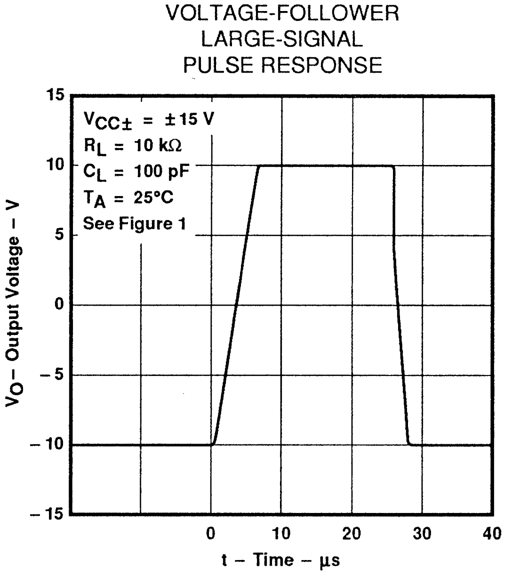


Figure 27

TYPICAL CHARACTERISTICS

NOISE VOLTAGE
(REFERRED TO INPUT)
0.1 TO 10 Hz

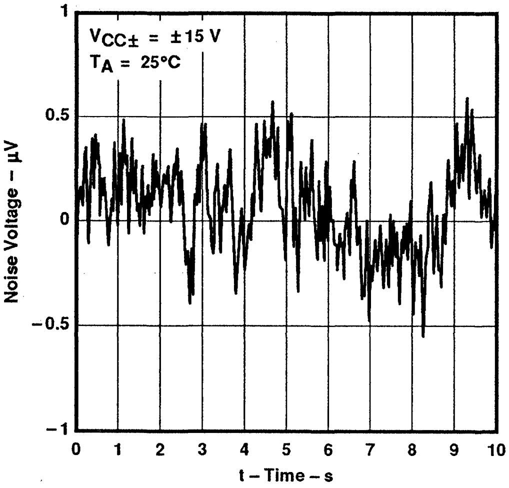


Figure 28

EQUIVALENT INPUT NOISE VOLTAGE
vs
FREQUENCY

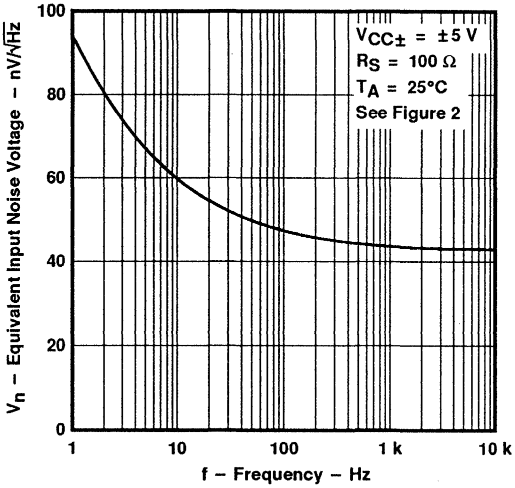


Figure 29

TOTAL HARMONIC DISTORTION
vs
FREQUENCY

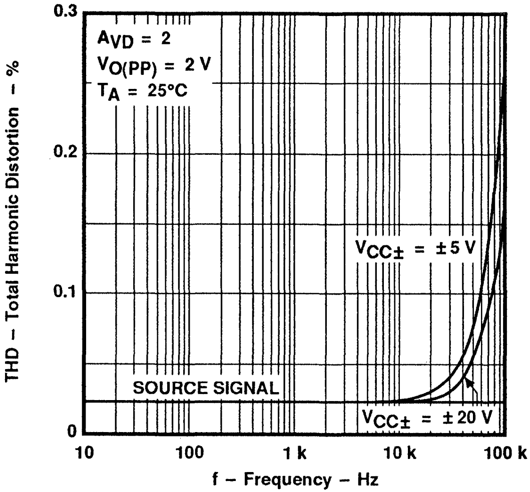


Figure 30

TOTAL HARMONIC DISTORTION
vs
FREQUENCY

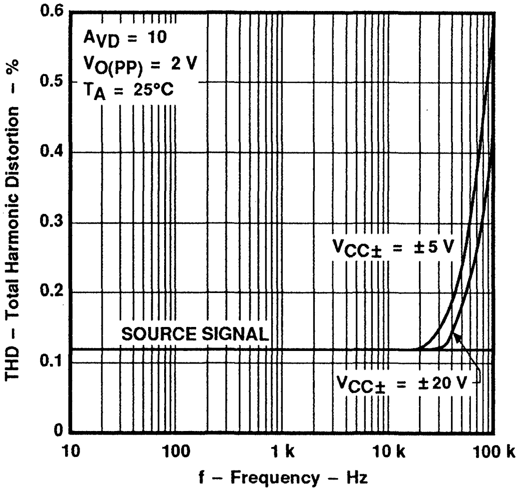


Figure 31

TYPICAL CHARACTERISTICS†

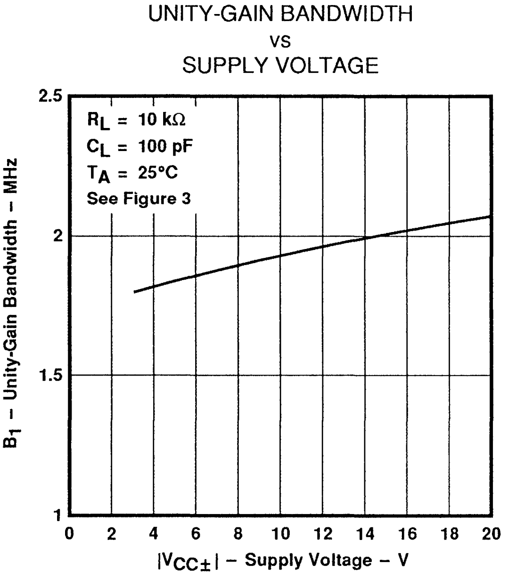


Figure 32

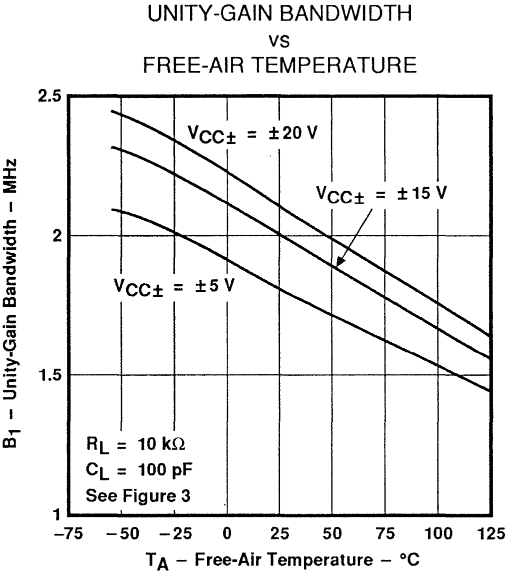


Figure 33

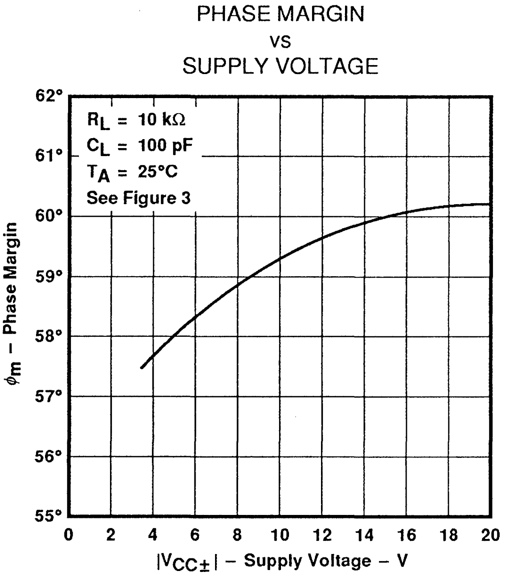


Figure 34

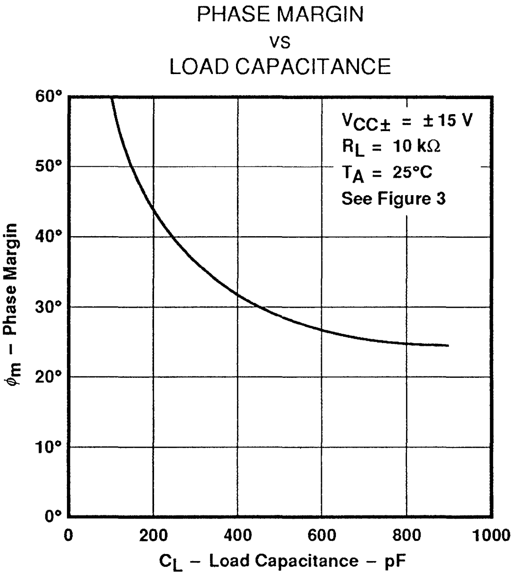


Figure 35

---

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

PHASE MARGIN
vs
FREE-AIR TEMPERATURE

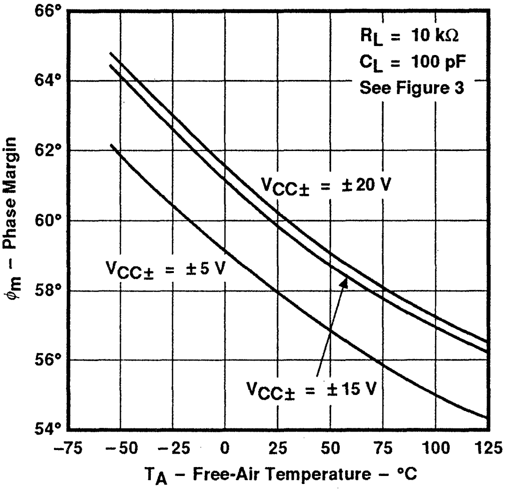


Figure 36

---

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

APPLICATION INFORMATION

macromodel information

Macromodel information provided was derived using *PSpice*™ *Parts*™ model generation software. The Boyle macromodel (see Note 5) and subcircuit in Figure 37 were generated using the TLE2062 typical electrical and operating characteristics at 25°C. Using this information, output simulations of the following key parameters can be generated to a tolerance of 20% (in most cases):

- Maximum positive output voltage swing
- Maximum negative output voltage swing
- Slew rate
- Quiescent power dissipation
- Input bias current
- Open-loop voltage amplification
- Unity-gain frequency
- Common-mode rejection ratio
- Phase margin
- dc output resistance
- ac output resistance
- Short-circuit output current limit

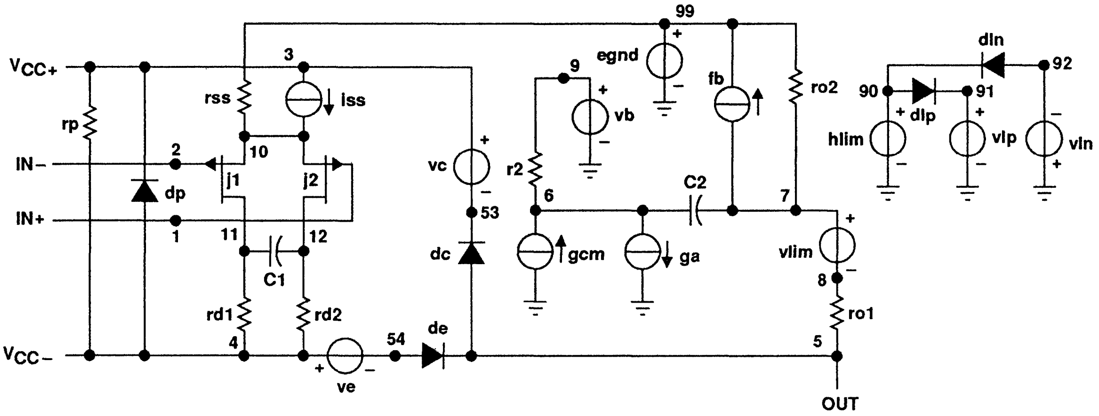
NOTE 5: G. R. Boyle, B. M. Cohn, D. O. Pederson, and J. E. Solomon, "Macromodeling of Integrated Circuit Operational Amplifiers", IEEE Journal of Solid-State Circuits, SC-9, 353 (1974).

PSpice and *Parts* are trademarks of MicroSim Corporation.

Macromodels, simulation models, or other models provided by TI, directly or indirectly, are not warranted by TI as fully representing all of the specifications and operating characteristics of the semiconductor product to which the model relates.

APPLICATION INFORMATION

macromodel information (continued)



```
.subckt TLE2062  1 2 3 4 5
  c1    11 12 1.457E-12
  c2     6  7 15.00E-12
  dc     5 53 dx
  de    54  5 dx
  dlp   90 91 dx
  dln   92 90 dx
  dp     4  3 dx
  egnd  99  0 poly(2) (3,0) (4,0) 0 .5 .5
  fb     7 99 poly(5) vb vc ve vlp vln 0 4.357E6 -4E6 4E6 4E6 -4E6
  ga     6  0 11 12 188.5E-6
  gcm    0  6 10 99 3.352E-9
  iss    3 10 dc 51.00E-6
  hlim  90  0 vlim 1K
  j1    11  2 10 jx
  j2    12  1 10 jx
  r2     6  9 100.0E3
  rd1    4 11 5.305E3
  rd2    4 12 5.305E3
  ro1    8  5 280
  ro2    7 99 280
  rp     3  4 113.2E3
  rss   10 99 3.922E6
  vb     9  0 dc 0
  vc     3 53 dc 2
  ve    54  4 dc 2
  vlim   7  8 dc 0
  vlp   91  0 dc 50
  vln    0 92 dc 50
.model dx D(Is=800.0E-18)
.model jx PJF(Is=2.000E-12 Beta=423E-6 Vto=-1)
.ends
```

Figure 37. Boyle Macromodel and Subcircuit

APPLICATION INFORMATION

input characteristics

The TLE2062, TLE2062A, and TLE2062B are specified with a minimum and a maximum input voltage that, if exceeded at either input, could cause the device to malfunction.

Because of the extremely high input impedance and resulting low bias current requirements, the TLE2062, TLE2062A, and TLE2062B are well suited for low-level signal processing; however, leakage currents on printed circuit boards and sockets can easily exceed bias current requirements and cause degradation in system performance. It is a good practice to include guard rings around inputs (see Figure 38). These guards should be driven from a low-impedance source at the same voltage level as the common-mode input.

The inputs of any unused amplifiers should be tied to ground to avoid possible oscillation.

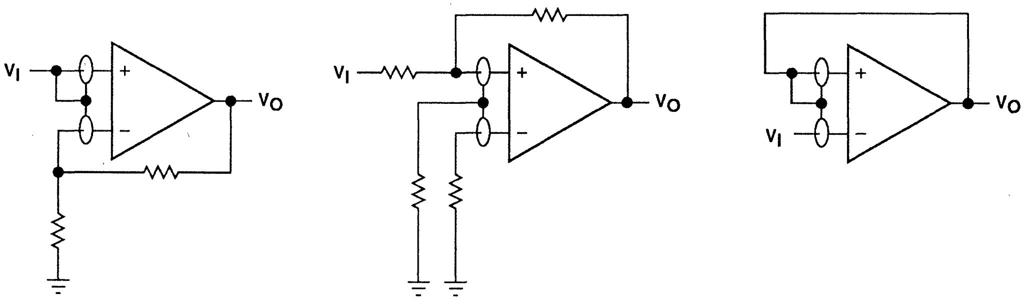


Figure 38. Use of Guard Rings

TLE2064, TLE2064A, TLE2064B, TLE2064Y
EXCALIBUR JFET-INPUT HIGH-OUTPUT-DRIVE µPOWER QUAD OPERATIONAL AMPLIFIERS

D3367, NOVEMBER 1989 – REVISED NOVEMBER 1991

available features

- Excellent Output Drive Capability
  V_O = ± 2.5 V Min at R_L = 100 Ω,
  $V_{CC\pm}$ = ± 5 V
  V_O = ± 12.5 V Min at R_L = 600 Ω,
  $V_{CC\pm}$ = ± 15 V
- Low Supply Current . . . 280 µA Typ Per Amplifier
- High Unity-Gain Bandwidth . . . 2.1 MHz Typ
- High Slew Rate . . . 3.4 V/µs Typ
- Macromodels Included
- Wide Operating Supply Voltage Range
  $V_{CC\pm}$ = ± 3.5 V to ± 20 V
- High Open-Loop Gain . . . 280 V/mV Typ
- Low Offset Voltage . . . 2 mV Max
- Low Offset Voltage Drift With Time
  0.04 µV/mo Typ
- Low Input Bias Current . . . 5 pA Typ

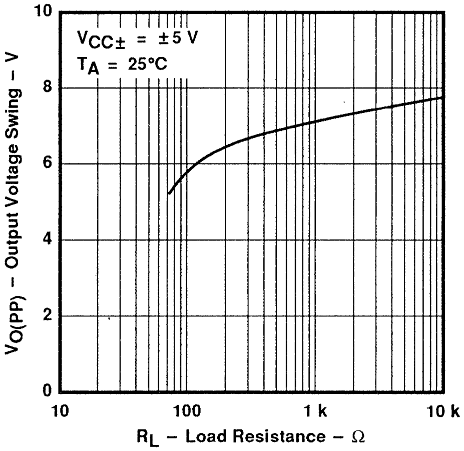
description

The TLE2064, TLE2064A, TLE2064B, and TLE2064Y are JFET-input, high-output-drive, micropower quad operational amplifiers manufactured using Texas Instruments Excalibur process. These devices combine outstanding output drive capability with low-power consumption, excellent dc precision, and wide bandwidth.

In addition to maintaining the traditional JFET advantages of fast slew rates and low input bias and offset currents, the Excalibur process offers outstanding parametric stability over time and temperature. This results in a "precision" device remaining precise even with changes in temperature and over years of use.

The TLE2064, TLE2064A, and TLE2064B are ideal choices for any application requiring excellent dc precision, high output drive, wide bandwidth, and low power consumption.

MAXIMUM PEAK-TO-PEAK
OUTPUT VOLTAGE SWING
vs
LOAD RESISTANCE



AVAILABLE OPTIONS

T_A	V_{IO} max AT 25°C	PACKAGE				CHIP FORM (Y)
		SMALL OUTLINE (D)	CHIP CARRIER (FK)	CERAMIC DIP (J)	PLASTIC DIP (N)	
0°C to 70°C	2 mV	—	—	—	—	TLE2064Y
	4 mV	TLE2064ACD	—	—	TLE2064ACN	
	6 mV	TLE2064CD	—	—	TLE2064CN	
– 40°C to 85°C	2 mV	—	—	—	—	
	4 mV	TLE2064AID	—	—	TLE2064AIN	
	6 mV	TLE2064ID	—	—	TLE2064IN	
– 55°C to 125°C	2 mV	—	—	—	—	
	4 mV	TLE2064AMD	TLE2064AMFK	TLE2064AMJ	TLE2064AMN	
	6 mV	TLE2064MD	TLE2064MFK	TLE2064MJ	TLE2064MN	

D packages are available taped and reeled. Add "R" suffix to device type, (e.g., TLE2064ACDR). Chips are tested at 25°C.

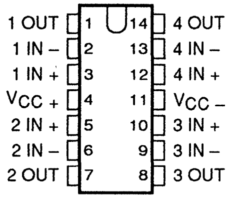
TEXAS INSTRUMENTS
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

description (continued)

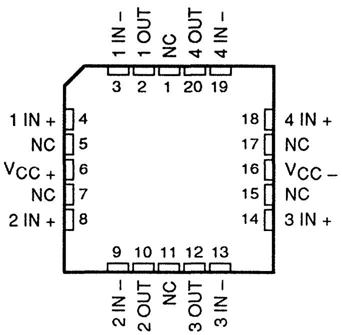
A variety of available options includes small-outline and chip-carrier versions for high-density system applications.

The C-suffix devices are characterized for operation from 0°C to 70°C. The I-suffix devices are characterized for operation from – 40°C to 85°C. The M-suffix devices are characterized for operation over the full military temperature range of –55°C to 125°C.

D, J, OR N PACKAGE
(TOP VIEW)

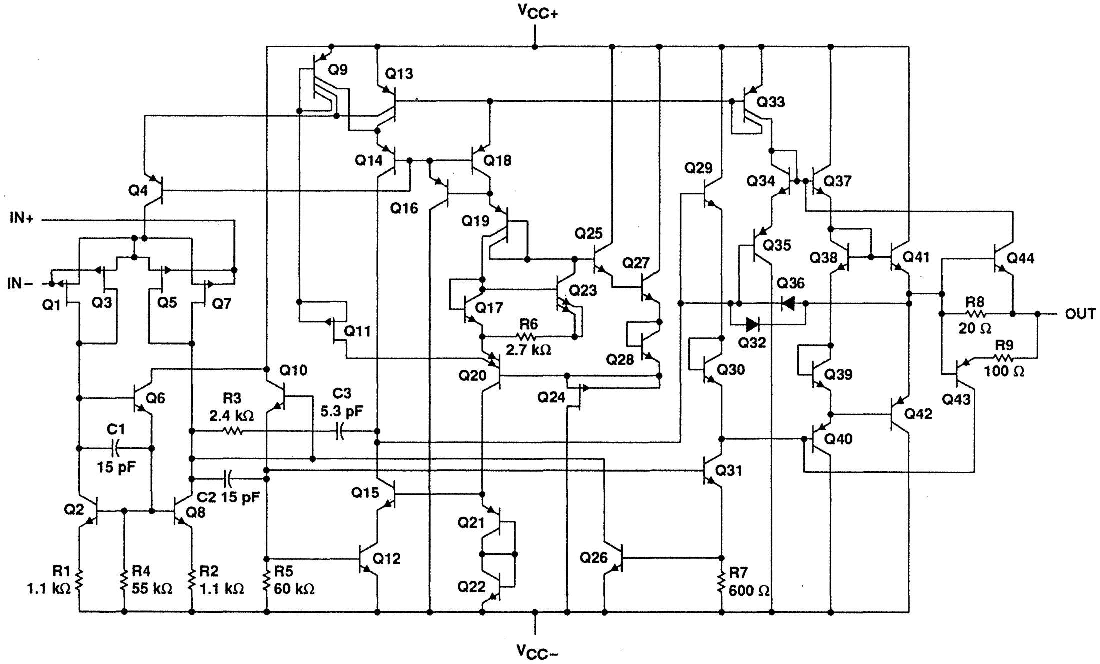


FK PACKAGE
(TOP VIEW)



NC – No internal connection

equivalent schematic (each channel)

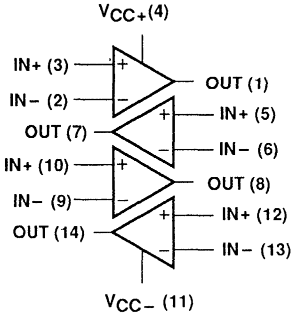


All component values are nominal.

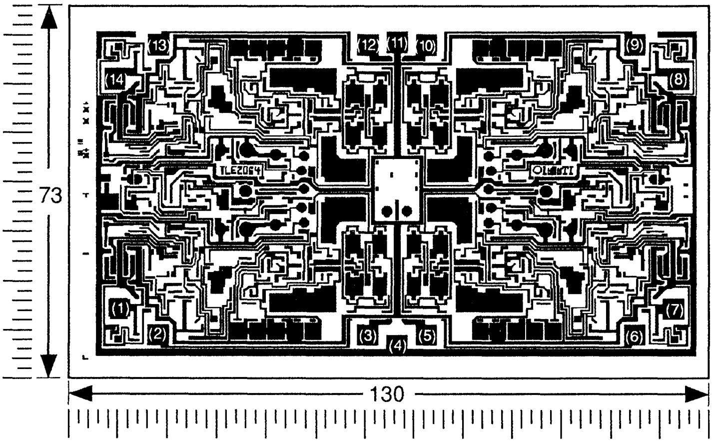
Component count: Diodes — 2 Resistors — 9
Capacitors — 3 Transistors — 42

chip information

These chips, properly assembled, display characteristics similar to the TLE2064. Thermal compression or ultrasonic bonding may be used on the doped aluminum bonding pads. Chips may be mounted with conductive epoxy or a gold-silicon preform.



BONDING PAD ASSIGNMENTS



CHIP THICKNESS:
15 TYPICAL

BONDING PADS:
4 X 4 MINIMUM

$T_J$max = 150°C

TOLERANCES
ARE ± 10%

ALL DIMENSIONS
ARE IN MILS

PIN (11) INTERNALLY
CONNECTED TO
BACKSIDE OF CHIP

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC+} (see Note 1)	22 V
Supply voltage, V_{CC-}	−22 V
Differential input voltage (see Note 2)	±44 V
Input voltage range, V_I (any input)	$V_{CC\pm}$
Input current, I_I (each input)	±1 mA
Output current, I_O (each output)	±80 mA
Total current into V_{CC+} terminal	80 mA
Total current out of V_{CC-} terminal	80 mA
Duration of short-circuit current at (or below) 25°C (see Note 3)	unlimited
Continuous total dissipation	See Dissipation Rating Table
Operating free-air temperature range, T_A: C-suffix	0°C to 70°C
I-suffix	−40°C to 85°C
M-suffix	−55°C to 125°C
Storage temperature range	−65°C to 150°C
Case temperature for 60 seconds: FK package	260°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D or N package	260°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: J package	300°C

NOTES: 1. All voltage values, except differential voltages, are with respect to the midpoint between V_{CC+} and V_{CC-}.
2. Differential voltages are at the noninverting input with respect to the inverting input.
3. The output may be shorted to either supply. Temperature and/or supply voltages must be limited to ensure that the maximum dissipation rating is not exceeded.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING	$T_A = 125°C$ POWER RATING
D	950 mW	7.6 mW/°C	608 mW	494 mW	190 mW
FK	1375 mW	11.0 mW/°C	880 mW	715 mW	275 mW
J	1375 mW	11.0 mW/°C	880 mW	715 mW	275 mW
N	1150 mW	9.2 mW/°C	736 mW	598 mW	230 mW

recommended operating conditions

		C-SUFFIX		I-SUFFIX		M-SUFFIX		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
Supply voltage, $V_{CC\pm}$		± 3.5	± 20	± 3.5	± 20	± 3.5	± 20	V
Common-mode input voltage, V_{IC}	$V_{CC\pm} = \pm 5$ V	− 1.6	4	− 1.6	4	− 1.6	4	V
	$V_{CC\pm} = \pm 15$ V	− 11	13	− 11	13	− 11	13	
	$V_{CC\pm} = \pm 20$ V	− 15	16.5	− 15	16.5	− 15	16.5	
Operating free-air temperature, T_A		0	70	− 40	85	− 55	125	°C

electrical characteristics at specified free-air temperature, $V_{CC\pm}$ = ±5 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS	T_A†	MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	TLE2064C	$V_{IC} = 0$, $R_S = 50\ \Omega$	25°C		1.2	7	mV
				Full range			7.9	
		TLE2064AC		25°C		1.2	6	
				Full range			6.9	
		TLE2064BC		25°C		0.8	3.5	
				Full range			4.4	
α_{VIO}	Temperature coefficient of input offset voltage			25°C		6		μV/°C
	Input offset voltage long-term drift (see Note 4)			Full range		0.04		μV/mo
I_{IO}	Input offset current			25°C		1		pA
				Full range			0.8	nA
I_{IB}	Input bias current			25°C		3		pA
				Full range			2	nA
V_{ICR}	Common-mode input voltage range			25°C	−1.6 to 4	−2 to 6		V
				Full range	−1.6 to 4			V
V_{OM+}	Maximum positive peak output voltage swing		$R_L = 10\ k\Omega$	25°C	3.5	3.7		V
				Full range	3.3			
			$R_L = 100\ \Omega$	25°C	2.5	3.1		
				Full range	2			
V_{OM-}	Maximum negative peak output voltage swing		$R_L = 10\ k\Omega$	25°C	−3.7	−3.9		V
				Full range	−3.3			
			$R_L = 100\ \Omega$	25°C	−2.5	−2.7		
				Full range	−2			
A_{VD}	Large-signal differential voltage amplification		$V_O = \pm 2.8$ V, $R_L = 10\ k\Omega$	25°C	15	80		V/mV
				Full range	2			
			$V_O = 0$ to 2 V, $R_L = 100\ \Omega$	25°C	0.75	45		
				Full range	0.5			
			$V_O = 0$ to −2 V, $R_L = 100\ \Omega$	25°C	0.5	3		
				Full range	0.15			
r_i	Input resistance			25°C		10^{12}		Ω
c_i	Input capacitance			25°C		4		pF
z_o	Open-loop output impedance		$I_O = 0$	25°C		560		Ω
CMRR	Common-mode rejection ratio		$V_{IC} = V_{ICR}$ min, $R_S = 50\ \Omega$	25°C	65	82		dB
				Full range	65			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm} / \Delta V_{IO}$)		$V_{CC\pm} = \pm 5$ V to ±20 V, $R_S = 50\ \Omega$	25°C	75	93		dB
				Full range	75			
I_{CC}	Supply current (four amplifiers)		$V_O = 0$, No load	25°C		1.12	1.3	mA
				Full range			1.3	
ΔI_{CC}	Supply current change over operating temperature range (four amplifiers)			Full range		52		μA
V_{O1}/V_{O2}	Crosstalk attenuation		$A_{VD} = 1000$, f = 1 kHz	25°C		120		dB

†Full range is 0°C to 70°C.

NOTE 4: Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at T_A = 150°C extrapolated to T_A = 25°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

operating characteristics at specified free-air temperature, $V_{CC\pm} = \pm 5$ V

PARAMETER		TEST CONDITIONS		T_A†	MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain (see Figure 1)	R_L = 10 kΩ,	C_L = 100 pF	25°C	2.2	3.4		V/μs
				Full range	2.1			
V_n	Equivalent input noise voltage (see Figure 2)	f = 10 Hz,	R_S = 100 Ω	25°C		59	100	nV/√Hz
		f = 1 kHz,	R_S = 100 Ω			43	60	
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 10 Hz		25°C		1.1		μV
I_n	Equivalent input noise current	f = 1 kHz		25°C		1		fA/√Hz
THD	Total harmonic distortion	A_{VD} = 2, $V_{O(PP)}$ = 2 V,	f = 10 kHz, R_L = 10 kΩ	25°C		0.025%		
B_1	Unity-gain bandwidth (see Figure 3)	R_L = 10 kΩ,	C_L = 100 pF	25°C		1.8		MHz
		R_L = 100 Ω,	C_L = 100 pF			1.3		
	Settling time	ε = 0.1%		25°C		5		μs
		ε = 0.01%				10		
B_{OM}	Maximum-output-swing bandwidth	A_{VD} = 1,	R_L = 10 kΩ	25°C		140		kHz
ϕ_m	Phase margin at unity gain (see Figure 3)	R_L = 10 kΩ,	C_L = 100 pF	25°C		58°		
		R_L = 100 Ω,	C_L = 100 pF			75°		

†Full range is 0°C to 70°C.

electrical characteristics at specified free-air temperature, $V_{CC\pm} = \pm 15$ V (unless otherwise noted)

PARAMETER			TEST CONDITIONS	T_A†	MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	TLE2064C	$V_{IC} = 0$, $R_S = 50\ \Omega$	25°C		0.9	6	mV
				Full range			6.9	
		TLE2064AC		25°C		0.9	4	
				Full range			4.9	
		TLE2064BC		25°C		0.7	2	
				Full range			4	
α_{VIO}	Temperature coefficient of input offset voltage			25°C		6		µV/°C
	Input offset voltage long-term drift (see Note 4)			Full range		0.004		µV/mo
I_{IO}	Input offset current			25°C		2		pA
				Full range			1	nA
I_{IB}	Input bias current			25°C		4		pA
				Full range			3	nA
V_{ICR}	Common-mode input voltage range			25°C	− 11 to 13	− 12 to 16		V
				Full range	− 11 to 13			V
V_{OM+}	Maximum positive peak output voltage swing		$R_L = 10\ k\Omega$	25°C	13.2	13.7		V
				Full range	13			
			$R_L = 600\ \Omega$	25°C	12.5	13.2		
				Full range	12			
V_{OM-}	Maximum negative peak output voltage swing		$R_L = 10\ k\Omega$	25°C	− 13.2	− 13.7		V
				Full range	− 13			
			$R_L = 600\ \Omega$	25°C	− 12.5	− 13		
				Full range	− 12			
A_{VD}	Large-signal differential voltage amplification		$V_O = \pm 10$ V, $R_L = 10\ k\Omega$	25°C	30	230		V/mV
				Full range	20			
			$V_O = 0$ to 8 V, $R_L = 600\ \Omega$	25°C	25	100		
				Full range	10			
			$V_O = 0$ to − 8 V, $R_L = 600\ \Omega$	25°C	3	25		
				Full range	1			
r_i	Input resistance			25°C		10^{12}		Ω
c_i	Input capacitance			25°C		4		pF
z_o	Open-loop output impedance		$I_O = 0$	25°C		560		Ω
CMRR	Common-mode rejection ratio		$V_{IC} = V_{ICR}$ min, $R_S = 50\ \Omega$	25°C	72	90		dB
				Full range	70			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm} / \Delta V_{IO}$)		$V_{CC\pm} = \pm 5$ V to ± 15 V, $R_S = 50\ \Omega$	25°C	75	93		dB
				Full range	75			
I_{CC}	Supply current (four amplifiers)		$V_O = 0$, No load	25°C		1.25	1.4	mA
				Full range			1.5	
ΔI_{CC}	Supply current change over operating temperature range (four amplifiers)			Full range		72		µA
V_{o1}/V_{o2}	Crosstalk attenuation		$A_{VD} = 1000$, f = 1 kHz	25°C		120		dB

†Full range is 0°C to 70°C.

NOTE 4: Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at $T_A = 150°C$ extrapolated to $T_A = 25°C$ using the Arrhenius equation and assuming an activation energy of 0.96 eV.

operating characteristics at specified free-air temperature, $V_{CC\pm} = \pm 15$ V

PARAMETER		TEST CONDITIONS		T_A†	MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain (see Figure 1)	R_L = 10 kΩ,	C_L = 100 pF	25°C	2.6	3.4		V/μs
				Full range	2.5			
V_n	Equivalent input noise voltage (see Figure 2)	f = 10 Hz,	R_S = 100 Ω	25°C		70	100	nV/√Hz
		f = 1 kHz,	R_S = 100 Ω			40	60	
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 10 Hz		25°C		1.1		μV
I_n	Equivalent input noise current	f = 1 kHz		25°C		1.1		fA/√Hz
THD	Total harmonic distortion	A_{VD} = 2, $V_{O(PP)}$ = 2 V,	f = 10 kHz, R_L = 10 kΩ	25°C		0.025%		
B_1	Unity-gain bandwidth (see Figure 3)	R_L = 10 kΩ,	C_L = 100 pF	25°C		2		MHz
		R_L = 600 Ω,	C_L = 100 pF			1.5		
	Settling time	ε = 0.1%		25°C		5		μs
		ε = 0.01%				10		
B_{OM}	Maximum-output-swing bandwidth	A_{VD} = 1,	R_L = 10 kΩ	25°C		40		kHz
ϕ_m	Phase margin at unity gain (see Figure 3)	R_L = 10 kΩ,	C_L = 100 pF	25°C		60°		
		R_L = 600 Ω,	C_L = 100 pF			70°		

†Full range is 0°C to 70°C.

electrical characteristics at specified free-air temperature, $V_{CC\pm} = \pm 20$ V (unless otherwise noted)

PARAMETER			TEST CONDITIONS	T_A†	MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	TLE2064C	$V_{IC} = 0$, $R_S = 50\ \Omega$	25°C		1	6	mV
				Full range			6.9	
		TLE2064AC		25°C		1	4.6	
				Full range			5.5	
		TLE2064BC		25°C		0.7	2.2	
				Full range			3.1	
α_{VIO}	Temperature coefficient of input offset voltage			Full range		6		µV/°C
	Input offset voltage long-term drift (see Note 4)			25°C		0.04		µV/mo
I_{IO}	Input offset current			25°C		3		pA
				Full range			1	nA
I_{IB}	Input bias current			25°C		5		pA
				Full range			3	nA
V_{ICR}	Common-mode input voltage range			25°C	−4 to 16.5	−17 to 21		V
				Full range	−15 to 16.5			V
V_{OM+}	Maximum positive peak output voltage swing		$R_L = 10\ k\Omega$	25°C	18.2	18.7		V
				Full range	18			
			$R_L = 600\ \Omega$	25°C	15	18.1		
				Full range	12			
V_{OM-}	Maximum negative peak output voltage swing		$R_L = 10\ k\Omega$	25°C	−18.2	−18.7		V
				Full range	−18			
			$R_L = 600\ \Omega$	25°C	−15	−18		
				Full range	−12			
A_{VD}	Large-signal differential voltage amplification		$V_O = \pm 15$ V, $R_L = 10\ k\Omega$	25°C	30	280		V/mV
				Full range	20			
			$V_O = 0$ to 10 V, $R_L = 600\ \Omega$	25°C	25	80		
				Full range	10			
			$V_O = 0$ to −10 V, $R_L = 600\ \Omega$	25°C	3	20		
				Full range	1			
r_i	Input resistance			25°C		10^{12}		Ω
c_i	Input capacitance			25°C		4		pF
z_o	Open-loop output impedance		$I_O = 0$	25°C		560		Ω
CMRR	Common-mode rejection ratio		$V_{IC} = V_{ICR}$ min, $R_S = 50\ \Omega$	25°C	75	91		dB
				Full range	70			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm} / \Delta V_{IO}$)		$V_{CC\pm} = \pm 5$ V to ±20 V, $R_S = 50\ \Omega$	25°C	75	93		dB
				Full range	70			
I_{CC}	Supply current (four amplifiers)		$V_O = 0$, No load	25°C		1.32	1.5	mA
				Full range			1.5	
ΔI_{CC}	Supply current change over operating temperature range (four amplifiers)			Full range		82		µA
V_{O1}/V_{O2}	Crosstalk attenuation		$A_{VD} = 1000$, $f = 1$ kHz	25°C		120		dB

†Full range is 0°C to 70°C

NOTE 4: Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at $T_A = 150°C$ extrapolated to $T_A = 25°C$ using the Arrhenius equation and assuming an activation energy of 0.96 eV.

operating characteristics at specified free-air temperature, $V_{CC\pm} = \pm 20$ V

PARAMETER		TEST CONDITIONS		T_A†	MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain (see Figure 1)	R_L = 10 kΩ,	C_L = 100 pF	25°C	2.8	3.4		V/μs
				Full range	2.5			
V_n	Equivalent input noise voltage (see Figure 2)	f = 10 Hz,	R_S = 100 Ω	25°C		75	100	nV/√Hz
		f = 1 kHz,	R_S = 100 Ω			40	60	
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 10 Hz		25°C		1.1		μV
I_n	Equivalent input noise current	f = 1 kHz		25°C		1.3		fA/√Hz
THD	Total harmonic distortion	A_{VD} = 2, $V_{O(PP)}$ = 2 V,	f = 10 kHz, R_L = 10 kΩ	25°C		0.025%		
B_1	Unity-gain bandwidth (see Figure 3)	R_L = 10 kΩ,	C_L = 100 pF	25°C		2.1		MHz
		R_L = 600 Ω,	C_L = 100 pF			1.6		
	Settling time	ε = 0.1%		25°C		5		μs
		ε = 0.01%				10		
B_{OM}	Maximum-output-swing bandwidth	A_{VD} = 1,	R_L = 10 kΩ	25°C		28		kHz
ϕ_m	Phase margin at unity gain (see Figure 3)	R_L = 10 kΩ,	C_L = 100 pF	25°C		60°		
		R_L = 600 Ω,	C_L = 100 pF			70°		

†Full range is 0°C to 70°C

electrical characteristics at specified free-air temperature, $V_{CC\pm} = \pm 5$ V (unless otherwise noted)

PARAMETER			TEST CONDITIONS	T_A†	MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	TLE2064I	$V_{IC} = 0$, $R_S = 50\ \Omega$	25°C		1.2	7	mV
				Full range			8.3	
		TLE2064AI		25°C		1.2	6	
				Full range			7.3	
		TLE2064BI		25°C		0.8	3.5	
				Full range			4.8	
α_{VIO}	Temperature coefficient of input offset voltage			Full range		6		μV/°C
	Input offset voltage long-term drift (see Note 4)			25°C		0.04		μV/mo
I_{IO}	Input offset current			25°C		1		pA
				Full range			2	nA
I_{IB}	Input bias current			25°C		3		pA
				Full range			4	nA
V_{ICR}	Common-mode input voltage range			25°C	− 1.6 to 4	− 2 to 6		V
				Full range	− 1.6 to 4			V
V_{OM+}	Maximum positive peak output voltage swing		$R_L = 10\ k\Omega$	25°C	3.5	3.7		V
				Full range	3.1			
			$R_L = 100\ \Omega$	25°C	2.5	3.1		
				Full range	2			
V_{OM-}	Maximum negative peak output voltage swing		$R_L = 10\ k\Omega$	25°C	− 3.7	− 3.9		V
				Full range	− 3.1			
			$R_L = 100\ \Omega$	25°C	− 2.5	− 2.7		
				Full range	− 2			
A_{VD}	Large-signal differential voltage amplification		$V_O = \pm 2.8$ V, $R_L = 10\ k\Omega$	25°C	15	80		V/mV
				Full range	2			
			$V_O = 0$ to 2 V, $R_L = 100\ \Omega$	25°C	0.75	45		
				Full range	0.5			
			$V_O = 0$ to − 2 V, $R_L = 100\ \Omega$	25°C	0.5	3		
				Full range	0.15			
r_i	Input resistance			25°C		10^{12}		Ω
c_i	Input capacitance			25°C		4		pF
z_o	Open-loop output impedance		$I_O = 0$	25°C		560		Ω
CMRR	Common-mode rejection ratio		$V_{IC} = V_{ICR}$ min, $R_S = 50\ \Omega$	25°C	65	82		dB
				Full range	65			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm} / \Delta V_{IO}$)		$V_{CC\pm} = \pm 5$ V to ± 20 V, $R_S = 50\ \Omega$	25°C	75	93		dB
				Full range	65			
I_{CC}	Supply current (four amplifiers)		$V_O = 0$, No load	25°C		1.12	1.3	mA
				Full range			1.3	
ΔI_{CC}	Supply current change over operating temperature range (four amplifiers)			Full range		108		μA
V_{o1}/V_{o2}	Crosstalk attenuation		$A_{VD} = 1000$, $f = 1$ kHz	25°C		120		dB

†Full range is − 40°C to 85°C

NOTE 4: Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at $T_A = 150°C$ extrapolated to $T_A = 25°C$ using the Arrhenius equation and assuming an activation energy of 0.96 eV.

operating characteristics at specified free-air temperature, $V_{CC\pm} = \pm 5$ V

PARAMETER		TEST CONDITIONS		T_A†	MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain (see Figure 1)	R_L = 10 kΩ,	C_L = 100 pF	25°C	2.2	3.4		V/µs
				Full range	1.7			
V_n	Equivalent input noise voltage (see Figure 2)	f = 10 Hz,	R_S = 100 Ω	25°C		59	100	nV/√Hz
		f = 1 kHz,	R_S = 100 Ω			43	60	
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 10 Hz		25°C		1.1		µV
I_n	Equivalent input noise current	f = 1 kHz		25°C		1		fA/√Hz
THD	Total harmonic distortion	A_{VD} = 2, $V_{O(PP)}$ = 2 V,	f = 10 kHz, R_L = 10 kΩ	25°C		0.025%		
B_1	Unity-gain bandwidth (see Figure 3)	R_L = 10 kΩ,	C_L = 100 pF	25°C		1.8		MHz
		R_L = 100 Ω,	C_L = 100 pF			1.3		
	Settling time	ε = 0.1%		25°C		5		µs
		ε = 0.01%				10		
B_{OM}	Maximum-output-swing bandwidth	A_{VD} = 1,	R_L = 10 kΩ	25°C		140		kHz
ϕ_m	Phase margin at unity gain (see Figure 3)	R_L = 10 kΩ,	C_L = 100 pF	25°C		58°		
		R_L = 100 Ω,	C_L = 100 pF			75°		

† Full range is – 40°C to 85°C

electrical characteristics at specified free-air temperature, $V_{CC\pm} = \pm 15$ V (unless otherwise noted)

PARAMETER			TEST CONDITIONS	T_A†	MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	TLE2064I	$V_{IC} = 0$, $R_S = 50\ \Omega$	25°C		0.9	6	mV
				Full range			7.3	
		TLE2064AI		25°C		0.9	4	
				Full range			5.3	
		TLE2064BI		25°C		0.7	2	
				Full range			3.3	
α_{VIO}	Temperature coefficient of input offset voltage			Full range		6		µV/°C
	Input offset voltage long-term drift (see Note 4)			25°C		0.04		µV/mo
I_{IO}	Input offset current			25°C		2		pA
				Full range			3	nA
I_{IB}	Input bias current			25°C		4		pA
				Full range			5	nA
V_{ICR}	Common-mode input voltage range			25°C	−11 to 13	−12 to 16		V
				Full range	−11 to 13			V
V_{OM+}	Maximum positive peak output voltage swing		$R_L = 10\ k\Omega$	25°C	13.2	13.7		V
				Full range	13			
			$R_L = 600\ \Omega$	25°C	12.5	13.2		
				Full range	12			
V_{OM-}	Maximum negative peak output voltage swing		$R_L = 10\ k\Omega$	25°C	−13.2	−13.7		V
				Full range	−13			
			$R_L = 600\ \Omega$	25°C	−12.5	−13		
				Full range	−12			
A_{VD}	Large-signal differential voltage amplification		$V_O = \pm 10$ V, $R_L = 10\ k\Omega$	25°C	30	230		V/mV
				Full range	20			
			$V_O = 0$ to 8 V, $R_L = 600\ \Omega$	25°C	25	100		
				Full range	10			
			$V_O = 0$ to −8 V, $R_L = 600\ \Omega$	25°C	3	25		
				Full range	1			
r_i	Input resistance			25°C		10^{12}		Ω
c_i	Input capacitance			25°C		4		pF
z_o	Open-loop output impedance		$I_O = 0$	25°C		560		Ω
CMRR	Common-mode rejection ratio		$V_{IC} = V_{ICR}$ min, $R_S = 50\ \Omega$	25°C	72	90		dB
				Full range	65			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm} / \Delta V_{IO}$)		$V_{CC\pm} = \pm 5$ V to ± 15 V, $R_S = 50\ \Omega$	25°C	75	93		dB
				Full range	65			
I_{CC}	Supply current (four amplifiers)		$V_O = 0$, No load	25°C		1.25	1.4	mA
				Full range			1.5	
ΔI_{CC}	Supply current change over operating temperature range (four amplifiers)			Full range		148		µA
V_{o1}/V_{o2}	Crosstalk attenuation		$A_{VD} = 1000$, $f = 1$ kHz	25°C		120		dB

† Full range is − 40°C to 85°C

NOTE 4: Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at $T_A = 150$°C extrapolated to $T_A = 25$°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

operating characteristics at specified free-air temperature, $V_{CC\pm}$ = ±15 V

PARAMETER		TEST CONDITIONS		T_A†	MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain (see Figure 1)	R_L = 10 kΩ,	C_L = 100 pF	25°C	2.6	3.4		V/μs
				Full range	2.1			
V_n	Equivalent input noise voltage (see Figure 2)	f = 10 Hz,	R_S = 100 Ω	25°C		70	100	nV/√Hz
		f = 1 kHz,	R_S = 100 Ω			40	60	
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 10 Hz		25°C		1.1		μV
I_n	Equivalent input noise current	f = 1 kHz		25°C		1.1		fA/√Hz
THD	Total harmonic distortion	A_{VD} = 2, $V_{O(PP)}$ = 2 V,	f = 10 kHz, R_L = 10 kΩ	25°C		0.025%		
B_1	Unity-gain bandwidth (see Figure 3)	R_L = 10 kΩ,	C_L = 100 pF	25°C		2		MHz
		R_L = 600 Ω,	C_L = 100 pF			1.5		
	Settling time	ε = 0.1%		25°C		5		μs
		ε = 0.01%				10		
B_{OM}	Maximum-output-swing bandwidth	A_{VD} = 1,	R_L = 10 kΩ	25°C		40		kHz
ϕ_m	Phase margin at unity gain (see Figure 3)	R_L = 10 kΩ,	C_L = 100 pF	25°C		60°		
		R_L = 600 Ω,	C_L = 100 pF			70°		

†Full range is – 40°C to 85°C

electrical characteristics at specified free-air temperature, $V_{CC\pm} = \pm 20$ V (unless otherwise noted)

PARAMETER			TEST CONDITIONS	T_A†	MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	TLE2064I	$V_{IC} = 0$, $R_S = 50\ \Omega$	25°C		1	6	mV
				Full range			7.3	
		TLE2064AI		25°C		1	4.6	
				Full range			5.9	
		TLE2064BI		25°C		0.7	2.2	
				Full range			3.5	
α_{VIO}	Temperature coefficient of input offset voltage			Full range		6		μV/°C
	Input offset voltage long-term drift (see Note 4)			25°C		0.04		μV/mo
I_{IO}	Input offset current			25°C		3		pA
				Full range			3	nA
I_{IB}	Input bias current			25°C		5		pA
				Full range			5	nA
V_{ICR}	Common-mode input voltage range			25°C	− 15 to 16.5	− 17 to 21		V
				Full range	− 15 to 16.5			V
V_{OM+}	Maximum positive peak output voltage swing		$R_L = 10\ k\Omega$	25°C	18.2	18.7		V
				Full range	18			
			$R_L = 600\ \Omega$	25°C	15	18.1		
				Full range	12			
V_{OM-}	Maximum negative peak output voltage swing		$R_L = 10\ k\Omega$	25°C	− 18.2	− 18.7		V
				Full range	− 18			
			$R_L = 600\ \Omega$	25°C	− 15	− 18		
				Full range	− 12			
A_{VD}	Large-signal differential voltage amplification		$V_O = \pm 15$ V, $R_L = 10\ k\Omega$	25°C	30	280		V/mV
				Full range	20			
			$V_O = 0$ to 10 V, $R_L = 600\ \Omega$	25°C	25	80		
				Full range	10			
			$V_O = 0$ to − 10 V, $R_L = 600\ \Omega$	25°C	3	20		
				Full range	1			
r_i	Input resistance			25°C		10^{12}		Ω
c_i	Input capacitance			25°C		4		pF
z_o	Open-loop output impedance		$I_O = 0$	25°C		560		Ω
CMRR	Common-mode rejection ratio		$V_{IC} = V_{ICR}$ min, $R_S = 50\ \Omega$	25°C	75	91		dB
				Full range	65			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm} / \Delta V_{IO}$)		$V_{CC\pm} = \pm 5$ V to ± 20 V, $R_S = 50\ \Omega$	25°C	75	93		dB
				Full range	65			
I_{CC}	Supply current (four amplifiers)		$V_O = 0$, No load	25°C		1.32	1.5	mA
				Full range			1.6	
ΔI_{CC}	Supply current change over operating temperature range (four amplifiers)			Full range		164		μA
V_{o1}/V_{o2}	Crosstalk attenuation		$A_{VD} = 1000$, $f = 1$ kHz	25°C		120		dB

† Full range is – 40°C to 85°C

NOTE 4: Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at $T_A = 150°C$ extrapolated to $T_A = 25°C$ using the Arrhenius equation and assuming an activation energy of 0.96 eV.

operating characteristics at specified free-air temperature, $V_{CC\pm} = \pm 20$ V

PARAMETER		TEST CONDITIONS		T_A†	MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain (see Figure 1)	R_L = 10 kΩ,	C_L = 100 pF	25°C	2.8	3.4		V/μs
				Full range	2.1			
V_n	Equivalent input noise voltage (see Figure 2)	f = 10 Hz,	R_S = 100 Ω	25°C		75	100	nV/√Hz
		f = 1 kHz,	R_S = 100 Ω			40	60	
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 10 Hz		25°C		1.1		μV
I_n	Equivalent input noise current	f = 1 kHz		25°C		1.3		fA/√Hz
THD	Total harmonic distortion	A_{VD} = 2, $V_{O(PP)}$ = 2 V,	f = 10 kHz, R_L = 10 kΩ	25°C		0.025%		
B_1	Unity-gain bandwidth (see Figure 3)	R_L = 10 kΩ,	C_L = 100 pF	25°C		2.1		MHz
		R_L = 600 Ω,	C_L = 100 pF			1.6		
	Settling time	ε = 0.1%		25°C		5		μs
		ε = 0.01%				10		
B_{OM}	Maximum-output-swing bandwidth	A_{VD} = 1,	R_L = 10 kΩ	25°C		28		kHz
ϕ_m	Phase margin at unity gain (see Figure 3)	R_L = 10 kΩ,	C_L = 100 pF	25°C		60°		
		R_L = 600 Ω,	C_L = 100 pF			70°		

†Full range is – 40°C to 85°C

electrical characteristics at specified free-air temperature, $V_{CC\pm} = \pm 5$ V (unless otherwise noted)

PARAMETER			TEST CONDITIONS	T_A†	MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	TLE2064M	$V_{IC} = 0$, $R_S = 50\ \Omega$	25°C		1.2	7	mV
				Full range			9	
		TLE2064AM		25°C		1.2	6	
				Full range			8	
		TLE2064BM		25°C		0.8	3.5	
				Full range			5.5	
α_{VIO}	Temperature coefficient of input offset voltage			Full range		6		µV/°C
	Input offset voltage long-term drift (see Note 4)			25°C		0.04		µV/mo
I_{IO}	Input offset current			25°C		1		pA
				Full range			15	nA
I_{IB}	Input bias current			25°C		3		pA
				Full range			30	nA
V_{ICR}	Common-mode input voltage range			25°C	− 1.6 to 4	− 2 to 6		V
				Full range	− 1.6 to 4			V
V_{OM+}	Maximum positive peak output voltage swing		$R_L = 10\ k\Omega$	25°C	3.5	3.7		V
				Full range	3			
		FK and J packages	$R_L = 600\ \Omega$	25°C	2.5	3.6		
				Full range	2			
		D and N packages	$R_L = 100\ \Omega$	25°C	2.5	3.1		
				Full range	2			
V_{OM-}	Maximum negative peak output voltage swing		$R_L = 10\ k\Omega$	25°C	− 3.5	− 3.9		V
				Full range	− 3			
		FK and J packages	$R_L = 600\ \Omega$	25°C	− 2.5	− 3.5		
				Full range	− 2			
		D and N packages	$R_L = 100\ \Omega$	25°C	− 2.5	− 2.7		
				Full range	− 2			
A_{VD}	Large-signal differential voltage amplification		$V_O = \pm 2.8$ V, $R_L = 10\ k\Omega$	25°C	15	80		V/mV
				Full range	2			
		FK and J packages	$V_O = 0$ to 2.5 V, $R_L = 600\ \Omega$	25°C	1	65		
				Full range	0.5			
			$V_O = 0$ to − 2.5 V, $R_L = 600\ \Omega$	25°C	1	16		
				Full range	0.5			
		D and N packages	$V_O = 0$ to 2 V, $R_L = 100\ \Omega$	25°C	0.75	45		
				Full range	0.25			
			$V_O = 0$ to − 2 V, $R_L = 100\ \Omega$	25°C	0.4	3		
				Full range	0.15			

† Full range is – 55°C to 125°C

NOTE 4: Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at $T_A = 150°C$ extrapolated to $T_A = 25°C$ using the Arrhenius equation and assuming an activation energy of 0.96 eV.

electrical characteristics at specified free-air temperature, $V_{CC\pm} = \pm 5$ V (unless otherwise noted) (continued)

PARAMETER		TEST CONDITIONS	T_A†	MIN	TYP	MAX	UNIT
r_i	Input resistance		25°C		10^{12}		Ω
c_i	Input capacitance		25°C		4		pF
z_o	Open-loop output impedance	$I_O = 0$	25°C		560		Ω
CMRR	Common-mode rejection ratio	$V_{IC} = V_{ICR}$ min, $R_S = 50\ \Omega$	25°C	65	82		dB
			Full range	60			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm} / \Delta V_{IO}$)	$V_{CC\pm} = \pm 5$ V to ± 20 V, $R_S = 50\ \Omega$	25°C	75	93		dB
			Full range	65			
I_{CC}	Supply current (four amplifiers)	$V_O = 0$, No load	25°C		1.12	1.3	mA
			Full range			1.3	
ΔI_{CC}	Supply current change over operating temperature range (four amplifiers)		Full range		144		μA
V_{o1}/V_{o2}	Crosstalk attenuation	$A_{VD} = 1000$, f = 1 kHz	25°C		120		dB

†Full range is – 55°C to 125°C

operating characteristics, $V_{CC\pm} = \pm 5$ V, $T_A = 25°C$

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain (see Figure 1)	$R_L = 10$ kΩ,	$C_L = 100$ pF		3.4		V/μs
V_n	Equivalent input noise voltage (see Figure 2)	f = 10 Hz,	$R_S = 100\ \Omega$		59		nV/√Hz
		f = 1 kHz,	$R_S = 100\ \Omega$		43		
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 10 Hz			1.1		μV
I_n	Equivalent input noise current	f = 1 kHz			1		fA/√Hz
THD	Total harmonic distortion	$A_{VD} = 2$, $V_{O(PP)} = 2$ V,	f = 10 kHz, $R_L = 10$ kΩ		0.025%		
B_1	Unity-gain bandwidth (see Figure 3)	$R_L = 10$ kΩ,	$C_L = 100$ pF		1.8		MHz
		$R_L = 600\ \Omega$,	$C_L = 100$ pF		1.3		μs
	Settling time	ε = 0.1%			5		
		ε = 0.01%			10		kHz
B_{OM}	Maximum-output-swing bandwidth	$A_{VD} = 1$,	$R_L = 10$ kΩ		140		
ϕ_m	Phase margin at unity gain (see Figure 3)	$R_L = 10$ kΩ,	$C_L = 100$ pF		58°		
		$R_L = 600\ \Omega$,	$C_L = 100$ pF		75°		

electrical characteristics at specified free-air temperature, $V_{CC\pm} = \pm 15$ V (unless otherwise noted)

PARAMETER			TEST CONDITIONS	T_A†	MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	TLE2064M	$V_{IC} = 0$, $R_S = 50\ \Omega$	25°C		0.9	6	mV
				Full range			8	
		TLE2064AM		25°C		0.9	4	
				Full range			6	
		TLE2064BM		25°C		0.7	2	
				Full range			4	
α_{VIO}	Temperature coefficient of input offset voltage			Full range		6		µV/°C
	Input offset voltage long-term drift (see Note 4)			25°C		0.04		µV/mo
I_{IO}	Input offset current			25°C		2		pA
				Full range			20	nA
I_{IB}	Input bias current			25°C		4		pA
				Full range			40	nA
V_{ICR}	Common-mode input voltage range			25°C	−11 to 13	−12 to 16		V
				Full range	−11 to 13			V
V_{OM+}	Maximum positive peak output voltage swing		$R_L = 10\ k\Omega$	25°C	13	13.7		V
				Full range	12.5			
			$R_L = 600\ \Omega$	25°C	12.5	13.2		
				Full range	12			
V_{OM-}	Maximum negative peak output voltage swing		$R_L = 10\ k\Omega$	25°C	−13	−13.7		V
				Full range	−12.5			
			$R_L = 600\ \Omega$	25°C	−13	−13		
				Full range	−12.5			
A_{VD}	Large-signal differential voltage amplification		$V_O = \pm 10$ V, $R_L = 10\ k\Omega$	25°C	30	230		V/mV
				Full range	20			
			$V_O = 0$ to 8 V, $R_L = 600\ \Omega$	25°C	25	100		
				Full range	7			
			$V_O = 0$ to −8 V, $R_L = 600\ \Omega$	25°C	3	25		
				Full range	1			
r_i	Input resistance			25°C		10^{12}		Ω
c_i	Input capacitance			25°C		4		pF
z_o	Open-loop output impedance		$I_O = 0$	25°C		560		Ω
CMRR	Common-mode rejection ratio		$V_{IC} = V_{ICR}$ min, $R_S = 50\ \Omega$	25°C	72	90		dB
				Full range	65			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm} / \Delta V_{IO}$)		$V_{CC\pm} = \pm 5$ V to ±15 V, $R_S = 50\ \Omega$	25°C	75	93		dB
				Full range	65			
I_{CC}	Supply current (four amplifiers)		$V_O = 0$, No load	25°C		1.25	1.4	mA
				Full range			1.5	
ΔI_{CC}	Supply current change over operating temperature range (four amplifiers)			Full range		194		µA
V_{o1}/V_{o2}	Crosstalk attenuation		$A_{VD} = 1000$, f = 1 kHz	25°C		120		dB

†Full range is − 55°C to 125°C

NOTE 4: Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at $T_A = 150°C$ extrapolated to $T_A = 25°C$ using the Arrhenius equation and assuming an activation energy of 0.96 eV.

operating characteristics at specified free-air temperature, $V_{CC\pm}$ = ±15 V

PARAMETER		TEST CONDITIONS		T_A	MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain (see Figure 1)	R_L = 10 kΩ,	C_L = 100 pF	25°C	2.6	3.4		V/μs
				Full range	1.8			
V_n	Equivalent input noise voltage (see Figure 2)	f = 10 Hz,	R_S = 100 Ω	25°C		70		nV/√Hz
		f = 1 kHz,	R_S = 100 Ω			40		
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 10 Hz		25°C		1.1		μV
I_n	Equivalent input noise current	f = 1 kHz		25°C		1.1		fA/√Hz
THD	Total harmonic distortion	A_{VD} = 2, $V_{O(PP)}$ = 2 V,	f = 10 kHz, R_L = 10 kΩ	25°C		0.025%		
B_1	Unity-gain bandwidth (see Figure 3)	R_L = 10 kΩ,	C_L = 100 pF	25°C		2		MHz
		R_L = 600 Ω,	C_L = 100 pF			1.5		
	Settling time	ε = 0.1%		25°C		5		μs
		ε = 0.01%				10		
B_{OM}	Maximum-output-swing bandwidth	A_{VD} = 1,	R_L = 10 kΩ	25°C		40		kHz
ϕ_m	Phase margin at unity gain (see Figure 3)	R_L = 10 kΩ,	C_L = 100 pF	25°C		60°		
		R_L = 600 Ω,	C_L = 100 pF			70°		

†Full range is – 55°C to 125°C

electrical characteristics at specified free-air temperature, $V_{CC\pm} = \pm 20$ V (unless otherwise noted)

PARAMETER			TEST CONDITIONS	T_A†	MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	TLE2064M	$V_{IC} = 0$, $R_S = 50\ \Omega$	25°C		1	6	mV
				Full range			8	
		TLE2064AM		25°C		1	4.6	
				Full range			6.6	
		TLE2064BM		25°C		0.7	2.2	
				Full range			4.2	
α_{VIO}	Temperature coefficient of input offset voltage			Full range		6		µV/°C
	Input offset voltage long-term drift (see Note 4)			25°C		0.04		µV/mo
I_{IO}	Input offset current			25°C		3		pA
				Full range			20	nA
I_{IB}	Input bias current			25°C		5		pA
				Full range			40	nA
V_{ICR}	Common-mode input voltage range			25°C	− 15 to 16.5	− 17 to 21		V
				Full range	− 15 to 16.5			V
V_{OM+}	Maximum positive peak output voltage swing		$R_L = 10\ k\Omega$	25°C	18	18.7		V
				Full range	17.5			
			$R_L = 600\ \Omega$	25°C	15	18.1		
				Full range	12			
V_{OM-}	Maximum negative peak output voltage swing		$R_L = 10\ k\Omega$	25°C	− 18	− 18.7		V
				Full range	− 17.5			
			$R_L = 600\ \Omega$	25°C	− 15	− 18		
				Full range	− 12			
A_{VD}	Large-signal differential voltage amplification		$V_O = \pm 15$ V, $R_L = 10\ k\Omega$	25°C	30	280		V/mV
				Full range	20			
			$V_O = 0$ to 10 V, $R_L = 600\ \Omega$	25°C	25	80		
				Full range	10			
			$V_O = 0$ to − 10 V, $R_L = 600\ \Omega$	25°C	3	20		
				Full range	1			
r_i	Input resistance			25°C		10^{12}		Ω
c_i	Input capacitance			25°C		4		pF
z_o	Open-loop output impedance		$I_O = 0$	25°C		560		Ω
CMRR	Common-mode rejection ratio		$V_{IC} = V_{ICR}$ min, $R_S = 50\ \Omega$	25°C	75	91		dB
				Full range	65			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm} / \Delta V_{IO}$)		$V_{CC\pm} = \pm 5$ V to ± 20 V, $R_S = 50\ \Omega$	25°C	75	93		dB
				Full range	65			
I_{CC}	Supply current (four amplifiers)		$V_O = 0$, No load	25°C		1.32	1.5	mA
				Full range			1.6	
ΔI_{CC}	Supply current change over operating temperature range (four amplifiers)			Full range		212		µA
V_{o1}/V_{o2}	Crosstalk attenuation		$A_{VD} = 1000$, f = 1 kHz	25°C		120		dB

†Full range is – 55°C to 125°C

NOTE 4: Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at T_A = 150°C extrapolated to T_A = 25°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

operating characteristics, $V_{CC\pm} = \pm 20$ V, $T_A = 25°C$

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain (see Figure 1)	$R_L = 10\ k\Omega$,	$C_L = 100\ pF$		3.4		V/µs
V_n	Equivalent input noise voltage (see Figure 2)	f = 10 Hz,	$R_S = 100\ \Omega$		75		nV/√Hz
		f = 1 kHz,	$R_S = 100\ \Omega$		40		
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 10 Hz			1.1		µV
I_n	Equivalent input noise current	f = 1 kHz			1.3		fA/√Hz
THD	Total harmonic distortion	$A_{VD} = 2$, $V_{O(PP)} = 2$ V,	f = 10 kHz, $R_L = 10\ k\Omega$		0.025%		
B_1	Unity-gain bandwidth (see Figure 3)	$R_L = 10\ k\Omega$,	$C_L = 100\ pF$		2.1		MHz
		$R_L = 600\ \Omega$,	$C_L = 100\ pF$		1.6		µs
	Settling time	ε = 0.1%			5		
		ε = 0.01%			10		kHz
B_{OM}	Maximum-output-swing bandwidth	$A_{VD} = 1$,	$R_L = 10\ k\Omega$		28		
ϕ_m	Phase margin at unity gain (see Figure 3)	$R_L = 10\ k\Omega$,	$C_L = 100\ pF$		60°		
		$R_L = 600\ \Omega$,	$C_L = 100\ pF$		70°		

electrical characteristics at $V_{CC\pm}$ = ±15 V, T_A = 25°C (unless otherwise noted)

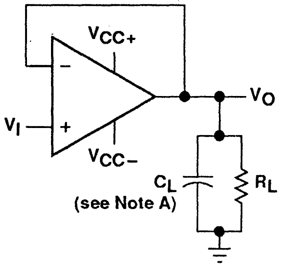
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	$V_{IC} = 0$, $R_S = 50\ \Omega$		0.9	6	mV
$\propto V_{io}$	Input offset voltage long-term drift (see Note 4)			0.04		μV/mo
I_{IO}	Input offset current			2		pA
I_{IB}	Input bias current			4		pA
V_{ICR}	Common-mode input voltage range		−11 to 13	−12 to 16		V
V_{OM+}	Maximum positive peak output voltage swing	$R_L = 10\ k\Omega$	13.2	13.7		V
		$R_L = 600\ \Omega$	12.5	13.2		
V_{OM-}	Maximum negative peak output voltage swing	$R_L = 10\ k\Omega$	−13.2	−13.7		V
		$R_L = 600\ \Omega$	−12.5	−13		
A_{VD}	Large-signal differential voltage amplification	$V_O = \pm 10$ V, $R_L = 10\ k\Omega$	30	230		V/mV
		$V_O = 0$ to 8 V, $R_L = 600\ \Omega$	25	100		
		$V_O = 0$ to −8 V, $R_L = 600\ \Omega$	3	25		
r_i	Input resistance			10^{12}		Ω
c_i	Input capacitance			4		pF
z_o	Open-loop ouput impedance	$I_O = 0$		560		Ω
CMRR	Common-mode rejection ratio	$R_S = 50\ \Omega$, $V_{IC} = V_{ICR}min$	72	90		dB
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC}/\Delta V_{IO}$)	$V_{CC\pm} = \pm 5$ V to ±15 V, $R_S = 50\ \Omega$	75	93		dB
I_{CC}	Supply current	$V_O = 0$, No load		1.25	1.4	mA
V_{o1}/V_{o2}	Crosstalk attentuation	$A_{VD} = 1000$, f = 1 kHz		120		dB

NOTE 4: Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at T_A = 150°C extrapolated to T_A = 25°C using the Arrhenius equation and assuming and activation energy of 0.96 eV.

operating characteristics at $V_{CC\pm}$ = ±15 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain	$R_L = 10\ k\Omega$, $C_L = 100$ pF	2.6	3.4		V/μs
V_n	Equivalent input noise voltage (see Figure 2)	f = 10 Hz, $R_S = 100\ \Omega$		70		nV/√Hz
		f = 1 kHz, $R_S = 100\ \Omega$		40		
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 10 Hz		1.1		μV
I_n	Equivalent input noise current	f = 1 Hz		1.1		fA/√Hz
THD	Total harmonic distortion	$A_{VD} = 2$, f = 10 kHz, $V_{O(PP)} = 2$ V, $R_L = 10\ k\Omega$		0.025%		
B_1	Unity gain-bandwidth (see Figure 3)	$R_L = 10\ k\Omega$, $C_L = 100$ pF		2		MHz
		$R_L = 600\ \Omega$, $C_L = 100$ pF		1.5		
	Settling time	0.1%		5		μs
		0.01%		10		
B_{OM}	Maximum-output-swing bandwidth	$A_{VD} = 1$, $R_L = 10\ k\Omega$		40		kHz
ϕ_m	Phase margin at unity gain (see Figure 3)	$R_L = 10\ k\Omega$, $C_L = 100$ pF		60°		
		$R_L = 600\ \Omega$, $C_L = 100$ pF		70°		

PARAMETER MEASUREMENT INFORMATION



NOTE A: C_L includes fixture capacitance.

Figure 1. Slew Rate Test Circuit

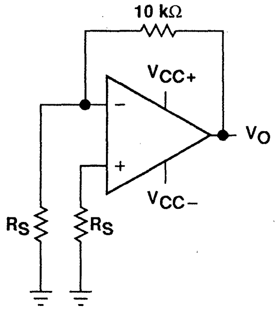
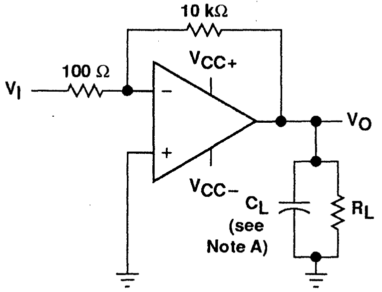


Figure 2. Noise Voltage Test Circuit



NOTE A: C_L includes fixture capacitance.

Figure 3. Unity-Gain Bandwidth and Phase Margin Test Circuit

typical values

Typical values as presented in this data sheet represent the median (50% point) of device parametric performance.

input bias and offset current

At the picoampere bias current level typical of the TLE2064, TLE2064A, and TLE2064B, accurate measurement of the bias current becomes difficult. Not only does this measurement require a picoammeter, but test socket leakages can easily exceed the actual device bias currents. To accurately measure these small currents, Texas Instruments uses a two-step process. The socket leakage is measured using picoammeters with bias voltages applied but with no device in the socket. The device is then inserted into the socket and a second test that measures both the socket leakage and the device input bias current is performed. The two measurements are then subtracted algebraically to determine the bias current of the device.

TYPICAL CHARACTERISTICS

table of graphs

			Figure
V_{IO}	Input offset voltage	Distribution	4
I_{IB}	Input bias current	vs Common-mode voltage	5
		vs Temperature	6
I_{IO}	Input offset current	vs Temperature	6
V_{ICR}	Common-mode input voltage range	vs Temperature	7
V_{OM}	Maximum peak output voltage swing	vs Output current	8, 9
		vs Supply voltage	10, 11, 12
$V_{O(PP)}$	Maximum peak-to-peak output voltage	vs Frequency	13, 14, 15
A_{VD}	Differential voltage amplification	vs Frequency	16
		vs Temperature	17
I_{OS}	Short-circuit output current	vs Time	18
		vs Temperature	19
z_o	Output impedance	vs Frequency	20
CMRR	Common-mode rejection ratio	vs Frequency	21
I_{CC}	Supply current	vs Supply voltage	22
		vs Temperature	23
	Pulse response	Small-signal	24, 25
		Large-signal	26, 27
	Noise voltage (referred to input)	0.1 to 10 Hz	28
V_n	Equivalent input noise voltage	vs Frequency	29
THD	Total harmonic distortion	vs Frequency	30, 31
B_1	Unity-gain bandwidth	vs Supply voltage	32
		vs Temperature	33
ϕ_m	Phase margin	vs Supply voltage	34
		vs Load capacitance	35
		vs Temperature	36
ϕ	Phase shift	vs Frequency	16

TYPICAL CHARACTERISTICS†

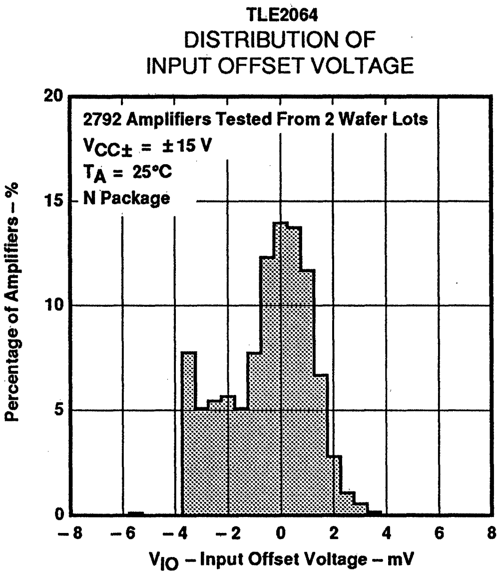


Figure 4

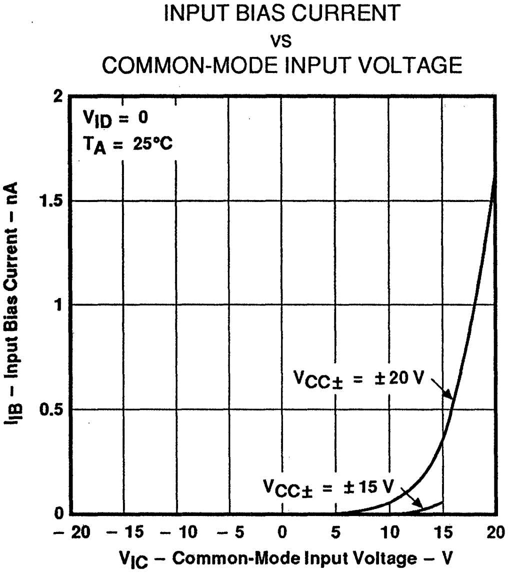


Figure 5

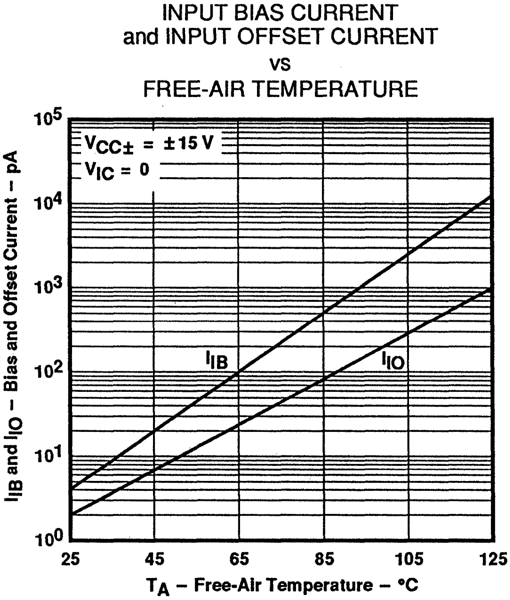


Figure 6

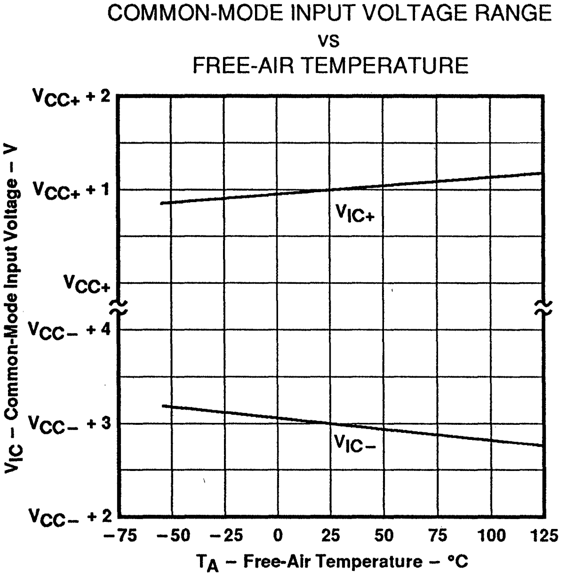


Figure 7

---

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS

MAXIMUM POSITIVE PEAK OUTPUT VOLTAGE
vs
OUTPUT CURRENT

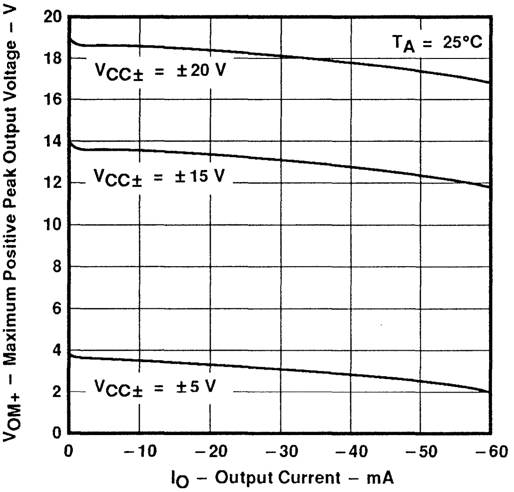


Figure 8

MAXIMUM NEGATIVE PEAK OUTPUT VOLTAGE
vs
OUTPUT CURRENT

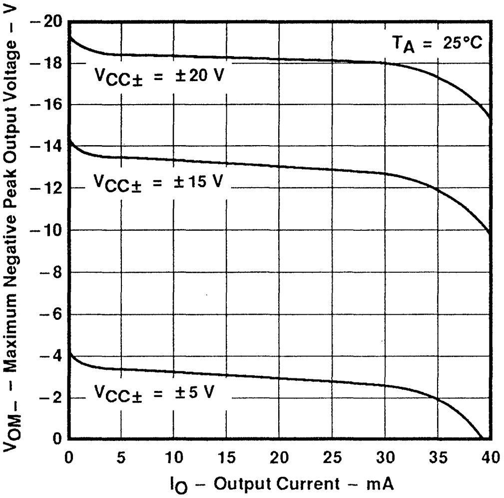


Figure 9

MAXIMUM PEAK OUTPUT VOLTAGE
vs
SUPPLY VOLTAGE

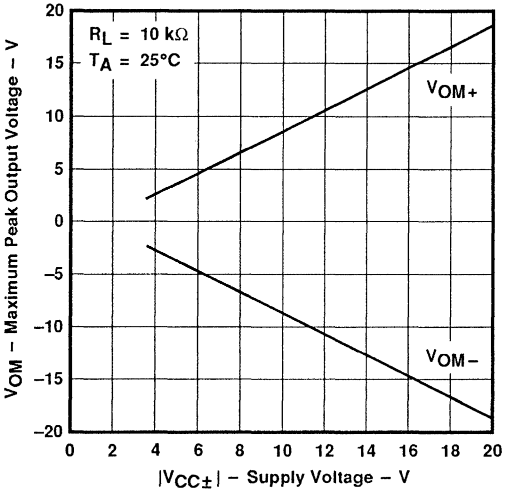


Figure 10

MAXIMUM PEAK OUTPUT VOLTAGE
vs
SUPPLY VOLTAGE

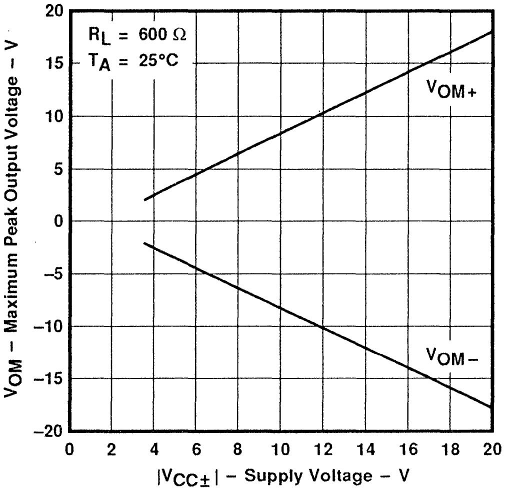


Figure 11

TYPICAL CHARACTERISTICS

MAXIMUM PEAK OUTPUT VOLTAGE
vs
SUPPLY VOLTAGE

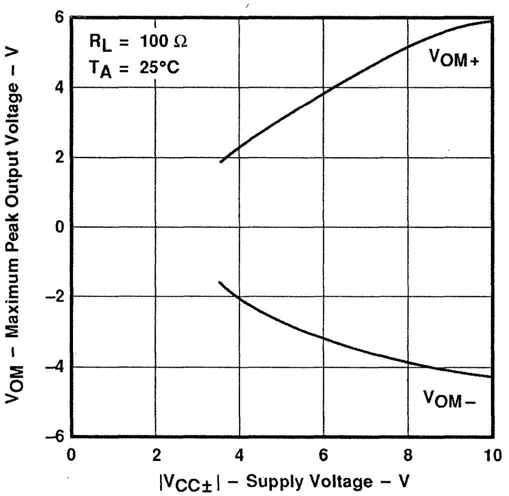


Figure 12

MAXIMUM PEAK-TO-PEAK
OUTPUT VOLTAGE
vs
FREQUENCY

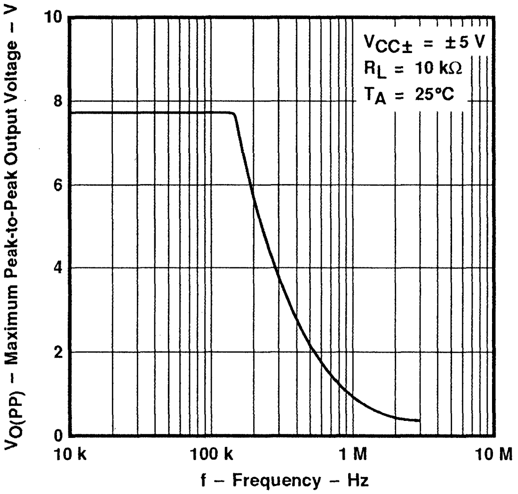


Figure 13

MAXIMUM PEAK-TO-PEAK
OUTPUT VOLTAGE
vs
FREQUENCY

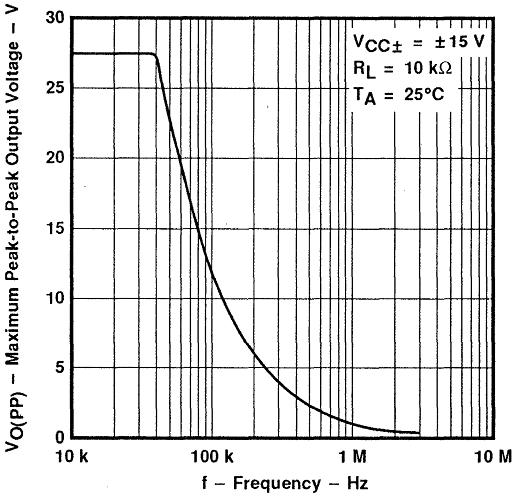


Figure 14

MAXIMUM PEAK-TO-PEAK
OUTPUT VOLTAGE
vs
FREQUENCY

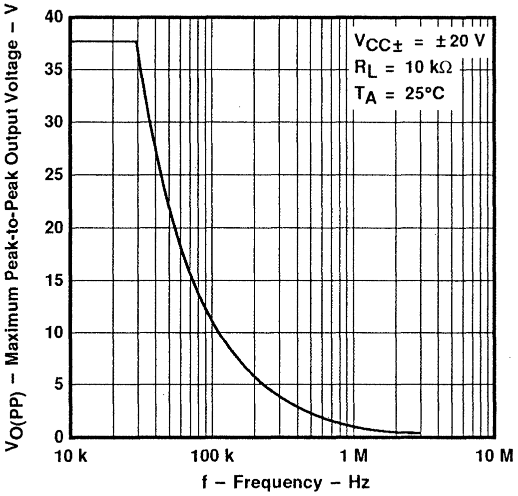


Figure 15

TYPICAL CHARACTERISTICS†

LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION and PHASE SHIFT vs FREQUENCY

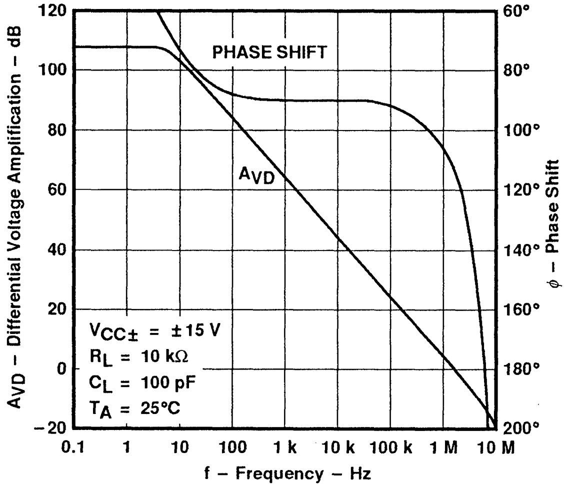


Figure 16

LARGE-SIGNAL VOLTAGE AMPLIFICATION vs FREE-AIR TEMPERATURE

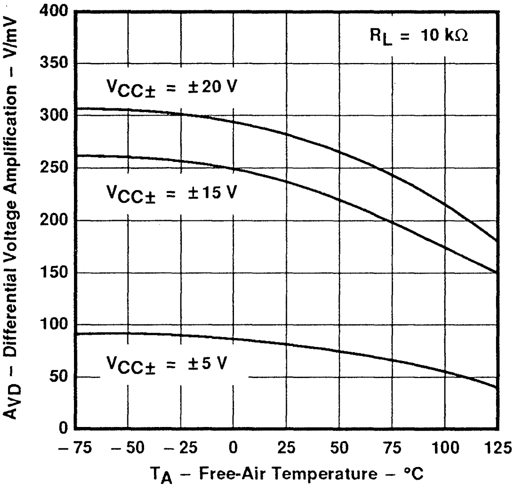


Figure 17

SHORT-CIRCUIT OUTPUT CURRENT vs ELAPSED TIME

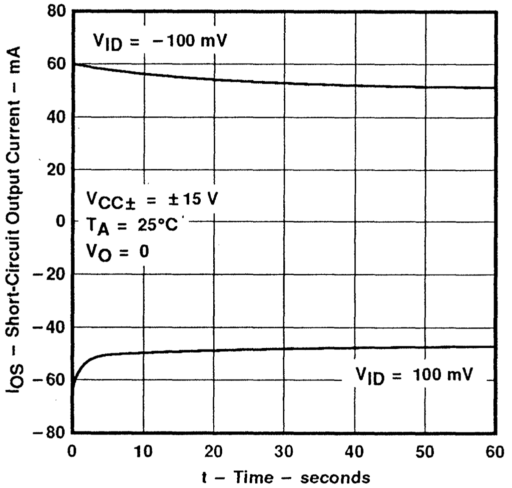


Figure 18

SHORT-CIRCUIT OUTPUT CURRENT vs FREE-AIR TEMPERATURE

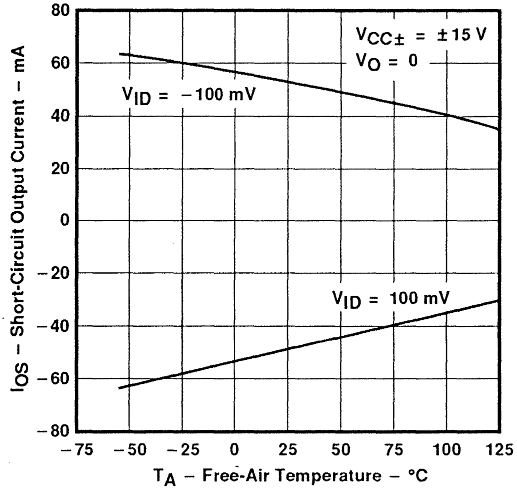


Figure 19

---

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

OUTPUT IMPEDANCE
vs
FREQUENCY

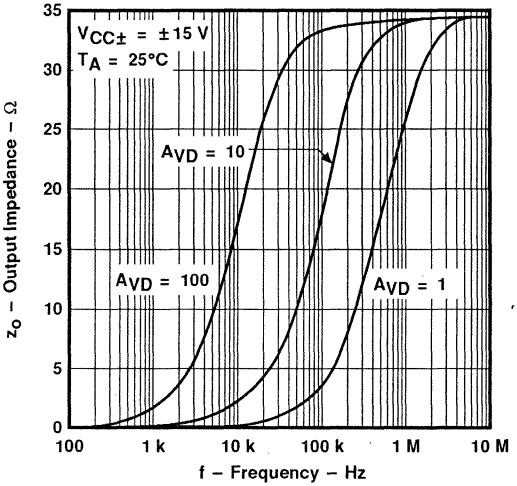


Figure 20

COMMON-MODE REJECTION RATIO
vs
FREQUENCY

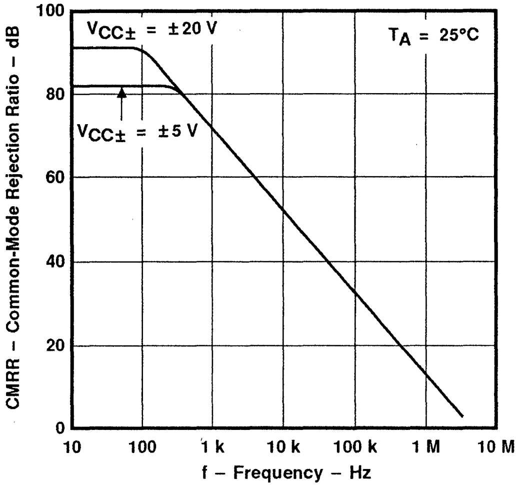


Figure 21

SUPPLY CURRENT
vs
SUPPLY VOLTAGE

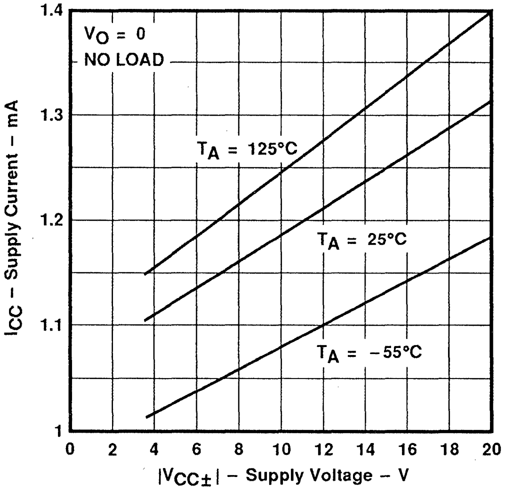


Figure 22

SUPPLY CURRENT
vs
FREE-AIR TEMPERATURE

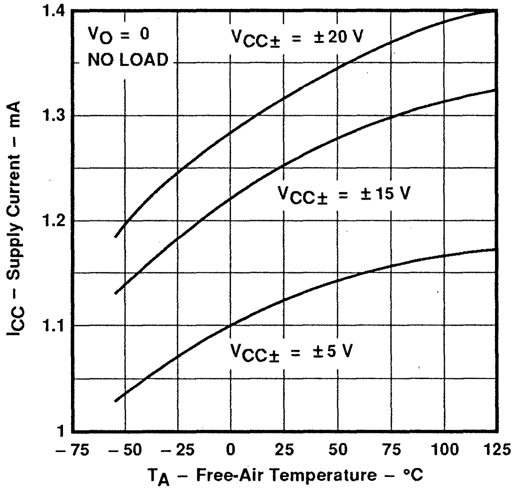


Figure 23

---

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS

VOLTAGE-FOLLOWER
SMALL-SIGNAL
PULSE RESPONSE

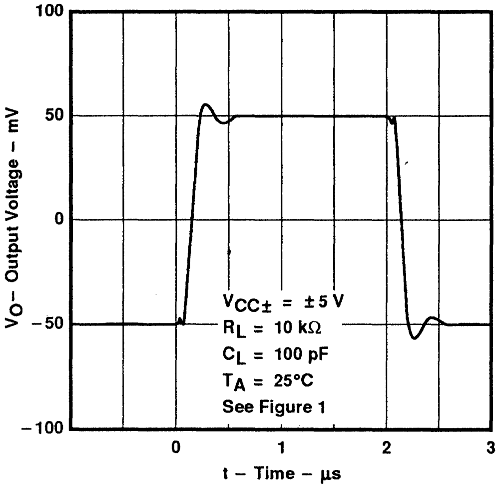


Figure 24

VOLTAGE-FOLLOWER
SMALL-SIGNAL
PULSE RESPONSE

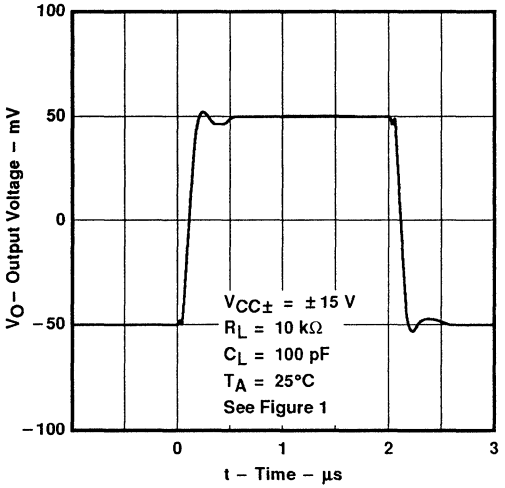


Figure 25

VOLTAGE-FOLLOWER
LARGE-SIGNAL
PULSE RESPONSE

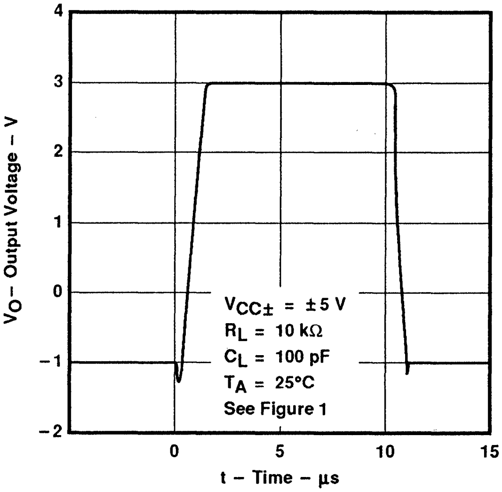


Figure 26

VOLTAGE-FOLLOWER
LARGE-SIGNAL
PULSE RESPONSE

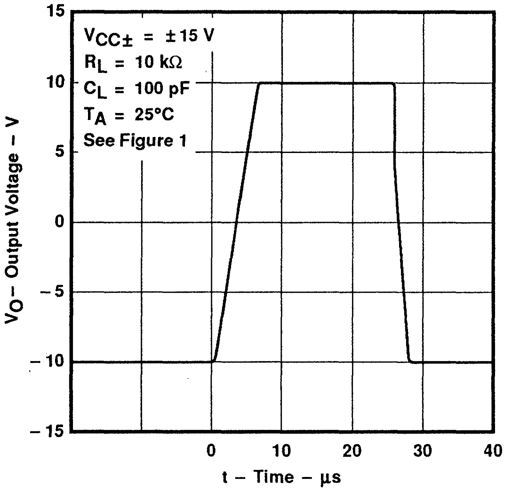


Figure 27

TYPICAL CHARACTERISTICS

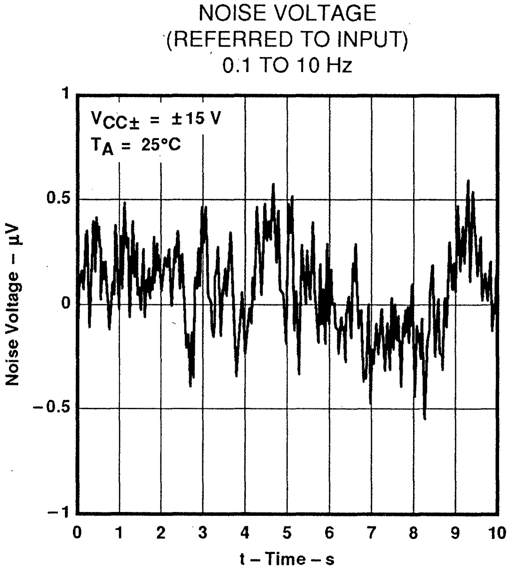


Figure 28

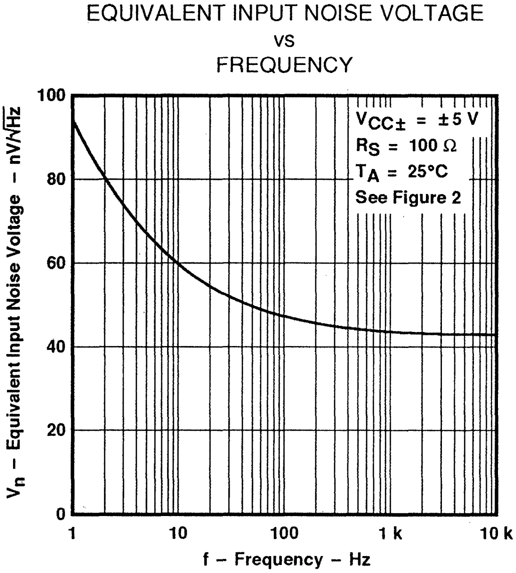


Figure 29

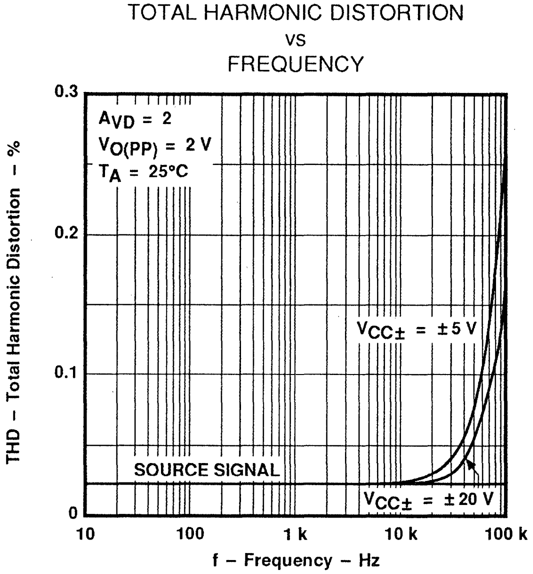


Figure 30

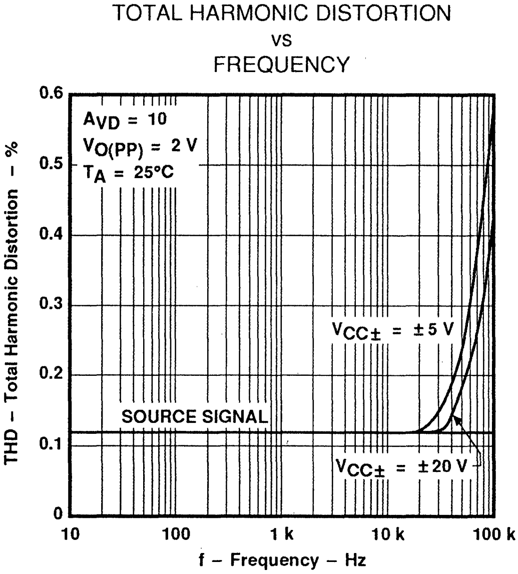


Figure 31

TYPICAL CHARACTERISTICS†

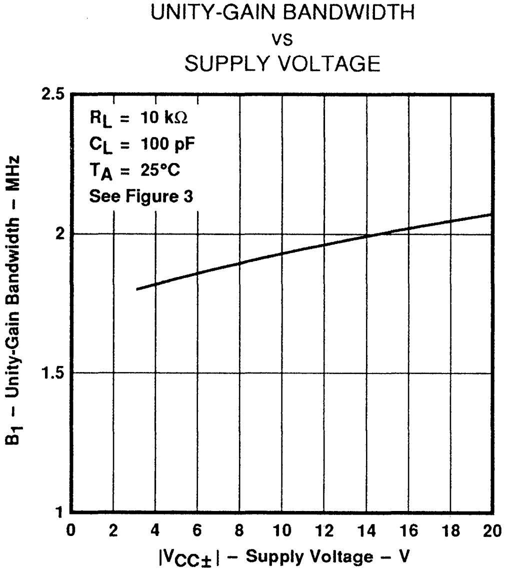


Figure 32

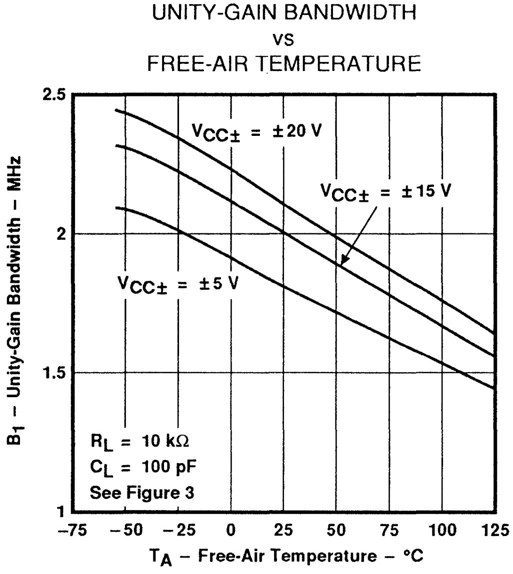


Figure 33

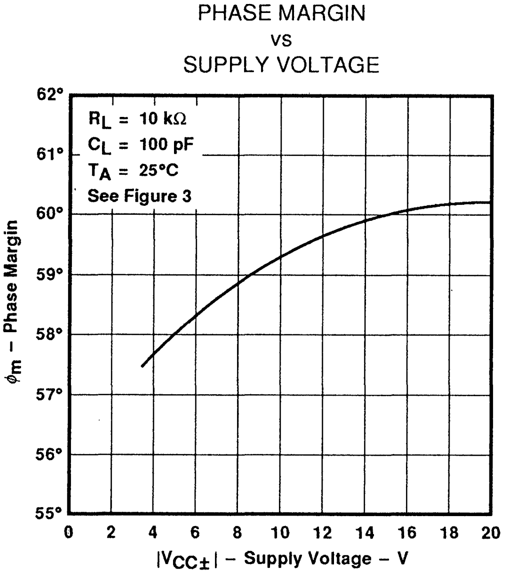


Figure 34

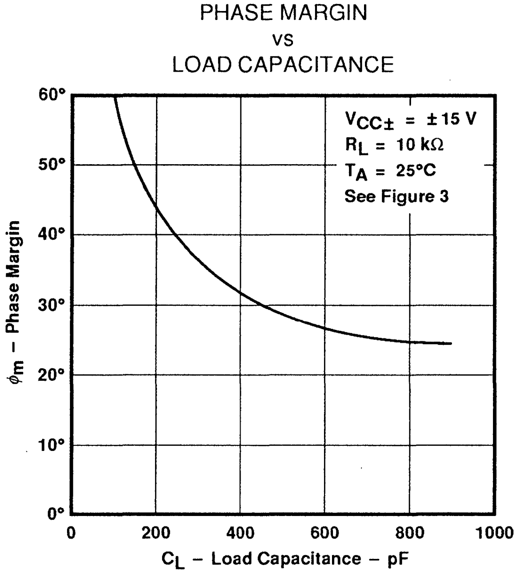


Figure 35

---

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

PHASE MARGIN
vs
FREE-AIR TEMPERATURE

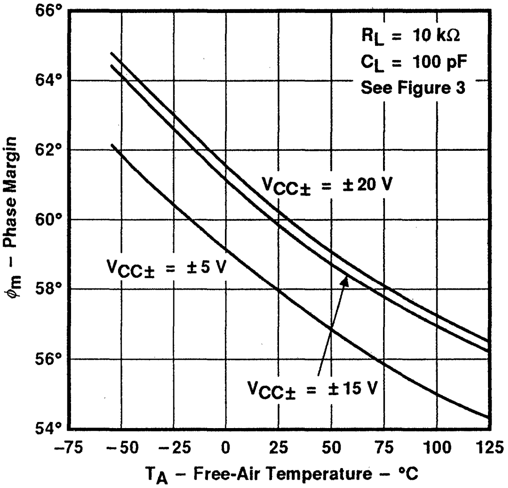


Figure 36

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL APPLICATION DATA

macromodel information

Macromodel information provided was derived using *PSpice*™ *Parts*™ model generation software. The Boyle macromodel (see Note 5) and subcircuit in Figure 37 were generated using the TLE2064 typical electrical and operating characteristics at 25°C. Using this information, output simulations of the following key parameters can be generated to a tolerance of 20% (in most cases):

- Maximum positive output voltage swing
- Maximum negative output voltage swing
- Slew rate
- Quiescent power dissipation
- Input bias current
- Open-loop voltage amplification
- Unity gain frequency
- Common-mode rejection ratio
- Phase margin
- dc output resistance
- ac output resistance
- Short-circuit output current limit

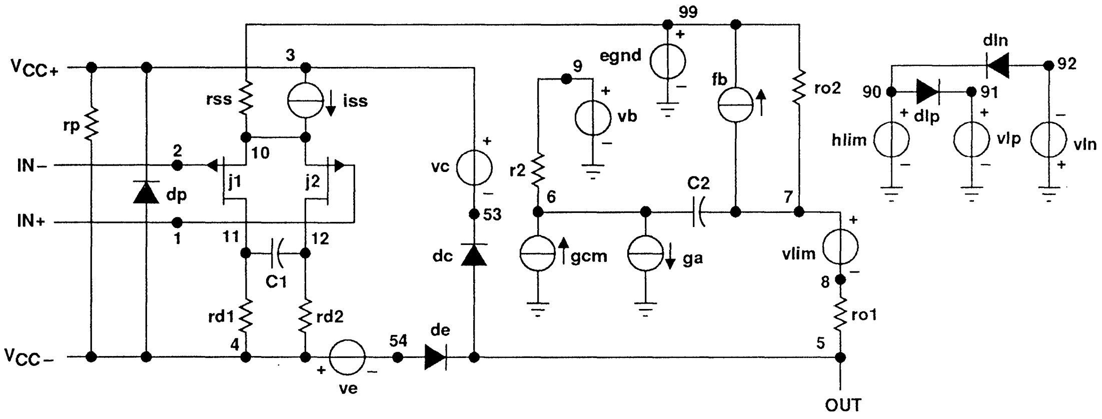
To model the TLE2064, TLE2064A, or TLE2064B, use four macromodels in your simulation.

NOTE 5: G. R. Boyle, B. M. Cohn, D. O. Pederson, and J. E. Solomon, *Macromodeling of Integrated Circuit Operational Amplifiers*, IEEE Journal of Solid-State Circuits, SC-9, 353 (1974).

PSpice and *Parts* are trademarks of MicroSim Corporation.

TYPICAL APPLICATION DATA

macromodel information (continued)



```
.subckt TLE2064  1 2 3 4 5
  c1    11 12 1.457E-12
  c2     6  7 15.00E-12
  dc     5 53 dx
  de    54  5 dx
  dlp   90 91 dx
  dln   92 90 dx
  dp     4  3 dx
  egnd  99  0 poly(2)  (3,0)  (4,0)  0 .5 .5
  fb     7 99 poly(5) vb vc ve vlp vln 0 4.357E6 -4E6 4E6 4E6 -4E6
  ga     6  0 11 12 188.5E-6
  gcm    0  6 10 99 3.352E-9
  iss    3 10 dc 51.00E-6
  hlim  90  0 vlim 1K
  j1    11  2 10 jx
  j2    12  1 10 jx
  r2     6  9 100.0E3
  rd1    4 11 5.305E3
  rd2    4 12 5.305E3
  ro1    8  5 280
  ro2    7 99 280
  rp     3  4 113.2E3
  rss   10 99 3.922E6
  vb     9  0 dc 0
  vc     3 53 dc 2
  ve    54  4 dc 2
  vlim   7  8 dc 0
  vlp   91  0 dc 50
  vln    0 92 dc 50
.model dx D(Is=800.0E-18)
.model jx PJF(Is=2.000E-12 Beta=423E-6 Vto=-1)
.ends
```

Figure 37. Boyle Macromodel and Subcircuit

APPLICATION INFORMATION

input characteristics

The TLE2064, TLE2064A and TLE2064B are specified with a minimum and a maximum input voltage that, if exceeded at either input, could cause the device to malfunction.

Because of the extremely high input impedance and resulting low bias current requirements, the TLE2064, TLE2064A and TLE2064B are well-suited for low-level signal processing; however, leakage currents on printed circuit boards and sockets can easily exceed bias current requirements and cause degradation in system performance. It is a good practice to include guard rings around inputs (see Figure 38). These guards should be driven from a low-impedance source at the same voltage level as the common-mode input.

The inputs of any unused amplifiers should be tied to ground to avoid possible oscillation.

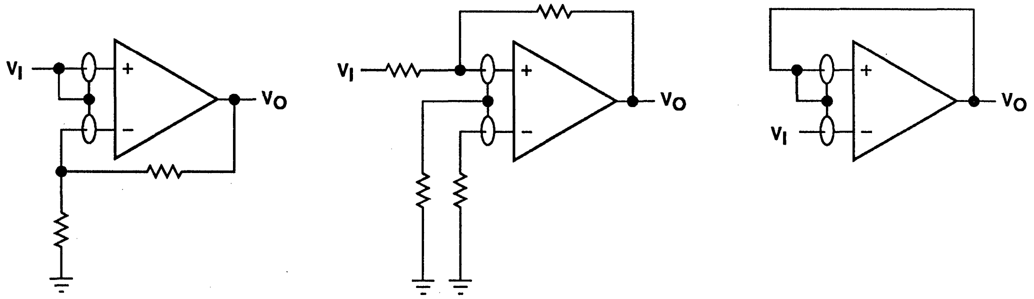


Figure 38. Use of Guard Rings

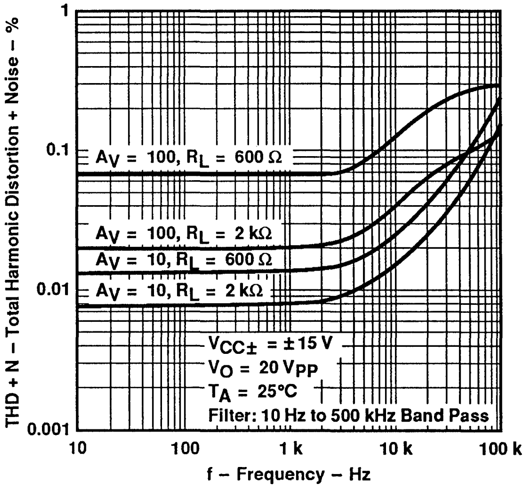
TLE2082, TLE2082A, TLE2082Y
EXCALIBUR HIGH-SPEED
JFET-INPUT DUAL OPERATIONAL AMPLIFIERS

D3958, AUGUST 1991

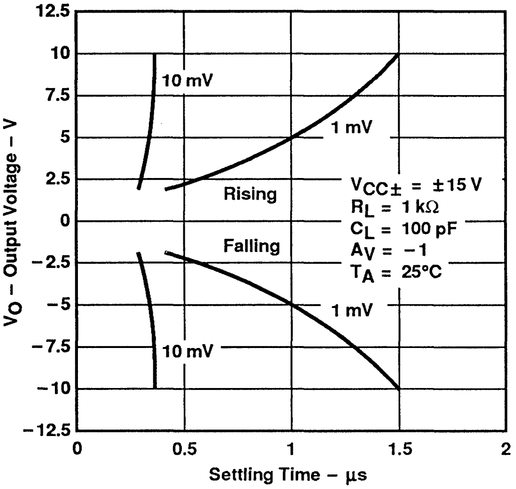
available features

- 40 V/µs Slew Rate Typ
- High-Gain Bandwidth Product . . . 10 MHz
- ±30 mA Minimum Short-Circuit Output Current
- Fast Settling Time . . . 400 ns to 10 mV
  10-V Step Typ . . . . 1.5 µs to 1 mV
- Wide Supply Range . . . ±2.25 V to ±22 V
- Input Range Includes the Positive Supply
- Macromodel Included

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
FREQUENCY



OUTPUT VOLTAGE
vs
SETTLING TIME



description

The TLE2082 and TLE2082A are high-performance, high-speed, internally-compensated JFET-input dual operational amplifiers built using Texas Instruments complementary bipolar Excalibur process. The TLE2082A has a lower input offset voltage than the TLE2082. Both are pin-compatible upgrades to standard industry products.

AVAILABLE OPTIONS

T_A	V_{IO} max AT 25°C	PACKAGE				CHIP FORM (Y)
		SMALL-OUTLINE (D)	CHIP CARRIER (FK)	CERAMIC DIP (JG)	PLASTIC DIP (P)	
0°C to 70°C	4 mV	TLE2082ACD	——	——	TLE2082ACP	TLE2082Y
	7 mV	TLE2082CD	——	——	TLE2082CP	
– 40°C to 85°C	4 mV	TLE2082AID	——	——	TLE2082AIP	
	7 mV	TLE2082ID	——	——	TLE2082IP	
– 55°C to 125°C	4 mV	TLE2082AMD	TLE2082AMFK	TLE2082AMJG	TLE2082AMP	
	7 mV	TLE2082MD	TLE2082MFK	TLE2082MJG	TLE2082MP	

D packages are available taped-and-reeled. Add "R" suffix to device type (e.g., TLE2082ACDR). Chips are tested at T_A = 25°C.

TEXAS INSTRUMENTS
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

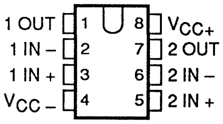
description (continued)

The design features a 30-V/µs minimum slew rate, which results in a high-power bandwidth. Settling time to 0.1% of a 10-V step (1 kΩ /100-pF load) is approximately 400 ns. Gain-bandwidth product is typically 10 MHz with an 8-MHz minimum. As such, the TLE2082 and TLE2082A offer significant speed and noise advantages at a low 1.5-mA typical supply current per channel.

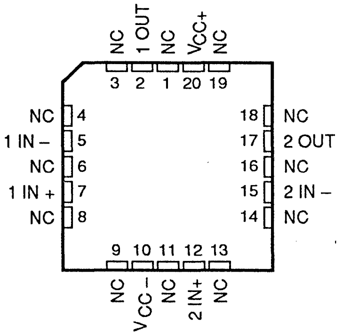
The input current characteristics traditionally associated with JFET-input amplifiers have been maintained. Input offset voltage is graded to a 4-mV maximum. Typically, temperature coefficient of input offset voltage is 2.4 µV/°C and typical CMRR and k_{SVR} are 98 dB and 99 dB, respectively. Device performance is relatively independent of supply voltage over the wide ±2.25-V to ±22-V range. The input common-mode voltage range extends from the positive supply down to $V_{CC-} + 4$ V without significant degradation to dynamic performance. Maximum peak output voltage swing is from $V_{CC+} - 1$ V to $V_{CC-} + 1$ V under light current loading conditions. The output is capable of sourcing and sinking currents internally limited to at least 30 mA and can sustain shorts to either supply. Care must be taken to ensure that maximum power dissipation is not exceeded for long durations.

Both the TLE2082 and TLE2082A are available in a wide variety of packages, including both the industry-standard 8-pin small-outline version and chip form for high density system applications. The C-suffix devices are characterized for operation from 0°C to 70°C, the I-suffix over the −40°C to 85°C range, and the M-suffix over the full military temperature range of −55°C to 125°C.

D, JG, OR P PACKAGE
(TOP VIEW)

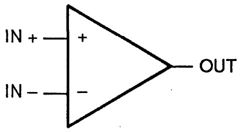


FK PACKAGE
(TOP VIEW)



NC – No internal connection

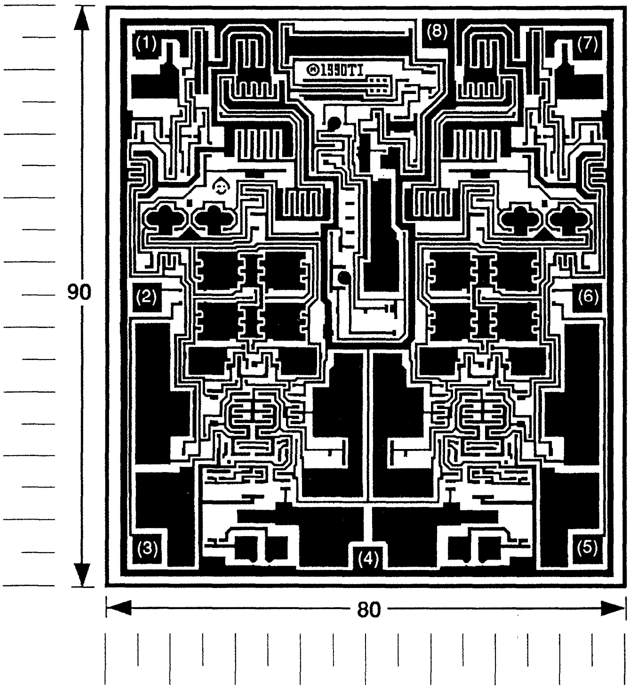
symbol

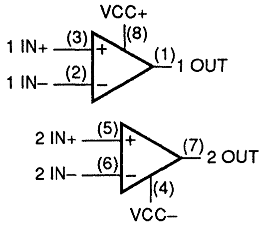


chip information

These chips, properly assembled, display characteristics similar to the TLE2082. Thermal compression or ultrasonic bonding may be used on the doped aluminum bonding pads. Chips may be mounted with conductive epoxy or a gold-silicon preform.

BONDING PAD ASSIGNMENTS





CHIP THICKNESS:
15 TYPICAL

BONDING PADS:
4 X 4 MINIMUM

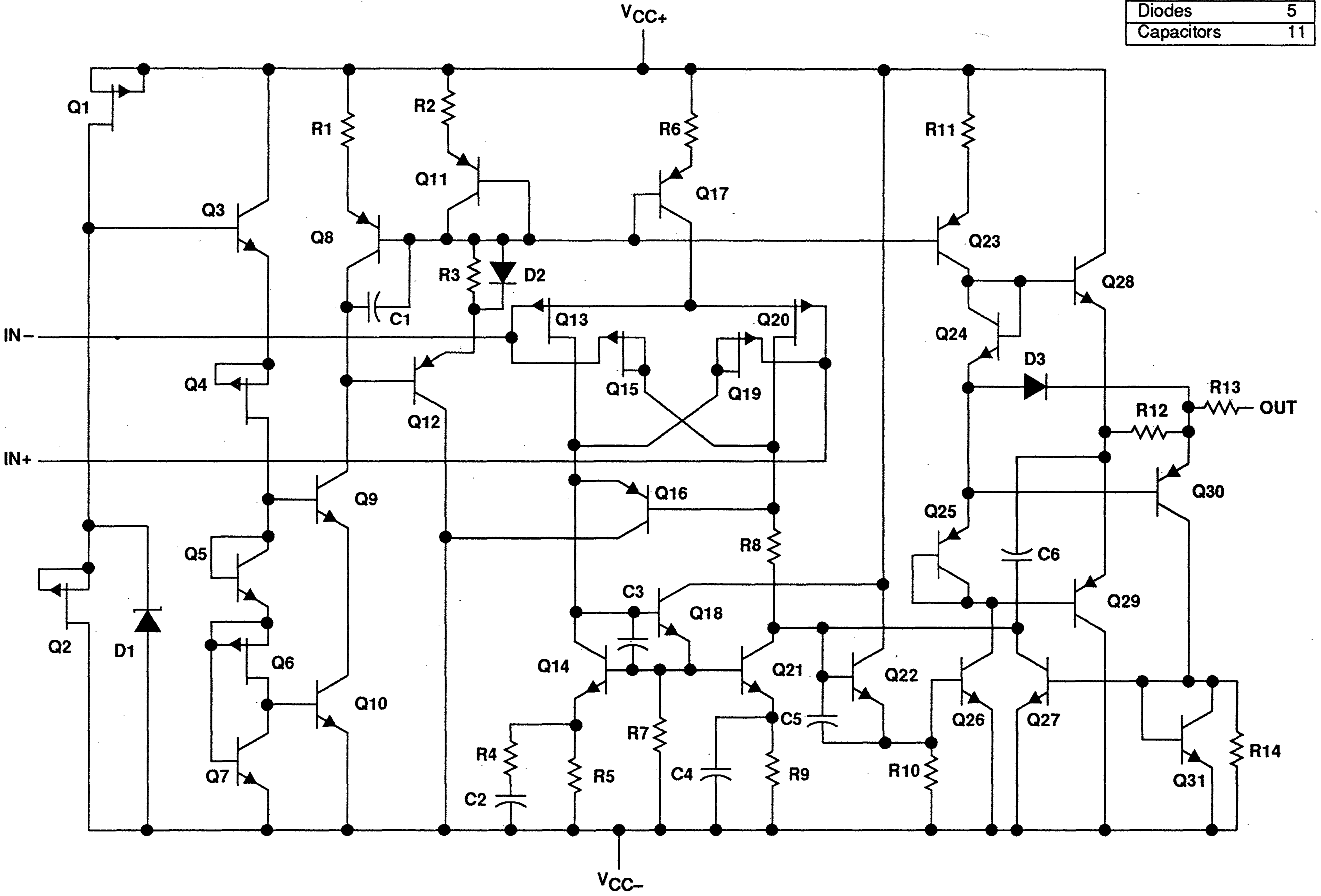
$T_J$max = 150°C

TOLERANCES
ARE ±10%

ALL DIMENSIONS
ARE IN MILS

equivalent schematic (each channel)

ACTUAL DEVICE COMPONENT COUNT	
Transistors	57
Resistors	37
Diodes	5
Capacitors	11



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC+} (see Note 1)	22 V
Supply voltage, V_{CC-} (see Note 1)	−22 V
Differential input voltage range (see Note 2)	V_{CC+} to V_{CC-}
Input voltage range, V_I (any input)	V_{CC+} to V_{CC-}
Input current, I_I (each input)	±1 mA
Output current, I_O (each output)	±80 mA
Total current into V_{CC+} terminal	160 mA
Total current out of V_{CC-} terminal	160 mA
Duration of short-circuit current at (or below) 25°C (see Note 3)	unlimited
Continuous total dissipation	See Dissipation Rating Table
Operating free-air temperature range, T_A: C-suffix	0°C to 70°C
I-suffix	−40°C to 85°C
M-suffix	−55°C to 125°C
Storage temperature range	−65°C to 150°C
Case temperature for 60 seconds: FK package	260°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D or P package	260°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: JG package	300°C

NOTES: 1. All voltage values, except differential voltages, are with respect to the midpoint between V_{CC+} and V_{CC-}.
2. Differential voltages are at the noninverting input with respect to the inverting input.
3. The output may be shorted to either supply. Temperature and/or supply voltages must be limited to ensure that the maximum dissipation rating is not exceeded.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING	$T_A = 125°C$ POWER RATING
D	725 mW	5.8 mW/°C	464 mW	377 mW	145 mW
FK	1375 mW	11.0 mW/°C	880 mW	715 mW	275 mW
JG	1050 mW	8.4 mW/°C	672 mW	546 mW	210 mW
P	1000 mW	8.0 mW/°C	640 mW	344 mW	200 mW

recommended operating conditions

		C-SUFFIX		I-SUFFIX		M-SUFFIX		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
Supply voltage, $V_{CC\pm}$		± 2.25	± 20	± 2.25	± 20	± 2.25	± 20	V
Common-mode input voltage, V_{IC}	$V_{CC\pm} = \pm 5$ V	− 1	5	− 1	5	− 1	5	V
	$V_{CC\pm} = \pm 15$ V	− 11	15	− 11	15	− 11	15	
Input voltage range	$V_{CC\pm} = \pm 5$ V	− 1	5	− 1	5	− 1	5	V
	$V_{CC\pm} = \pm 15$ V	− 11	15	− 11	15	− 11	15	
Operating free-air temperature, T_A		0	70	− 40	85	− 55	125	°C

electrical characteristics at specified free-air temperature, $V_{CC\pm} = \pm 5$ V

PARAMETER		TEST CONDITIONS		T_A†	TLE2082C			TLE2082AC			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	$V_{IC} = 0$, $V_O = 0$, $R_S = 50\ \Omega$		25°C		0.9	7		0.65	4	mV
				Full range			8.1			5.1	
α_{VIO}	Temperature coefficient of input offset voltage			Full range		2.3	25		2.3	25	µV/°C
I_{IO}	Input offset current	$V_{IC} = 0$, $V_O = 0$, See Figure 4		25°C		5	100		5	100	pA
				Full range			350			350	
I_{IB}	Input bias current			25°C		15	175		15	175	pA
				Full range			850			850	
V_{ICR}	Common-mode input voltage range	$R_S = 50\ \Omega$		25°C	5 to −1	5 to −1.9		5 to −1	5 to −1.9		V
				Full range	5 to −0.9			5 to −0.9			
V_{OM+}	Maximum positive peak output voltage swing	$I_O = -200\ \mu A$		25°C	3.8	4.1		3.8	4.1		V
				Full range	3.7			3.7			
		$I_O = -2$ mA		25°C	3.7	3.9		3.7	3.9		
				Full range	3.6			3.6			
		$I_O = -20$ mA		25°C	1.5	2.3		1.5	2.3		
				Full range	1.5			1.5			
V_{OM-}	Maximum negative peak output voltage swing	$I_O = 200\ \mu A$		25°C	−3.8	− 4.2		−3.8	− 4.2		V
				Full range	−3.7			−3.7			
		$I_O = 2$ mA		25°C	−3.7	− 4.1		−3.7	− 4.1		
				Full range	−3.6			−3.6			
		$I_O = 20$ mA		25°C	−1.5	−2.4		−1.5	−2.4		
				Full range	−1.5			−1.5			
A_{VD}	Large-signal differential voltage amplification	$V_O = \pm 2.3$ V	$R_L = 600\ \Omega$	25°C	85	91		85	91		dB
				Full range	84			84			
			$R_L = 2\ k\Omega$	25°C	90	100		90	100		
				Full range	89			89			
			$R_L = 10\ k\Omega$	25°C	95	106		95	106		
				Full range	94			94			
r_i	Input resistance	$V_{IC} = 0$		25°C		10^{12}			10^{12}		Ω
c_i	Input capacitance	$V_{IC} = 0$, See Figure 5	Common mode	25°C		11			11		pF
			Differential	25°C		2.5			2.5		
z_o	Open-loop output impedance	f = 1 MHz		25°C		80			80		Ω
CMRR	Common-mode rejection ratio	$V_{IC} = V_{ICR}$ min, $V_O = 0$, $R_S = 50\ \Omega$		25°C	70	89		70	89		dB
				Full range	68			68			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm} / \Delta V_{IO}$)	$V_{CC\pm} = \pm 5$ V to ± 15 V, $V_O = 0$, $R_S = 50\ \Omega$		25°C	82	99		82	99		dB
				Full range	80			80			
I_{CC}	Supply current (both channels)	$V_O = 0$, No load		25°C	2.7	2.9	3.4	2.7	2.9	3.4	mA
				Full range			3.4			3.4	
a_x	Crosstalk attenuation	$V_{IC} = 0$, $R_L = 2\ k\Omega$		25°C		120			120		dB
I_{OS}	Short-circuit output current	$V_O = 0$	$V_{ID} = 1$ V	25°C		−35			−35		mA
			$V_{ID} = -1$ V			45			45		

†Full range is 0°C to 70°C.

operating characteristics at specified free-air temperature, $V_{CC\pm} = \pm 5$ V

PARAMETER		TEST CONDITIONS		T_A†	TLE2082C			TLE2082AC			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
SR +	Positive slew rate	$V_{O(PP)} = \pm 2.3$ V, $A_{VD} = -1$, $R_L = 2$ kΩ, $C_L = 100$ pF, See Figure 1		25°C		35			35		V/μs
				Full range	23			23			
SR −	Negative slew rate			25°C		38			38		V/μs
				Full range	23			23			
	Settling time	$A_{VD} = -1$, 2-V Step, $R_L = 1$ kΩ, $C_L = 100$ pF	To 10 mV	25°C		0.25			0.25		μs
			To 1 mV			0.4			0.4		
V_n	Equivalent input noise voltage	$R_S = 20$ Ω, See Figure 3	f = 10 Hz	25°C		85			85		nV/√Hz
			f = 10 kHz			13			13		
$V_{n(PP)}$	Peak-to-peak equivalent input noise voltage		f = 10 Hz to 10 kHz	25°C		6			6		μV
			f = 0.1 Hz to 10 Hz			0.6			0.6		
I_n	Equivalent input noise current	$V_{IC} = 0$, f = 10 kHz		25°C		2.8			2.8		fA/√Hz
THD + N	Total harmonic distortion plus noise	$V_{O(PP)} = 5$ V, $A_{VD} = 10$, f = 1 kHz, $R_L = 2$ kΩ, $R_S = 25$ Ω		25°C		0.013%			0.013%		
B_1	Unity gain bandwidth	$V_I = 10$ mV, $R_L = 2$ kΩ, $C_L = 25$ pF, See Figure 2		25°C		9.4			9.4		MHz
B_{OM}	Maximum output-swing bandwidth	$V_{O(PP)} = 4$ V, $A_{VD} = -1$, $R_L = 2$ kΩ, $C_L = 25$ pF		25°C		2.8			2.8		MHz
ϕ_m	Phase margin at unity gain	$V_I = 10$ mV, $R_L = 2$ kΩ, $C_L = 25$ pF, See Figure 2		25°C		56°			56°		

†Full range is 0°C to 70°C.

electrical characteristics at specified free-air temperature, $V_{CC\pm}$ = ± 15 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A†	TLE2082C			TLE2082AC			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_{IC} = 0, V_O = 0, R_S = 50 Ω		25°C		1.1	7		0.7	4	mV
				Full range			8.1			5.1	
α_{VIO}	Temperature coefficient of input offset voltage			Full range		2.4	25		2.4	25	μV/°C
I_{IO}	Input offset current	V_{IC} = 0, V_O = 0, See Figure 4		25°C		6	100		6	100	pA
				Full range			350			350	
I_{IB}	Input bias current			25°C		20	175		20	175	pA
				Full range			900			900	
V_{ICR}	Common-mode input voltage range	R_S = 50 Ω		25°C	15 to −11	15 to −11.9		15 to −11	15 to −11.9		V
				Full range	15 to −10.9			15 to −10.9			
V_{OM+}	Maximum positive peak output voltage swing	I_O = −200 μA		25°C	13.8	14.1		13.8	14.1		V
				Full range	13.7			13.7			
		I_O = −2 mA		25°C	13.7	13.9		13.7	13.9		
				Full range	13.6			13.6			
		I_O = −20 mA		25°C	11.5	12.3		11.5	12.3		
				Full range	11.5			11.5			
V_{OM-}	Maximum negative peak output voltage swing	I_O = 200 μA		25°C	−13.8	−14.2		−13.8	−14.2		V
				Full range	−13.7			−13.7			
		I_O = 2 mA		25°C	−13.7	−14		−13.7	−14		
				Full range	−13.6			−13.6			
		I_O = 20 mA		25°C	−11.5	−12.4		−11.5	−12.4		
				Full range	−11.5			−11.5			
A_{VD}	Large-signal differential voltage amplification	V_O = ± 10 V	R_L = 600 Ω	25°C	85	96		85	96		dB
				Full range	84			84			
			R_L = 2 kΩ	25°C	95	109		95	109		
				Full range	94			94			
			R_L = 10 kΩ	25°C	95	118		95	118		
				Full range	94			94			
r_i	Input resistance	V_{IC} = 0		25°C		10^{12}			10^{12}		Ω
c_i	Input capacitance	V_{IC} = 0, See Figure 5	Common mode	25°C		7.5			7.5		pF
			Differential	25°C		2.5			2.5		
z_o	Open-loop output impedance	f = 1 MHz		25°C		80			80		Ω
CMRR	Common-mode rejection ratio	V_{IC} = V_{ICR} min, V_O = 0, R_S = 50 Ω		25°C	80	98		80	98		dB
				Full range	79			79			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm} / \Delta V_{IO}$)	$V_{CC\pm}$ = ± 5 V to ± 15 V, V_O = 0, R_S = 50 Ω		25°C	82	99		82	99		dB
				Full range	81			81			
I_{CC}	Supply current (both channels)	V_O = 0, No load		25°C	2.7	3.1	3.4	2.7	3.1	3.4	mA
				Full range			3.4			3.4	
a_x	Crosstalk attenuation	V_{IC} = 0, R_L = 2 kΩ		25°C		120			120		dB
I_{OS}	Short-circuit output current	V_O = 0	V_{ID} = 1 V	25°C	−30	− 45		−30	− 45		mA
			V_{ID} = −1 V		30	48		30	48		

† Full range is 0°C to 70°C.

operating characteristics at specified free-air temperature, $V_{CC\pm} = \pm 15$ V

PARAMETER		TEST CONDITIONS		T_A†	TLE2082C			TLE2082AC			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
SR +	Positive slew rate	$V_{O(PP)}$ = 10 V, A_{VD} = −1, R_L = 2 kΩ, C_L = 100 pF, See Figure 1		25°C	30	40		30	40		V/μs
				Full range	27			27			
SR −	Negative slew rate			25°C	30	45		30	45		V/μs
				Full range	27			27			
	Settling time	A_{VD} = −1, 10-V Step, R_L = 1 kΩ, C_L = 100 pF	To 10 mV	25°C		0.4			0.4		μs
			To 1 mV			1.5			1.5		
V_n	Equivalent input noise voltage	R_S = 20 Ω, See Figure 3	f = 10 Hz	25°C		97			97		nV/√Hz
			f = 10 kHz			13.7			13.7		
$V_{n(PP)}$	Peak-to-peak equivalent input noise voltage		f = 10 Hz to 10 kHz	25°C		6			6		μV
			f = 0.1 Hz to 10 Hz			0.6			0.6		
I_n	Equivalent input noise current	V_{IC} = 0, f = 10 kHz		25°C		2.8			2.8		fA/√Hz
THD + N	Total harmonic distortion plus noise	$V_{O(PP)}$ = 20 V, A_{VD} = 10, f = 1 kHz, R_L = 2 kΩ, R_S = 25 Ω		25°C		0.008%			0.008%		
B_1	Unity-gain bandwidth	V_I = 10 mV, R_L = 2 kΩ, C_L = 25 pF, See Figure 2		25°C	8	10		8	10		MHz
B_{OM}	Maximum output-swing bandwidth	$V_{O(PP)}$ = 20 V, A_{VD} = −1, R_L = 2 kΩ, C_L = 25 pF		25°C	478	637		478	637		kHz
ϕ_m	Phase margin at unity gain	V_I = 10 mV, R_L = 2 kΩ, C_L = 25 pF, See Figure 2		25°C		57°			57°		

†Full range is 0°C to 70°C.

electrical characteristics at specified free-air temperature, $V_{CC\pm}$ = ± 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A†	TLE2082I			TLE2082AI			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_{IC} = 0, V_O = 0, R_S = 50 Ω,		25°C		0.9	7		0.65	4	mV
				Full range			8.5			5.5	
α_{VIO}	Temperature coefficient of input offset voltage			Full range		2.4	25		2.4	25	μV/°C
I_{IO}	Input offset current	V_{IC} = 0, V_O = 0, See Figure 4		25°C		5	100		5	100	pA
				Full range			950			950	
I_{IB}	Input bias current			25°C		15	175		15	175	pA
				Full range			2			2	nA
V_{ICR}	Common-mode input voltage range	R_S = 50 Ω		25°C	5 to −1	5 to −1.9		5 to −1	5 to −1.9		V
				Full range	5 to −0.8			5 to −0.8			
V_{OM+}	Maximum positive peak output voltage swing	I_O = −200 μA		25°C	3.8	4.1		3.8	4.1		V
				Full range	3.7			3.7			
		I_O = −2 mA		25°C	3.7	3.9		3.7	3.9		
				Full range	3.6			3.6			
		I_O = −20 mA		25°C	1.5	2.3		1.5	2.3		
				Full range	1.5			1.5			
V_{OM-}	Maximum negative peak output voltage swing	I_O = 200 μA		25°C	−3.8	−4.2		−3.8	−4.2		V
				Full range	−3.7			−3.7			
		I_O = 2 mA		25°C	−3.7	−4.1		−3.7	−4.1		
				Full range	−3.6			−3.6			
		I_O = 20 mA		25°C	−1.5	−2.4		−1.5	−2.4		
				Full range	−1.5			−1.5			
A_{VD}	Large-signal differential voltage amplification	V_O = ± 2.3 V	R_L = 600 Ω	25°C	85	91		85	91		dB
				Full range	84			84			
			R_L = 2 kΩ	25°C	90	100		90	100		
				Full range	89			89			
			R_L = 10 kΩ	25°C	95	106		95	106		
				Full range	94			94			
r_i	Input resistance	V_{IC} = 0		25°C		10^{12}			10^{12}		Ω
c_i	Input capacitance	V_{IC} = 0, See Figure 5	Common mode	25°C		11			11		pF
			Differential	25°C		2.5			2.5		
z_o	Open-loop output impedance	f = 1 MHz		25°C		80			80		Ω
CMRR	Common-mode rejection ratio	V_{IC} = V_{ICR} min, V_O = 0, R_S = 50 Ω		25°C	70	89		70	89		dB
				Full range	68			68			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm} / \Delta V_{IO}$)	$V_{CC\pm}$ = ± 5 V to ± 15 V, V_O = 0, R_S = 50 Ω		25°C	82	99		82	99		dB
				Full range	80			80			
I_{CC}	Supply current (both channels)	V_O = 0, No load		25°C	2.7	2.9	3.4	2.7	2.9	3.4	mA
				Full range			3.4			3.4	
a_x	Crosstalk attenuation	V_{IC} = 0, R_L = 2 kΩ		25°C		120			120		dB
I_{OS}	Short-circuit output current	V_O = 0	V_{ID} = 1 V	25°C		−35			−35		mA
			V_{ID} = −1 V			45			45		

†Full range is – 40°C to 85°C.

operating characteristics at specified free-air temperature, $V_{CC\pm}$ = ±5 V

PARAMETER		TEST CONDITIONS		T_A†	TLE2082I			TLE2082AI			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
SR+	Positive slew rate	$V_{O(PP)}$ = ±2.3 V, A_{VD} = −1, R_L = 2 kΩ, C_L = 100 pF, See Figure 1		25°C		35			35		V/µs
				Full range	22			22			
SR−	Negative slew rate			25°C		38			38		V/µs
				Full range	22			22			
	Settling time	A_{VD} = −1, 2-V Step, R_L = 1 kΩ, C_L = 100 pF	To 10 mV	25°C		0.25			0.25		µs
			To 1 mV			0.4			0.4		
V_n	Equivalent input noise voltage	R_S = 20 Ω, See Figure 3	f = 10 Hz	25°C		85			85		nV/√Hz
			f = 10 kHz			13			13		
$V_{n(PP)}$	Peak-to-peak equivalent input noise voltage		f = 10 Hz to 10 kHz	25°C		6			6		µV
			f = 0.1 Hz to 10 Hz			0.6			0.6		
I_n	Equivalent input noise current	V_{IC} = 0, f = 10 kHz		25°C		2.8			2.8		fA/√Hz
THD + N	Total harmonic distortion plus noise	$V_{O(PP)}$ = 5 V, A_{VD} = 10, f = 1 kHz, R_L = 2 kΩ, R_S = 25 Ω		25°C		0.013%			0.013%		
B_1	Unity-gain bandwidth	V_I = 10 mV, R_L = 2 kΩ, C_L = 25 pF, See Figure 2		25°C		9.4			9.4		MHz
B_{OM}	Maximum output-swing bandwidth	$V_{O(PP)}$ = 4 V, A_{VD} = −1, R_L = 2 kΩ, C_L = 25 pF		25°C		2.8			2.8		MHz
ϕ_m	Phase margin at unity gain	V_I = 10 mV, R_L = 2 kΩ, C_L = 25 pF, See Figure 2		25°C		56°			56°		

† Full range is – 40°C to 85°C.

electrical characteristics at specified free-air temperature, $V_{CC\pm}$ = ±15 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A†	TLE2082I			TLE2082AI			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_{IC} = 0, V_O = 0, R_S = 50 Ω,		25°C		1.1	7		0.7	4	mV
				Full range			8.5			5.5	
α_{VIO}	Temperature coefficient of input offset voltage			Full range		2.4	25		2.4	25	μV/°C
I_{IO}	Input offset current	V_{IC} = 0, V_O = 0, See Figure 4		25°C		6	100		6	100	pA
				Full range			950			950	
I_{IB}	Input bias current			25°C		20	175		20	175	pA
				Full range			2.5			2.5	nA
V_{ICR}	Common-mode input voltage range	R_S = 50 Ω		25°C	15 to −11	15 to −11.9		15 to −11	15 to −11.9		V
				Full range	15 to −10.8			15 to −10.8			
V_{OM+}	Maximum positive peak output voltage swing	I_O = −200 μA		25°C	13.8	14.1		13.8	14.1		V
				Full range	13.7			13.7			
		I_O = −2 mA		25°C	13.7	13.9		13.7	13.9		
				Full range	13.6			13.6			
		I_O = −20 mA		25°C	11.5	12.3		11.5	12.3		
				Full range	11.5			11.5			
V_{OM-}	Maximum negative peak output voltage swing	I_O = 200 μA		25°C	−13.8	−14.2		−13.8	−14.2		V
				Full range	−13.7			−13.7			
		I_O = 2 mA		25°C	−13.7	−14		−13.7	−14		
				Full range	−13.6			−13.6			
		I_O = 20 mA		25°C	−11.5	−12.4		−11.5	−12.4		
				Full range	−11.5			−11.5			
A_{VD}	Large-signal differential voltage amplification	V_O = ± 10 V	R_L = 600 Ω	25°C	85	96		85	96		dB
				Full range	83			83			
			R_L = 2 kΩ	25°C	95	109		95	109		
				Full range	94			94			
			R_L = 10 kΩ	25°C	95	118		95	118		
				Full range	94			94			
r_i	Input resistance	V_{IC} = 0		25°C		10^{12}			10^{12}		Ω
c_i	Input capacitance	V_{IC} = 0, See Figure 5	Common mode	25°C		7.5			7.5		pF
			Differential	25°C		2.5			2.5		
z_o	Open-loop output impedance	f = 1 MHz		25°C		80			80		Ω
CMRR	Common-mode rejection ratio	V_{IC} = V_{ICR} min, V_O = 0, R_S = 50 Ω		25°C	80	98		80	98		dB
				Full range	79			79			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm} / \Delta V_{IO}$)	$V_{CC\pm}$ = ±5 V to ±15 V, V_O = 0, R_S = 50 Ω		25°C	82	99		82	99		dB
				Full range	80			80			
I_{CC}	Supply current (both channels)	V_O = 0, No load		25°C	2.7	3.1	3.4	2.7	3.1	3.4	mA
				Full range			3.4			3.4	
a_x	Crosstalk attenuation	V_{IC} = 0, R_L = 2 kΩ		25°C		120			120		dB
I_{OS}	Short-circuit output current	V_O = 0	V_{ID} = 1 V	25°C	−30	−45		−30	−45		mA
			V_{ID} = −1 V		30	48		30	48		

†Full range is – 40°C to 85°C.

operating characteristics at specified free-air temperature, $V_{CC\pm}$ = ±15 V

PARAMETER		TEST CONDITIONS		T_A†	TLE2082I			TLE2082AI			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
SR+	Positive slew rate	$V_{O(PP)}$ = 10 V, A_{VD} = −1, R_L = 2 kΩ, C_L = 100 pF, See Figure 1		25°C	30	40		30	40		V/μs
				Full range	24			24			
SR−	Negative slew rate			25°C	30	45		30	45		V/μs
				Full range	24			24			
	Settling time	A_{VD} = −1, 10-V Step, R_L = 1 kΩ, C_L = 100 pF	To 10 mV	25°C		0.4			0.4		μs
			To 1 mV			1.5			1.5		
V_n	Equivalent input noise voltage	R_S = 20 Ω, See Figure 3	f = 10 Hz	25°C		97			97		nV/√Hz
			f = 10 kHz			13.7			13.7		
$V_{n(PP)}$	Peak-to-peak equivalent input noise voltage		f = 10 Hz to 10 kHz	25°C		6			6		μV
			f = 0.1 Hz to 10 Hz			0.6			0.6		
I_n	Equivalent input noise current	V_{IC} = 0, f = 10 kHz		25°C		2.8			2.8		fA/√Hz
THD + N	Total harmonic distortion plus noise	$V_{O(PP)}$ = 20 V, A_{VD} = 10, f = 1 kHz, R_L = 2 kΩ, R_S = 25 Ω		25°C		0.008%			0.008%		
B_1	Unity-gain bandwidth	V_I = 10 mV, R_L = 2 kΩ, C_L = 25 pF, See Figure 2		25°C	8	10		8	10		MHz
B_{OM}	Maximum output-swing bandwidth	$V_{O(PP)}$ = 20 V, A_{VD} = −1, R_L = 2 kΩ, C_L = 25 pF		25°C	478	637		478	637		kHz
ϕ_m	Phase margin at unity gain	V_I = 10 mV, R_L = 2 kΩ, C_L = 25 pF, See Figure 2		25°C		57°			57°		

†Full range is −40°C to 85°C.

electrical characteristics at specified free-air temperature, $V_{CC\pm} = \pm 5$ V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A†	TLE2082M			TLE2082AM			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	$V_{IC} = 0$, $V_O = 0$, $R_S = 50\ \Omega$,		25°C		0.9	7		0.65	4	mV
				Full range			9.5			6.5	
α_{VIO}	Temperature coefficient of input offset voltage			Full range		2.3	25*		2.3	25*	µV/°C
I_{IO}	Input offset current	$V_{IC} = 0$, $V_O = 0$, See Figure 4		25°C		5	100		5	100	pA
				Full range			7.5			7.5	nA
I_{IB}	Input bias current			25°C		15	175		15	175	pA
				Full range			60			60	nA
V_{ICR}	Common-mode input voltage range	$R_S = 50\ \Omega$		25°C	5 to −1	5 to −1.9		5 to −1	5 to −1.9		V
				Full range	5 to −0.8			5 to −0.8			
V_{OM+}	Maximum positive peak output voltage swing	$I_O = -200\ \mu A$		25°C	3.8	4.1		3.8	4.1		V
				Full range	3.6			3.6			
		$I_O = -2$ mA		25°C	3.7	3.9		3.7	3.9		
				Full range	3.5			3.5			
		$I_O = -20$ mA		25°C	1.5	2.3		1.5	2.3		
				Full range	1.4			1.4			
V_{OM-}	Maximum negative peak output voltage swing	$I_O = 200\ \mu A$		25°C	−3.8	−4.2		−3.8	−4.2		V
				Full range	−3.6			−3.6			
		$I_O = 2$ mA		25°C	−3.7	−4.1		−3.7	−4.1		
				Full range	−3.5			−3.5			
		$I_O = 20$ mA		25°C	−1.5	−2.4		−1.5	−2.4		
				Full range	−1.4			−1.4			
A_{VD}	Large-signal differential voltage amplification	$V_O = \pm 2.3$ V	$R_L = 600\ \Omega$	25°C	85	91		85	91		dB
				Full range	83			83			
			$R_L = 2\ k\Omega$	25°C	90	100		90	100		
				Full range	88			88			
			$R_L = 10\ k\Omega$	25°C	95	106		95	106		
				Full range	93			93			
r_i	Input resistance	$V_{IC} = 0$		25°C		10^{12}			10^{12}		Ω
c_i	Input capacitance	$V_{IC} = 0$, See Figure 5	Common mode	25°C		11			11		pF
			Differential	25°C		2.5			2.5		
z_o	Open-loop output impedance	f = 1 MHz		25°C		80			80		Ω
CMRR	Common-mode rejection ratio	$V_{IC} = V_{ICR}$ min, $V_O = 0$, $R_S = 50\ \Omega$		25°C	70	89		70	89		dB
				Full range	68			68			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm} / \Delta V_{IO}$)	$V_{CC\pm} = \pm 5$ V to ± 15 V, $V_O = 0$, $R_S = 50\ \Omega$		25°C	82	99		82	99		dB
				Full range	80			80			
I_{CC}	Supply current (both channels)	$V_O = 0$, No load		25°C	2.7	2.9	3.4	2.7	2.9	3.4	mA
				Full range			3.4			3.4	
a_x	Crosstalk attenuation	$V_{IC} = 0$, $R_L = 2\ k\Omega$		25°C		120			120		dB
I_{OS}	Short-circuit output current	$V_O = 0$	$V_{ID} = 1$ V	25°C		−35			−35		mA
			$V_{ID} = -1$ V			45			45		

*On products compliant to MIL-STD-883, Class B, this parameter is not production tested.
†Full range is −55°C to 125°C.

operating characteristics at specified free-air temperature, $V_{CC\pm}$ = ±5 V

PARAMETER		TEST CONDITIONS		T_A†	TLE2082M			TLE2082AM			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
SR+	Positive slew rate	$V_{O(PP)}$ = ± 2.3 V, A_{VD} = − 1, R_L = 2 kΩ, C_L = 100 pF, See Figure 1		25°C		35			35		V/μs
				Full range	20			20			
SR−	Negative slew rate			25°C		38			38		V/μs
				Full range	20			20			
	Settling time	A_{VD} = − 1, 2-V Step, R_L = 1 kΩ, C_L = 100 pF	To 10 mV	25°C		0.25			0.25		μs
			To 1 mV			0.4			0.4		
V_n	Equivalent input noise voltage	R_S = 20 Ω, See Figure 3	f = 10 Hz	25°C		85			85		nV/√Hz
			f = 10 kHz			13			13		
$V_{n(PP)}$	Peak-to-peak equivalent input noise voltage		f = 10 Hz to 10 kHz	25°C		6			6		μV
			f = 0.1 Hz to 10 Hz			0.6			0.6		
I_n	Equivalent input noise current	V_{IC} = 0, f = 10 kHz		25°C		2.8			2.8		fA/√Hz
THD + N	Total harmonic distortion plus noise	$V_{O(PP)}$ = 5 V, A_{VD} = 10, f = 1 kHz, R_L = 2 kΩ, R_S = 25 Ω		25°C		0.013%			0.013%		
B_1	Unity-gain bandwidth	V_I = 10 mV, R_L = 2 kΩ, C_L = 25 pF, See Figure 2		25°C		9.4*			9.4*		MHz
B_{OM}	Maximum output-swing bandwidth	$V_{O(PP)}$ = 4 V, A_{VD} = −1, R_L = 2 kΩ, C_L = 25 pF		25°C		2.8*			2.8*		MHz
ϕ_m	Phase margin at unity gain	V_I = 10 mV, R_L = 2 kΩ, C_L = 25 pF, See Figure 2		25°C		56°			56°		

*On products compliant to MIL-STD-883, Class B, this parameter is not production tested.
†Full range is −55°C to 125°C.

electrical characteristics at specified free-air temperature, $V_{CC\pm} = \pm 15$ V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A†	TLE2082M			TLE2082AM			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	$V_{IC} = 0$, $V_O = 0$, $R_S = 50\ \Omega$,		25°C		1.1	7		0.7	4	mV
				Full range			9.5			6.5	
α_{VIO}	Temperature coefficient of input offset voltage			Full range		2.4	25*		2.4	25*	μV/°C
I_{IO}	Input offset current	$V_{IC} = 0$, $V_O = 0$, See Figure 4		25°C		6	100		6	100	pA
				Full range			7.5			7.5	nA
I_{IB}	Input bias current			25°C		20	175		20	175	pA
				Full range			65			65	nA
V_{ICR}	Common-mode input voltage range	$R_S = 50\ \Omega$		25°C	15 to −11	15 to −11.9		15 to −11	15 to −11.9		V
				Full range	15 to −10.8			15 to −10.8			
V_{OM+}	Maximum positive peak output voltage swing	$I_O = -200\ \mu A$		25°C	13.8	14.1		13.8	14.1		V
				Full range	13.6			13.6			
		$I_O = -2$ mA		25°C	13.7	13.9		13.7	13.9		
				Full range	13.5			13.5			
		$I_O = -20$ mA		25°C	11.5	12.3		11.5	12.3		
				Full range	11.4			11.4			
V_{OM-}	Maximum negative peak output voltage swing	$I_O = 200\ \mu A$		25°C	−13.8	−14.2		−13.8	−14.2		V
				Full range	−13.6			−13.6			
		$I_O = 2$ mA		25°C	−13.7	−14		−13.7	−14		
				Full range	−13.5			−13.5			
		$I_O = 20$ mA		25°C	−11.5	−12.4		−11.5	−12.4		
				Full range	−11.4			−11.4			
A_{VD}	Large-signal differential voltage amplification	$V_O = \pm 10$ V	$R_L = 600\ \Omega$	25°C	85	96		85	96		dB
				Full range	83			83			
			$R_L = 2\ k\Omega$	25°C	95	109		95	109		
				Full range	93			93			
			$R_L = 10\ k\Omega$	25°C	95	118		95	118		
				Full range	93			93			
r_i	Input resistance	$V_{IC} = 0$		25°C		10^{12}			10^{12}		Ω
c_i	Input capacitance	$V_{IC} = 0$, See Figure 5	Common mode	25°C		7.5			7.5		pF
			Differential	25°C		2.5			2.5		
z_o	Open-loop output impedance	f = 1 MHz		25°C		80			80		Ω
CMRR	Common-mode rejection ratio	$V_{IC} = V_{ICR}$ min, $V_O = 0$, $R_S = 50\ \Omega$		25°C	80	98		80	98		dB
				Full range	78			78			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm} / \Delta V_{IO}$)	$V_{CC\pm} = \pm 5$ V to ± 15 V, $V_O = 0$, $R_S = 50\ \Omega$		25°C	82	99		82	99		dB
				Full range	80			80			
I_{CC}	Supply current (both channels)	$V_O = 0$, No load		25°C	2.7	3.1	3.4	2.7	3.1	3.4	mA
				Full range			3.4			3.4	
a_x	Crosstalk attenuation	$V_{IC} = 0$, $R_L = 2\ k\Omega$		25°C		120			120		dB
I_{OS}	Short-circuit output current	$V_O = 0$	$V_{ID} = 1$ V	25°C	−30	−45		−30	−45		mA
			$V_{ID} = -1$ V		30	48		30	48		

*On products compliant to MIL-STD-883, Class B, this parameter is not production tested.
†Full range is −55°C to 125°C.

operating characteristics at specified free-air temperature, $V_{CC\pm}$ = ±15 V

PARAMETER		TEST CONDITIONS		T_A†	TLE2082M			TLE2082AM			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
SR+	Positive slew rate	$V_{O(PP)}$ = 10 V, A_{VD} = −1, R_L = 2 kΩ, C_L = 100 pF, See Figure 1		25°C	30	40		30	40		V/µs
				Full range	22			22			
SR−	Negative slew rate			25°C	30	45		30	45		V/µs
				Full range	22			22			
	Settling time	A_{VD} = −1, 10-V Step, R_L = 1 kΩ, C_L = 100 pF	To 10 mV	25°C		0.4			0.4		µs
			To 1 mV			1.5			1.5		
V_n	Equivalent input noise voltage	R_S = 20 Ω, See Figure 3	f = 10 Hz	25°C		97			97		nV/√Hz
			f = 10 kHz			13.7			13.7		
$V_{n(PP)}$	Peak-to-peak equivalent input noise voltage		f = 10 Hz to 10 kHz	25°C		6			6		µV
			f = 0.1 Hz to 10 Hz			0.6			0.6		
I_n	Equivalent input noise current	V_{IC} = 0, f = 10 kHz		25°C		2.8			2.8		fA/√Hz
THD + N	Total harmonic distortion plus noise	$V_{O(PP)}$ = 20 V, A_{VD} = 10, f = 1 kHz, R_L = 2 kΩ, R_S = 25 Ω		25°C		0.008%			0.008%		
B_1	Unity-gain bandwidth	V_I = 10 mV, R_L = 2 kΩ, C_L = 25 pF, See Figure 2		25°C	8*	10		8*	10		MHz
B_{OM}	Maximum output-swing bandwidth	$V_{O(PP)}$ = 20 V, A_{VD} = −1, R_L = 2 kΩ, C_L = 25 pF		25°C	478*	637		478*	637		kHz
ϕ_m	Phase margin at unity gain	V_I = 10 mV, R_L = 2 kΩ, C_L = 25 pF, See Figure 2		25°C		57°			57°		

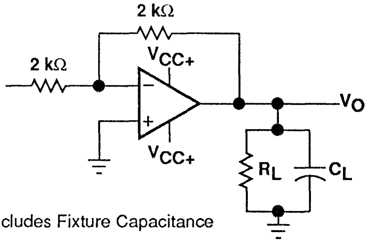
*On products compliant to MIL-STD-883, Class B, this parameter is not production tested.

†Full range is −55°C to 125°C.

electrical characteristics at $V_{CC\pm}$ = ±15 V, T_A = 25°C (unless otherwise noted)

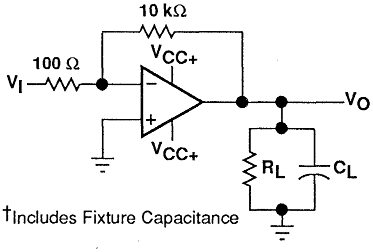
PARAMETER		TEST CONDITIONS		TLE2082Y			UNIT
				MIN	TYP	MAX	
V_{IO}	Input offset voltage	$V_{IC} = 0$, $V_O = 0$, $R_S = 50\ \Omega$			1.1	7	mV
I_{IO}	Input offset current	$V_{IC} = 0$, $V_O = 0$, See Figure 4			6	100	pA
I_{IB}	Input bias current				20	175	pA
V_{ICR}	Common-mode input voltage range	$R_S = 50\ \Omega$		15 to −11	15 to 11.9		V
V_{OM+}	Maximum positive peak output voltage swing	$I_O = -200\ \mu A$		13.8	14.1		V
		$I_O = -2$ mA		13.7	13.9		
		$I_O = -20$ mA		11.5	12.3		
V_{OM-}	Maximum negative peak output voltage swing	$I_O = 200\ \mu A$		−13.8	−14.2		V
		$I_O = 2$ mA		−13.7	−14		
		$I_O = 20$ mA		−11.5	−12.4		
A_{VD}	Large-signal differential voltage amplification	$V_O = \pm 10$ V	$R_L = 600\ \Omega$	85	96		dB
			$R_L = 2\ k\Omega$	95	109		
			$R_L = 10\ k\Omega$	95	118		
r_i	Input resistance	$V_{IC} = 0$			10^{12}		Ω
c_i	Input capacitance	$V_{IC} = 0$, See Fig. 5	Common mode		7.5		pF
			Differential		2.5		
z_o	Open-loop output impedance	f = 1 MHz			80		Ω
CMRR	Common-mode rejection ratio	$V_{IC} = V_{ICR}$ min, $V_O = 0$, $R_S = 50\ \Omega$		80	98		dB
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm} / \Delta V_{IO}$)	$V_{CC\pm} = \pm 5$ V to ±15 V, $V_O = 0$, $R_S = 50\ \Omega$		82	99		dB
I_{CC}	Supply current (both channels)	$V_O = 0$, No load		2.7	3.1	3.4	mA
I_{OS}	Short-circuit output current	$V_O = 0$	$V_{ID} = 1$ V	−30	−45		mA
			$V_{ID} = -1$ V	30	48		

PARAMETER MEASUREMENT INFORMATION



†Includes Fixture Capacitance

Figure 1. Slew Rate



†Includes Fixture Capacitance

Figure 2. Unity-Gain Bandwidth and Phase Margin Test Circuit

PARAMETER MEASUREMENT INFORMATION

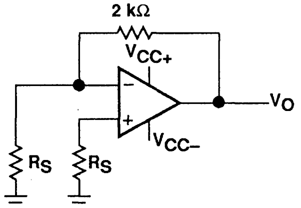


Figure 3. Noise Voltage Test Circuit

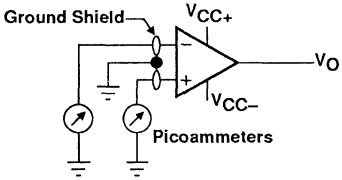
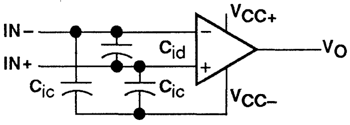


Figure 4. Input Bias and Offset Current Test Circuit



(Common Mode and Differential)

Figure 5. Internal Input Capacitance

typical values

Typical values presented in this data sheet represent the median (50% point) of device parametric performance.

input bias and offset current

At the picoampere bias current level typical of the TLE2082 and TLE2082A, accurate measurement of the bias becomes difficult. Not only does this measurement require a picoammeter, but test socket leakages can easily exceed the actual device bias currents. To accurately measure these small currents, Texas Instruments uses a two-step process. The socket leakage is measured using picoammeters with bias voltages applied, but with no device in the socket. The device is then inserted in the socket and a second test is performed that measures both the socket leakage and the device input bias current. The two measurements are then subtracted algebraically to determine the bias current of the device.

TYPICAL CHARACTERISTICS

table of graphs

			FIGURE #
V_{IO}	Input offset voltage	Distribution	6
αV_{IO}	Temperature coefficient of input offset voltage	Distribution	7
I_{IO}	Input offset current	vs Temperature	8,9
I_{IB}	Input bias current	vs Temperature	8,9
		vs V_{CC}	10
V_{ICR}	Common-mode input voltage range	vs Temperature	11
V_{ID}	Differential input voltage	vs Output voltage	12,13
V_{OM+}	Maximum positive peak output voltage	vs Output current	14
		vs Temperature	16,17
		vs V_{CC}	18
V_{OM-}	Maximum negative peak output voltage	vs Output current	15
		vs Temperature	16,17
		vs V_{CC}	18
$V_{O(PP)}$	Maximum peak-to-peak output voltage swing	vs Frequency	19
V_O	Output voltage	vs Settling time	20
A_{VD}	Differential voltage amplification	vs R_L	21
		vs Temperature	22,23
		vs Frequency	24
z_o	Output impedance	vs Frequency	25
CMRR	Common-mode rejection ratio	vs Frequency	26
		vs Temperature	27
k_{SVR}	Supply-voltage rejection ratio	vs Frequency	28
		vs Temperature	29
I_{CC}	Supply current	vs Supply voltage	30
		vs Temperature	31
		vs Differential input voltage	32,33
I_{OS}	Short-circuit output current	vs V_{CC}	34
		vs Time	35
		vs Temperature	36
SR	Slew rate	vs Temperature	37,38
		vs R_L	39
		vs Differential input voltage	40
V_n	Input-referred noise voltage	vs Frequency	41
		vs Noise bandwidth	42
		Over a 10-second time interval	43
	Third-octave spectral noise density	vs Frequency	44
THD + N	Total harmonic distortion plus noise	vs Frequency	45,46
B_1	Unity-gain bandwidth	vs Load capacitance	47
GBWP	Gain bandwidth product	vs Temperature	48
		vs V_{CC}	49
A_m	Gain margin	vs Load capacitance	50
ϕ_m	Phase margin	vs Temperature	51
		vs V_{CC}	52
		vs Load capacitance	53
ϕ	Phase shift	vs Frequency	24
	Large-signal pulse response, noninverting	vs Time	54
	Small-signal pulse response	vs Time	55
		vs Frequency	56
a_x	Crosstalk attenuation	vs Frequency	57

TYPICAL CHARACTERISTICS†

DISTRIBUTION OF TLE2082 INPUT OFFSET VOLTAGE

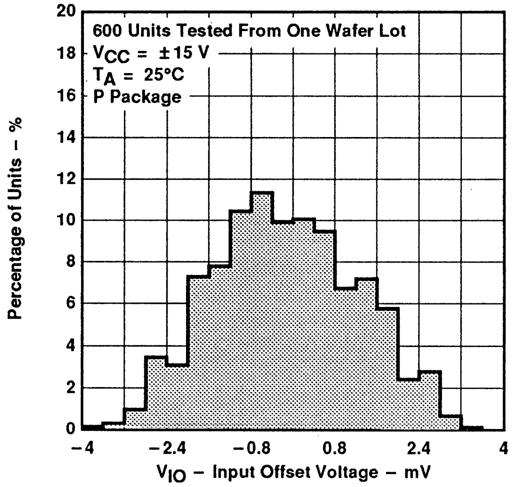


Figure 6

DISTRIBUTION OF TLE2082 INPUT OFFSET VOLTAGE TEMPERATURE COEFFICIENT

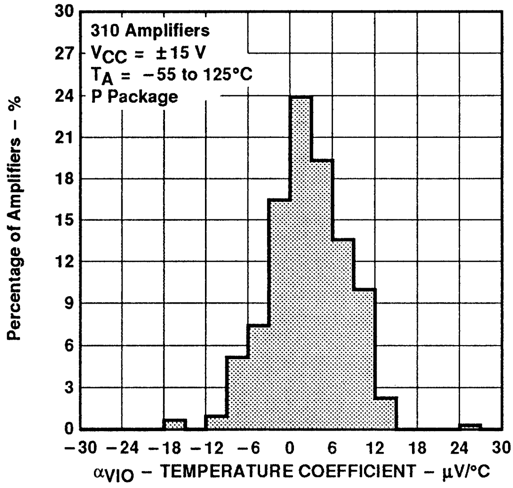


Figure 7

INPUT BIAS CURRENT AND INPUT OFFSET CURRENT vs FREE-AIR TEMPERATURE

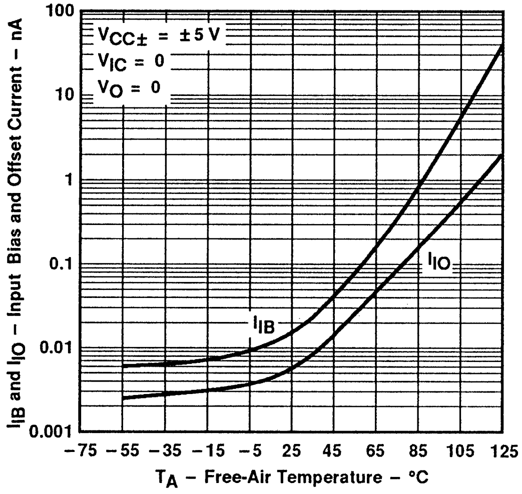


Figure 8

INPUT BIAS CURRENT AND OFFSET CURRENT vs FREE-AIR TEMPERATURE

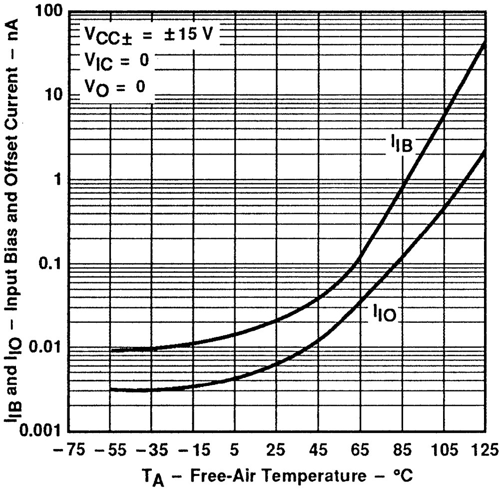


Figure 9

---

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

INPUT BIAS CURRENT
vs
SUPPLY VOLTAGE

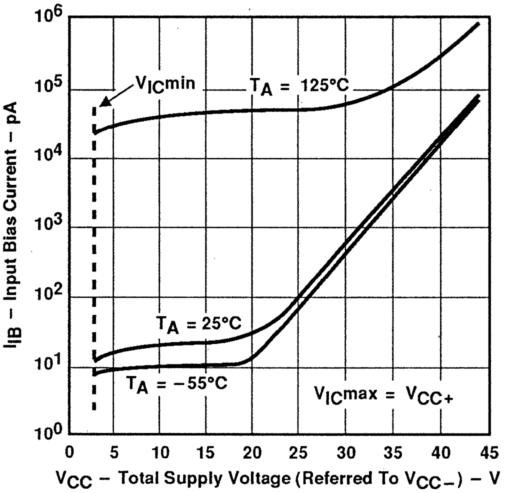


Figure 10

COMMON-MODE INPUT VOLTAGE RANGE
vs
TEMPERATURE

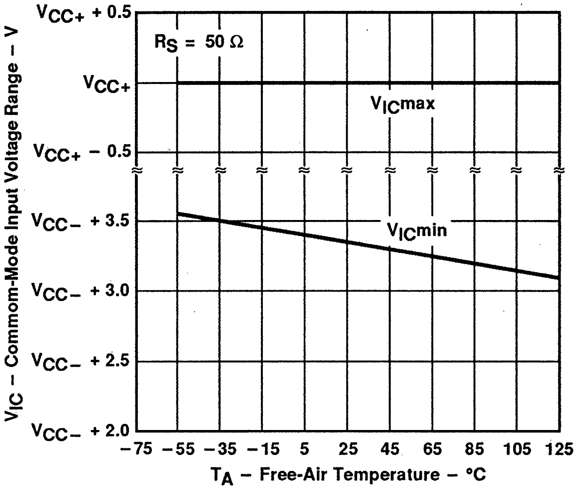


Figure 11

DIFFERENTIAL INPUT VOLTAGE
vs
OUTPUT VOLTAGE

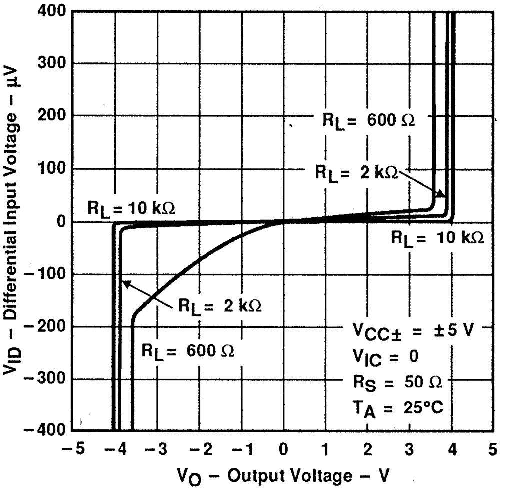


Figure 12

DIFFERENTIAL INPUT VOLTAGE
vs
OUTPUT VOLTAGE

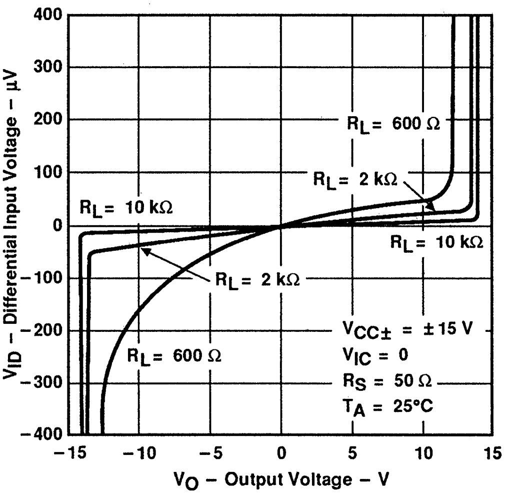


Figure 13

---

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

MAXIMUM POSITIVE PEAK OUTPUT VOLTAGE vs OUTPUT CURRENT

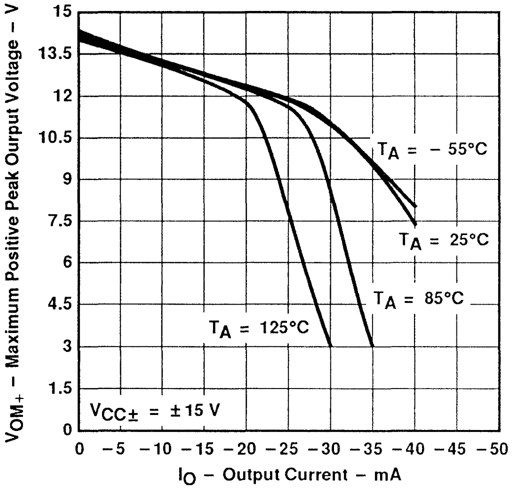


Figure 14

MAXIMUM NEGATIVE PEAK OUTPUT VOLTAGE vs OUTPUT CURRENT

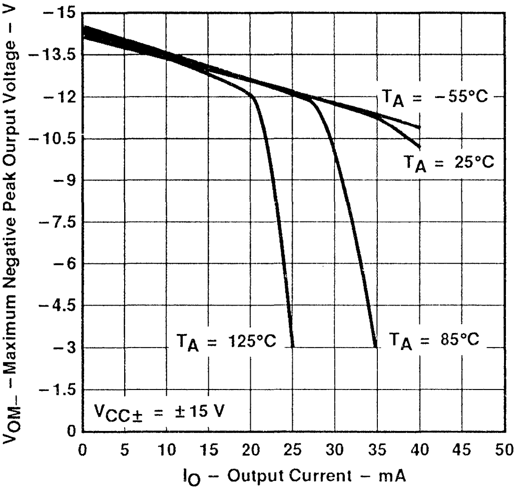


Figure 15

MAXIMUM PEAK OUTPUT VOLTAGE vs FREE-AIR TEMPERATURE

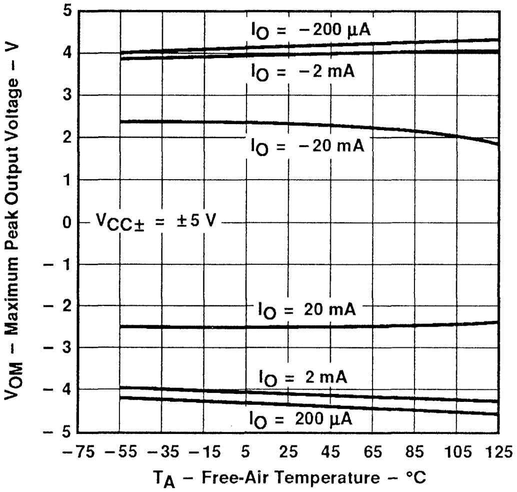


Figure 16

MAXIMUM PEAK OUTPUT VOLTAGE vs FREE-AIR TEMPERATURE

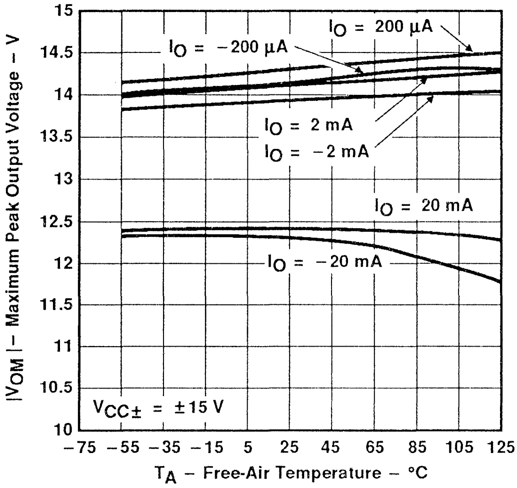


Figure 17

---

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

MAXIMUM PEAK OUTPUT VOLTAGE
vs
SUPPLY VOLTAGE

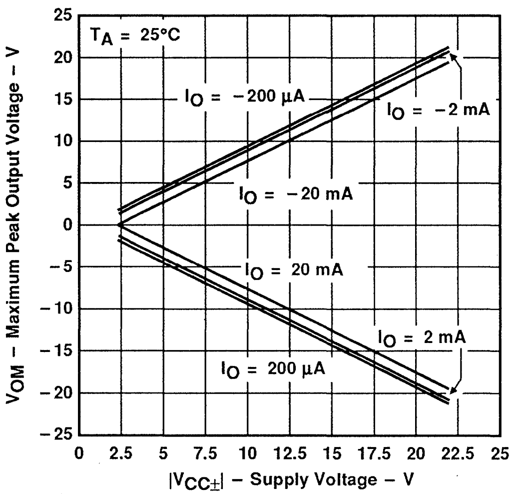


Figure 18

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE
vs
FREQUENCY

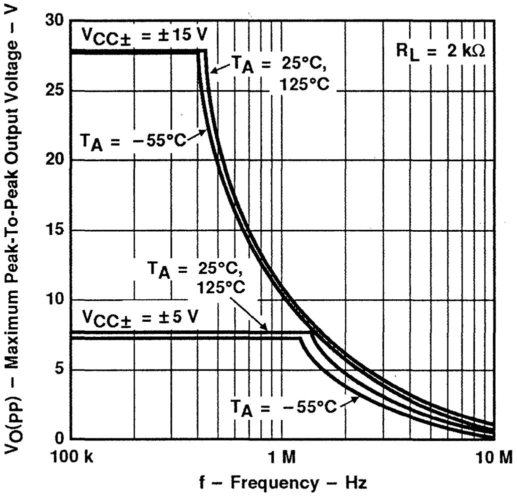


Figure 19

OUTPUT VOLTAGE
vs
SETTLING TIME

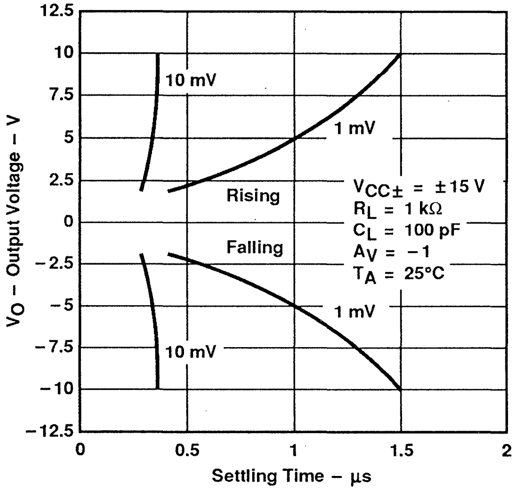


Figure 20

LARGE-SIGNAL DIFFERENTIAL
VOLTAGE AMPLIFICATION
vs
LOAD RESISTANCE

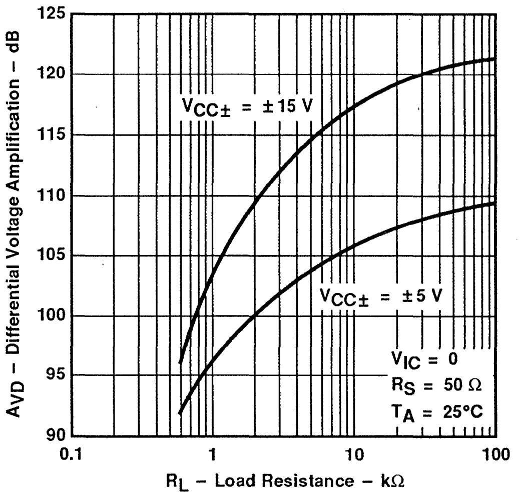


Figure 21

---

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION vs FREE-AIR TEMPERATURE

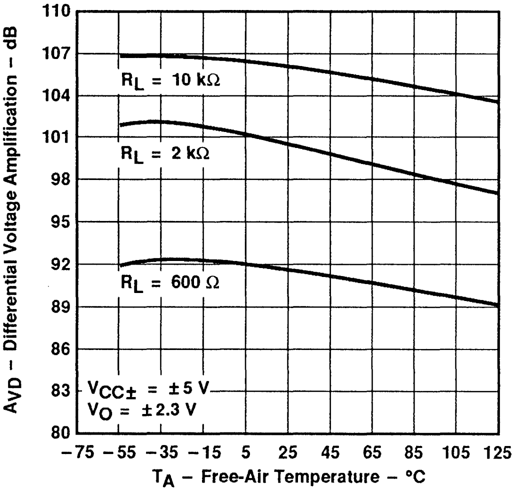


Figure 22

LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION vs FREE-AIR TEMPERATURE

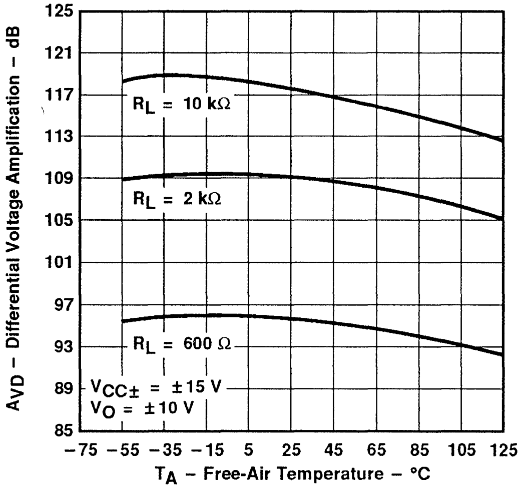


Figure 23

SMALL-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION AND PHASE SHIFT vs FREQUENCY

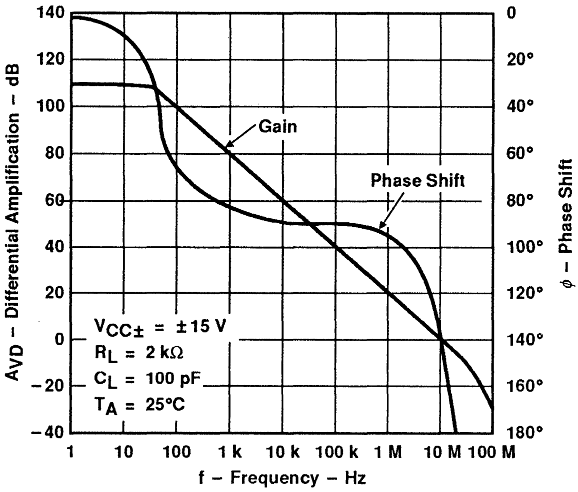


Figure 24

CLOSED-LOOP OUTPUT IMPEDANCE vs FREQUENCY

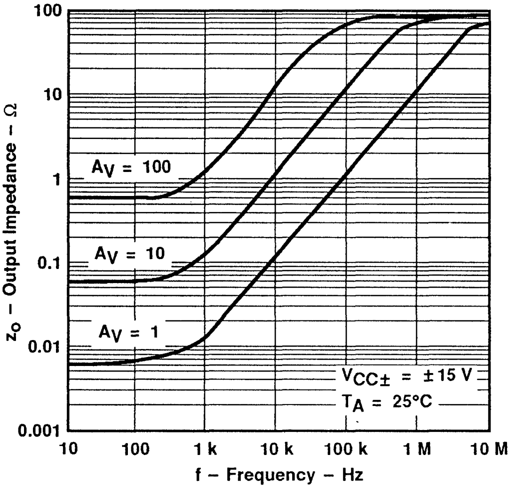


Figure 25

---

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

COMMON-MODE REJECTION RATIO vs FREQUENCY

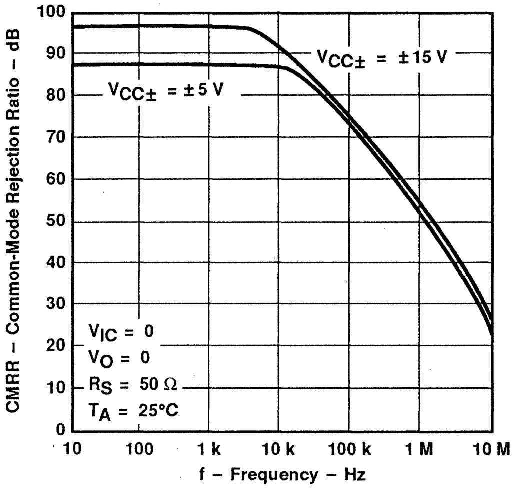


Figure 26

COMMON-MODE REJECTION RATIO vs FREE-AIR TEMPERATURE

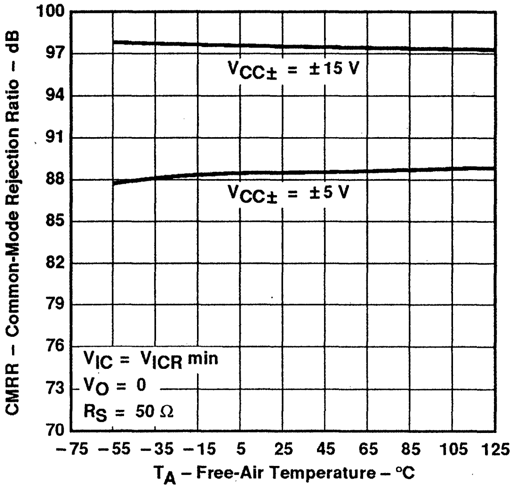


Figure 27

SUPPLY-VOLTAGE REJECTION RATIO vs FREQUENCY

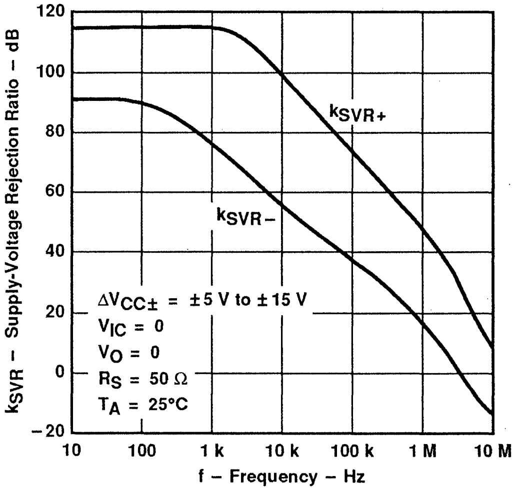


Figure 28

SUPPLY-VOLTAGE REJECTION RATIO vs FREE-AIR TEMPERATURE

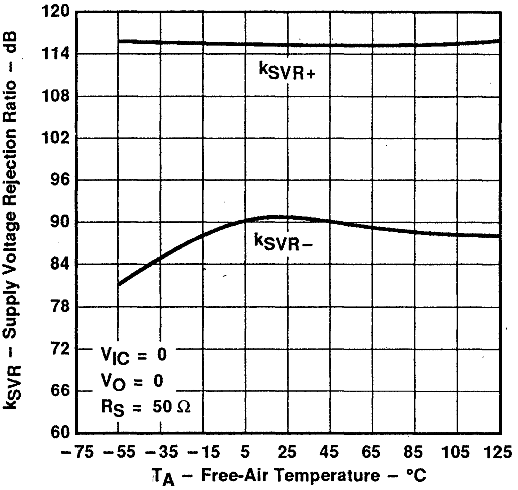


Figure 29

---

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS[†]

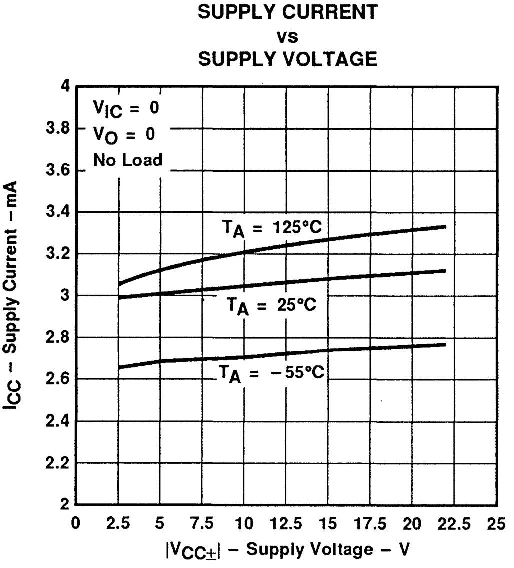


Figure 30

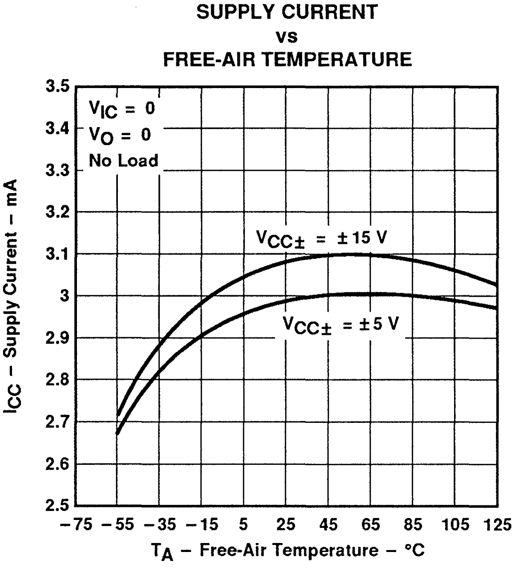


Figure 31

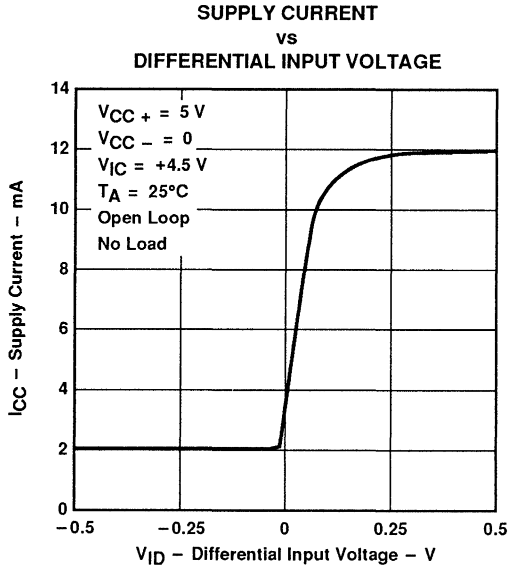


Figure 32

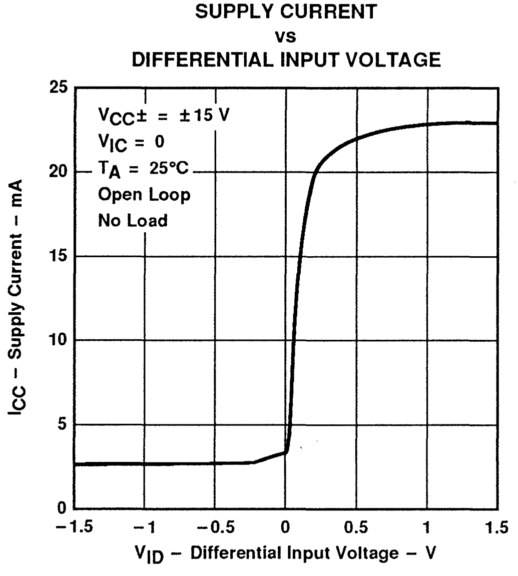


Figure 33

[†] Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

SHORT-CIRCUIT OUTPUT CURRENT
vs
SUPPLY VOLTAGE

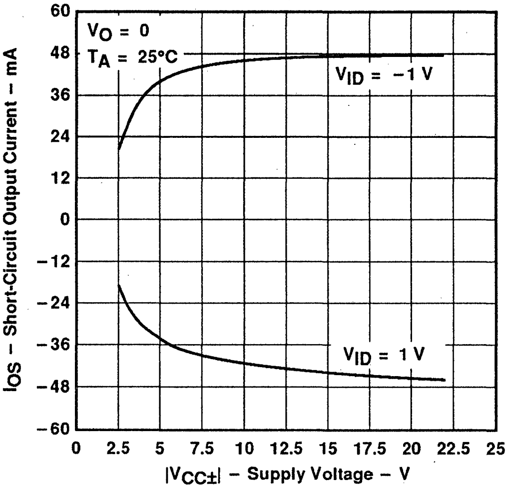


Figure 34

SHORT-CIRCUIT OUTPUT CURRENT
vs
TIME

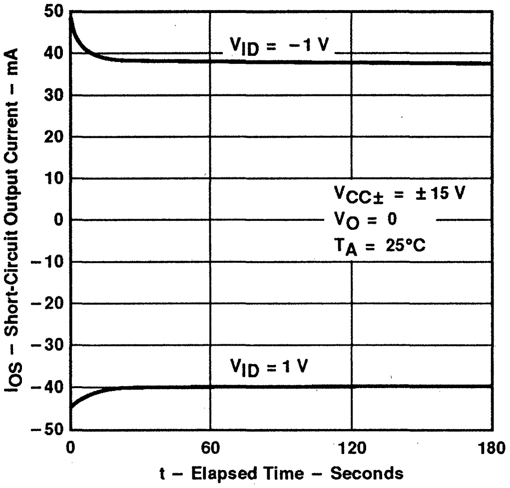


Figure 35

SHORT-CIRCUIT OUTPUT CURRENT
vs
FREE-AIR TEMPERATURE

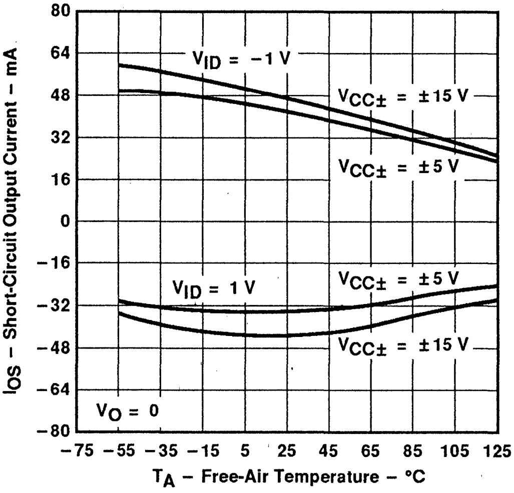


Figure 36

SLEW RATE
vs
FREE-AIR TEMPERATURE

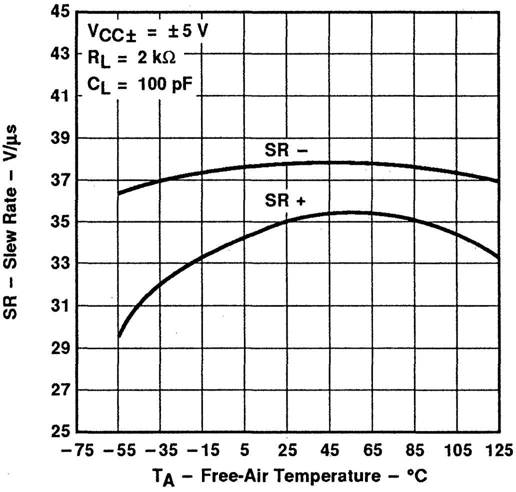


Figure 37

---

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

SLEW RATE
vs
FREE-AIR TEMPERATURE

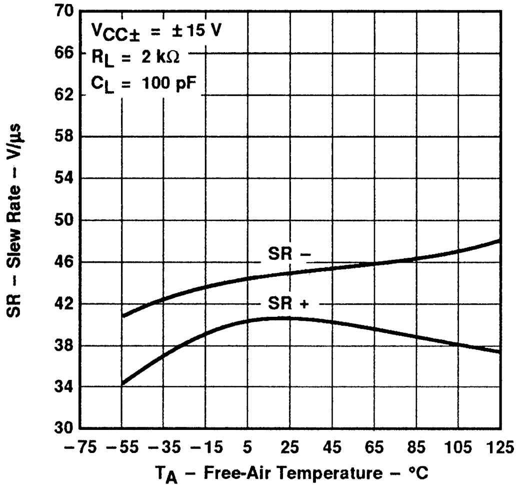


Figure 38

SLEW RATE
vs
LOAD RESISTANCE

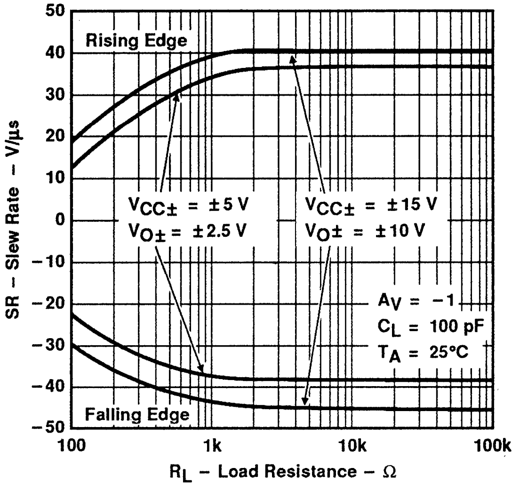


Figure 39

SLEW RATE
vs
DIFFERENTIAL INPUT VOLTAGE

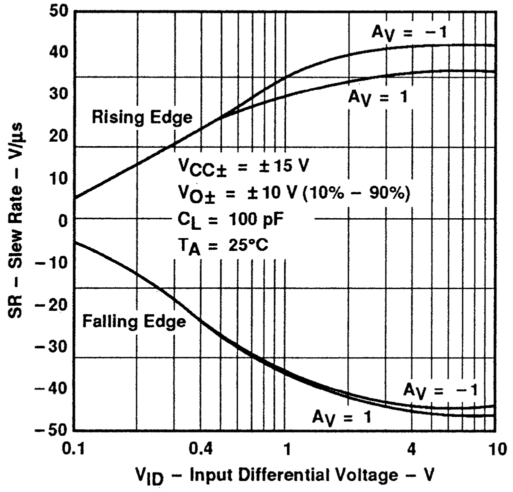


Figure 40

INPUT-REFERRED NOISE VOLTAGE SPECTRAL DENSITY
vs
FREQUENCY

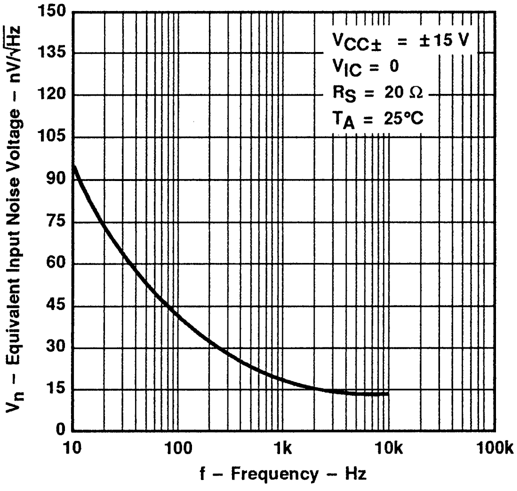


Figure 41

---

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS

INPUT-REFERRED NOISE VOLTAGE vs NOISE BANDWIDTH

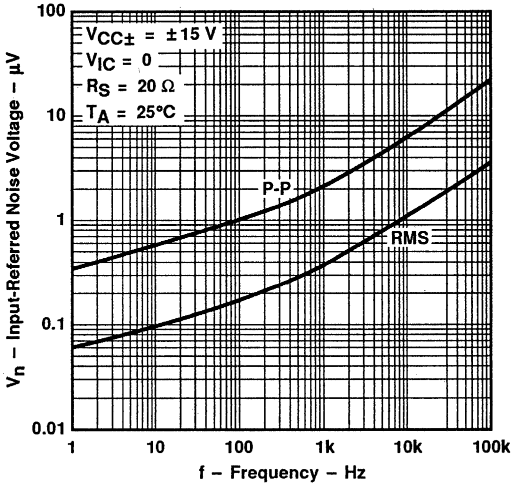


Figure 42

INPUT-REFERRED NOISE VOLTAGE OVER A 10-SECOND TIME INTERVAL

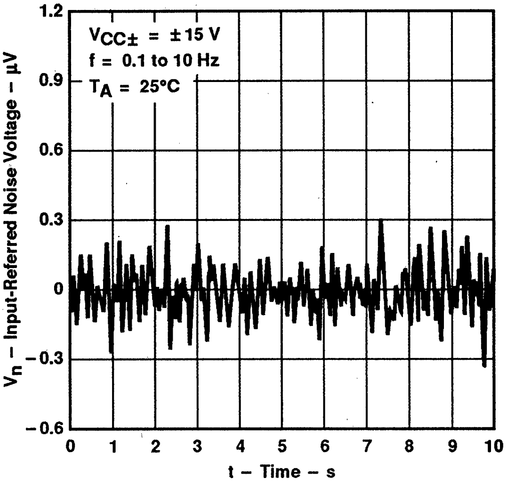


Figure 43

THIRD-OCTAVE SPECTRAL NOISE DENSITY vs FREQUENCY

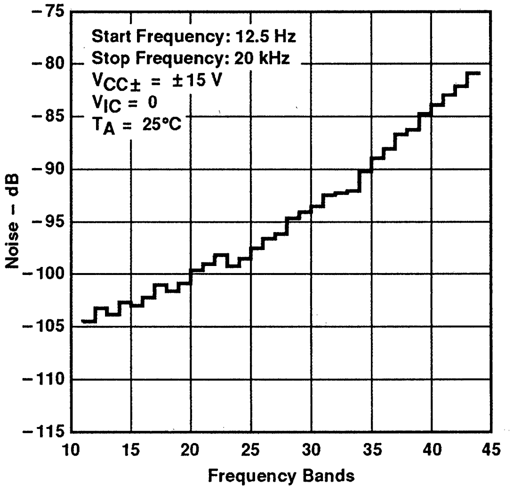


Figure 44

TOTAL HARMONIC DISTORTION PLUS NOISE vs FREQUENCY

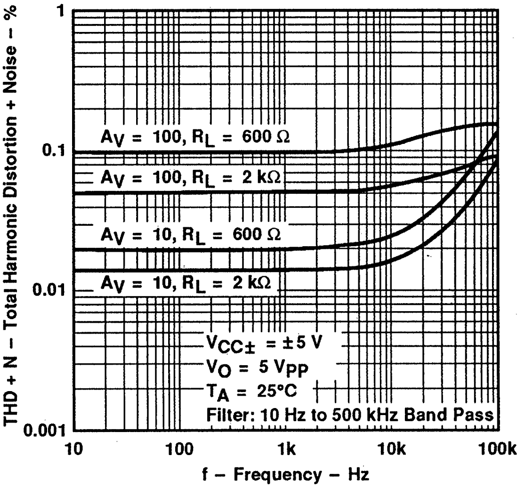


Figure 45

TYPICAL CHARACTERISTICS†

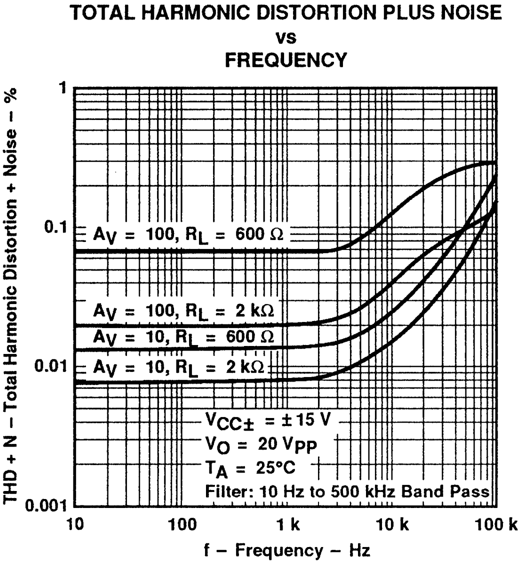


Figure 46

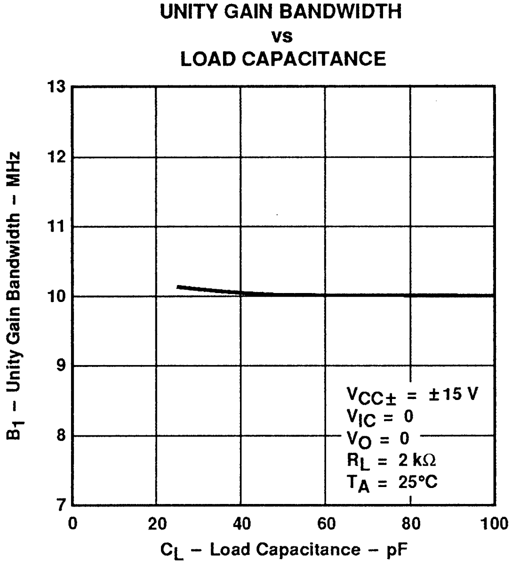


Figure 47

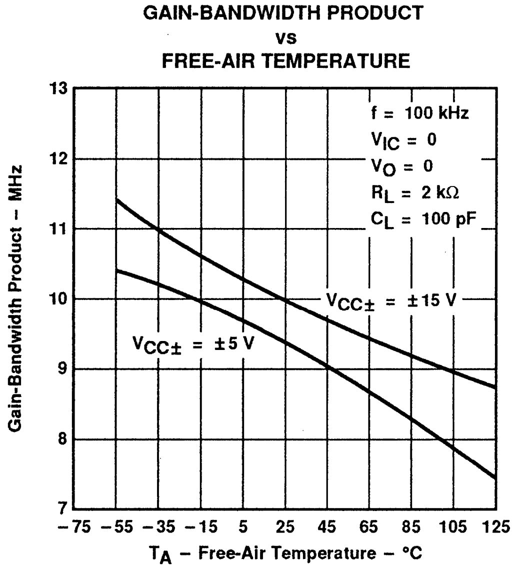


Figure 48

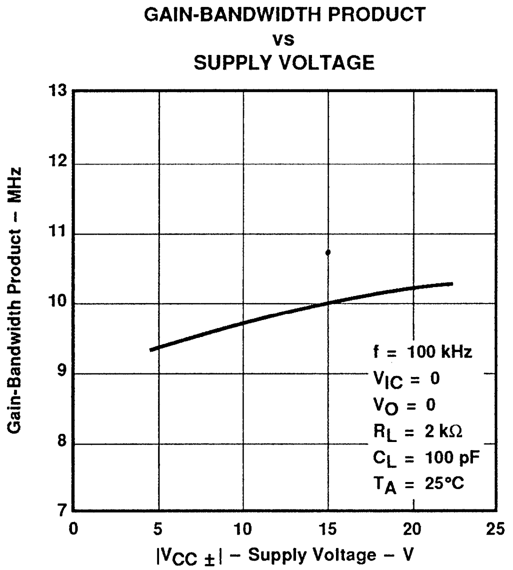


Figure 49

---

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

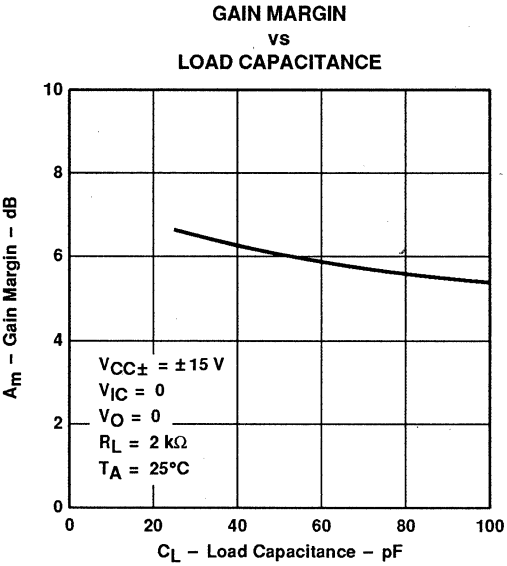


Figure 50

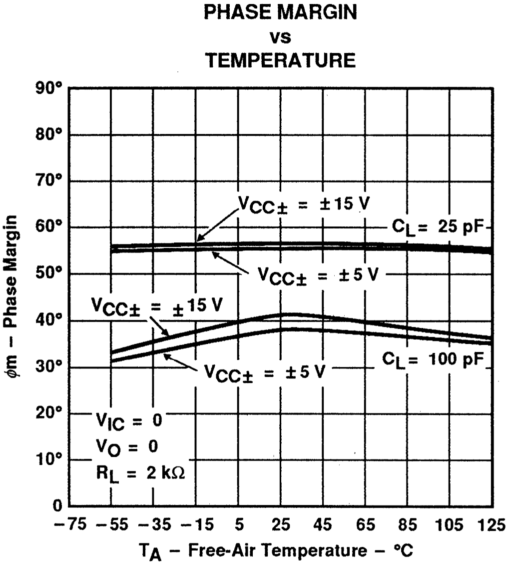


Figure 51

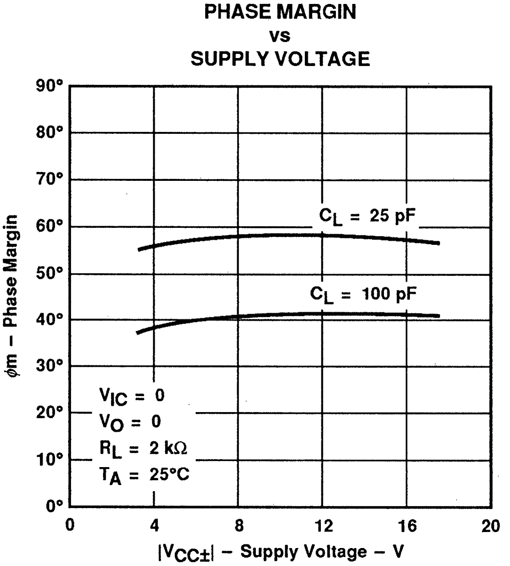


Figure 52

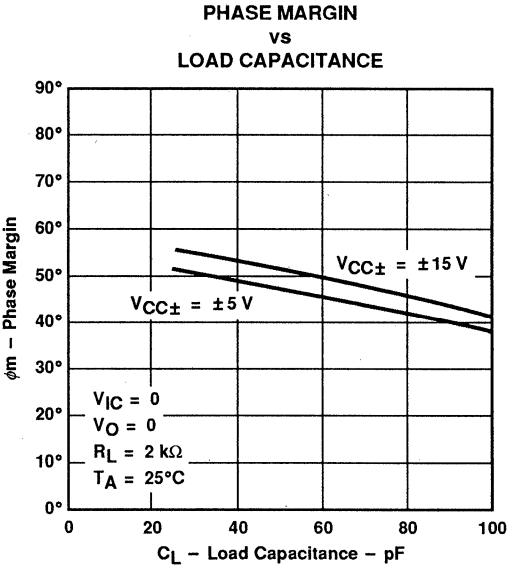


Figure 53

---

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

NONINVERTING LARGE-SIGNAL PULSE RESPONSE

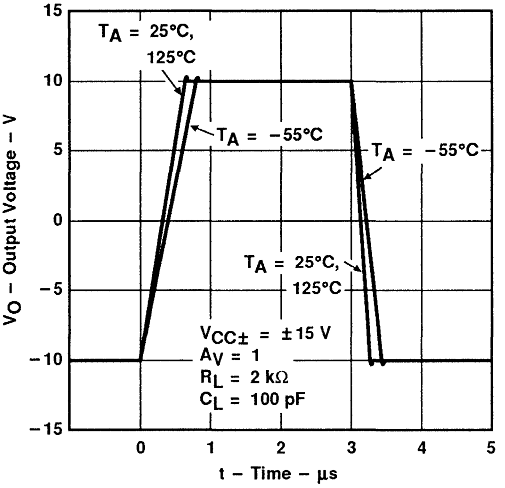


Figure 54

SMALL-SIGNAL PULSE RESPONSE

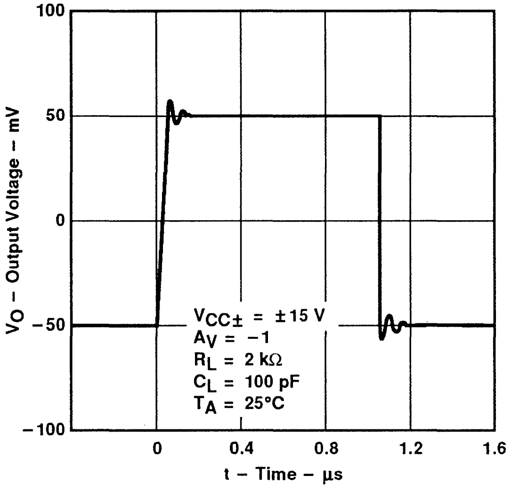


Figure 55

SMALL-SIGNAL RESPONSE vs FREQUENCY

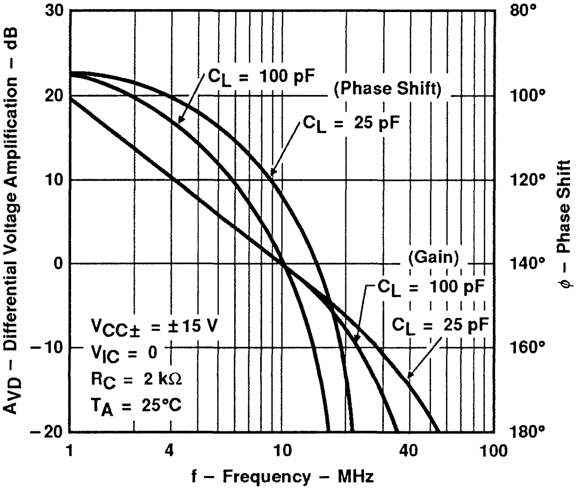


Figure 56

CROSSTALK ATTENUATION vs FREQUENCY

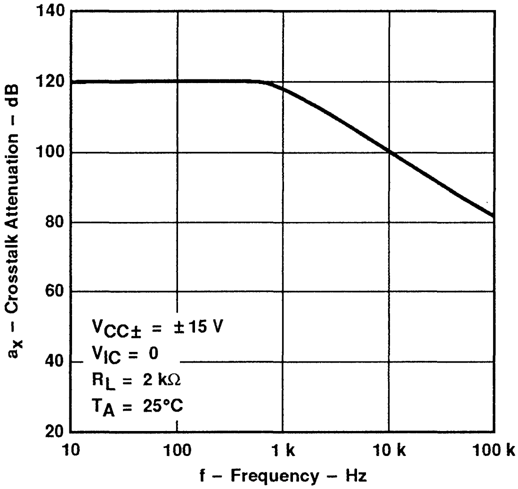


Figure 57

---

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

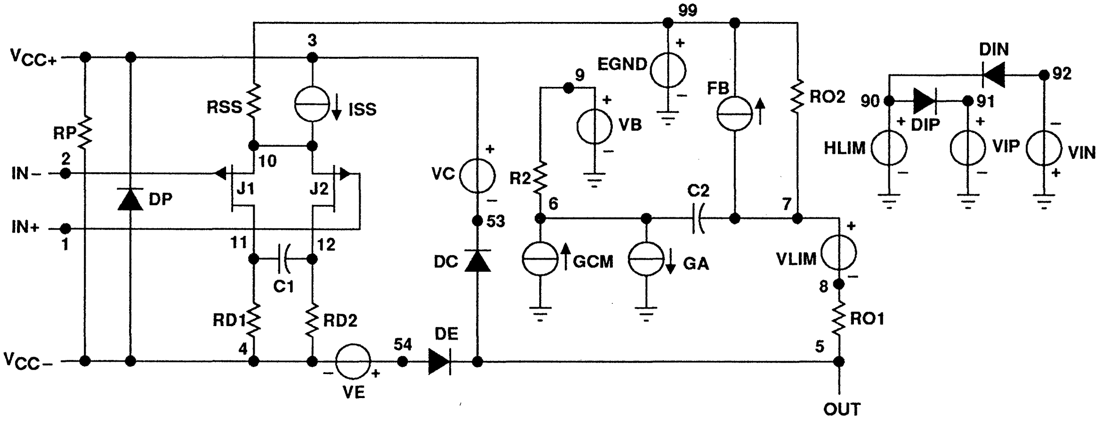
APPLICATION INFORMATION

macromodel information

Macromodel information provided was derived using *PSpice*™ *Parts*™ model generation software. The Boyle macromodel (see Note 4) and subcircuit in Figure 58 were generated using the TLE2082 typical electrical and operating characteristics at T_A = 25°C. Using this information, output simulations of the following key parameters can be generated to a tolerance of 20% (in most cases):

- Maximum positive output voltage swing
- Maximum negative output voltage swing
- Slew rate
- Quiescent power dissipation
- Input bias current
- Open-loop voltage amplification
- Unity gain frequency
- Common-mode rejection ratio
- Phase margin
- dc output resistance
- ac output resistance
- Short-circuit output current limit

NOTE 4: G. R. Boyle, B. M. Cohn, D. O. Pederson, and J. E. Solomon, "Macromodeling of Integrated Circuit Operational Amplifiers", IEEE Journal of Solid-State Circuits, SC-9, 353 (1974).



```
.SUBCKT TLE2082 1 2 3 4 5
  C1    11 12  2.2E-12
  C2     6  7  10.00E-12
  DC     5 53  DX
  DE    54  5  DX
  DLP   90 91  DX
  DLN   92 90  DX
  DP     4  3  DX
  EGND  99  0  POLY(2)  (3,0)  (4,0)  0 .5 .5
  FB     7 99  POLY(5)  VB VC VE VLP VLN 0
+ 5.607E6 -6E6 6E6 6E6 -6E6
  GA     6  0  11 12 333.0E-6
  GCM    0  6  10 99 7.436E-9
  ISS    3 10  DC 400.0E-6
  HLIM  90  0  VLIM 1K
  J1    11  2  10 JX
  J2    12  1  10 JX
  R2     6   9 100.0E3
  RD1    4  11 3.003E3
  RD2    4  12 3.003E3
  RO1    8   5 80
  RO2    7  99 80
  RP     3   4 27.30E3
  RSS   10  99 500.0E3
  VB     9   0 DC 0
  VC     3  53 DC 2.20
  VE    54   4 DC 2.20
  VLIM   7   8 DC 0
  VLP   91   0 DC 45
  VLN    0  92 DC 45
.MODEL DX D(IS=800.0E-18)
.MODEL JX PJF(IS=15.00E-12 BETA=554.5E-6
+ VTO=-.6)
.ENDS
```

Figure 58. Boyle Macromodel and Subcircuit

PSpice and *Parts* are trademarks of MicroSim Corporation.

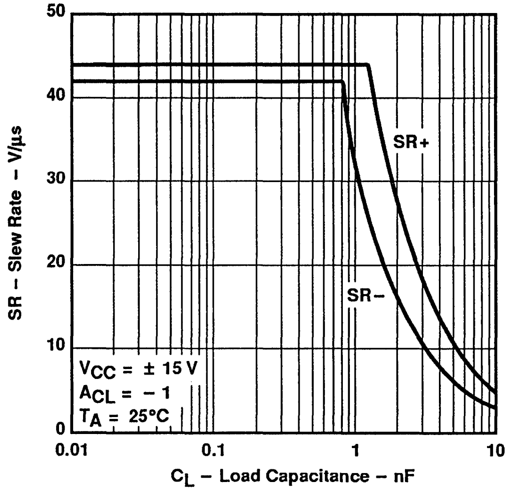
TLE2141, TLE2141A, TLE2141Y
EXCALIBUR LOW-NOISE HIGH-SPEED PRECISION OPERATIONAL AMPLIFIERS

D3652, NOVEMBER 1990 – REVISED FEBRUARY 1991

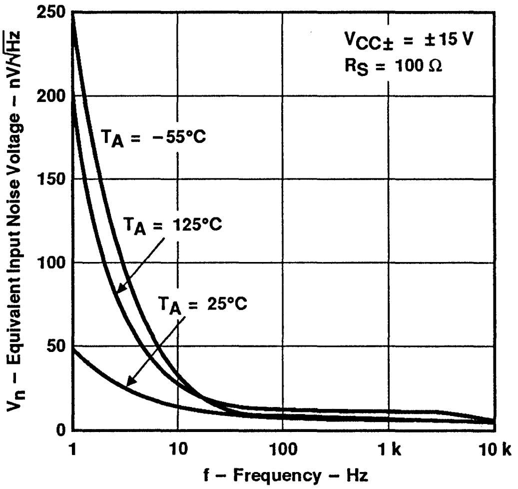
available features

- **Low Noise:**
  10 Hz . . . 15 nV/√Hz
  1 kHz . . . 10.5 nV/√Hz
- **10,000-pF Load Capability**
- **20-mA Min Short Circuit Output Current**
- **30-V/μs Min Slew Rate**
- **High Gain-Bandwidth Product . . . 5.9 MHz**
- **Low V_{IO} . . . 500 μV Max at 25°C**
- **Single or Split Supply . . . 4 V to 44 V**
- **Fast Settling Time . . . 340 ns to 0.1%**
  400 ns to 0.01%
- **Saturation Recovery . . . 150 ns**
- **Large Output Swing . . . V_{CC-} + 0.1 V**
  to V_{CC+} − 1 V

SLEW RATE
vs
LOAD CAPACITANCE



EQUIVALENT INPUT NOISE VOLTAGE
vs
FREQUENCY



description

The TLE2141 and TLE2141A are high-performance, internally compensated operational amplifiers built using Texas Instruments complementary bipolar Excalibur process. The TLE2141A is a tighter offset voltage grade of the TLE2141. Both are pin-compatible upgrades to standard industry products.

AVAILABLE OPTIONS

T_A	V_{IO} max AT 25°C	PACKAGE				
		SMALL-OUTLINE (D)	CHIP CARRIER (FK)	CERAMIC DIP (JG)	PLASTIC DIP (P)	CHIP FORM (Y)
0°C to 70°C	500 μV	TLE2141ACD	——	——	TLE2141ACP	TLE2141Y
	900 μV	TLE2141CD	——	——	TLE2141CP	
− 40°C to 105°C	500 μV	TLE2141AID	——	——	TLE2141AIP	
	900 μV	TLE2141ID	——	——	TLE2141IP	
− 55°C to 125°C	500 μV	TLE2141AMD	TLE2141AMFK	TLE2141AMJG	TLE2141AMP	
	900 μV	TLE2141MD	TLE2141MFK	TLE2141MJG	TLE2141MP	

D packages are available taped-and-reeled. Add "R" suffix to device type, (e.g., TLE2141ACDR).

TEXAS INSTRUMENTS
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

description (continued)

The design incorporates a patent-pending input stage that simultaneously achieves low audio band noise of 10.5 nV/√Hz with a 10-Hz 1/f corner and symmetrical 40-V/µs slew rate typically with loads up to 800 pF. The resulting low distortion and high power-bandwidth are important in hi-fi audio applications. A fast settling time of 340 ns to 0.1% of a 10-V step with a 2-kΩ /100-pF load is useful in fast actuator/positioning drivers. Under similar test conditions, settling time to 0.01% is 400 ns.

The devices are stable with capacitive loads up to 10 nF, although the 6 MHz bandwidth decreases to 1.8 MHz at this high loading level. As such, the TLE2141 and TLE2141A are useful for low droop sample-and-holds and direct buffering of long cables, including 4-20 mA current loops.

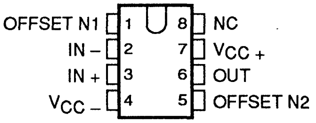
The special design also exhibits an improved insensitivity to inherent IC component mismatches as is evidenced by a 500-µV maximum offset voltage and 1.7-µV/°C typical drift. Minimum common-mode rejection ratio and supply-voltage rejection ratio are 85 dB and 90 dB, respectively.

Device performance is relatively independent of supply voltage over the ±2-V to ±22-V range. Inputs can operate between V_{CC-} −0.3 V to V_{CC+} −1.8 V without inducing phase reversal, although excessive input current may flow out of each input exceeding the lower common-mode input range. The all NPN output stage provides a nearly rail-to-rail output swing of V_{CC-}+0.1 V to V_{CC+}−1 V under light current loading conditions. The device can sustain shorts to either supply since output current is internally limited, but care must be taken to ensure that maximum package power dissipation is not exceeded.

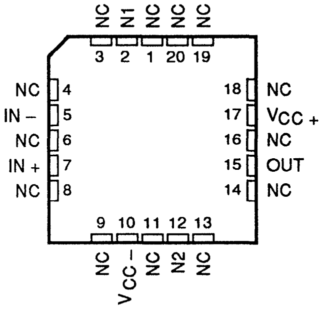
Both versions can also be used as comparators. Differential inputs of $V_{CC\pm}$ can be maintained without damage to the device. Open-loop propagation delay with TTL supply levels is typically 200 ns. This gives a good indication as to output stage saturation recovery when the device is over-driven beyond the limits of recommended output swing.

Both the TLE2141 and TLE2141A are available in a wide variety of packages, including both the industry-standard 8-pin small-outline version and chip form for high-density system applications. The C-suffix devices are characterized for operation from 0°C to 70°C, the I-suffix from −40°C to 105°C, and the M-suffix over the full military temperature range of −55°C to 125°C.

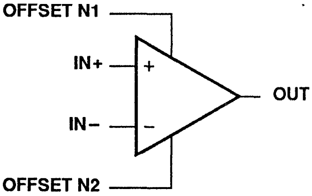
D, JG, OR P PACKAGE
(TOP VIEW)



FK PACKAGE
(TOP VIEW)



symbol

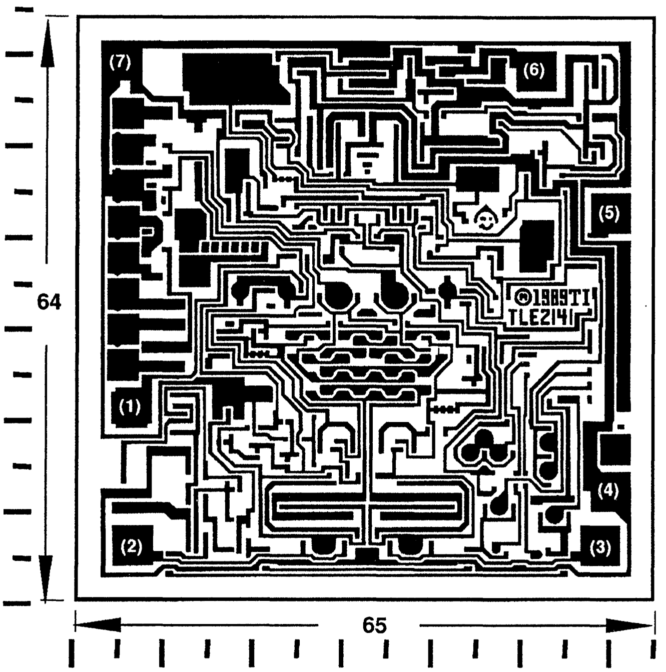


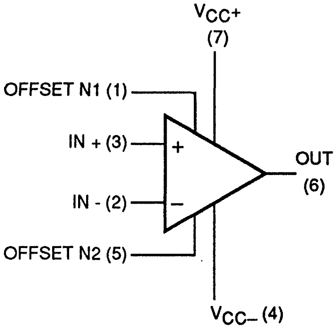
NC – No internal connection

chip information

These chips, properly assembled, display characteristics similar to the TLE2141, (see electrical table on page 18). Thermal compression or ultrasonic bonding may be used on the doped aluminum bonding pads. Chips may be mounted with conductive epoxy or a gold-silicon preform.

BONDING PAD ASSIGNMENTS





CHIP THICKNESS:
15 TYPICAL

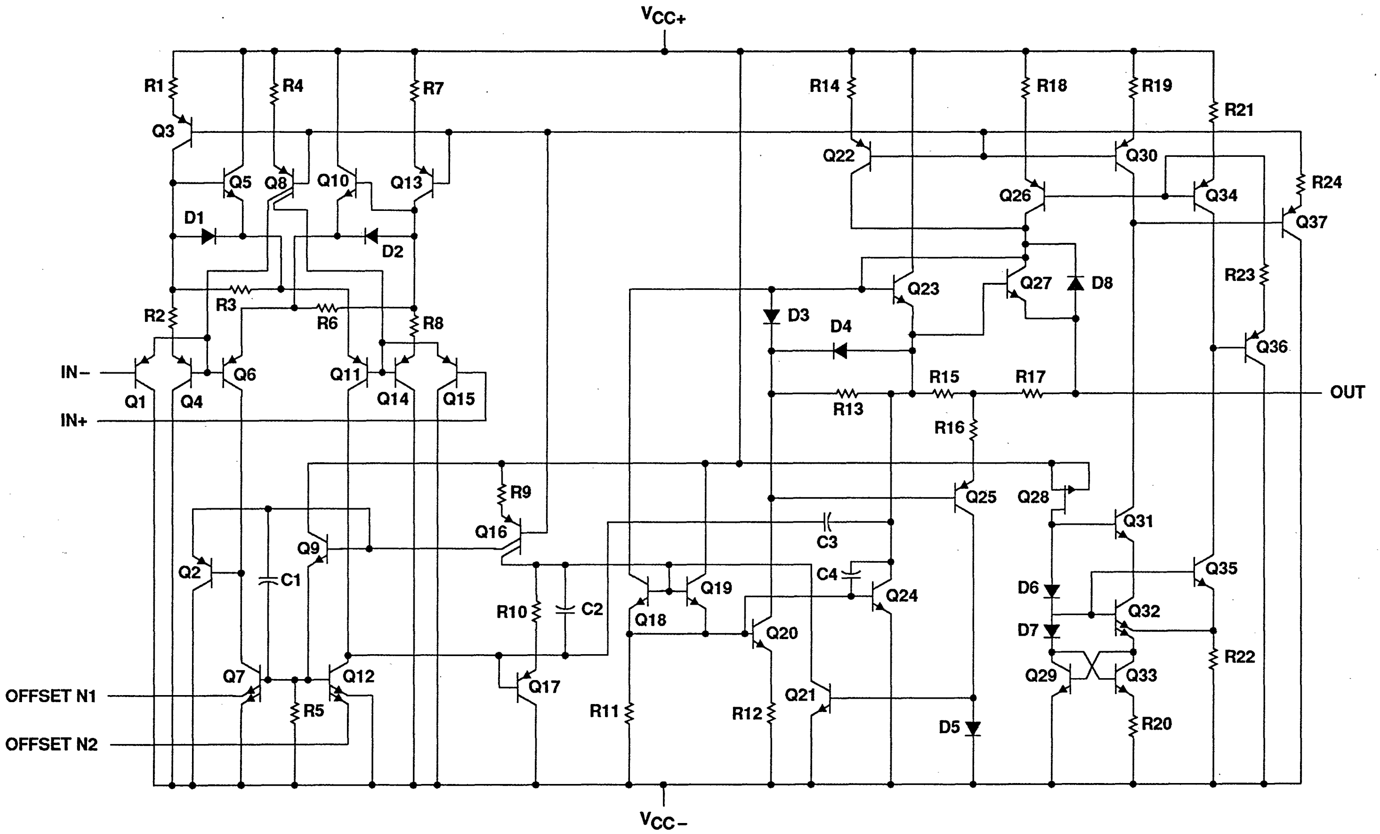
BONDING PADS:
4 X 4 MINIMUM

T_J max = 150°C

TOLERANCES
ARE ± 10%

ALL DIMENSIONS
ARE IN MILS

equivalent schematic



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC+} (see Note 1)	22 V
Supply voltage, V_{CC-}	−22 V
Differential input voltage (see Note 2)	±44 V
Input voltage range, V_I (any input)	V_{CC+} to $V_{CC-} - 0.3$ V
Input current, I_I (each input)	±1 mA
Output current, I_O	±80 mA
Total current into V_{CC+} terminal	80 mA
Total current out of V_{CC-} terminal	80 mA
Duration of short-circuit current at (or below) 25°C (see Note 3)	unlimited
Continuous total dissipation	See Dissipation Rating Table
Operating free-air temperature range, T_A: C-suffix	0°C to 70°C
I-suffix	−40°C to 105°C
M-suffix	−55°C to 125°C
Storage temperature range	−65°C to 150°C
Case temperature for 60 seconds: FK package	260°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D or P package	260°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: JG or L package	300°C

NOTES: 1. All voltage values, except differential voltages, are with respect to the midpoint between V_{CC+} and V_{CC-}.
2. Differential voltages are at the noninverting input with respect to the inverting input. Excessive current will flow if input is brought below $V_{CC-} - 0.3$ V.
3. The output may be shorted to either supply. Temperature and/or supply voltages must be limited to ensure that the maximum dissipation rating is not exceeded.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 105°C$ POWER RATING	$T_A = 125°C$ POWER RATING
D	725 mW	5.8 mW/°C	464 mW	261 mW	145 mW
FK	1375 mW	11.0 mW/°C	880 mW	495 mW	275 mW
JG	1050 mW	8.4 mW/°C	672 mW	378 mW	210 mW
L	650 mW	5.2 mW/°C	416 mW	234 mW	130 mW
P	1000 mW	8.0 mW/°C	640 mW	360 mW	200 mW

recommended operating conditions

		C-SUFFIX		I-SUFFIX		M-SUFFIX		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
Supply voltage, $V_{CC\pm}$		± 2	± 22	± 2	± 22	± 2	± 22	V
Common-mode input voltage, V_{IC}	$V_{CC} = 5$ V	0	2.9	0	2.7	0	2.7	V
	$V_{CC\pm} = \pm 15$ V	− 15	12.9	− 15	12.7	− 15	12.7	
Operating free-air temperature, T_A		0	70	− 40	105	− 55	125	°C

electrical characteristics at specified free-air temperature, V_{CC} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A†	TLE2141C			TLE2141AC			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_O = 2.5 V, R_S = 50 Ω, V_{IC} = 2.5 V	25°C		225	1400		200	1000	μV
			Full range			1700			1300	
α_{VIO}	Temperature coefficient of input offset voltage		Full range		1.7			1.7		μV/°C
I_{IO}	Input offset current		25°C		8	100		8	100	nA
			Full range			150			150	
I_{IB}	Input bias current		25°C		−0.8	−2		−0.8	−2	μA
			Full range			−2.1			−2.1	
V_{ICR}	Common-mode input voltage range	R_S = 50 Ω	25°C	0 to 3	−0.3 to 3.2		0 to 3	−0.3 to 3.2		V
			Full range	0 to 2.9			0 to 2.9			
V_{OH}	High-level output voltage	I_{OH} = −150 μA	25°C	3.9	4.1		3.9	4.1		V
			Full range	3.8			3.8			
		I_{OH} = −1.5 mA	25°C	3.8	4		3.8	4		
			Full range	3.7			3.7			
		I_{OH} = −15 mA	25°C	3.2	3.7		3.2	3.7		
			Full range	3.2			3.2			
V_{OL}	Low-level output voltage	I_{OL} = 150 μA	25°C		75	125		75	125	mV
			Full range			150			150	
		I_{OL} = 1.5 mA	25°C		150	225		150	225	
			Full range			250			250	
		I_{OL} = 15 mA	25°C		1.2	1.6		1.2	1.6	V
			Full range			1.7			1.7	
A_{VD}	Large-signal differential voltage amplification	V_{CC} = ±2.5 V, R_L = 2 kΩ, V_O = 1 V to − 1.5 V	25°C	50	220		50	220		V/mV
			Full range	25			25			
r_i	Input resistance		25°C		70			70		MΩ
c_i	Input capacitance		25°C		2.5			2.5		pF
z_o	Open-loop output impedance	f = 1 MHz	25°C		30			30		Ω
CMRR	Common-mode rejection ratio	V_{IC} = V_{ICR} min, R_S = 50 Ω	25°C	85	118		85	118		dB
			Full range	80			80			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm}/\Delta V_{IO}$)	$V_{CC\pm}$ = ±2.5 V to ±15 V, R_S = 50 Ω	25°C	90	106		90	106		dB
			Full range	85			85			
I_{CC}	Supply current	V_O = 2.5 V, No load, V_{IC} = 2.5 V	25°C		3.4	4.4		3.4	4.4	mA
			Full range			4.6			4.6	

†Full range is 0°C to 70°C.

operating characteristics at specified free-air temperature, V_{CC} = 5 V

PARAMETER		TEST CONDITIONS		T_A	TLE2141C			TLE2141AC			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
SR +	Positive slew rate	$A_{VD} = -1$, $R_L = 2\ k\Omega$†, $C_L = 500\ pF$		25°C		45			45		V/μs
SR −	Negative slew rate					42			42		
	Settling time	$A_{VD} = -1$, 2.5-V Step	To 0.1%	25°C		0.16			0.16		μs
			To 0.01%			0.22			0.22		
V_n	Equivalent input noise voltage	$R_S = 100\ \Omega$, $f = 10\ Hz$		25°C		15			15		nV/√Hz
		$R_S = 100\ \Omega$, $f = 1\ kHz$				10.5			10.5		
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 1 Hz		25°C		0.48			0.48		μV
		f = 0.1 Hz to 10 Hz				0.51			0.51		
I_n	Equivalent input noise current	f = 10 Hz		25°C		1.92			1.92		pA/√Hz
		f = 1 kHz				0.5			0.5		
THD + N	Total harmonic distortion plus noise	V_O = 1 V to 3 V, $R_L = 2\ k\Omega$†, $A_{VD} = 2$, f = 10 kHz		25°C		0.0052 %			0.0052 %		
B_1	Unity-gain bandwidth	$R_L = 2\ k\Omega$†, $C_L = 100\ pF$		25°C		5.9			5.9		MHz
	Gain-bandwidth product	$R_L = 2\ k\Omega$†, $C_L = 100\ pF$, f = 100 kHz		25°C		5.8			5.8		MHz
B_{OM}	Maximum output-swing bandwidth	$R_L = 2\ k\Omega$†, $V_{O(PP)} = 2\ V$, $A_{VD} = 1$, $C_L = 100\ pF$		25°C		6.6			6.6		MHz
ϕ_m	Phase margin at unity-gain	$R_L = 2\ k\Omega$†, $C_L = 100\ pF$		25°C		57°			57°		

† R_L terminates at 2.5 V.

electrical characteristics at specified free-air temperature, $V_{CC\pm}$ = ± 15 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A†	TLE2141C			TLE2141AC			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_{IC} = 0, R_S = 50 Ω, V_O = 0	25°C		200	900		175	500	μV
			Full range			1300			800	
α_{VIO}	Temperature coefficient of input offset voltage		Full range		1.7			1.7		μV/°C
I_{IO}	Input offset current		25°C		7	100		7	100	nA
			Full range			150			150	
I_{IB}	Input bias current		25°C		− 0.7	− 1.5		− 0.7	− 1.5	μA
			Full range			− 1.6			− 1.6	
V_{ICR}	Common-mode input voltage range	R_S = 50 Ω	25°C	− 15 to 13	− 15.3 to 13.2		− 15 to 13	− 15.3 to 13.2		V
			Full range	− 15 to 12.9	− 15.3 to 13.1		− 15 to 12.9	− 15.3 to 13.1		
V_{OM+}	Maximum positive peak output voltage swing	I_O = − 150 μA	25°C	13.8	14.1		13.8	14.1		V
			Full range	13.7			13.7			
		I_O = − 1.5 mA	25°C	13.7	14		13.7	14		
			Full range	13.6			13.6			
		I_O = − 15 mA	25°C	13.1	13.7		13.1	13.7		
			Full range	13			13			
V_{OM-}	Maximum negative peak output voltage swing	I_O = 150 μA	25°C	− 14.7	− 14.9		− 14.7	− 14.9		V
			Full range	− 14.6			− 14.6			
		I_O = 1.5 mA	25°C	− 14.5	− 14.8		− 14.5	− 14.8		
			Full range	− 14.4			− 14.4			
		I_O = 15 mA	25°C	− 13.4	− 13.8		− 13.4	− 13.8		
			Full range	− 13.3			− 13.3			
A_{VD}	Large-signal differential voltage amplification	V_O = ± 10 V	25°C	100	450		100	450		V/mV
			Full range	75			75			
r_i	Input resistance	R_L = 2 kΩ	25°C		65			65		MΩ
c_i	Input capacitance		25°C		2.5			2.5		pF
z_o	Open-loop output impedance	f = 1 MHz	25°C		30			30		Ω
CMRR	Common-mode rejection ratio	V_{IC} = V_{ICR} min, R_S = 50 Ω	25°C	85	108		85	108		dB
			Full range	80			80			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm} / \Delta V_{IO}$)	$V_{CC\pm}$ = ± 2.5 V to ± 15 V, R_S = 50 Ω	25°C	90	106		90	106		dB
			Full range	85			85			
I_{OS}	Short-circuit output current	V_O = 0, V_{ID} = 1 V	25°C	− 25	− 50		− 25	− 50		mA
		V_O = 0, V_{ID} = − 1 V		20	31		20	31		
I_{CC}	Supply current	V_O = 0, No load	25°C		3.5	4.5		3.5	4.5	mA
			Full range			4.7			4.7	

†Full range is 0°C to 70°C.

operating characteristics at specified free-air temperature, $V_{CC\pm}$ = ±15 V

PARAMETER		TEST CONDITIONS		T_A	TLE2141C			TLE2141AC			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
SR +	Positive slew rate	A_{VD} = −1, R_L = 2 kΩ, C_L = 500 pF		25°C	30	45		30	45		V/μs
SR −	Negative slew rate			25°C	30	42		30	42		
	Settling time	A_{VD} = −1, 10-V Step	To 0.1%	25°C		0.34			0.34		μs
			To 0.01%			0.4			0.4		
V_n	Equivalent input noise voltage	R_S = 100 Ω, f = 10 Hz		25°C		15			15		nV/√Hz
		R_S = 100 Ω, f = 1 kHz				10.5			10.5		
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 1 Hz		25°C		0.48			0.48		μV
		f = 0.1 Hz to 10 Hz				0.51			0.51		
I_n	Equivalent input noise current	f = 10 Hz		25°C		1.89			1.89		pA/√Hz
		f = 1 kHz				0.47			0.47		
THD + N	Total harmonic distortion plus noise	$V_{O(PP)}$ = 20 V, R_L = 2 kΩ, A_{VD} = 10, f = 10 kHz		25°C		0.01%			0.01%		
B_1	Unity-gain bandwidth	R_L = 2 kΩ, C_L = 100 pF		25°C		6			6		MHz
	Gain-bandwidth product	R_L = 2 kΩ, C_L = 100 pF, f = 100 kHz		25°C		5.9			5.9		MHz
B_{OM}	Maximum output-swing bandwidth	$V_{O(PP)}$ = 20 V, R_L = 2 kΩ, A_{VD} = 1, C_L = 100 pF		25°C		668			668		kHz
ϕ_m	Phase margin at unity gain	R_L = 2 kΩ, C_L = 100 pF		25°C		58°			58°		

electrical characteristics at specified free-air temperature, V_{CC} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A†	TLE2141I			TLE2141AI			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_O = 2.5 V, R_S = 50 Ω, V_{IC} = 2.5 V		25°C		225	1400		200	1000	μV
				Full range			1900			1500	
α_{VIO}	Temperature coefficient of input offset voltage			Full range		1.7			1.7		μV/°C
I_{IO}	Input offset current			25°C		8	100		8	100	nA
				Full range			200			200	
I_{IB}	Input bias current			25°C		−0.8	−2		−0.8	−2	μA
				Full range			−2.2			−2.2	
V_{ICR}	Common-mode input voltage range	R_S = 50 Ω		25°C	0 to 3	−0.3 to 3.2		0 to 3	−0.3 to 3.2		V
				Full range	0 to 2.7	−0.3 to 2.9		0 to 2.7	−0.3 to 2.9		
V_{OH}	High-level output voltage	I_{OH} = −150 μA		25°C	3.9	4.1		3.9	4.1		V
		I_{OH} = −1.5 mA			3.8	4		3.8	4		
		I_{OH} = −15 mA			3.2	3.7		3.2	3.7		
		I_{OH} = −100 μA		Full range	3.8			3.8			
		I_{OH} = −1 mA			3.7			3.7			
		I_{OH} = −10 mA			3.3			3.3			
V_{OL}	Low-level output voltage	I_{OL} = 150 μA		25°C		75	125		75	125	mV
		I_{OL} = 1.5 mA				150	225		150	225	
		I_{OL} = 15 mA				1.2	1.6		1.2	1.6	V
		I_{OL} = 100 μA		Full range			175			175	mV
		I_{OL} = 1 mA					225			225	
		I_{OL} = 10 mA					1.4			1.4	V
A_{VD}	Large-signal differential voltage amplification	V_{CC} = ± 2.5 V, R_L = 2 kΩ, V_O = 1 V to − 1.5 V		25°C	50	220		50	220		V/mV
				Full range	10			10			
r_i	Input resistance			25°C		70			70		MΩ
c_i	Input capacitance			25°C		2.5			2.5		pF
z_o	Open-loop output impedance	f = 1 MHz		25°C		30			30		Ω
CMRR	Common-mode rejection ratio	V_{IC} = V_{ICR} min, R_S = 50 Ω		25°C	85	118		85	118		dB
				Full range	80			80			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm}/\Delta V_{IO}$)	$V_{CC\pm}$ = ± 2.5 V to ± 15 V, R_S = 50 Ω		25°C	90	106		90	106		dB
				Full range	85			85			
I_{CC}	Supply current	V_O = 2.5 V, V_{IC} = 2.5 V	No load,	25°C		3.4	4.4		3.4	4.4	mA
				Full range			4.6			4.6	

†Full range is −40°C to 105°C.

operating characteristics at specified free-air temperature, V_{CC} = 5 V

PARAMETER		TEST CONDITIONS		T_A	TLE2142I			TLE2141AI			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
SR +	Positive slew rate	A_{VD} = −1, R_L = 2 kΩ†, C_L = 500 pF		25°C		45			45		V/µs
SR −	Negative slew rate					42			42		
	Settling time	A_{VD} = −1, 2.5-V Step	To 0.1%	25°C		0.16			0.16		µs
			To 0.01%			0.22			0.22		
V_n	Equivalent input noise voltage	R_S = 100 Ω, f = 10 Hz		25°C		15			15		nV/√Hz
		R_S = 100 Ω, f = 1 kHz				10.5			10.5		
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 1 Hz		25°C		0.48			0.48		µV
		f = 0.1 Hz to 10 Hz				0.51			0.51		
I_n	Equivalent input noise current	f = 10 Hz		25°C		1.92			1.92		pA/√Hz
		f = 1 kHz				0.5			0.5		
THD + N	Total harmonic distortion plus noise	V_O = 1 V to 3 V, R_L = 2 kΩ†, A_{VD} = 2 f = 10 kHz		25°C		0.0052 %			0.0052 %		
B_1	Unity-gain bandwidth	R_L = 2 kΩ†, C_L = 100 pF		25°C		5.9			5.9		MHz
	Gain-bandwidth product	R_L = 2 kΩ†, C_L = 100 pF, f = 100 kHz		25°C		5.8			5.8		MHz
B_{OM}	Maximum output-swing bandwidth	R_L = 2 kΩ†, $V_{O(PP)}$ = 2 V, A_{VD} = 1, C_L = 100 pF		25°C		6.6			6.6		MHz
ϕ_m	Phase margin at unity-gain	R_L = 2 kΩ†, C_L = 100 pF		25°C		57°			57°		

† R_L terminates at 2.5 V.

electrical characteristics at specified free-air temperature, $V_{CC\pm} = \pm 15$ V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A†	TLE2141I			TLE2141AI			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	$V_{IC} = 0$, $R_S = 50\ \Omega$, $V_O = 0$	25°C		200	900		175	500	µV
			Full range			1500			1000	
α_{VIO}	Temperature coefficient of input offset voltage		Full range		1.7			1.7		µV/°C
I_{IO}	Input offset current		25°C		7	100		7	100	nA
			Full range			200			200	
I_{IB}	Input bias current		25°C		– 0.7	– 1.5		– 0.7	– 1.5	µA
			Full range			– 1.7			– 1.7	
V_{ICR}	Common-mode input voltage range	$R_S = 50\ \Omega$	25°C	– 15 to 13	– 15.3 to 13.2		– 15 to 13	– 15.3 to 13.2		V
			Full range	– 15 to 12.7	– 15.3 to 12.9		– 15 to 12.7	– 15.3 to 12.9		
V_{OM+}	Maximum positive peak output voltage swing	$I_O = -150\ \mu A$	25°C	13.8	14.1		13.8	14.1		V
		$I_O = -1.5$ mA		13.7	14		13.7	14		
		$I_O = -15$ mA		13.1	13.7		13.1	13.7		
		$I_O = -100\ \mu A$	Full range	13.7			13.7			
		$I_O = -1$ mA		13.6			13.6			
		$I_O = -10$ mA		13.1			13.1			
V_{OM-}	Maximum negative peak output voltage swing	$I_O = 150\ \mu A$	25°C	– 14.7	– 14.9		– 14.7	– 14.9		V
		$I_O = 1.5$ mA		– 14.5	– 14.8		– 14.5	– 14.8		
		$I_O = 15$ mA		– 13.4	– 13.8		– 13.4	– 13.8		
		$I_O = 100\ \mu A$	Full range	– 14.6			– 14.6			
		$I_O = 1$ mA		– 14.5			– 14.5			
		$I_O = 10$ mA		– 13.4			– 13.4			
A_{VD}	Large-signal differential voltage amplification	$V_O = \pm 10$ V, $R_L = 2\ k\Omega$	25°C	100	450		100	450		V/mV
			Full range	40			40			
r_i	Input resistance		25°C		65			65		MΩ
c_i	Input capacitance		25°C		2.5			2.5		pF
z_o	Open-loop output impedance	f = 1 MHz	25°C		30			30		Ω
CMRR	Common-mode rejection ratio	$V_{IC} = V_{ICR}$ min, $R_S = 50\ \Omega$	25°C	85	108		85	108		dB
			Full range	80			80			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm} / \Delta V_{IO}$)	$V_{CC\pm} = \pm 2.5$ V to ± 15 V, $R_S = 50\ \Omega$	25°C	90	106		90	106		dB
			Full range	85			85			
I_{OS}	Short-circuit output current	$V_O = 0$, $V_{ID} = 1$ V	25°C	– 25	– 50		– 25	– 50		mA
		$V_O = 0$, $V_{ID} = -1$ V		20	31		20	31		
I_{CC}	Supply current	$V_O = 0$, No load	25°C		3.5	4.5		3.5	4.5	mA
			Full range			4.7			4.7	

†Full range is –40C to 105°C.

operating characteristics at specified free-air temperature, $V_{CC\pm} = \pm 15$ V

PARAMETER		TEST CONDITIONS		T_A	TLE2141I			TLE2141AI			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
SR +	Positive slew rate	$A_{VD} = -1$, $R_L = 2\ k\Omega$, $C_L = 500$ pF		25°C	30	45		30	45		V/μs
SR −	Negative slew rate			25°C	30	42		30	42		
	Settling time	$A_{VD} = -1$, 10-V Step	To 0.1%	25°C		0.34			0.34		μs
			To 0.01%			0.4			0.4		
V_n	Equivalent input noise voltage	$R_S = 100\ \Omega$, f = 10 Hz		25°C		15			15		nV/√Hz
		$R_S = 100\ \Omega$, f = 1 kHz				10.5			10.5		
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 1 Hz		25°C		0.48			0.48		μV
		f = 0.1 Hz to 10 Hz				0.51			0.51		
I_n	Equivalent input noise current	f = 10 Hz		25°C		1.89			1.89		pA/√Hz
		f = 1 kHz				0.47			0.47		
THD + N	Total harmonic distortion plus noise	$V_{O(PP)} = 20$ V, $R_L = 2\ k\Omega$, $A_{VD} = 10$, f = 10 kHz		25°C		0.01%			0.01%		
B_1	Unity-gain bandwidth	$R_L = 2\ k\Omega$, $C_L = 100$ pF		25°C		6			6		MHz
	Gain-bandwidth product	$R_L = 2\ k\Omega$, $C_L = 100$ pF, f = 100 kHz		25°C		5.9			5.9		MHz
B_{OM}	Maximum output-swing bandwidth	$V_{O(PP)} = 20$ V, $R_L = 2\ k\Omega$, $A_{VD} = 1$, $C_L = 100$ pF		25°C		668			668		kHz
ϕ_m	Phase margin at unity gain	$R_L = 2\ k\Omega$, $C_L = 100$ pF		25°C		58°			58°		

electrical characteristics at specified free-air temperature, V_{CC} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A†	TLE2141M			TLE2141AM			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_O = 2.5 V, R_S = 50 Ω, V_{IC} = 2.5 V	25°C		225	1400		200	1000	µV
			Full range			2100			1700	
α_{VIO}	Temperature coefficient of input offset voltage		Full range		1.7			1.7		µV/°C
I_{IO}	Input offset current		25°C		8	100		8	100	nA
			Full range			250			250	
I_{IB}	Input bias current		25°C		− 0.8	− 2		− 0.8	− 2	µA
			Full range			− 2.3			− 2.3	
V_{ICR}	Common-mode input voltage range	R_S = 50 Ω	25°C	0 to 3	− 0.3 to 3.2		0 to 3	− 0.3 to 3.2		V
			Full range	0 to 2.7	− 0.3 to 2.9		0 to 2.7	− 0.3 to 2.9		
V_{OH}	High-level output voltage	I_{OH} = − 150 µA	25°C	3.9	4.1		3.9	4.1		V
		I_{OH} = − 1.5 mA		3.8	4		3.8	4		
		I_{OH} = − 15 mA		3.2	3.7		3.2	3.7		
		I_{OH} = − 100 µA	Full range	3.75			3.75			
		I_{OH} = − 1 mA		3.65			3.65			
		I_{OH} = − 10 mA		3.25			3.25			
V_{OL}	Low-level output voltage	I_{OL} = 150 µA	25°C		75	125		75	125	mV
		I_{OL} = 1.5 mA			150	225		150	225	
		I_{OL} = 15 mA			1.2	1.4		1.2	1.4	V
		I_{OL} = 100 µA	Full range			200			200	mV
		I_{OL} = 1 mA				250			250	
		I_{OL} = 10 mA				1.25			1.25	V
A_{VD}	Large-signal differential voltage amplification	$V_{CC\pm}$ = ± 2.5 V, R_L = 2kΩ, V_O = 1 V to − 1.5 V	25°	50	220		50	220		V/mV
			Full range	5			5			
r_i	Input resistance		25°C		70			70		MΩ
c_i	Input capacitance		25°C		2.5			2.5		pF
z_o	Open-loop output impedance	f = 1 MHz	25°C		30			30		Ω
CMRR	Common-mode rejection ratio	V_{IC} = V_{ICR} min, R_S = 50 Ω	25°C	85	118		85	118		dB
			Full range	80			80			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm} / \Delta V_{IO}$)	$V_{CC\pm}$ = ± 2.5 V to ± 15 V, R_S = 50 Ω	25°C	90	106		90	106		dB
			Full range	85			85			
I_{CC}	Supply current	V_O = 2.5 V, No load, V_{IC} = 2.5 V	25°C		3.4	4.4		3.4	4.4	mA
			Full range			4.6			4.6	

†Full range is –55°C to 125° C.

operating characteristics, V_{CC} = 5 V

PARAMETER		TEST CONDITIONS		T_A	TLE2141M			TLE2141AM			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
SR+	Positive slew rate	A_{VD} = −1, R_L = 2 kΩ†, C_L = 500 pF		25°C		45			45		V/µs
SR−	Negative slew rate					42			42		
	Settling time	A_{VD} = −1, 2.5-V Step	To 0.1%	25°C		0.16			0.16		µs
			To 0.01%			0.22			0.22		
V_n	Equivalent input noise voltage	R_S = 100 Ω, f = 10 Hz		25°C		15			15		nV/√Hz
		R_S = 100 Ω, f = 1 kHz				10.5			10.5		
$V_{N(PP}$	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 1 Hz		25°C		0.48			0.48		µV
		f = 0.1 Hz to 10 Hz				0.51			0.51		
I_n	Equivalent input noise current	f = 10 Hz		25°C		1.92			1.92		pA/√Hz
		f = 1 kHz				0.5			0.5		
THD+N	Total harmonic distortion plus noise	V_O = 1 V to 3 V, R_L = 2 kΩ†, A_{VD} = 2, f = 10 kHz		25°C		0.0052%			0.0052%		
B1	Unity-gain bandwidth	R_L = 2 kΩ†, C_L = 100 pF		25°C		5.9			5.9		MHz
	Gain-bandwidth product	R_L = 2 kΩ†, C_L = 100 pF, f = 100 kHz		25°C		5.8			5.8		MHz
B_{OM}	Maximum output-swing bandwidth	R_L = 2 kΩ†, $V_{O(PP)}$ = 2 V, A_{VD} = 1		25°C		6.6			6.6		MHz
ϕ_m	Phase margin at unity gain	R_L = 2 kΩ†, C_L = 100 pF		25°C		57°			57°		

†RL terminates at 2.5 V.

electrical characteristics at specified free-air temperature, $V_{CC\pm}$ = ± 15 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A†	TLE2141M			TLE2141AM			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_{IC} = 0, R_S = 50 Ω		25°C		200	900		175	500	μV
				Full range			1700			1200	
α_{VIO}	Temperature coefficient of input offset voltage			Full range		1.7			1.7		μV/°C
I_{IO}	Input offset current			25°C		7	100		7	100	nA
				Full range			250			250	
I_{IB}	Input bias current			25°C		− 0.7	− 1.5		− 0.7	− 1.5	μA
				Full range			− 1.8			− 1.8	
V_{ICR}	Common-mode input voltage range	R_S = 50 Ω		25°C	− 15 to 13	− 15.3 to 13.2		− 15 to 13	− 15.3 to 13.2		V
				Full range	− 15 to 12.7	− 15.3 to 12.9		− 15 to 12.7	− 15.3 to 12.9		
V_{OM+}	Maximum positive peak output voltage swing	I_O = − 150 μA		25°C	13.8	14.1		13.8	14.1		V
		I_O = − 1.5 mA			13.7	14		13.7	14		
		I_O = − 15 mA			13.1	13.7		13.1	13.7		
		I_O = − 100 μA		Full range	13.7			13.7			
		I_O = − 1 mA			13.6			13.6			
		I_O = − 10 mA			13.1			13.1			
V_{OM-}	Maximum negative peak output voltage swing	I_O = 150 μA		25°C	− 14.7	− 14.9		− 14.7	− 14.9		V
		I_O = 1.5 mA			− 14.5	− 14.8		− 14.5	− 14.8		
		I_O = 15 mA			− 13.4	− 13.8		− 13.4	− 13.8		
		I_O = 100 μA		Full range	− 14.6			− 14.6			
		I_O = 1 mA			− 14.5			− 14.5			
		I_O = 10 mA			− 13.4			− 13.4			
A_{VD}	Large-signal differential voltage amplification	V_O = ± 10 V, R_L = 2 kΩ		25°C	100	450		100	450		V/mV
				Full range	20			20			
r_i	Input resistance			25°C		65			65		MΩ
c_i	Input capacitance			25°C		2.5			2.5		pF
z_o	Open-loop output impedance	f = 1 MHz		25°C		30			30		Ω
CMRR	Common-mode rejection ratio	V_{IC} = V_{ICR} min, R_S = 50 Ω		25°C	85	108		85	108		dB
				Full range	80			80			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm} / \Delta V_{IO}$)	$V_{CC\pm}$ = ± 2.5 V to ± 15 V, R_S = 50 Ω		25°C	90	106		90	106		dB
				Full range	85			85			
I_{OS}	Short-circuit output current	V_O = 0	V_{ID} = 1 V	25°C	− 25	− 50		− 25	− 50		mA
			V_{ID} = − 1 V		20	31		20	31		
I_{CC}	Supply current	V_O = 0, No load, V_{IC} = 2.5 V		25°C		3.5	4.5		3.5	4.5	mA
				Full range			4.7			4.7	

†Full range is −55°C to 125°C.

operating characteristics, $V_{CC\pm}$ = ±15 V

PARAMETER		TEST CONDITIONS		T_A	TLE2141M			TLE2141AM			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
SR +	Positive slew rate	A_{VD} = −1, R_L = 2 kΩ, C_L = 100 pF		25°C	30	45		30	45		V/μs
SR −	Negative slew rate			25°C	30	42		30	42		
	Settling time	A_{VD} = −1, 10-V Step	To 0.1%	25°C		0.34			0.34		μs
			To 0.01%			.4			.4		
V_n	Equivalent input noise voltage	R_S = 100 Ω, f = 10 Hz		25°C		15			15		nV/√Hz
		R_S = 100 Ω, f = 1 kHz				10.5			10.5		
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 1 Hz		25°C		0.48			0.48		μV
		f = 0.1 Hz to 10 Hz				0.51			0.51		
I_n	Equivalent input noise current	f = 10 Hz		25°C		1.89			1.89		pA/√Hz
		f = 1 kHz				0.47			0.47		
THD + N	Total harmonic distortion plus noise	$V_{O(PP)}$ = 20 V, R_L = 2 kΩ, A_{VD} = 10, f = 10 kHz		25°C		0.01 %			0.01 %		
B_1	Unity-gain bandwidth	R_L = 2 kΩ, C_L = 100 pF		25°C		6			6		MHz
	Gain-bandwidth product	R_L = 2 kΩ, C_L = 100 pF, f = 100 kHz		25°C		5.9			5.9		MHz
B_{OM}	Maximum output-swing bandwidth	$V_{O(PP)}$ = 20 V, R_L = 2 kΩ, A_{VD} = 1, C_L = 100 pF		25°C		668			668		kHz
ϕ_m	Phase margin at unity gain	R_L = 2 kΩ, C_L = 100 pF		25°C		58°			58°		

electrical characteristics at specified free-air temperature, $V_{CC\pm} = \pm 15$ V, $T_A = 25°C$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	$V_{IC} = 0$, $R_S = 50\ \Omega$, $V_O = 0$			200	1000	µV
I_{IO}	Input offset current				7	100	nA
I_{IB}	Input bias current				−0.7	−1.5	µA
V_{ICR}	Common-mode input voltage range	$R_S = 50\ \Omega$		−15 to 13	−15.3 to 13.2		V
V_{OM+}	Maximum positive peak output voltage swing	$I_O = -150\ \mu A$		13.8	14.1		V
		$I_O = -1.5$ mA		13.7	14		
		$I_O = -15$ mA		13.3	13.7		
V_{OM-}	Maximum negative peak output voltage swing	$I_O = 150\ \mu A$		−14.7	−14.9		V
		$I_O = 1.5$ mA		−14.5	−14.8		
		$I_O = 15$ mA		−13.4	−13.8		
A_{VD}	Large-signal differential voltage amplification	$V_O = \pm 10$ V, $R_L = 2\ k\Omega$		100	450		V/mV
r_i	Input resistance				65		MΩ
c_i	Input capacitance				2.5		pF
z_o	Open-loop output impedance	f = 1 MHz			30		Ω
CMRR	Common-mode rejection ratio	$V_{IC} = V_{ICR}$ min, $R_S = 50\ \Omega$		80	108		dB
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm} / \Delta V_{IO}$)	$V_{CC\pm} = \pm 2.5$ V to ± 15 V, $R_S = 50\ \Omega$		85	106		dB
I_{OS}	Short-circuit output current	$V_O = 0$	$V_{ID} = 1$ V	−25	−50		mA
			$V_{ID} = -1$ V	20	31		
I_{CC}	Supply current	$V_O = 0$, No load			3.5	4.5	mA

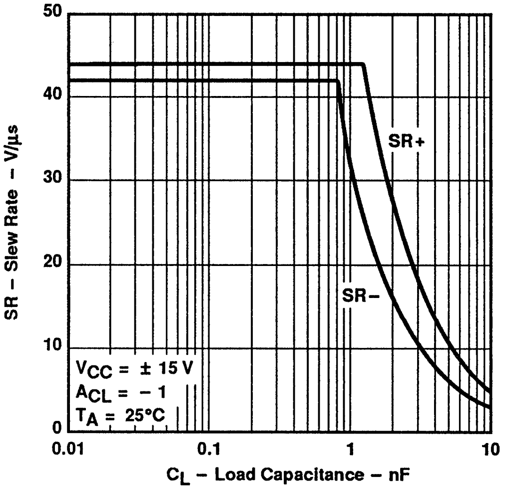
TLE2142, TLE2142A, TLE2142Y
EXCALIBUR LOW-NOISE HIGH-SPEED PRECISION DUAL OPERATIONAL AMPLIFIERS

D3667, DECEMBER 1990

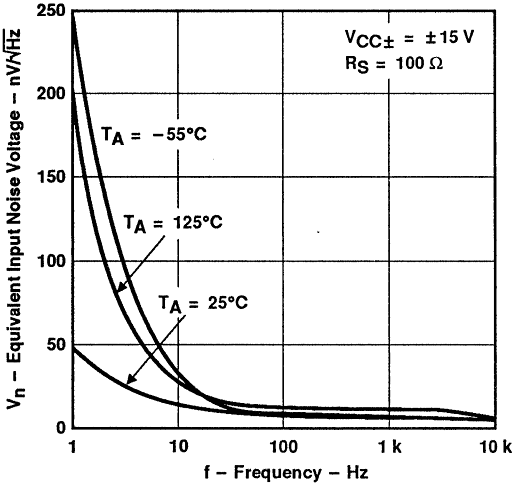
available features

- Low Noise:
  10 Hz . . . 15 nV/√Hz
  1 kHz . . . 10.5 nV/√Hz
- 10,000-pF Load Capability
- 20-mA Min Short-Circuit Output Current
- 30-V/µs Min Slew Rate
- High Gain-Bandwidth Product . . . 5.9 MHz
- Low V_{IO} . . . 750 µV Max at 25°C
- Single or Split Supply . . . 4 V to 44 V
- Fast Settling Time . . . 340 ns to 0.1%
  400 ns to 0.01%
- Saturation Recovery . . . 150 ns
- Large Output Swing . . . V_{CC-} + 0.1 V to V_{CC+} − 1 V

SLEW RATE
vs
LOAD CAPACITANCE



EQUIVALENT INPUT NOISE VOLTAGE
vs
FREQUENCY



description

The TLE2142 and TLE2142A are high-performance internally compensated operational amplifiers built using Texas Instruments complementary bipolar Excalibur process. The TLE2142A is a tighter offset voltage grade of the TLE2142. Both are pin-compatible upgrades to standard industry products.

AVAILABLE OPTIONS

T_A	V_{IO} max AT 25°C	PACKAGE					
		SMALL-OUTLINE (D)	CHIP CARRIER (FK)	CERAMIC DIP (JG)	METAL CAN (L)	PLASTIC DIP (P)	CHIP FORM (Y)
0°C to 70°C	750 µV	TLE2142ACD	—	—	—	TLE2142ACP	TLE2142Y
	1200 µV	TLE2142CD	—	—	—	TLE2142CP	
− 40°C to 105°C	750 µV	TLE2142AID	—	—	—	TLE2142AIP	
	1200 µV	TLE2142ID	—	—	—	TLE2142IP	
− 55°C to 125°C	750 µV	TLE2142AMD	TLE2142AMFK	TLE2142AMJG	TLE2142AML	TLE2142AMP	
	1200 µV	TLE2142MD	TLE2142MFK	TLE2142MJG	TLE2142ML	TLE2142MP	

D packages are available taped and reeled. Add "R" suffix to device type, (e.g., TLE2142ACDR).

description (continued)

The design incorporates a patent-pending input stage that simultaneously achieves low audio band noise of 10.5 nV/$\sqrt{Hz}$ with a 6-Hz 1/f corner and symmetrical 40-V/µs slew rate typically with loads up to 800 pF. The resulting low distortion and high power-bandwidth are important in hi-fi audio applications. A fast settling time of 340 ns to 0.1% of a 10-V step with a 2-kΩ/100-pF load is useful in fast actuator/positioning drivers. Under similar test conditions, settling time to 0.01% is 400 ns.

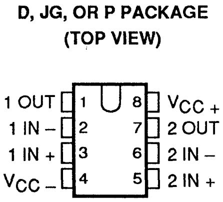
The devices are stable with capacitive loads up to 10 nF, although the 6-MHz bandwidth decreases to 1.8 MHz at this high loading level. As such, the TLE2142 and TLE2142A are useful for low droop sample-and-holds and direct buffering of long cables, including 4 mA to 20 mA current loops.

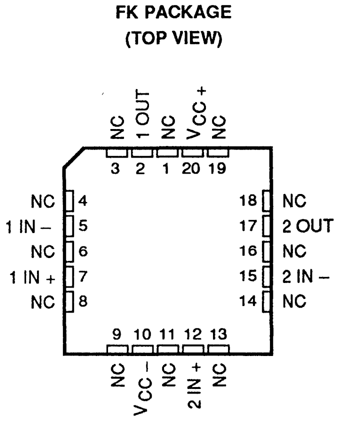
The special design also exhibits an improved insensitivity to inherent IC component mismatches as is evidenced by a 750-µV maximum offset voltage and 1.7-µV/°C typical drift. Minimum common-mode rejection ratio and supply-voltage rejection ratio are 85 dB and 90 dB, respectively.

Device performance is relatively independent of supply voltage over the ±2-V to ±22-V range. Inputs can operate between $V_{CC-}-0.3$ V to $V_{CC+}-1.8$ V without inducing phase reversal, although excessive input current may flow out of each input exceeding the lower common-mode input range. The all-NPN output stage provides a nearly rail-to-rail output swing of $V_{CC-}+0.1$ V to $V_{CC+}-1$ V under light current loading conditions. The device can sustain shorts to either supply since output current is internally limited, but care must be taken to ensure that maximum package power dissipation is not exceeded.

Both versions can also be used as comparators. Differential inputs of $V_{CC\pm}$ can be maintained without damage to the device. Open-loop propagation delay with TTL supply levels is typically 200 ns. This gives a good indication as to output stage saturation recovery when the device is over-driven beyond the limits of recommended output swing.

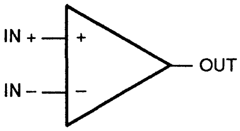
Both the TLE2142 and TLE2142A are available in a wide variety of packages, including both the industry-standard 8-pin small-outline version and chip form for high-density system applications. The C-suffix devices are characterized for operation from 0°C to 70°C, the I-suffix from −40°C to 105°C, and the M-suffix over the full military temperature range of −55°C to 125°C.





NC – No internal connection

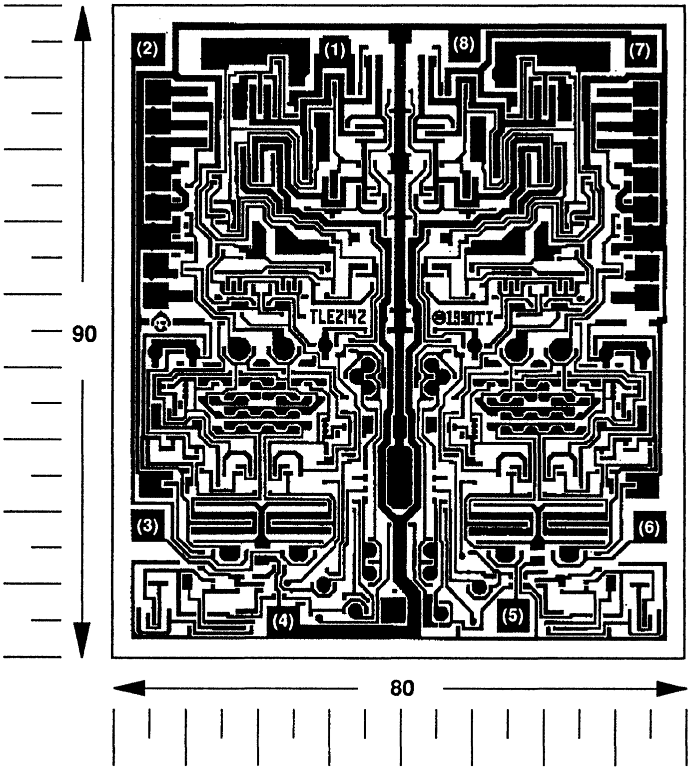
symbol

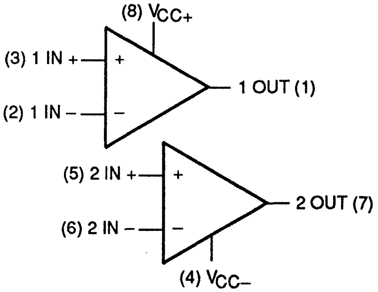


chip information

These chips, properly assembled, display characteristics similar to the TLE2142, (see electrical table on page 18). Thermal compression or ultrasonic bonding may be used on the doped aluminum bonding pads. Chips may be mounted with conductive epoxy or a gold-silicon preform.

BONDING PAD ASSIGNMENTS





CHIP THICKNESS:
15 TYPICAL

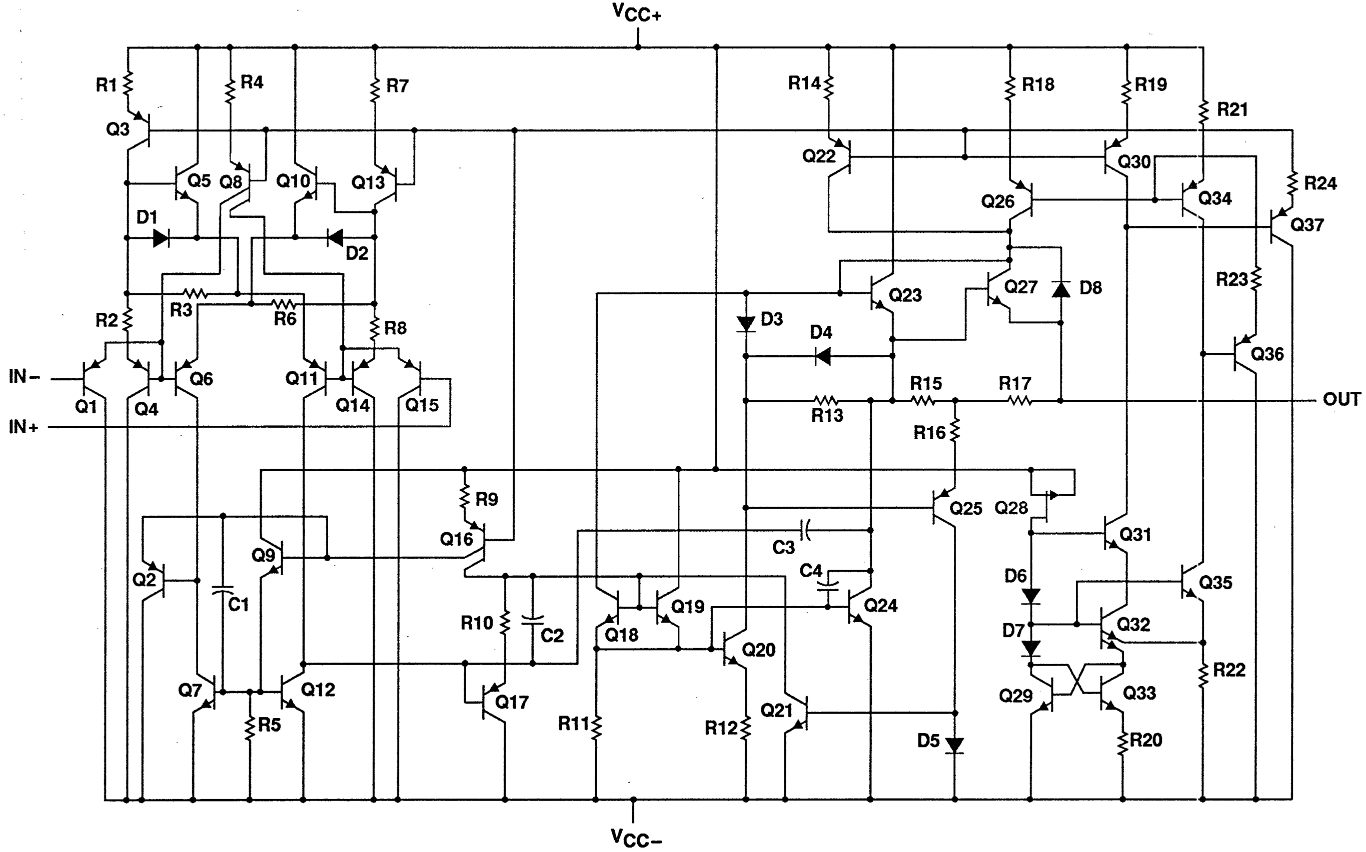
BONDING PADS:
4 X 4 MINIMUM

$T_J$max = 150°C

TOLERANCES
ARE ± 10%

ALL DIMENSIONS
ARE IN MILS

equivalent schematic (per amplifier)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC+} (see Note 1)	22 V
Supply voltage, V_{CC-}	−22 V
Differential input voltage (see Note 2)	V_{CC+} to V_{CC-}
Input voltage range, V_I (any input)	V_{CC+} to $V_{CC-} - 0.3$ V
Input current, I_I (each input)	±1 mA
Output current, I_O	±80 mA
Total current into V_{CC+} terminal	160 mA
Total current out of V_{CC-} terminal	160 mA
Duration of short-circuit current at (or below) 25°C (see Note 3)	unlimited
Continuous total dissipation	See Dissipation Rating Table
Operating free-air temperature range, T_A: C-suffix	0°C to 70°C
I-suffix	−40°C to 105°C
M-suffix	−55°C to 125°C
Storage temperature range	−65°C to 150°C
Case temperature for 60 seconds: FK package	260°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D or P package	260°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: JG or L package	300°C

NOTES: 1. All voltage values, except differential voltages, are with respect to the midpoint between V_{CC+} and V_{CC-}.

2. Differential voltages are at the noninverting input with respect to the inverting input. Excessive current will flow if input is brought below $V_{CC-} - 0.3$ V.

3. The output may be shorted to either supply. Temperature and/or supply voltages must be limited to ensure that the maximum dissipation rating is not exceeded.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 105°C$ POWER RATING	$T_A = 125°C$ POWER RATING
D	725 mW	5.8 mW/°C	464 mW	261 mW	145 mW
FK	1375 mW	11.0 mW/°C	880 mW	495 mW	275 mW
JG	1050 mW	8.4 mW/°C	672 mW	378 mW	210 mW
L	650 mW	5.2 mW/°C	416 mW	234 mW	130 mW
P	1000 mW	8.0 mW/°C	640 mW	360 mW	200 mW

recommended operating conditions

		C-SUFFIX		I-SUFFIX		M-SUFFIX		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
Supply voltage, $V_{CC\pm}$		± 2	± 22	± 2	± 22	± 2	± 22	V
Common-mode input voltage, V_{IC}	$V_{CC} = 5$ V	0	2.9	0	2.7	0	2.7	V
	$V_{CC\pm} = 15$ V	− 15	12.9	− 15	12.7	− 15	12.7	
Operating free-air temperature, T_A		0	70	− 40	105	− 55	125	°C

electrical characteristics at specified free-air temperature, V_{CC} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A†	TLE2142C MIN	TLE2142C TYP	TLE2142C MAX	TLE2142AC MIN	TLE2142AC TYP	TLE2142AC MAX	UNIT
V_{IO}	Input offset voltage	V_O = 2.5 V, R_S = 50 Ω, V_{IC} = 2.5 V	25°C		220	1900		200	1500	μV
			Full range			2200			1800	
α_{VIO}	Temperature coefficient of input offset voltage		Full range		1.7			1.7		μV/°C
I_{IO}	Input offset current		25°C		8	100		8	100	nA
			Full range			150			150	
I_{IB}	Input bias current		25°C		−0.8	−2		−0.8	−2	μA
			Full range			−2.1			−2.1	
V_{ICR}	Common-mode input voltage range	R_S = 50 Ω	25°C	0 to 3	−0.3 to 3.2		0 to 3	−0.3 to 3.2		V
			Full range	0 to 2.9			0 to 2.9			
V_{OH}	High-level output voltage	I_{OH} = −150 μA	25°C	3.9	4.1		3.9	4.1		V
			Full range	3.8			3.8			
		I_{OH} = −1.5 mA	25°C	3.8	4		3.8	4		
			Full range	3.7			3.7			
		I_{OH} = −15 mA	25°C	3.4	3.7		3.4	3.7		
			Full range	3.4			3.4			
V_{OL}	Low-level output voltage	I_{OL} = 150 μA	25°C		75	125		75	125	mV
			Full range			150			150	
		I_{OL} = 1.5 mA	25°C		150	225		150	225	
			Full range			250			250	
		I_{OL} = 15 mA	25°C		1.2	1.4		1.2	1.4	V
			Full range			1.5			1.5	
A_{VD}	Large-signal differential voltage amplification	V_{CC} = ±2.5 V, R_L = 2 kΩ, V_O = 1 V to −1.5 V	25°C	50	220		50	220		V/mV
			Full range	25			25			
r_i	Input resistance		25°C		70			70		MΩ
c_i	Input capacitance		25°C		2.5			2.5		pF
z_o	Open-loop output impedance	f = 1 MHz	25°C		30			30		Ω
CMRR	Common-mode rejection ratio	V_{IC} = V_{ICR} min, R_S = 50 Ω	25°C	85	118		85	118		dB
			Full range	80			80			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm} / \Delta V_{IO}$)	$V_{CC\pm}$ = ±2.5 V to ±15 V, R_S = 50 Ω	25°C	90	106		90	106		dB
			Full range	85			85			
I_{CC}	Supply current	V_O = 2.5 V, No load, V_{IC} = 2.5 V	25°C		6.6	8.8		6.6	8.8	mA
			Full range			9.2			9.2	

† Full range is 0°C to 70°C.

operating characteristics at specified free-air temperature, V_{CC} = 5 V

PARAMETER		TEST CONDITIONS		T_A	TLE2142C			TLE2142AC			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
SR +	Positive slew rate	A_{VD} = − 1, R_L = 2 kΩ†, C_L = 500 pF		25°C		45			45		V/μs
SR −	Negative slew rate					42			42		
	Settling time	A_{VD} = − 1, 2.5-V Step	To 0.1%	25°C		0.16			0.16		μs
			To 0.01%			0.22			0.22		
V_n	Equivalent input noise voltage	R_S = 100 Ω, f = 10 Hz		25°C		15			15		nV/√Hz
		R_S = 100 Ω, f = 1 kHz				10.5			10.5		
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 1 Hz		25°C		0.48			0.48		μV
		f = 0.1 Hz to 10 Hz				0.51			0.51		
I_n	Equivalent input noise current	f = 10 Hz		25°C		1.92			1.92		pA/√Hz
		f = 1 kHz				0.5			0.5		
THD + N	Total harmonic distortion plus noise	V_O = 1 V to 3 V, R_L = 2 kΩ†, A_{VD} = 2, f = 10 kHz		25°C		0.0052 %			0.0052 %		
B_1	Unity-gain bandwidth	R_L = 2 kΩ†, C_L = 100 pF		25°C		5.9			5.9		MHz
	Gain-bandwidth product	R_L = 2 kΩ†, C_L = 100 pF, f = 100 kHz		25°C		5.8			5.8		MHz
B_{OM}	Maximum output-swing bandwidth	R_L = 2 kΩ†, $V_{O(PP)}$ = 2 V, A_{VD} = 1, C_L = 100 pF		25°C		6.6			6.6		MHz
ϕ_m	Phase margin at unity-gain	R_L = 2 kΩ†, C_L = 100 pF		25°C		57°			57°		

† Note: R_L terminates at 2.5 V.

electrical characteristics at specified free-air temperature, $V_{CC\pm} = \pm 15$ V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A†	TLE2142C			TLE2142AC			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	$V_{IC} = 0$, $R_S = 50\ \Omega$, $V_O = 0$	25°C		290	1200		275	750	µV
			Full range			1600			1200	
α_{VIO}	Temperature coefficient of input offset voltage		Full range		1.7			1.7		µV/°C
I_{IO}	Input offset current		25°C		7	100		7	100	nA
			Full range			150			150	
I_{IB}	Input bias current		25°C		−0.7	−1.5		−0.7	−1.5	µA
			Full range			−1.6			−1.6	
V_{ICR}	Common-mode input voltage range	$R_S = 50\ \Omega$	25°C	−15 to 13	−15.3 to 13.2		−15 to 13	−15.3 to 13.2		V
			Full range	−15 to 12.9	−15.3 to 13.1		−15 to 12.9	−15.3 to 13.1		
V_{OM+}	Maximum positive peak output voltage swing	$I_O = -150\ \mu A$	25°C	13.8	14.1		13.8	14.1		V
			Full range	13.7			13.7			
		$I_O = -1.5$ mA	25°C	13.7	14		13.7	14		
			Full range	13.6			13.6			
		$I_O = -15$ mA	25°C	13.3	13.7		13.3	13.7		
			Full range	13.2			13.2			
V_{OM-}	Maximum negative peak output voltage swing	$I_O = 150\ \mu A$	25°C	−14.7	−14.9		−14.7	−14.9		V
			Full range	−14.6			−14.6			
		$I_O = 1.5$ mA	25°C	−14.5	−14.8		−14.5	−14.8		
			Full range	−14.4			−14.4			
		$I_O = 15$ mA	25°C	−13.4	−13.8		−13.4	−13.8		
			Full range	−13.3			−13.3			
A_{VD}	Large-signal differential voltage amplification	$V_O = \pm 10$ V	25°C	100	450		100	450		V/mV
			Full range	75			75			
r_i	Input resistance	$R_L = 2\ k\Omega$	25°C		65			65		MΩ
c_i	Input capacitance		25°C		2.5			2.5		pF
z_o	Open-loop output impedance	f = 1 MHz	25°C		30			30		Ω
CMRR	Common-mode rejection ratio	$V_{IC} = V_{ICR}$ min, $R_S = 50\ \Omega$	25°C	85	108		85	108		dB
			Full range	80			80			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm} / \Delta V_{IO}$)	$V_{CC\pm} = \pm 2.5$ V to ± 15 V, $R_S = 50\ \Omega$	25°C	90	106		90	106		dB
			Full range	85			85			
I_{OS}	Short-circuit output current	$V_O = 0$, $V_{ID} = 1$ V	25°C	−25	−50		−25	−50		mA
		$V_{ID} = -1$ V		20	31		20	31		
I_{CC}	Supply current	$V_O = 0$, No load	25°C		6.9	9		6.9	9	mA
			Full range			9.4			9.4	

† Full range is 0°C to 70°C.

operating characteristics at specified free-air temperature, $V_{CC\pm}$ = ±15 V

PARAMETER		TEST CONDITIONS		T_A	TLE2142C			TLE2142AC			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
SR +	Positive slew rate	A_{VD} = −1, R_L = 2 kΩ, C_L = 500 pF		25°C	30	45		30	45		V/μs
SR −	Negative slew rate			25°C	30	42		30	42		
	Settling time	A_{VD} = −1, 10-V Step	To 0.1%	25°C		0.34			0.34		μs
			To 0.01%			0.4			0.4		
V_n	Equivalent input noise voltage	R_S = 100 Ω, f = 10 Hz		25°C		15			15		nV/√Hz
		R_S = 100 Ω, f = 1 kHz				10.5			10.5		
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 1 Hz		25°C		0.48			0.48		μV
		f = 0.1 Hz to 10 Hz				0.51			0.51		
I_n	Equivalent input noise current	f = 10 Hz		25°C		1.89			1.89		pA/√Hz
		f = 1 kHz				0.47			0.47		
THD + N	Total harmonic distortion plus noise	V_O = 20 V_{PP}, R_L = 2 kΩ, A_{VD} = 10, f = 10 kHz		25°C		0.01%			0.01%		
B_1	Unity-gain bandwidth	R_L = 2 kΩ, C_L = 100 pF		25°C		6			6		MHz
	Gain-bandwidth product	R_L = 2 kΩ, C_L = 100 pF, f = 100 kHz		25°C		5.9			5.9		MHz
B_{OM}	Maximum output-swing bandwidth	$V_{O(PP)}$ = 20 V, R_L = 2 kΩ, A_{VD} = 1, C_L = 100 pF		25°C		668			668		kHz
ϕ_m	Phase margin at unity gain	R_L = 2 kΩ, C_L = 100 pF		25°C		58°			58°		

electrical characteristics at specified free-air temperature, V_{CC} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A†	TLE2142I			TLE2142AI			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_O = 2.5 V, R_S = 50 Ω, V_{IC} = 2.5 V	25°C		220	1900		220	1500	μV
			Full range			2400			2000	
α_{VIO}	Temperature coefficient of input offset voltage		Full range		1.7			1.7		μV/°C
I_{IO}	Input offset current		25°C		8	100		8	100	nA
			Full range			200			200	
I_{IB}	Input bias current		25°C		− 0.8	− 2		− 0.8	− 2	μA
			Full range			− 2.2			− 2.2	
V_{ICR}	Common-mode input voltage range	R_S = 50 Ω	25°C	0 to 3	− 0.3 to 3.2		0 to 3	− 0.3 to 3.2		V
			Full range	0 to 2.7	− 0.3 to 2.9		0 to 2.7	− 0.3 to 2.9		
V_{OH}	High-level output voltage	I_{OH} = − 150 μA	25°C	3.9	4.1		3.9	4.1		V
		I_{OH} = − 1.5 mA		3.8	4		3.8	4		
		I_{OH} = − 15 mA		3.4	3.7		3.4	3.7		
		I_{OH} = 100 μA	Full range	3.8			3.8			
		I_{OH} = 1 mA		3.7			3.7			
		I_{OH} = 10 mA		3.5			3.5			
V_{OL}	Low-level output voltage	I_{OL} = 150 μA	25°C		75	125		75	125	mV
		I_{OL} = 1.5 mA			150	225		150	225	
		I_{OL} = 15 mA			1.2	1.4		1.2	1.4	V
		I_{OL} = 100 μA	Full range			175			175	mV
		I_{OL} = 1 mA				225			225	
		I_{OL} = 10 mA				1.2			1.2	V
A_{VD}	Large-signal differential voltage amplification	V_{CC} = ± 2.5 V, R_L = 2 kΩ, V_O = 1 V to − 1.5 V	25°C	50	220		50	220		V/mV
			Full range	10			10			
r_i	Input resistance		25°C		70			70		MΩ
c_i	Input capacitance		25°C		2.5			2.5		pF
z_o	Open-loop output impedance	f = 1 MHz	25°C		30			30		Ω
CMRR	Common-mode rejection ratio	V_{IC} = V_{ICR} min, R_S = 50 Ω	25°C	85	118		85	118		dB
			Full range	80			80			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm} / \Delta V_{IO}$)	$V_{CC\pm}$ = ± 2.5 V to ± 15 V, R_S = 50 Ω	25°C	90	106		90	106		dB
			Full range	85			85			
I_{CC}	Supply current	V_O = 2.5 V, No load V_{IC} = 2.5 V	25°C		6.6	8.8		6.6	8.8	mA
			Full range			9.2			9.2	

† Full range is − 40°C to 105°C.

operating characteristics at specified free-air temperature, V_{CC} = 5 V

PARAMETER		TEST CONDITIONS	T_A	TLE2142I			TLE2142AI			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
SR +	Positive slew rate	A_{VD} = −1, R_L = 2 kΩ†, C_L = 500 pF	25°C		45			45		V/μs
SR −	Negative slew rate				42			42		
	Settling time	A_{VD} = −1, 2.5-V Step, To 0.1%	25°C		0.16			0.16		μs
		To 0.01%			0.22			0.22		
V_n	Equivalent input noise voltage	R_S = 100 Ω, f = 10 Hz	25°C		15			15		nV/√Hz
		R_S = 100 Ω, f = 1 kHz			10.5			10.5		
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 1 Hz	25°C		0.48			0.48		μV
		f = 0.1 Hz to 10 Hz			0.51			0.51		
I_n	Equivalent input noise current	f = 10 Hz	25°C		1.92			1.92		pA/√Hz
		f = 1 kHz			0.5			0.5		
THD + N	Total harmonic distortion plus noise	V_O = 1 V to 3 V, R_L = 2 kΩ†, A_{VD} = 2, f = 10 kHz	25°C		0.0052 %			0.0052 %		
B_1	Unity-gain bandwidth	R_L = 2 kΩ†, C_L = 100 pF	25°C		5.9			5.9		MHz
	Gain-bandwidth product	R_L = 2 kΩ†, C_L = 100 pF, f = 100 kHz	25°C		5.8			5.8		MHz
B_{OM}	Maximum output-swing bandwidth	R_L = 2 kΩ†, $V_{O(PP)}$ = 2 V, A_{VD} = 1, C_L = 100 pF	25°C		6.6			6.6		MHz
ϕ_m	Phase margin at unity-gain	R_L = 2 kΩ†, C_L = 100 pF	25°C		57°			57°		

† Note: R_L terminates at 2.5 V.

electrical characteristics at specified free-air temperature, $V_{CC\pm}$ = ± 15 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A†	TLE2142I			TLE2142AI			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_{IC} = 0, R_S = 50 Ω, V_O = 0	25°C		290	1200		275	750	µV
			Full range			1800			1400	
α_{VIO}	Temperature coefficient of input offset voltage		Full range		1.7			1.7		µV/°C
I_{IO}	Input offset current		25°C		7	100		7	100	nA
			Full range			200			200	
I_{IB}	Input bias current		25°C		− 0.7	− 1.5		− 0.7	− 1.5	µA
			Full range			− 1.7			− 1.7	
V_{ICR}	Common-mode input voltage range	R_S = 50 Ω	25°C	− 15 to 13	− 15.3 to 13.2		− 15 to 13	− 15.3 to 13.2		V
			Full range	− 15 to 12.7	− 15.3 to 12.9		− 15 to 12.7	− 15.3 to 12.9		
V_{OM+}	Maximum positive peak output voltage swing	I_O = − 150 µA,	25°C	13.8	14.1		13.8	14.1		V
		I_O = − 1.5 mA,		13.7	14		13.7	14		
		I_O = − 15 mA		13.3	13.7		13.3	13.7		
		I_O = − 100 µA,	Full range	13.7			13.7			
		I_O = − 1 mA,		13.6			13.6			
		I_O = − 10 mA		13.3			13.3			
V_{OM-}	Maximum negative peak output voltage swing	I_O = 150 µA,	25°C	− 14.7	− 14.9		− 14.7	− 14.9		V
		I_O = 1.5 mA,		− 14.5	− 14.8		− 14.5	− 14.8		
		I_O = 15 mA		− 13.4	− 13.8		− 13.4	− 13.8		
		I_O = 100 µA,	Full range	− 14.6			− 14.6			
		I_O = 1 mA,		− 14.5			− 14.5			
		I_O = 10 mA		− 13.4			− 13.4			
A_{VD}	Large-signal differential voltage amplification	V_O = ± 10 V, R_L = 2 kΩ	25°C	100	450		100	450		V/mV
			Full range	40			40			
r_i	Input resistance		25°C		65			65		MΩ
c_i	Input capacitance		25°C		2.5			2.5		pF
z_o	Open-loop output impedance	f = 1 MHz	25°C		30			30		Ω
CMRR	Common-mode rejection ratio	V_{IC} = V_{ICR} min	25°C	85	108		85	108		dB
		R_S = 50 Ω	Full range	80			80			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm} / \Delta V_{IO}$)	$V_{CC\pm}$ = ± 2.5 V to ± 15 V,	25°C	90	106		90	106		dB
		R_S = 50 Ω	Full range	85			85			
I_{OS}	Short-circuit output current	V_O = 0, V_{ID} = 1 V	25°C	− 25	− 50		− 25	− 50		mA
		V_{ID} = − 1 V		20	31		20	31		
I_{CC}	Supply current	V_O = 0, No load	25°C		6.9	9		6.9	9	mA
			Full range			9.4			9.4	

† Full range is −40°C to 105°C.

operating characteristics at specified free-air temperature, $V_{CC\pm} = \pm 15$ V

PARAMETER		TEST CONDITIONS	T_A	TLE2142I			TLE2142AI			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
SR +	Positive slew rate	$A_{VD} = -1$, $R_L = 2\ k\Omega$, $C_L = 500$ pF	25°C	30	45		30	45		V/μs
SR −	Negative slew rate		25°C	30	42		30	42		
	Settling time	$A_{VD} = -1$, 10-V Step, To 0.1%	25°C		0.34			0.34		μs
		$A_{VD} = -1$, 10-V Step, To 0.01%			0.4			0.4		
V_n	Equivalent input noise voltage	$R_S = 100\ \Omega$, f = 10 Hz	25°C		15			15		nV/√Hz
		$R_S = 100\ \Omega$, f = 1 kHz			10.5			10.5		
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 1 Hz	25°C		0.48			0.48		μV
		f = 0.1 Hz to 10 Hz			0.51			0.51		
I_n	Equivalent input noise current	f = 10 Hz	25°C		1.89			1.89		pA/√Hz
		f = 1 kHz			0.47			0.47		
THD + N	Total harmonic distortion plus noise	$V_{O(PP)} = 20$ V, $R_L = 2\ k\Omega$, $A_{VD} = 10$, f = 10 kHz	25°C		0.01%			0.01%		
B_1	Unity-gain bandwidth	$R_L = 2\ k\Omega$, $C_L = 100$ pF	25°C		6			6		MHz
	Gain-bandwidth product	$R_L = 2\ k\Omega$, $C_L = 100$ pF, f = 100 kHz	25°C		5.9			5.9		MHz
B_{OM}	Maximum output-swing bandwidth	$V_{O(PP)} = 20$ V, $R_L = 2\ k\Omega$, $A_{VD} = 1$, $C_L = 100$ pF	25°C		668			668		kHz
ϕ_m	Phase margin at unity gain	$R_L = 2\ k\Omega$, $C_L = 100$ pF	25°C		58°			58°		

electrical characteristics at specified free-air temperature, V_{CC} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A†	TLE2142M			TLE2142AM			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_O = 2.5 V, R_S = 50 Ω, V_{IC} = 2.5 V	25°C		220	1900		200	1500	μV
			Full range			2600			2200	
α_{VIO}	Temperature coefficient of input offset voltage		Full range		1.7			1.7		μV/°C
I_{IO}	Input offset current		25°C		8	100		8	100	nA
			Full range			250			250	
I_{IB}	Input bias current		25°C		−0.8	−2		−0.8	−2	μA
			Full range			−2.3			−2.3	
V_{ICR}	Common-mode input voltage range	R_S = 50 Ω	25°C	0 to 3	−0.3 to 3.2		0 to 3	−0.3 to 3.2		V
			Full range	0 to 2.7	−0.3 to 2.9		0 to 2.7	−0.3 to 2.9		
V_{OH}	High-level output voltage	I_{OH} = −150 μA	25°C	3.9	4.1		3.9	4.1		V
		I_{OH} = −1.5 mA		3.8	4		3.8	4		
		I_{OH} = −15 mA		3.4	3.7		3.4	3.7		
		I_{OH} = 100 μA	Full range	3.75			3.75			
		I_{OH} = 1 mA		3.65			3.65			
		I_{OH} = 10 mA		3.45			3.45			
V_{OL}	Low-level output voltage	I_{OL} = 150 μA	25°C		75	125		75	125	mV
		I_{OL} = 1.5 mA			150	225		150	225	
		I_{OL} = 15 mA			1.2	1.4		1.2	1.4	V
		I_{OL} = 100 μA	Full range			200			200	mV
		I_{OL} = 1 mA				250			250	
		I_{OL} = 10 mA				1.25			1.25	V
A_{VD}	Large-signal differential voltage amplification	V_{CC} = ±2.5 V, R_L = 2 kΩ, V_O = 1 V to −1.5 V	25°	50	220		50	220		V/mV
			Full range	5			5			
r_i	Input resistance		25°C		70			70		MΩ
c_i	Input capacitance		25°C		2.5			2.5		pF
z_o	Open-loop output impedance	f = 1 MHz	25°C		30			30		Ω
CMRR	Common-mode rejection ratio	V_{IC} = V_{ICR} min, R_S = 50 Ω	25°C	85	118		85	118		dB
			Full range	80			80			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm}/\Delta V_{IO}$)	$V_{CC\pm}$ = ±2.5 V to ±15 V, R_S = 50 Ω	25°C	90	106		90	106		dB
			Full range	85			85			
I_{CC}	Supply current	V_O = 2.5 V, No load V_{IC} = 2.5 V	25°C		6.6	8.8		6.6	8.8	mA
			Full range			9.2			9.2	

† Full range is −55°C to 125°C.

operating characteristics, V_{CC} = 5 V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A	TLE2142M			TLE2142AM			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
SR +	Positive slew rate	A_{VD} = −1, R_L = 2 kΩ,† C_L = 500 pF	25°C		45			45		V/μs
SR −	Negative slew rate				42			42		
V_n	Settling time	A_{VD} = −1, 2.5-V Step, To 0.1%	25°C		0.16			0.16		μs
		To 0.01%			0.22			0.22		
$V_{N(PP)}$	Equivalent input noise voltage	R_S = 100 Ω, f = 10 Hz	25°C		15			15		nV/√Hz
		R_S = 100 Ω, f = 1 kHz			10.5			10.5		
I_n	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 1 Hz	25°C		0.48			0.48		μV
		f = 0.1 Hz to 10 Hz			0.51			0.51		
THD + N	Equivalent input noise current	f = 10 Hz	25°C		1.92			1.92		pA/√Hz
		f = 1 kHz			0.5			0.5		
B_1	Total harmonic distortion plus noise	V_O = 1 V to 3 V, R_L = 2 kΩ†, A_{VD} = 2, f = 10 kHz	25°C		0.0052%			0.0052%		
	Unity-gain bandwidth	R_L = 2 kΩ†, C_L = 100 pF	25°C		5.9			5.9		MHz
B_{OM}	Gain-bandwidth product	R_L = 2 kΩ†, C_L = 100 pF, f = 100 kHz	25°C		5.8			5.8		MHz
ϕ_m	Maximum output-swing bandwidth	R_L = 2 kΩ†, $V_{O(PP)}$ = 2 V, A_{VD} = 1	25°C		6.6			6.6		MHz
	Phase margin	R_L = 2 kΩ†, C_L = 100 pF			57°			57°		

† R_L terminates at 2.5 V.

electrical characteristics at specified free-air temperature, $V_{CC\pm}$ = ±15 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A†	TLE2142M			TLE2142AM			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_{IC} = 0, R_S = 50 Ω,		25°C		290	1200		275	750	μV
				Full range			2000			1600	
α_{VIO}	Temperature coefficient of input offset voltage			Full range		1.7			1.7		μV/°C
I_{IO}	Input offset current			25°C		7	100		7	100	nA
				Full range			250			250	
I_{IB}	Input bias current			25°C		−0.7	−1.5		−0.7	−1.5	μA
				Full range			−1.8			−1.8	
V_{ICR}	Common-mode input voltage range	R_S = 50 Ω		25°C	−15 to 13	−15.3 to 13.2		−15 to 13	−15.3 to 13.2		V
				Full range	−15 to 12.7	−15.3 to 12.9		−15 to 12.7	−15.3 to 12.9		
V_{OM+}	Maximum positive peak output voltage swing	I_O = −150 μA		25°C	13.8	14.1		13.8	14.1		V
		I_O = −1.5 mA			13.7	14		13.7	14		
		I_O = −15 mA			13.3	13.7		13.3	13.7		
		I_O = −100 μA		Full range	13.7			13.7			
		I_O = −1 mA			13.6			13.6			
		I_O = −10 mA			13.3			13.3			
V_{OM-}	Maximum negative peak output voltage swing	I_O = 150 μA		25°C	−14.7	−14.9		−14.7	−14.9		V
		I_O = 1.5 mA			−14.5	−14.8		−14.5	−14.8		
		I_O = 15 mA			−13.4	−13.8		−13.4	−13.8		
		I_O = 100 μA		Full range	−14.6			−14.6			
		I_O = 1 mA			−14.5			−14.5			
		I_O = 10 mA			−13.4			−13.4			
A_{VD}	Large-signal differential voltage amplification	V_O = ±10 V, R_L = 2 kΩ		25°C	100	450		100	450		V/mV
				Full range	20			20			
r_i	Input resistance			25°C		65			65		MΩ
c_i	Input capacitance			25°C		2.5			2.5		pF
z_o	Open-loop output impedance	f = 1 MHz		25°C		30			30		Ω
CMRR	Common-mode rejection ratio	V_{IC} = V_{ICR} min, R_S = 50 Ω		25°C	85	108		85	108		dB
				Full range	80			80			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm}/\Delta V_{IO}$)	$V_{CC\pm}$ = ±2.5 V to ±15 V, R_S = 50 Ω		25°C	90	106		90	106		dB
				Full range	85			85			
I_{OS}	Short-circuit output current	V_O = 0	V_{ID} = 1 V	25°C	−25	−50		−25	−50		mA
			V_{ID} = −1 V		20	31		20	31		
I_{CC}	Supply current	V_O = 0, No load, V_{IC} = 2.5 V		25°C		6.9	9		6.9	9	mA
				Full range			9.4			9.4	

† Full range is −55°C to 125°C.

operating characteristics, $V_{CC\pm}$ = ±15 V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A	TLE2142M			TLE2142AM			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
SR +	Positive slew rate	R_L = 2 kΩ, A_{VD} = −1,		25°C	30	45		30	45		V/μs
SR −	Negative slew rate	C_L = 100 pF		25°C	30	42		30	42		
	Settling time	A_{VD} = −1,	To 0.1%	25°C		0.34			0.34		μs
		10-V Step	To 0.01%			.4			.4		
V_n	Equivalent input noise voltage	R_S = 100 Ω, f = 10 Hz		25°C		15			15		nV/√Hz
		R_S = 100 Ω, f = 1 kHz				10.5			10.5		
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 1 Hz		25°C		0.48			0.48		μV
		f = 0.1 Hz to 10 Hz				0.51			0.51		
I_n	Equivalent input noise current	f = 10 Hz		25°C		1.89			1.89		pA/√Hz
		f = 1 kHz				0.47			0.47		
THD + N	Total harmonic distortion plus noise	$V_{O(PP)}$ = 20 V, R_L = 2 kΩ, A_{VD} = 10, f = 10 kHz		25°C		0.01 %			0.01 %		
B_1	Unity-gain bandwidth	R_L = 2 kΩ, C_L = 100 pF		25°C		6			6		MHz
	Gain-bandwidth product	R_L = 2 kΩ, C_L = 100 pF, f = 100 kHz		25°C		5.9			5.9		MHz
B_{OM}	Maximum output-swing bandwidth	$V_{O(PP)}$ = 20 V, R_L = 2 kΩ, A_{VD} = 1, C_L = 100 pF		25°C		668			668		kHz
ϕ_m	Phase margin at unity gain	R_L = 2 kΩ, C_L = 100 pF		25°C		58°			58°		

electrical characteristics at specified free-air temperature, $V_{CC\pm}$ = ±15 V, T_A = 25°C

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	V_{IC} = 0, R_S = 50 Ω, V_O = 0			150	875	μV
I_{IO}	Input offset current				7	100	nA
I_{IB}	Input bias current				−0.7	−1.5	μA
V_{ICR}	Common-mode input voltage range	R_S = 50 Ω		−15 to 13	−15.3 to 13.2		V
V_{OM+}	Maximum positive peak output voltage swing	I_O = −150 μA		13.8	14.1		V
		I_O = −1.5 mA		13.7	14		
		I_O = −15 mA		13.3	13.7		
V_{OM-}	Maximum negative peak output voltage swing	I_O = 150 μA		−14.7	−14.9		V
		I_O = 1.5 mA		−14.5	−14.8		
		I_O = 15 mA		−13.4	−13.8		
A_{VD}	Large-signal differential voltage amplification	V_O = ±10 V, R_L = 2 kΩ		100	450		V/mV
r_i	Input resistance				65		MΩ
c_i	Input capacitance				2.5		pF
z_o	Open-loop output impedance	f = 1 MHz			30		Ω
CMRR	Common-mode rejection ratio	V_{IC} = V_{ICR} min, R_S = 50 Ω		80	108		dB
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm} / \Delta V_{IO}$)	$V_{CC\pm}$ = ±2.5 V to ±15 V, R_S = 50 Ω		85	106		dB
I_{OS}	Short-circuit output current	V_O = 0	V_{ID} = 1 V	−25	−50		mA
			V_{ID} = −1 V	20	31		
I_{CC}	Supply current	V_O = 0, No load			6.9	9.0	mA

TYPICAL CHARACTERISTICS

	TABLE OF GRAPHS			FIGURE
V_{IO}	Input offset voltage		Distribution	1
I_{IO}	Input offset current		vs Temperature	2
I_{IB}	Input bias current		vs Temperature	3
			vs Common-mode voltage	4
V_{OM+}	Maximum positive peak output voltage		vs Supply voltage	5
			vs Temperature	6
			vs Output current	7
			vs Settling time	9
V_{OM-}	Maximum negative peak output voltage		vs Supply voltage	5
			vs Temperature	6
			vs Output current	8
			vs Settling time	9
$V_{O(PP)}$	Maximum peak-to-peak output voltage swing		vs Frequency	10
V_{OH}	High-level output voltage		vs Output current	11
V_{OL}	Low-level output voltage		vs Output current	12
A_{VD}	Differential voltage amplification		vs Temperature	13
			vs Frequency	14
z_o	Closed loop output impedance		vs Frequency	15
I_{OS}	Short-circuit output current		vs Temperature	16
CMRR	Common-mode rejection ratio		vs Frequency	17
			vs Temperature	18
k_{SVR}	Supply-voltage rejection ratio		vs Frequency	19
			vs Temperature	20
I_{CC}	Supply current		vs Temperature	21
			vs Supply-voltage	22
V_N	Noise voltage		vs Frequency	23
V_{NPP}	Noise voltage		Over a 10-second period	24
I_n	Equivalent input noise current		vs Frequency	25
THD + N	Total harmonic distortion plus noise		vs Frequency	26
SR	Slew rate		vs Temperature	27
			vs Load capacitance	28
	Pulse response	Noninverting large-signal	vs Time	29
		Inverting large-signal	vs Time	30
		Small-signal	vs Time	31
B_1	Unity-gain bandwidth		vs Load capacitance	32
	Gain margin		vs Load capacitance	33
ϕ_m	Phase margin		vs Load capacitance	34
	Phase shift		vs Frequency	14

TYPICAL CHARACTERISTICS†

TLE2142 DISTRIBUTION OF INPUT OFFSET VOLTAGE

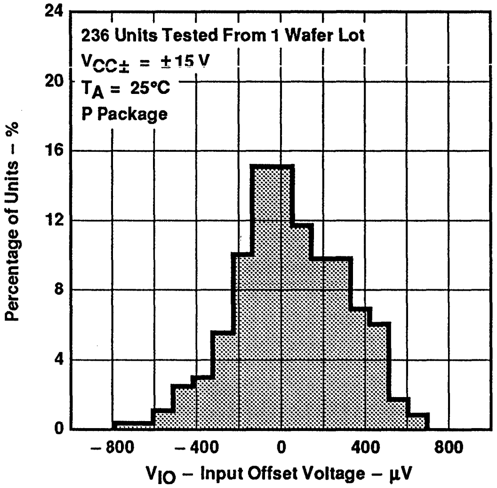


Figure 1

INPUT OFFSET CURRENT vs FREE-AIR TEMPERATURE

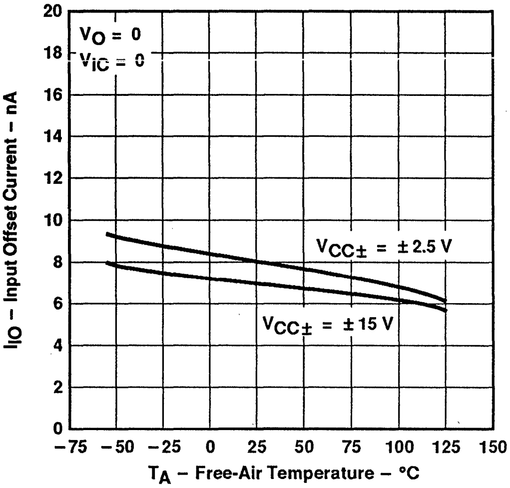


Figure 2

INPUT BIAS CURRENT vs FREE-AIR TEMPERATURE

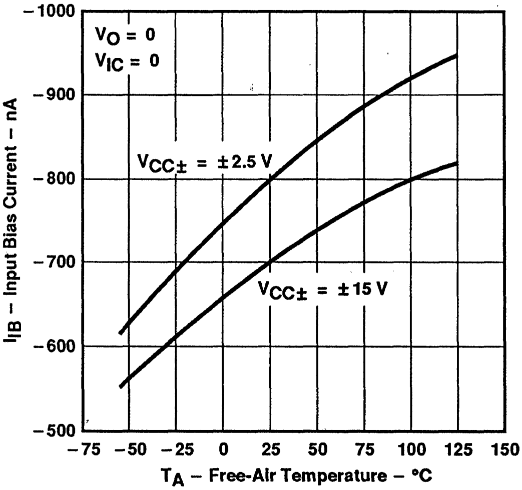


Figure 3

INPUT BIAS CURRENT vs COMMON-MODE INPUT VOLTAGE

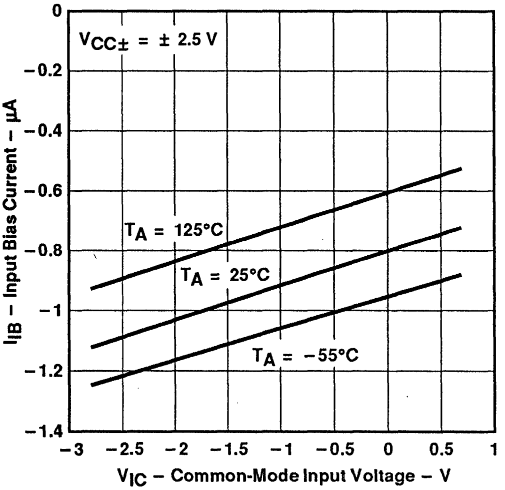


Figure 4

---

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

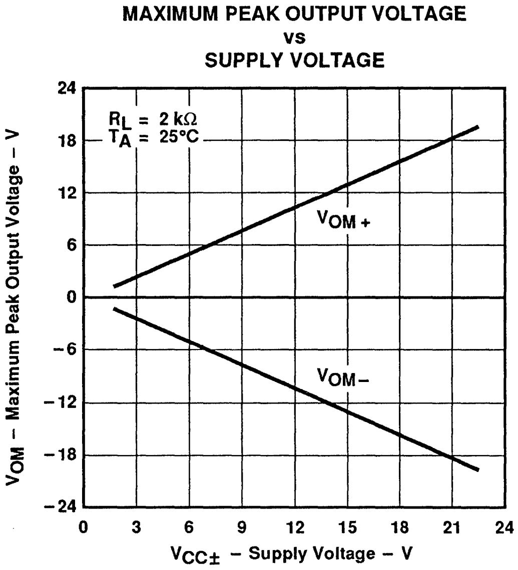

MAXIMUM PEAK OUTPUT VOLTAGE
vs
SUPPLY VOLTAGE

Figure 5

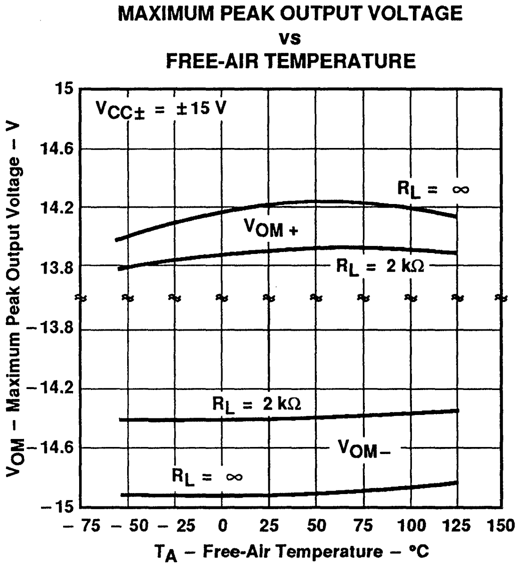

MAXIMUM PEAK OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

Figure 6

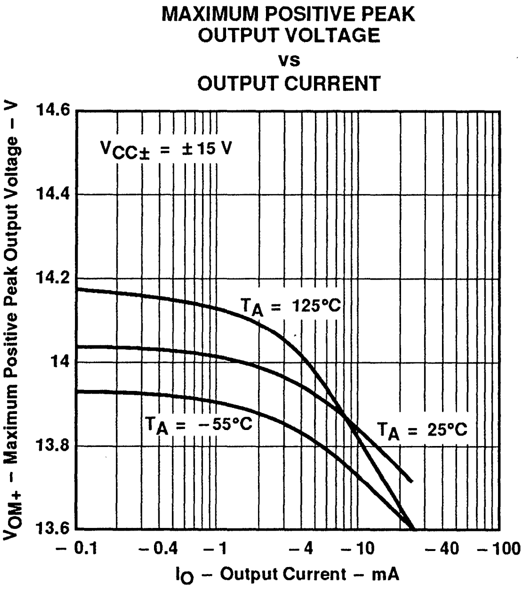

MAXIMUM POSITIVE PEAK
OUTPUT VOLTAGE
vs
OUTPUT CURRENT

Figure 7

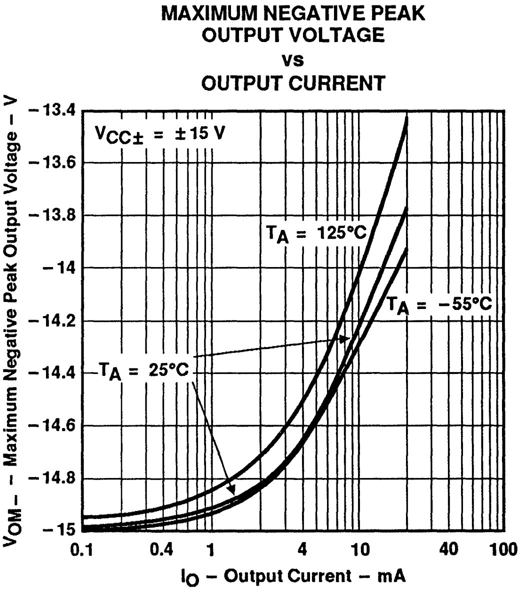

MAXIMUM NEGATIVE PEAK
OUTPUT VOLTAGE
vs
OUTPUT CURRENT

Figure 8

---

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

MAXIMUM PEAK OUTPUT VOLTAGE vs SETTLING TIME

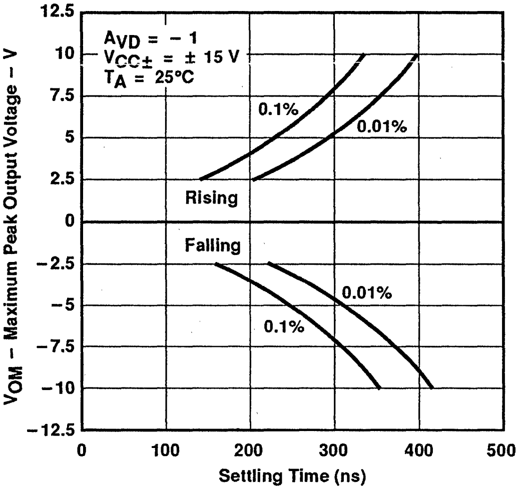


Figure 9

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE vs FREQUENCY

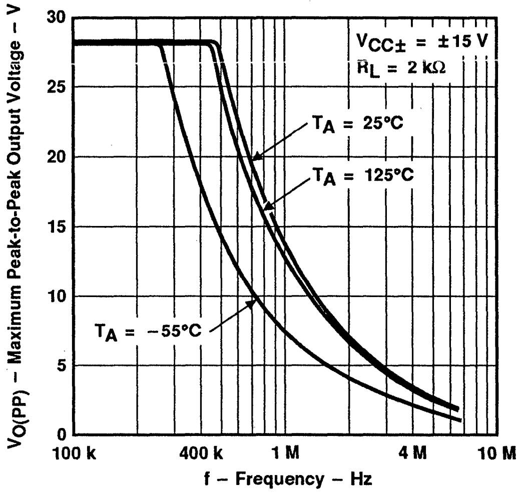


Figure 10

HIGH-LEVEL OUTPUT VOLTAGE vs OUTPUT CURRENT

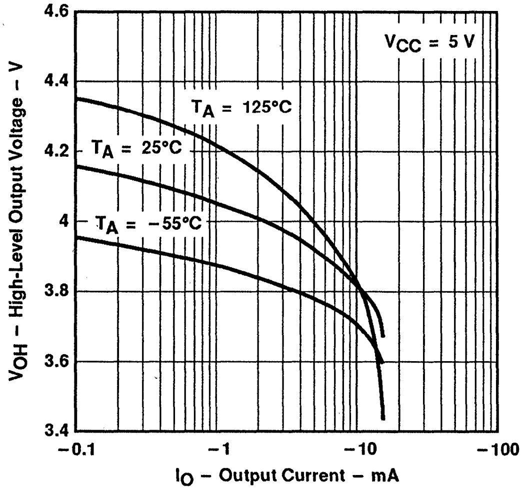


Figure 11

LOW-LEVEL OUTPUT VOLTAGE vs OUTPUT CURRENT

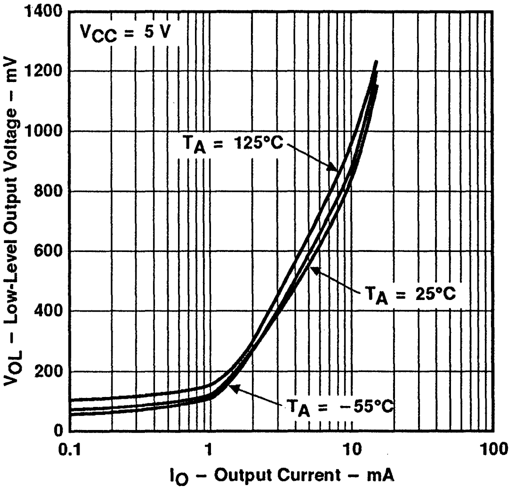


Figure 12

---

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION vs FREE-AIR TEMPERATURE

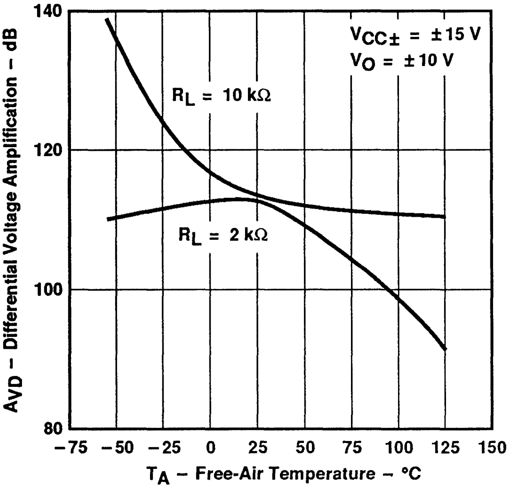


Figure 13

LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION AND PHASE SHIFT vs FREQUENCY

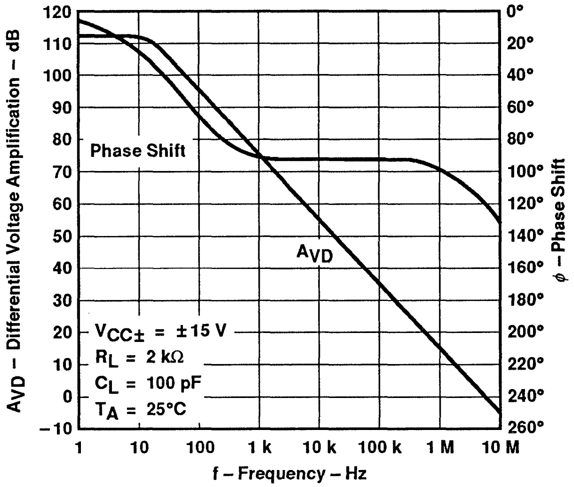


Figure 14

CLOSED-LOOP OUTPUT IMPEDANCE vs FREQUENCY

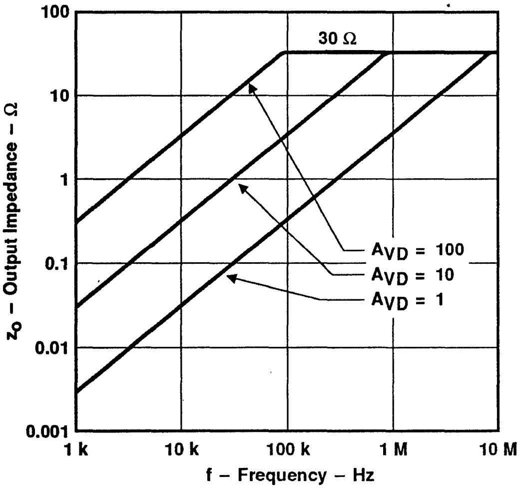


Figure 15

SHORT-CIRCUIT OUTPUT CURRENT vs FREE-AIR TEMPERATURE

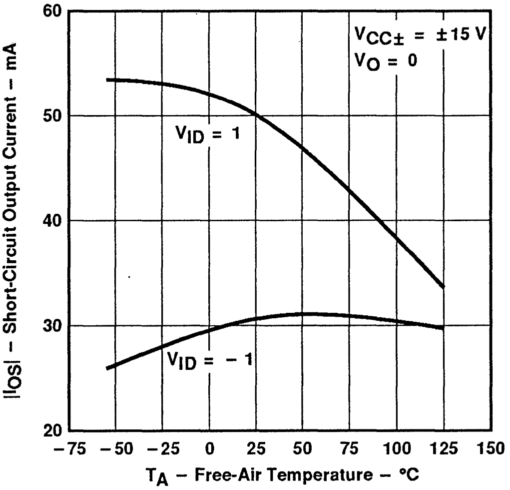


Figure 16

---

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

COMMON-MODE REJECTION RATIO vs FREQUENCY

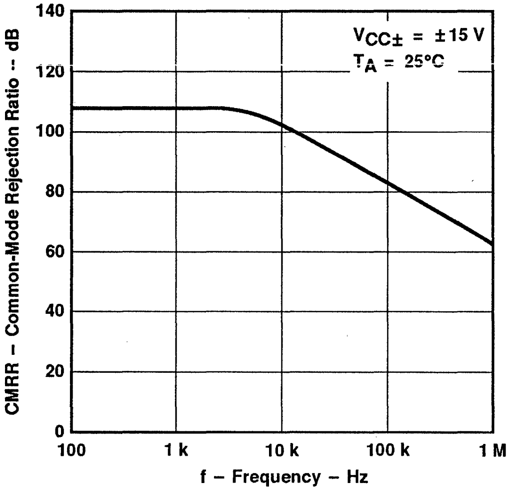


Figure 17

COMMON-MODE REJECTION RATIO vs FREQUENCY FREE-AIR TEMPERATURE

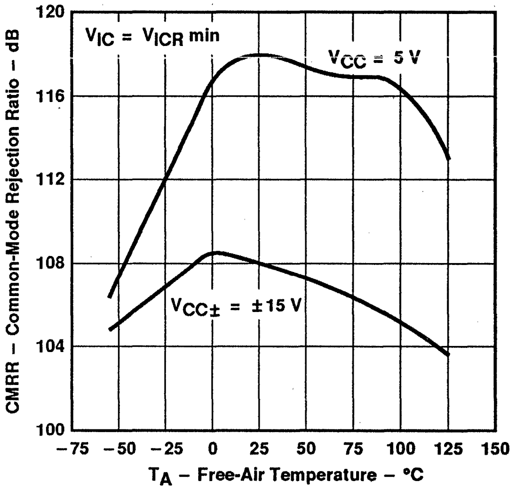


Figure 18

SUPPLY VOLTAGE REJECTION RATIO vs FREQUENCY

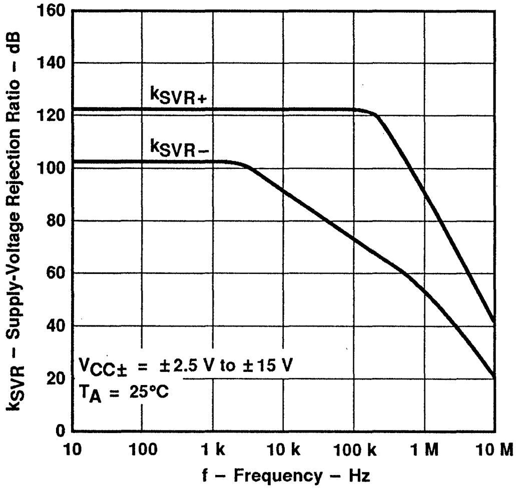


Figure 19

SUPPLY-VOLTAGE REJECTION RATIO vs FREE-AIR TEMPERATURE

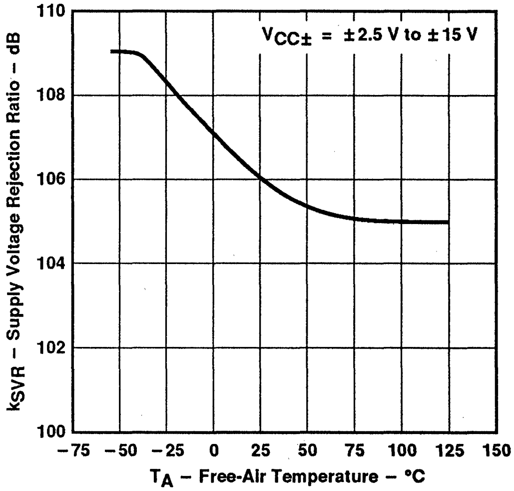


Figure 20

---

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

SUPPLY CURRENT
vs
FREE-AIR TEMPERATURE

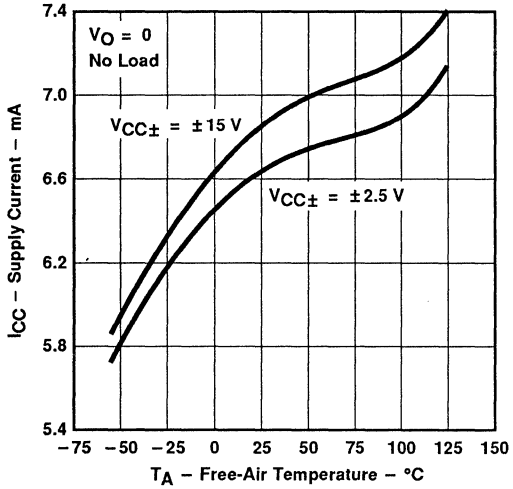


Figure 21

SUPPLY CURRENT
vs
SUPPLY VOLTAGE

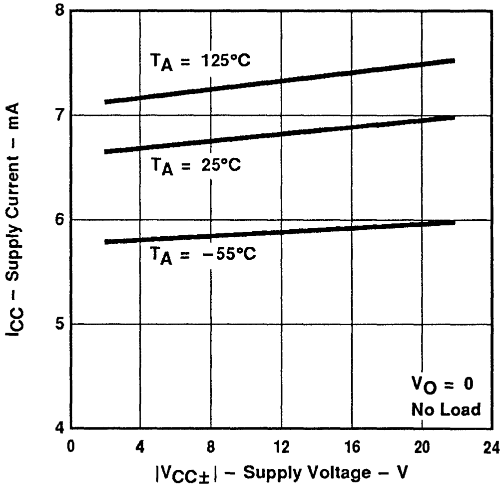


Figure 22

EQUIVALENT INPUT NOISE VOLTAGE
vs
FREQUENCY

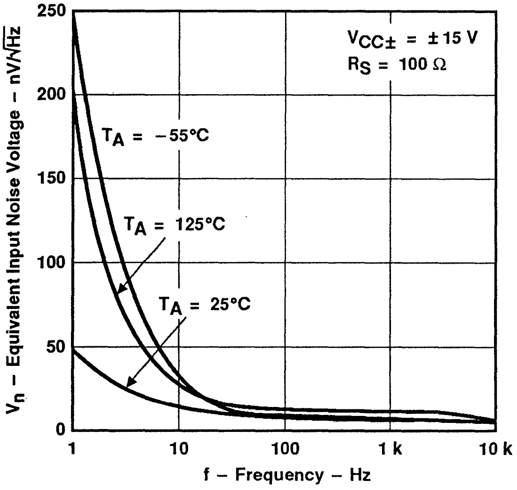


Figure 23

EQUIVALENT INPUT NOISE VOLTAGE
OVER A 10-SECOND PERIOD

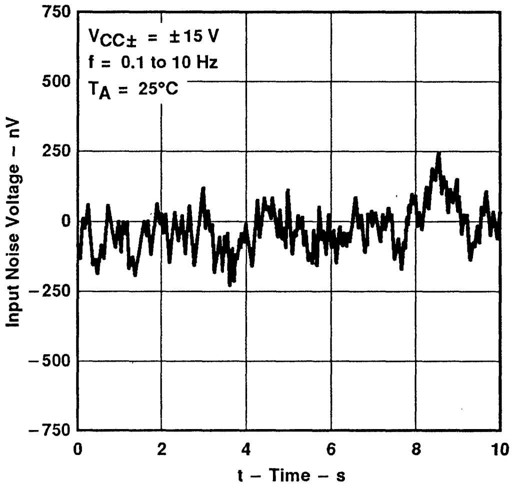


Figure 24

---

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

NOISE CURRENT vs FREQUENCY

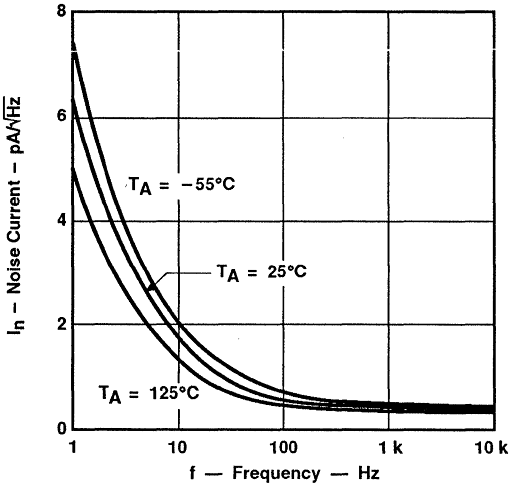


Figure 25

TOTAL HARMONIC DISTORTION PLUS NOISE vs FREQUENCY

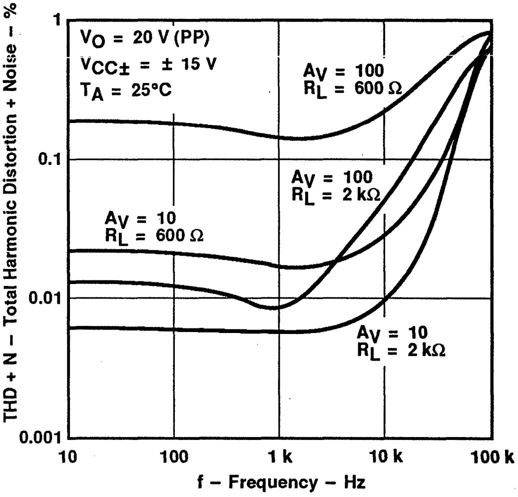


Figure 26

SLEW RATE vs FREE-AIR TEMPERATURE

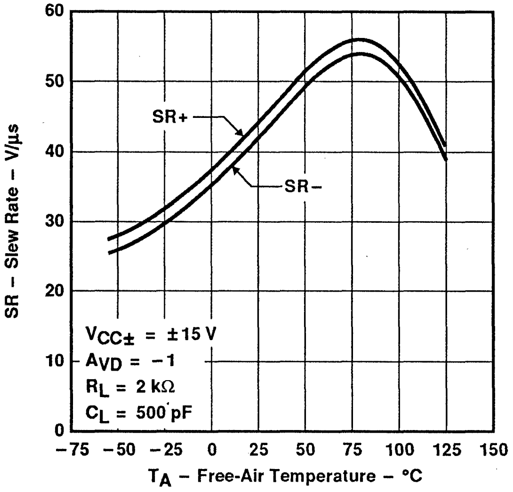


Figure 27

SLEW RATE vs LOAD CAPACITANCE

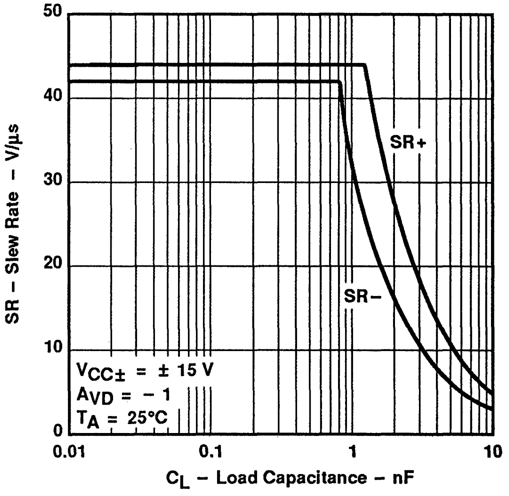


Figure 28

---

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

NONINVERTING
LARGE-SIGNAL
PULSE RESPONSE

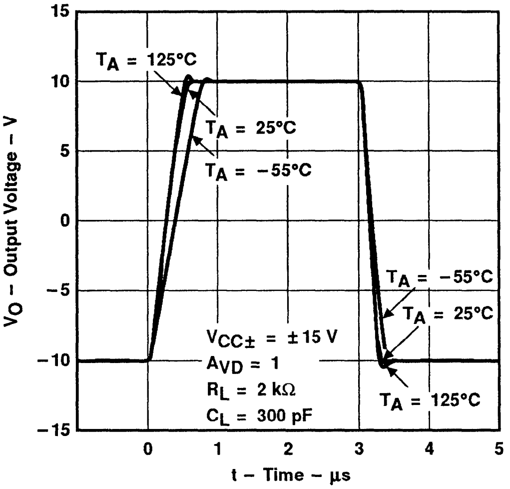


Figure 29

INVERTING
LARGE-SIGNAL
PULSE RESPONSE

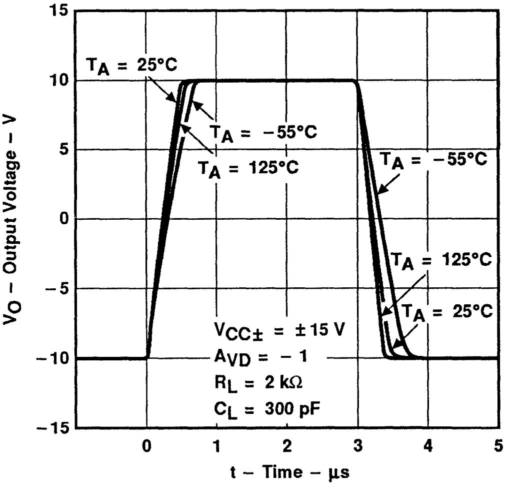


Figure 30

SMALL SIGNAL
PULSE RESPONSE

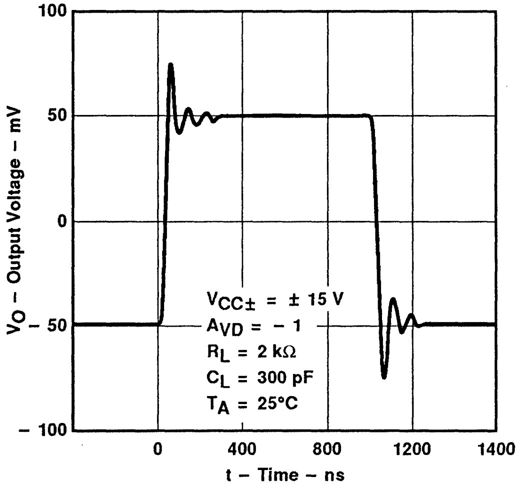


Figure 31

UNITY-GAIN BANDWIDTH
vs
LOAD CAPACITANCE

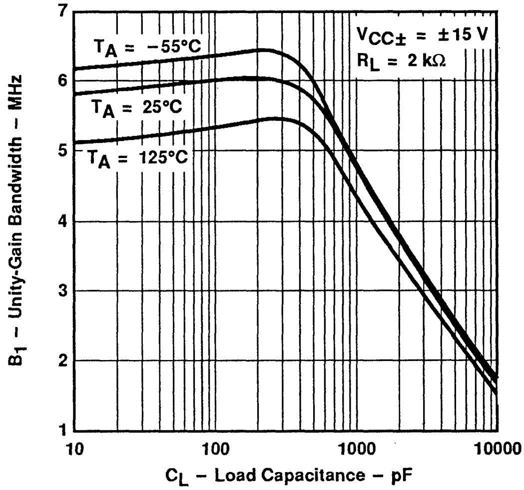


Figure 32

---

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS[†]

GAIN MARGIN vs LOAD CAPACITANCE

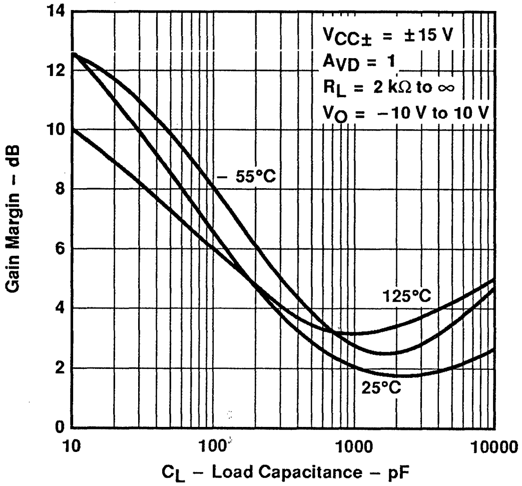


Figure 33

PHASE MARGIN vs LOAD CAPACITANCE

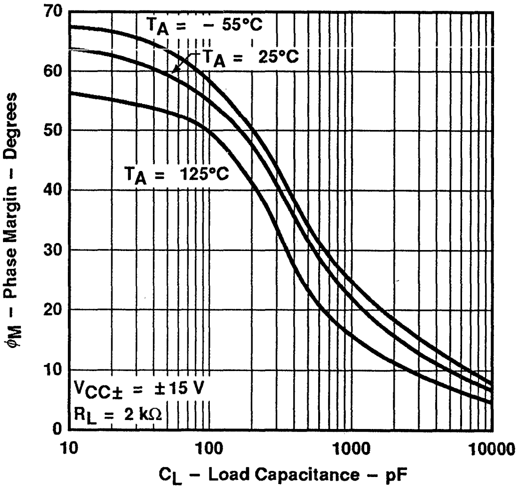


Figure 34

[†] Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

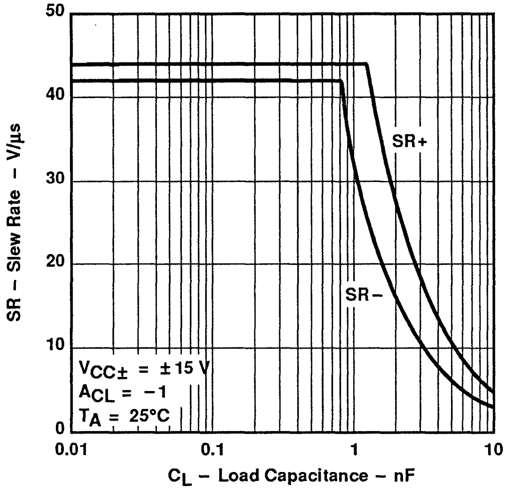
TLE2144, TLE2144A, TLE2144Y
EXCALIBUR LOW-NOISE HIGH-SPEED PRECISION QUAD OPERATIONAL AMPLIFIERS

D3964, NOVEMBER 1991

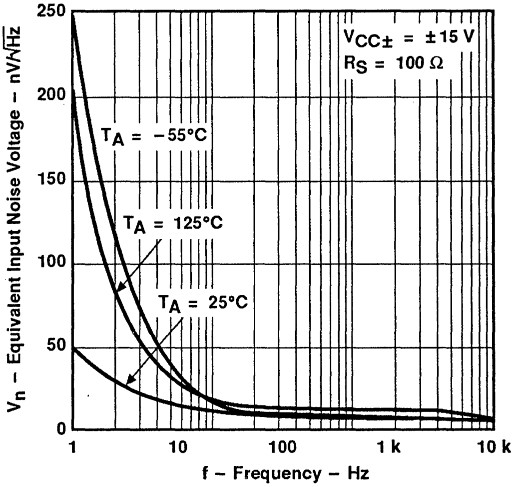
available features

- Low Noise:
  10 Hz . . . 15 nV/$\sqrt{\text{Hz}}$
  1 kHz . . . 10.5 nV/$\sqrt{\text{Hz}}$
- 10,000-pF Load Capability
- 20-mA Min Short-Circuit Output Current
- 30-V/μs Min Slew Rate
- High Gain-Bandwidth Product . . . 5.9 MHz
- Low V_{IO} . . . 1.5 mV Max at 25°C
- Single or Split Supply . . . 4 V to 44 V
- Fast Settling Time . . . 340 ns to 0.1%
  400 ns to 0.01%
- Saturation Recovery . . . 150 ns
- Large Output Swing . . . V_{CC-} + 0.1 V to V_{CC+} −1 V

SLEW RATE
vs
LOAD CAPACITANCE



EQUIVALENT INPUT NOISE VOLTAGE
vs
FREQUENCY



description

The TLE2144 and TLE2144A are high-performance internally compensated operational amplifiers built using the Texas Instruments complementary bipolar Excalibur process. The TLE2144A is a tighter offset voltage grade of the TLE2144. Both are pin-compatible upgrades to standard industry products.

AVAILABLE OPTIONS

T_A	V_{IO} max AT 25°C	PACKAGE				CHIP FORM (Y)
		SMALL-OUTLINE (DW)	CHIP CARRIER (FK)	CERAMIC DIP (J)	PLASTIC DIP (N)	
0°C to	1.5 mV	—	—	—	TLE2144ACN	TLE2144Y
70°C	2.4 mV	TLE2144CDW	—	—	TLE2144CN	
− 40°C to	1.5 mV	—	—	—	TLE2144AIN	
105°C	2.4 mV	TLE2144IDW	—	—	TLE2144IN	
− 55°C to	1.5 mV	—	TLE2144AMFK	TLE2144AMJ	TLE2144AMN	
125°C	2.4 mV	TLE2144MDW	TLE2144MFK	TLE2144MJ	TLE2144MN	

DW packages are available taped and reeled. Add "R" suffix to device type (e.g., TLE2144CDWR). Chips are tested at T_A = 25°C.

TEXAS INSTRUMENTS
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

description (continued)

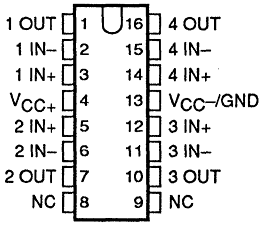
The design incorporates a patent-pending input stage that simultaneously achieves low audio band noise of 10.5 nV/$\sqrt{Hz}$ with a 6-Hz 1/f corner and symmetrical 40-V/µs slew rate typically with loads up to 800 pF. The resulting low distortion and high power bandwidth are important in high-fidelity audio applications. A fast settling time of 340-ns to 0.1% of a 10-V step with a 2-kΩ/100-pF load is useful in fast actuator/positioning drivers. Under similar test conditions, settling time to 0.01% is 400 ns The devices are stable with capacitive loads up to 10 nF, although the 6-MHz bandwidth decreases to 1.8 MHz at this high loading level. As such, the TLE2144 and TLE2144A are useful for low-droop sample and holds and direct buffering of long cables, including 4-mA to 20-mA current loops. The special design also exhibits an improved insensitivity to inherent integrated circuit component mismatches as is evidenced by a 1.5-mV maximum offset voltage and 1.7-µV/°C typical drift. Minimum common-mode rejection ratio and supply-voltage rejection ratio are 85 dB and 90 dB, respectively.

Device performance is relatively independent of supply voltage over the ±2-V to ±22-V range. Inputs can operate between V_{CC-}−0.3 V to V_{CC+}−1.8 V without inducing phase reversal, although excessive input current may flow out of each input exceeding the lower common-mode input range. The all-NPN output stage provides a nearly rail-to-rail output swing of V_{CC-}+0.1 V to V_{CC+}−1 V under light current loading conditions. The device can sustain shorts to either supply since output current is internally limited, but care must be taken to ensure that maximum package power dissipation is not exceeded.

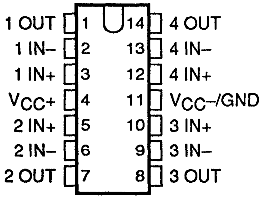
Both versions can also be used as comparators. Differential inputs of $V_{CC\pm}$ can be maintained without damage to the device. Open-loop propagation delay with TTL supply levels is typically 200 ns. This gives a good indication as to output stage saturation recovery when the device is overdriven beyond the limits of recommended output swing.

Both the TLE2144 and TLE2144A are available in a wide variety of packages, including the industry-standard 8-pin small-outline version and chip form for high-density system applications. The C-suffix devices are characterized for operation from 0°C to 70°C, the I-suffix from −40°C to 105°C, and the M-suffix over the full military temperature range of −55°C to 125°C.

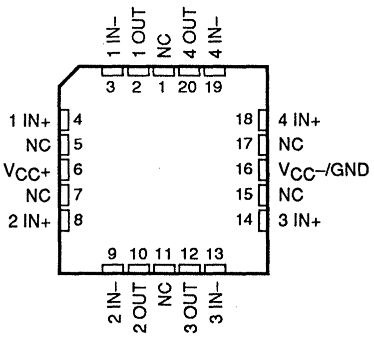
DW PACKAGE
(TOP VIEW)



J OR N PACKAGE
(TOP VIEW)

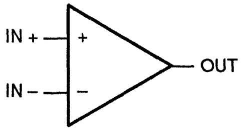


FK PACKAGE
(TOP VIEW)



NC – No internal connection

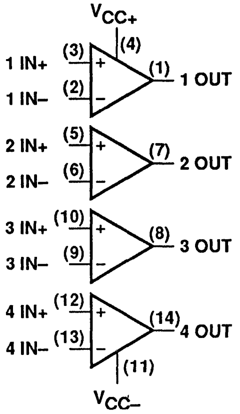
symbol

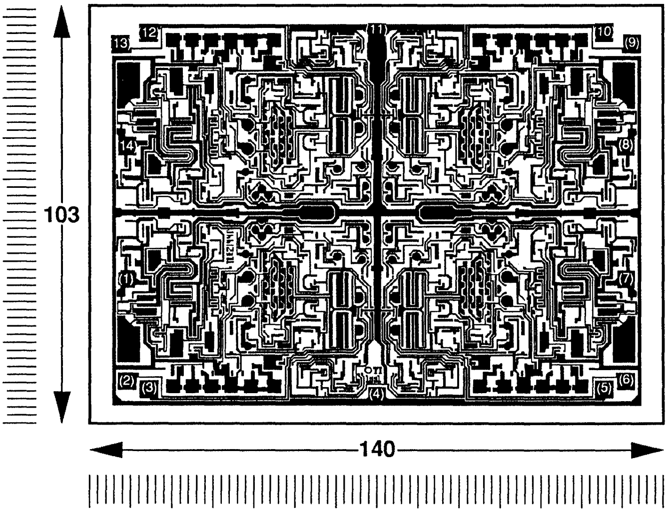


chip information

These chips, properly assembled, display characteristics similar to the TLE2144C. Thermal compression or ultrasonic bonding may be used on the doped aluminum bonding pads. Chips may be mounted with conductive epoxy or a gold-silicon preform.

BONDING PAD ASSIGNMENTS





CHIP THICKNESS:
15 TYPICAL

BONDING PADS:
4 X 4 MINIMUM

$T_Jmax = 150°C$

TOLERANCES
ARE ± 10%

ALL DIMENSIONS
ARE IN MILS

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC+} (see Note 1)	22 V
Supply voltage, V_{CC-}	−22 V
Differential input voltage range (see Note 2)	V_{CC+} to V_{CC-}
Input voltage range, V_I (any input)	V_{CC+} to V_{CC-} − 0.3 V
Input current, I_I (each input)	±1 mA
Output current, I_O	±80 mA
Total current into V_{CC+} terminal	160 mA
Total current out of V_{CC-} terminal	160 mA
Duration of short-circuit current at (or below) 25°C (see Note 3)	unlimited
Continuous total dissipation	See Dissipation Rating Table
Operating free-air temperature range, T_A: C-suffix	0°C to 70°C
I-suffix	−40°C to 105°C
M-suffix	−55°C to 125°C
Storage temperature range	−65°C to 150°C
Case temperature for 60 seconds: FK package	260°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: DW or N package	260°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: J package	300°C

NOTES: 1. All voltage values, except differential voltages, are with respect to the midpoint between V_{CC+} and V_{CC-}.

2. Differential voltages are at the noninverting input with respect to the inverting input. Excessive current will flow if input is brought below V_{CC-} − 0.3 V.

3. The output may be shorted to either supply. Temperature and/or supply voltages must be limited to ensure that the maximum dissipation rating is not exceeded.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 105°C$ POWER RATING	$T_A = 125°C$ POWER RATING
DW	1025 mW	8.2 mW/°C	656 mW	369 mW	205 mW
FK	1375 mW	11 mW/°C	880 mW	495 mW	275 mW
J	1375 mW	11 mW/°C	880 mW	495 mW	275 mW
N	1150 mW	9.2 mW/°C	736 mW	414 mW	230 mW

recommended operating conditions

		C-SUFFIX		I-SUFFIX		M-SUFFIX		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
Supply voltage, $V_{CC\pm}$		± 2	± 22	± 2	± 22	± 2	± 22	V
Common-mode input voltage, V_{IC}	V_{CC} = 5 V	0	2.9	0	2.7	0	2.7	V
	$V_{CC\pm}$ = ±15 V	− 15	12.9	− 15	12.7	− 15	12.7	
Operating free-air temperature, T_A		0	70	− 40	105	− 55	125	°C

electrical characteristics at specified free-air temperature, V_{CC} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A†	TLE2144C			TLE2144AC			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_O = 2.5 V, R_S = 50 Ω, V_{IC} = 2.5 V	25°C		0.5	3.8		0.5	3	mV
			Full range			4.4			3.6	
α_{VIO}	Temperature coefficient of input offset voltage		Full range		1.7			1.7		μV/°C
I_{IO}	Input offset current		25°C		8	100		8	100	nA
			Full range			150			150	
I_{IB}	Input bias current		25°C		–0.8	–2		–0.8	–2	μA
			Full range			–2.1			–2.1	
V_{ICR}	Common-mode input voltage range	R_S = 50 Ω	25°C	0 to 3	–0.3 to 3.2		0 to 3	–0.3 to 3.2		V
			Full range	0 to 2.9			0 to 2.9			
V_{OH}	High-level output voltage	I_{OH} = –150 μA	25°C	3.9	4.1		3.9	4.1		V
			Full range	3.8			3.8			
		I_{OH} = –1.5 mA	25°C	3.8	4		3.8	4		
			Full range	3.7			3.7			
		I_{OH} = –15 mA	25°C	3.4	3.7		3.4	3.7		
			Full range	3.4			3.4			
V_{OL}	Low-level output voltage	I_{OL} = 150 μA	25°C		75	125		75	125	mV
			Full range			150			150	
		I_{OL} = 1.5 mA	25°C		150	225		150	225	
			Full range			250			250	
		I_{OL} = 15 mA	25°C		1.2	1.6		1.2	1.6	V
			Full range			1.7			1.7	
A_{VD}	Large-signal differential voltage amplification	V_{CC} = ± 2.5 V, R_L = 2 kΩ, V_O = 1 V to –1.5 V	25°C	50	95		50	95		V/mV
			Full range	25			25			
r_i	Input resistance		25°C		70			70		MΩ
c_i	Input capacitance		25°C		2.5			2.5		pF
z_o	Open-loop output impedance	f = 1 MHz	25°C		30			30		Ω
CMRR	Common-mode rejection ratio	V_{IC} = V_{ICR} min, R_S = 50 Ω	25°C	85	118		85	118		dB
			Full range	80			80			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm} / \Delta V_{IO}$)	$V_{CC\pm}$ = ± 2.5 V to ± 15 V, R_S = 50 Ω	25°C	90	106		90	106		dB
			Full range	85			85			
I_{CC}	Supply current	V_O = 2.5 V, No load, V_{IC} = 2.5 V	25°C		13.2	17.6		13.2	17.6	mA
			Full range			18.5			18.5	

†Full range is 0°C to 70°C.

operating characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS		TLE2144C			TLE2144AC			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
SR +	Positive slew rate	A_{VD} = −1, R_L = 2 kΩ†, C_L = 500 pF			45			45		V/µs
SR −	Negative slew rate				42			42		
	Settling time	A_{VD} = −1, 2.5-V Step	To 0.1%		0.16			0.16		µs
			To 0.01%		0.22			0.22		
V_n	Equivalent input noise voltage	R_S = 100 Ω, f = 10 Hz			15			15		nV/√Hz
		R_S = 100 Ω, f = 1 kHz			10.5			10.5		
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 1 Hz			0.48			0.48		µV
		f = 0.1 Hz to 10 Hz			0.51			0.51		
I_n	Equivalent input noise current	f = 10 Hz			1.92			1.92		pA/√Hz
		f = 1 kHz			0.5			0.5		
THD + N	Total harmonic distortion plus noise	V_O = 1 V to 3 V, R_L = 2 kΩ†, A_{VD} = 2, f = 10 kHz			0.0052 %			0.0052 %		
B_1	Unity-gain bandwidth	R_L = 2 kΩ†, C_L = 100 pF			5.9			5.9		MHz
	Gain-bandwidth product	R_L = 2 kΩ†, C_L = 100 pF, f = 100 kHz			5.8			5.8		MHz
B_{OM}	Maximum output-swing bandwidth	R_L = 2 kΩ†, $V_{O(PP)}$ = 2 V, A_{VD} = 1, C_L = 100 pF			6.6			6.6		MHz
ϕ_m	Phase margin at unity-gain	R_L = 2 kΩ†, C_L = 100 pF			57°			57°		

† R_L terminates at 2.5 V.

electrical characteristics at specified free-air temperature, $V_{CC\pm}$ = ± 15 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A†	TLE2144C			TLE2144AC			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_{IC} = 0, R_S = 50 Ω, V_O = 0	25°C		0.6	2.4		0.5	1.5	mV
			Full range			3.2			2.4	
α_{VIO}	Temperature coefficient of input offset voltage		Full range		1.7			1.7		µV/°C
I_{IO}	Input offset current		25°C		7	100		7	100	nA
			Full range			150			150	
I_{IB}	Input bias current		25°C		–0.7	–1.5		–0.7	–1.5	µA
			Full range			–1.6			–1.6	
V_{ICR}	Common-mode input voltage range	R_S = 50 Ω	25°C	–15 to 13	–15.3 to 13.2		–15 to 13	–15.3 to 13.2		V
			Full range	–15 to 12.9	–15.3 to 13.1		–15 to 12.9	–15.3 to 13.1		
V_{OM+}	Maximum positive peak output voltage swing	I_O = –150 µA	25°C	13.8	14.1		13.8	14.1		V
			Full range	13.7			13.7			
		I_O = – 1.5 mA	25°C	13.7	14		13.7	14		
			Full range	13.6			13.6			
		I_O = –15 mA	25°C	13.1	13.7		13.1	13.7		
			Full range	13			13			
V_{OM-}	Maximum negative peak output voltage swing	I_O = 150 µA	25°C	–14.7	–14.9		–14.7	–14.9		V
			Full range	–14.6			–14.6			
		I_O = 1.5 mA	25°C	–14.5	–14.8		–14.5	–14.8		
			Full range	–14.4			–14.4			
		I_O = 15 mA	25°C	–13.4	–13.8		–13.4	–13.8		
			Full range	–13.3			–13.3			
A_{VD}	Large-signal differential voltage amplification	V_O = ± 10 V	25°C	100	170		100	170		V/mV
			Full range	75			75			
r_i	Input resistance	R_L = 2 kΩ	25°C		65			65		MΩ
c_i	Input capacitance		25°C		2.5			2.5		pF
z_o	Open-loop output impedance	f = 1 MHz	25°C		30			30		Ω
CMRR	Common-mode rejection ratio	V_{IC} = V_{ICR} min, R_S = 50 Ω	25°C	85	108		85	108		dB
			Full range	80			80			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm}/\Delta V_{IO}$)	$V_{CC\pm}$ = ± 2.5 V to ± 15 V, R_S = 50 Ω	25°C	90	106		90	106		dB
			Full range	85			85			
I_{OS}	Short-circuit output current	V_O = 0, V_{ID} = 1 V	25°C	–25	–50		–25	–50		mA
		V_O = 0, V_{ID} = –1 V		20	31		20	31		
I_{CC}	Supply current	V_O = 0, No load	25°C		13.8	18		13.8	18	mA
			Full range			18.8			18.8	

†Full range is 0°C to 70°C.

operating characteristics, $V_{CC\pm}$ = ±15 V, T_A = 25°C

PARAMETER		TEST CONDITIONS		TLE2144C			TLE2144AC			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
SR +	Positive slew rate	A_{VD} = −1, R_L = 2 kΩ, C_L = 500 pF		30	45		30	45		V/μs
SR −	Negative slew rate			30	42		30	42		
	Settling time	A_{VD} = −1, 10-V Step	To 0.1%		0.34			0.34		μs
			To 0.01%		0.4			0.4		
V_n	Equivalent input noise voltage	R_S = 100 Ω, f = 10 Hz			15			15		nV/√Hz
		R_S = 100 Ω, f = 1 kHz			10.5			10.5		
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 1 Hz			0.48			0.48		μV
		f = 0.1 Hz to 10 Hz			0.51			0.51		
I_n	Equivalent input noise current	f = 10 Hz			1.89			1.89		pA/√Hz
		f = 1 kHz			0.47			0.47		
THD + N	Total harmonic distortion plus noise	V_O = 20 V_{PP}, R_L = 2 kΩ, A_{VD} = 10, f = 10 kHz			0.01%			0.01%		
B_1	Unity-gain bandwidth	R_L = 2 kΩ, C_L = 100 pF			6			6		MHz
	Gain-bandwidth product	R_L = 2 kΩ, C_L = 100 pF, f = 100 kHz			5.9			5.9		MHz
B_{OM}	Maximum output-swing bandwidth	$V_{O(PP)}$ = 20 V, R_L = 2 kΩ, A_{VD} = 1, C_L = 100 pF			668			668		kHz
ϕ_m	Phase margin at unity gain	R_L = 2 kΩ, C_L = 100 pF			58°			58°		

electrical characteristics at specified free-air temperature, V_{CC} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A†	TLE2144I			TLE2144AI			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_{IC} = 0, R_S = 50 Ω, V_O = 0	25°C		0.5	3.8		0.5	3	mV
			Full range			4.8			4	
α_{VIO}	Temperature coefficient of input offset voltage		Full range		1.7			1.7		μV/°C
I_{IO}	Input offset current		25°C		8	100		8	100	nA
			Full range			200			200	
I_{IB}	Input bias current		25°C		–0.8	–2		–0.8	–2	μA
			Full range			–2.2			–2.2	
V_{ICR}	Common-mode input voltage range	R_S = 50 Ω	25°C	0 to 3	–0.3 to 3.2		0 to 3	–0.3 to 3.2		V
			Full range	0 to 2.7	–0.3 to 2.9		0 to 2.7	–0.3 to 2.9		
V_{OH}	High-level output voltage	I_{OH} = –150 μA	25°C	3.9	4.1		3.9	4.1		V
		I_{OH} = –1.5 mA		3.8	4		3.8	4		
		I_{OH} = –15 mA		3.4	3.7		3.4	3.7		
		I_{OH} = 100 μA	Full range	3.8			3.8			
		I_{OH} = 1 mA		3.7			3.7			
		I_{OH} = 10 mA		3.5			3.5			
V_{OL}	Low-level output voltage	I_{OL} = 150 μA	25°C		75	125		75	125	mV
		I_{OL} = 1.5 mA			150	225		150	225	
		I_{OL} = 15 mA			1.2	1.6		1.2	1.6	V
		I_{OL} = 100 μA	Full range			175			175	mV
		I_{OL} = 1 mA				225			225	
		I_{OL} = 10 mA				1.4			1.4	V
A_{VD}	Large-signal differential voltage amplification	V_{CC} = ± 2.5 V, R_L = 2 kΩ, V_O = 1 V to –1.5 V	25°C	50	95		50	95		V/mV
			Full range	10			10			
r_i	Input resistance		25°C		70			70		MΩ
c_i	Input capacitance		25°C		2.5			2.5		pF
z_o	Open-loop output impedance	f = 1 MHz	25°C		30			30		Ω
CMRR	Common-mode rejection ratio	V_{IC} = V_{ICR} min, R_S = 50 Ω	25°C	85	118		85	118		dB
			Full range	80			80			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm} / \Delta V_{IO}$)	$V_{CC\pm}$ = ± 2.5 V to ± 15 V, R_S = 50 Ω	25°C	90	106		90	106		dB
			Full range	85			85			
I_{CC}	Supply current	V_O = 2.5 V, No load, V_{IC} = 2.5 V	25°C		13.2	17.6		13.2	17.6	mA
			Full range			18.4			18.4	

†Full range is – 40°C to 105°C.

operating characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS		TLE2144I			TLE2144AI			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
SR +	Positive slew rate	A_{VD} = −1, R_L = 2 kΩ†, C_L = 500 pF			45			45		V/µs
SR −	Negative slew rate				42			42		
	Settling time	A_{VD} = −1, 2.5-V Step	To 0.1%		0.16			0.16		µs
			To 0.01%		0.22			0.22		
V_n	Equivalent input noise voltage	R_S = 100 Ω, f = 10 Hz			15			15		nV/√Hz
		R_S = 100 Ω, f = 1 kHz			10.5			10.5		
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 1 Hz			0.48			0.48		µV
		f = 0.1 Hz to 10 Hz			0.51			0.51		
I_n	Equivalent input noise current	f = 10 Hz			1.92			1.92		pA/√Hz
		f = 1 kHz			0.5			0.5		
THD + N	Total harmonic distortion plus noise	V_O = 1 V to 3 V, R_L = 2 kΩ†, A_{VD} = 2, f = 10 kHz			0.0052 %			0.0052 %		
B_1	Unity-gain bandwidth	R_L = 2 kΩ†, C_L = 100 pF			5.9			5.9		MHz
	Gain-bandwidth product	R_L = 2 kΩ†, C_L = 100 pF, f = 100 kHz			5.8			5.8		MHz
B_{OM}	Maximum output-swing bandwidth	R_L = 2 kΩ†, $V_{O(PP)}$ = 2 V, A_{VD} = 1, C_L = 100 pF			6.6			6.6		MHz
ϕ_m	Phase margin at unity-gain	R_L = 2 kΩ†, C_L = 100 pF			57°			57°		

† R_L terminates at 2.5 V.

electrical characteristics at specified free-air temperature, $V_{CC\pm} = \pm 15$ V (unless otherwise noted)

	PARAMETER	TEST CONDITIONS	T_A†	TLE2144I			TLE2144AI			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	$V_{IC} = 0$, $R_S = 50\ \Omega$, $V_O = 0$	25°C		0.6	2.4		0.5	1.5	mV
			Full range			3.2			2.8	
α_{VIO}	Temperature coefficient of input offset voltage		Full range		1.7			1.7		µV/°C
I_{IO}	Input offset current		25°C		7	100		7	100	nA
			Full range			200			200	
I_{IB}	Input bias current		25°C		−0.7	−1.5		−0.7	−1.5	µA
			Full range			−1.7			−1.7	
V_{ICR}	Common-mode input voltage range	$R_S = 50\ \Omega$	25°C	−15 to 13	−15.3 to 13.2		−15 to 13	−15.3 to 13.2		V
			Full range	−15 to 12.7	−15.3 to 12.9		−15 to 12.7	−15.3 to 12.9		
V_{OM+}	Maximum positive peak output voltage swing	$I_O = -150\ \mu A$,	25°C	13.8	14.1		13.8	14.1		V
		$I_O = -1.5$ mA,		13.7	14		13.7	14		
		$I_O = -15$ mA		13.1	13.7		13.1	13.7		
		$I_O = -100\ \mu A$,	Full range	13.7			13.7			
		$I_O = -1$ mA,		13.6			13.6			
		$I_O = -10$ mA		13.1			13.1			
V_{OM-}	Maximum negative peak output voltage swing	$I_O = 150\ \mu A$,	25°C	−14.7	−14.9		−14.7	−14.9		V
		$I_O = 1.5$ mA,		−14.5	−14.8		−14.5	−14.8		
		$I_O = 15$ mA		−13.4	−13.8		−13.4	−13.8		
		$I_O = 100\ \mu A$,	Full range	−14.6			−14.6			
		$I_O = 1$ mA,		−14.5			−14.5			
		$I_O = 10$ mA		−13.4			−13.4			
A_{VD}	Large-signal differential voltage amplification	$V_O = \pm 10$ V, $R_L = 2\ k\Omega$	25°C	100	170		100	170		V/mV
			Full range	40			40			
r_i	Input resistance		25°C		65			65		MΩ
c_i	Input capacitance		25°C		2.5			2.5		pF
z_o	Open-loop output impedance	f = 1 MHz	25°C		30			30		Ω
CMRR	Common-mode rejection ratio	$V_{IC} = V_{ICR}$ min	25°C	85	108		85	108		dB
		$R_S = 50\ \Omega$	Full range	80			80			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm} / \Delta V_{IO}$)	$V_{CC\pm} = \pm 2.5$ V to ± 15 V,	25°C	90	106		90	106		dB
		$R_S = 50\ \Omega$	Full range	85			85			
I_{OS}	Short-circuit output current	$V_O = 0$, $V_{ID} = 1$ V	25°C	−25	−50		−25	−50		mA
		$V_O = 0$, $V_{ID} = -1$ V		20	31		20	31		
I_{CC}	Supply current	$V_O = 0$, No load	25°C		13.8	18		13.8	18	mA
			Full range			18.8			18.8	

†Full range is – 40°C to 105°C.

operating characteristics, $V_{CC\pm}$ = ±15 V, T_A = 25°C

PARAMETER		TEST CONDITIONS		TLE2144I			TLE2144AI			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
SR +	Positive slew rate	A_{VD} = −1, R_L = 2 kΩ, C_L = 500 pF		30	45		30	45		V/µs
SR −	Negative slew rate			30	42		30	42		
	Settling time	A_{VD} = −1, 10-V Step	To 0.1%		0.34			0.34		µs
			To 0.01%		0.4			0.4		
V_n	Equivalent input noise voltage	R_S = 100 Ω, f = 10 Hz			15			15		nV/√Hz
		R_S = 100 Ω, f = 1 kHz			10.5			10.5		
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 1 Hz			0.48			0.48		µV
		f = 0.1 Hz to 10 Hz			0.51			0.51		
I_n	Equivalent input noise current	f = 10 Hz			1.89			1.89		pA/√Hz
		f = 1 kHz			0.47			0.47		
THD + N	Total harmonic distortion plus noise	$V_{O(PP)}$ = 20 V, R_L = 2 kΩ, A_{VD} = 10, f = 10 kHz			0.01%			0.01%		
B_1	Unity-gain bandwidth	R_L = 2 kΩ, C_L = 100 pF			6			6		MHz
	Gain-bandwidth product	R_L = 2 kΩ, C_L = 100 pF, f = 100 kHz			5.9			5.9		MHz
B_{OM}	Maximum output-swing bandwidth	$V_{O(PP)}$ = 20 V, R_L = 2 kΩ, A_{VD} = 1, C_L = 100 pF			668			668		kHz
ϕ_m	Phase margin at unity gain	R_L = 2 kΩ, C_L = 100 pF			58°			58°		

electrical characteristics at specified free-air temperature, V_{CC} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A†	TLE2144M			TLE2144AM			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_O = 2.5 V, R_S = 50 Ω, V_{IC} = 2.5 V	25°C		0.5	3.8		0.5	3	mV
			Full range			5.2			4.4	
α_{VIO}	Temperature coefficient of input offset voltage		Full range		1.7			1.7		µV/°C
I_{IO}	Input offset current		25°C		8	100		8	100	nA
			Full range			250			250	
I_{IB}	Input bias current		25°C		−0.8	−2		−0.8	−2	µA
			Full range			−2.3			−2.3	
V_{ICR}	Common-mode input voltage range	R_S = 50 Ω	25°C	0 to 3	−0.3 to 3.2		0 to 3	−0.3 to 3.2		V
			Full range	0 to 2.7	−0.3 to 2.9		0 to 2.7	−0.3 to 2.9		
V_{OH}	High-level output voltage	I_{OH} = −150 µA	25°C	3.9	4.1		3.9	4.1		V
		I_{OH} = −1.5 mA		3.8	4		3.8	4		
		I_{OH} = −15 mA		3.4	3.7		3.4	3.7		
		I_{OH} = 100 µA	Full range	3.75			3.75			
		I_{OH} = 1 mA		3.65			3.65			
		I_{OH} = 10 mA		3.45			3.45			
V_{OL}	Low-level output voltage	I_{OL} = 150 µA	25°C		75	125		75	125	mV
		I_{OL} = 1.5 mA			150	225		150	225	
		I_{OL} = 15 mA			1.2	1.6		1.2	1.6	V
		I_{OL} = 100 µA	Full range			200			200	mV
		I_{OL} = 1 mA				250			250	
		I_{OL} = 10 mA				1.45			1.45	V
A_{VD}	Large-signal differential voltage amplification	V_{CC} = ± 2.5 V, R_L = 2 kΩ, V_O = 1 V to −1.5 V	25°	50	95		50	95		V/mV
			Full range	5			5			
r_i	Input resistance		25°C		70			70		MΩ
c_i	Input capacitance		25°C		2.5			2.5		pF
z_o	Open-loop output impedance	f = 1 MHz	25°C		30			30		Ω
CMRR	Common-mode rejection ratio	V_{IC} = V_{ICR} min, R_S = 50 Ω	25°C	85	118		85	118		dB
			Full range	80			80			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm} / \Delta V_{IO}$)	$V_{CC\pm}$ = ± 2.5 V to ± 15 V, R_S = 50 Ω	25°C	90	106		90	106		dB
			Full range	85			85			
I_{CC}	Supply current	V_O = 2.5 V, No load V_{IC} = 2.5 V	25°C		13.2	17.6		13.2	17.6	mA
			Full range			18.4			18.4	

†Full range is −55°C to 125°C.

operating characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS		TLE2144M			TLE2144AM			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
SR +	Positive slew rate	A_{VD} = −1,	R_L = 2 kΩ,†		45			45		V/µs
SR −	Negative slew rate	C_L = 500 pF			42			42		
V_n	Settling time	A_{VD} = −1, 2.5-V Step	To 0.1%		0.16			0.16		µs
			To 0.01%		0.22			0.22		
$V_{N(PP)}$	Equivalent input noise voltage	R_S = 100 Ω,	f = 10 Hz		15			15		nV/√Hz
		R_S = 100 Ω,	f = 1 kHz		10.5			10.5		
I_n	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 1 Hz			0.48			0.48		µV
		f = 0.1 Hz to 10 Hz			0.51			0.51		
THD + N	Equivalent input noise current	f = 10 Hz			1.92			1.92		pA/√Hz
		f = 1 kHz			0.5			0.5		
B_1	Total harmonic distortion plus noise	V_O = 1 V to 3 V, A_{VD} = 2,	R_L = 2 kΩ†, f = 10 kHz		0.0052%			0.0052%		
	Unity-gain bandwidth	R_L = 2 kΩ†,	C_L = 100 pF		5.9			5.9		MHz
B_{OM}	Gain-bandwidth product	R_L = 2 kΩ†, f = 100 kHz	C_L = 100 pF,		5.8			5.8		MHz
ϕ_m	Maximum output-swing bandwidth	R_L = 2 kΩ†, A_{VD} = 1	$V_{O(PP)}$ = 2 V,		6.6			6.6		MHz
	Phase margin	R_L = 2 kΩ†,	C_L = 100 pF		57°			57°		

†R_L terminates at 2.5 V.

electrical characteristics at specified free-air temperature, $V_{CC\pm}$ = ± 15 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A†	TLE2144M			TLE2144AM			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_{IC} = 0, R_S = 50 Ω,	25°C		0.6	2.4		0.5	1.5	mV
			Full range			4			3.2	
α_{VIO}	Temperature coefficient of input offset voltage		Full range		1.7			1.7		μV/°C
I_{IO}	Input offset current		25°C		7	100		7	100	nA
			Full range			250			250	
I_{IB}	Input bias current		25°C		−0.7	−1.5		−0.7	−1.5	μA
			Full range			−1.8			−1.8	
V_{ICR}	Common-mode input voltage range	R_S = 50 Ω	25°C	−15 to 13	−15.3 to 13.2		−15 to 13	−15.3 to 13.2		V
			Full range	−15 to 12.7	−15.3 to 12.9		−15 to 12.7	−15.3 to 12.9		
V_{OM+}	Maximum positive peak output voltage swing	I_O = −150 μA	25°C	13.8	14.1		13.8	14.1		V
		I_O = −1.5 mA		13.7	14		13.7	14		
		I_O = −15 mA		13.1	13.7		13.1	13.7		
		I_O = −100 μA	Full range	13.7			13.7			
		I_O = −1 mA		13.6			13.6			
		I_O = −10 mA		13.1			13.1			
V_{OM-}	Maximum negative peak output voltage swing	I_O = 150 μA	25°C	−14.7	−14.9		−14.7	−14.9		V
		I_O = 1.5 mA		−14.5	−14.8		−14.5	−14.8		
		I_O = 15 mA		−13.4	−13.8		−13.4	−13.8		
		I_O = 100 μA	Full range	−14.6			−14.6			
		I_O = 1 mA		−14.5			−14.5			
		I_O = 10 mA		−13.4			−13.4			
A_{VD}	Large-signal differential voltage amplification	V_O = ± 10 V, R_L = 2 kΩ	25°C	100	170		100	170		V/mV
			Full range	20			20			
r_i	Input resistance		25°C		65			65		MΩ
c_i	Input capacitance		25°C		2.5			2.5		pF
z_o	Open-loop output impedance	f = 1 MHz	25°C		30			30		Ω
CMRR	Common-mode rejection ratio	V_{IC} = V_{ICR} min, R_S = 50 Ω	25°C	85	108		85	108		dB
			Full range	80			80			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm} / \Delta V_{IO}$)	$V_{CC\pm}$ = ± 2.5 V to ± 15 V, R_S = 50 Ω	25°C	90	106		90	106		dB
			Full range	85			85			
I_{OS}	Short-circuit output current	V_O = 0, V_{ID} = 1 V	25°C	−25	−50		−25	−50		mA
		V_{ID} = −1 V		20	31		20	31		
I_{CC}	Supply current	V_O = 0, No load, V_{IC} = 2.5 V	25°C		13.8	18		13.8	18	mA
			Full range			18.8			18.8	

†Full range is −55°C to 125°C.

operating characteristics, $V_{CC\pm}$ = ±15 V, T_A = 25°C

PARAMETER		TEST CONDITIONS		TLE2144M			TLE2144AM			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
SR +	Positive slew rate	R_L = 2 kΩ, C_L = 100 pF	A_{VD} = −1,	30	45		30	45		V/μs
SR −	Negative slew rate			30	42		30	42		
	Settling time	A_{VD} = −1, 10-V Step	To 0.1%		0.34			0.34		μs
			To 0.01%		.4			.4		
V_n	Equivalent input noise voltage	R_S = 100 Ω,	f = 10 Hz		15			15		nV/√Hz
		R_S = 100 Ω,	f = 1 kHz		10.5			10.5		
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 1 Hz			0.48			0.48		μV
		f = 0.1 Hz to 10 Hz			0.51			0.51		
I_n	Equivalent input noise current	f = 10 Hz			1.89			1.89		pA/√Hz
		f = 1 kHz			0.47			0.47		
THD + N	Total harmonic distortion plus noise	$V_{O(PP)}$ = 20 V, A_{VD} = 10,	R_L = 2 kΩ, f = 10 kHz		0.01 %			0.01 %		
B_1	Unity-gain bandwidth	R_L = 2 kΩ,	C_L = 100 pF		6			6		MHz
	Gain-bandwidth product	R_L = 2 kΩ, f = 100 kHz	C_L = 100 pF,		5.9			5.9		MHz
B_{OM}	Maximum output-swing bandwidth	$V_{O(PP)}$ = 20 V, A_{VD} = 1,	R_L = 2 kΩ, C_L = 100 pF		668			668		kHz
ϕ_m	Phase margin at unity gain	R_L = 2 kΩ,	C_L = 100 pF		58°			58°		

electrical characteristics at $V_{CC\pm}$ = ±15 V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	$V_{IC} = 0$, $R_S = 50\ \Omega$, $V_O = 0$			0.3	1.8	mV
I_{IO}	Input offset current				7	100	nA
I_{IB}	Input bias current				–0.7	–1.5	µA
V_{ICR}	Common-mode input voltage range	$R_S = 50\ \Omega$		–15 to 13	–15.3 to 13.2		V
V_{OM+}	Maximum positive peak output voltage swing	$I_O = -150\ \mu A$		13.8	14.1		V
		$I_O = -1.5$ mA		13.7	14		
		$I_O = -15$ mA		13.3	13.7		
V_{OM-}	Maximum negative peak output voltage swing	$I_O = 150\ \mu A$		–14.7	–14.9		V
		$I_O = 1.5$ mA		–14.5	–14.8		
		$I_O = 15$ mA		–13.4	–13.8		
A_{VD}	Large-signal differential voltage amplification	$V_O = \pm 10$ V, $R_L = 2\ k\Omega$		100	450		V/mV
r_i	Input resistance				65		MΩ
c_i	Input capacitance				2.5		pF
z_o	Open-loop output impedance	f = 1 MHz			30		Ω
CMRR	Common-mode rejection ratio	$V_{IC} = V_{ICR}$ min, $R_S = 50\ \Omega$		80	108		dB
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm} / \Delta V_{IO}$)	$V_{CC\pm} = \pm 2.5$ V to ±15 V, $R_S = 50\ \Omega$		85	106		dB
I_{OS}	Short-circuit output current	$V_O = 0$	$V_{ID} = 1$ V	–25	–50		mA
			$V_{ID} = -1$ V	20	31		
I_{CC}	Supply current	$V_O = 0$, No load			13.8	18	mA

TYPICAL CHARACTERISTICS

	TABLE OF GRAPHS			FIGURE
V_{IO}	Input offset voltage		Distribution	1
I_{IO}	Input offset current		vs Temperature	2
I_{IB}	Input bias current		vs Temperature	3
			vs Common-mode voltage	4
V_{OM+}	Maximum peak output voltage		vs Supply voltage	5
			vs Temperature	6
			vs Output current	7
			vs Settling time	9
V_{OM-}	Maximum peak output voltage		vs Supply voltage	5
			vs Temperature	6
			vs Output current	8
			vs Settling time	9
$V_{O(PP)}$	Maximum peak-to-peak output voltage swing		vs Frequency	10
V_{OH}	High-level output voltage		vs Output current	11
V_{OL}	Low-level output voltage		vs Output current	12
A_{VD}	Differential voltage amplification		vs Temperature	13
			vs Frequency	14
z_o	Closed loop output impedance		vs Frequency	15
I_{OS}	Short-circuit output current		vs Temperature	16
CMRR	Common-mode rejection ratio		vs Frequency	17
			vs Temperature	18
k_{SVR}	Supply-voltage rejection ratio		vs Frequency	19
			vs Temperature	20
I_{CC}	Supply current		vs Temperature	21
			vs Supply-voltage	22
V_n	Noise voltage		vs Frequency	23
$V_{N(PP)}$	Noise voltage		Over a 10-second period	24
I_n	Noise current		vs Frequency	25
THD + N	Total harmonic distortion plus noise		vs Frequency	26
SR	Slew rate		vs Temperature	27
			vs Load capacitance	28
	Pulse response	Noninverting large-signal	vs Time	29
		Inverting large-signal	vs Time	30
		Small-signal	vs Time	31
B_1	Unity-gain bandwidth		vs Load capacitance	32
	Gain margin		vs Load capacitance	33
ϕ_m	Phase margin		vs Load capacitance	34
	Phase shift		vs Frequency	14

TYPICAL CHARACTERISTICS†

TLE2144 DISTRIBUTION OF INPUT OFFSET VOLTAGE

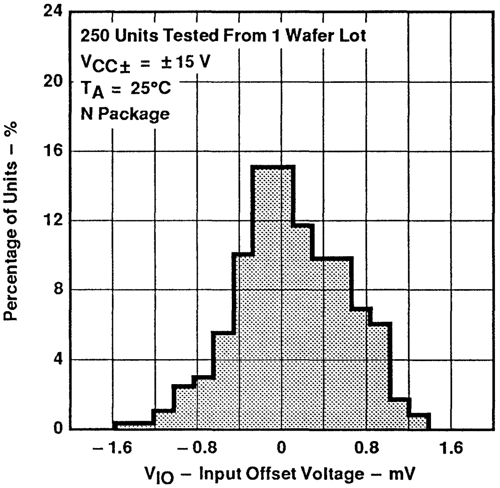


Figure 1

INPUT OFFSET CURRENT vs FREE-AIR TEMPERATURE

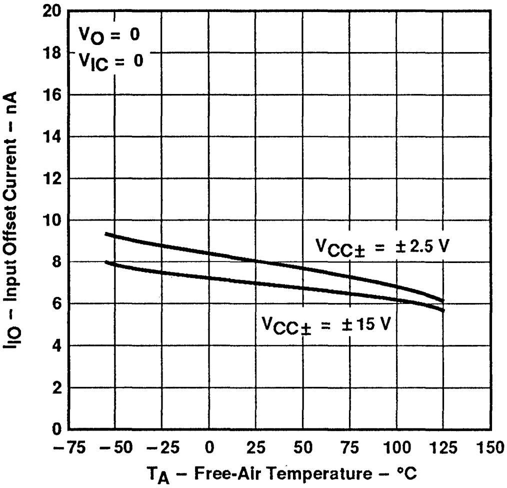


Figure 2

INPUT BIAS CURRENT vs FREE-AIR TEMPERATURE

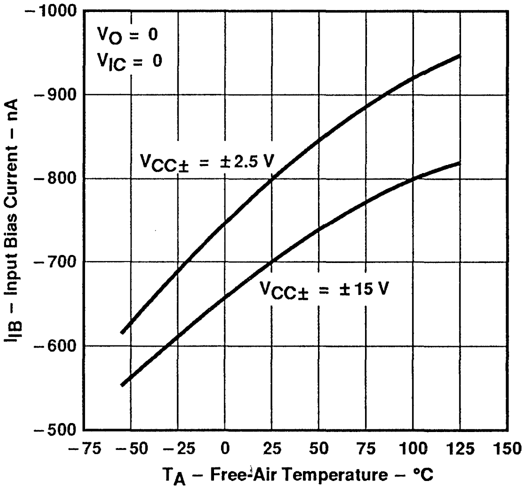


Figure 3

INPUT BIAS CURRENT vs COMMON-MODE INPUT VOLTAGE

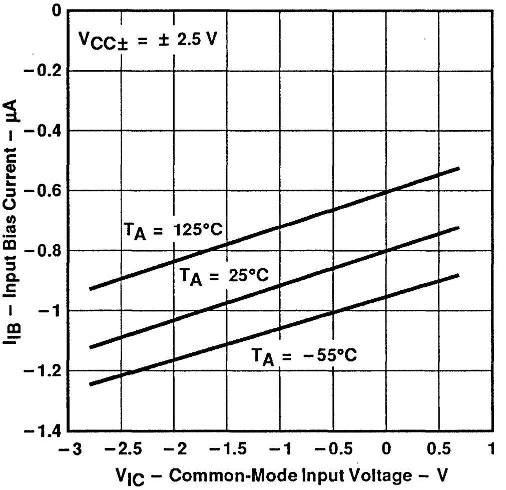


Figure 4

---

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

MAXIMUM PEAK OUTPUT VOLTAGE vs SUPPLY VOLTAGE

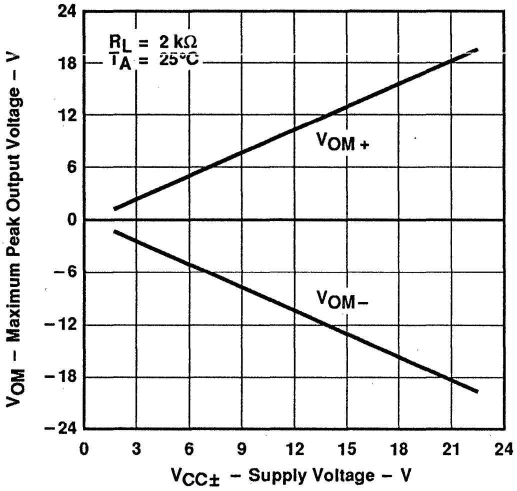


Figure 5

MAXIMUM PEAK OUTPUT VOLTAGE vs FREE-AIR TEMPERATURE

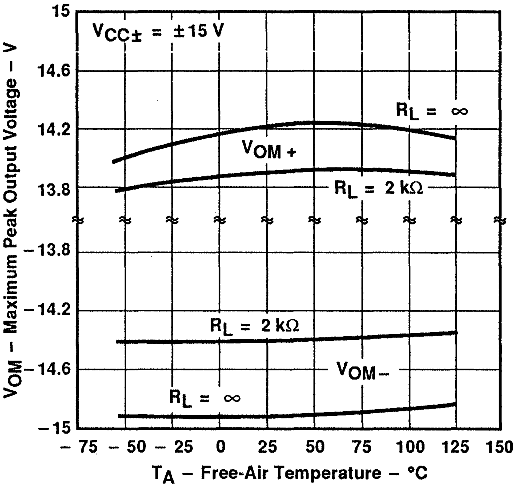


Figure 6

MAXIMUM POSITIVE PEAK OUTPUT VOLTAGE vs OUTPUT CURRENT

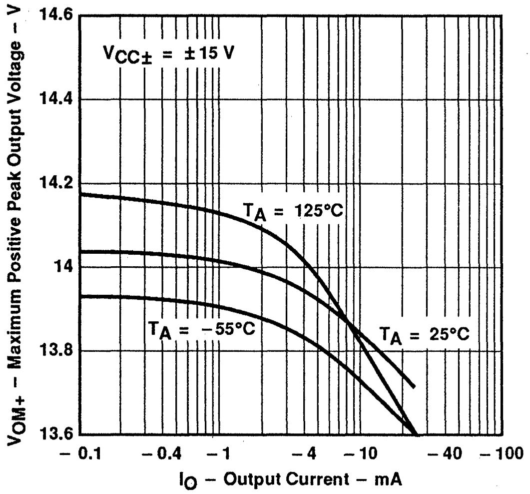


Figure 7

MAXIMUM NEGATIVE PEAK OUTPUT VOLTAGE vs OUTPUT CURRENT

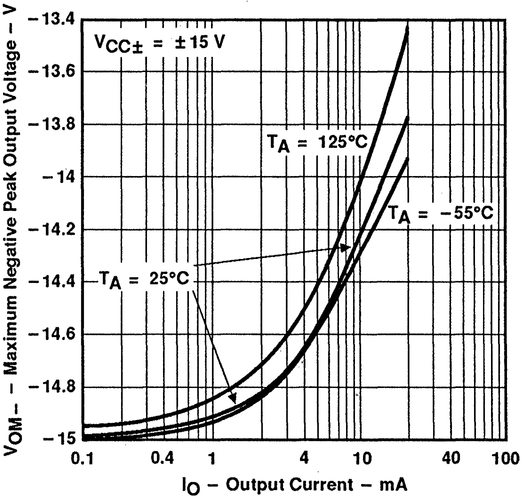


Figure 8

---

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

MAXIMUM PEAK OUTPUT VOLTAGE
vs
SETTLING TIME

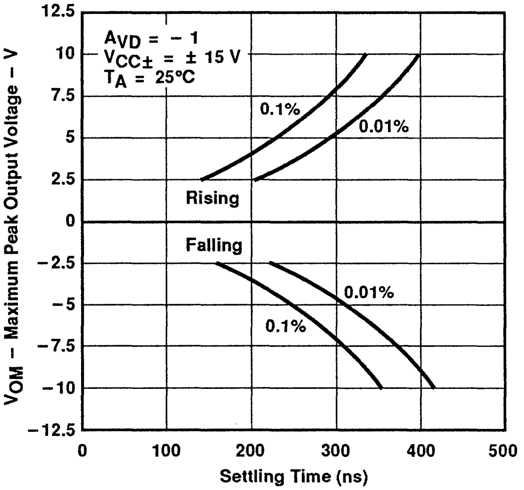


Figure 9

MAXIMUM PEAK-TO-PEAK
OUTPUT VOLTAGE
vs
FREQUENCY

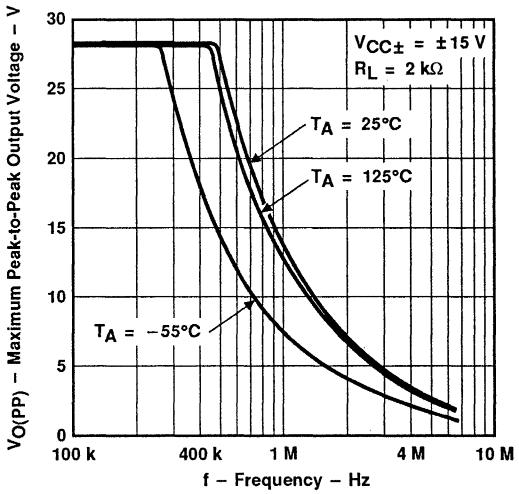


Figure 10

HIGH-LEVEL OUTPUT VOLTAGE
vs
OUTPUT CURRENT

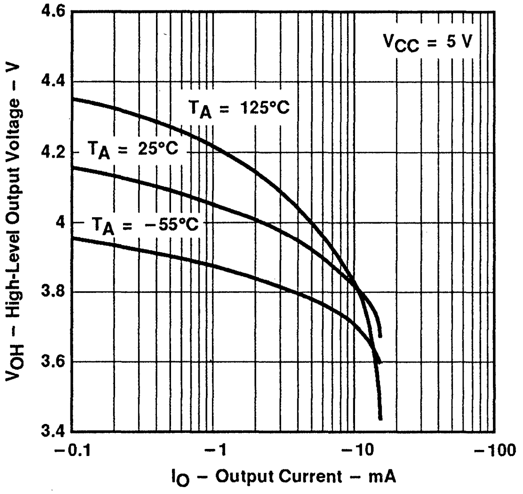


Figure 11

LOW-LEVEL OUTPUT VOLTAGE
vs
OUTPUT CURRENT

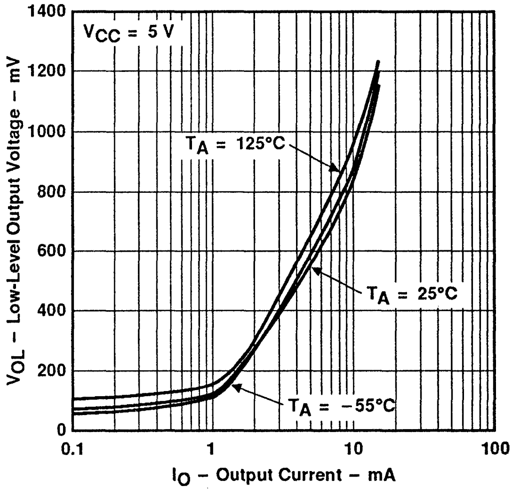


Figure 12

---

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION vs FREE-AIR TEMPERATURE

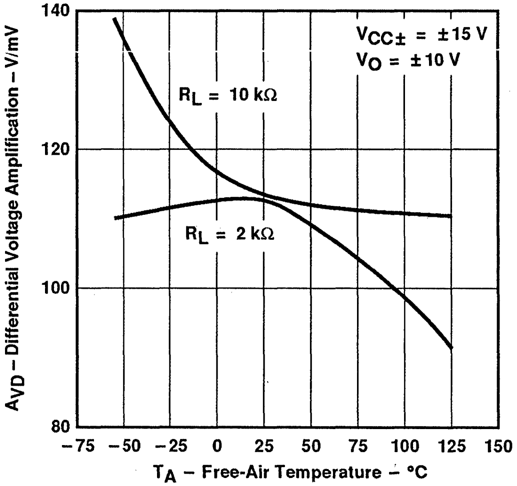


Figure 13

LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION AND PHASE SHIFT vs FREQUENCY

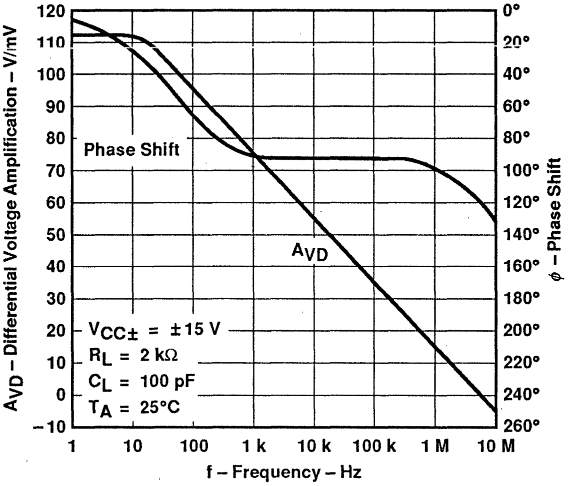


Figure 14

CLOSED-LOOP OUTPUT IMPEDANCE vs FREQUENCY

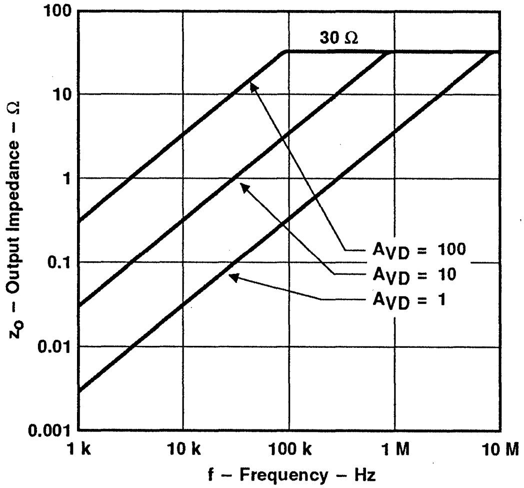


Figure 15

SHORT-CIRCUIT OUTPUT CURRENT vs FREE-AIR TEMPERATURE

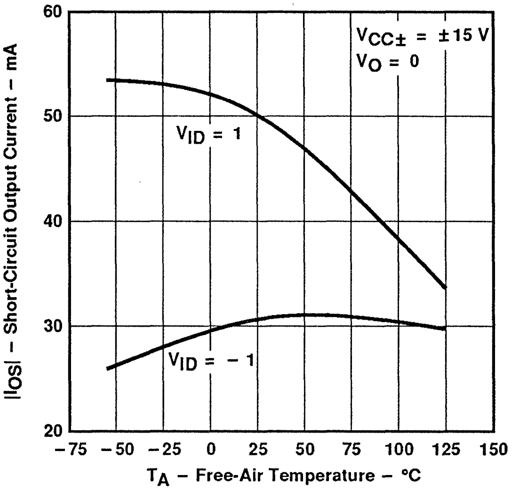


Figure 16

---

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS[†]

COMMON-MODE REJECTION RATIO vs FREQUENCY

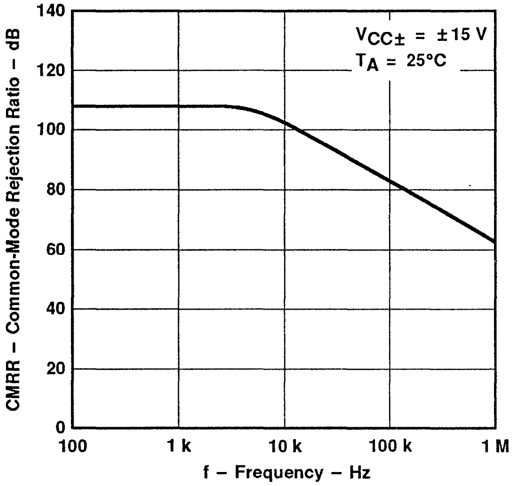


Figure 17

COMMON-MODE REJECTION RATIO vs FREE-AIR TEMPERATURE

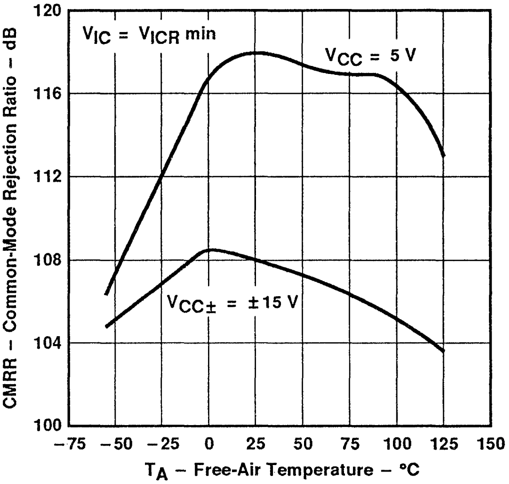


Figure 18

SUPPLY-VOLTAGE REJECTION RATIO vs FREQUENCY

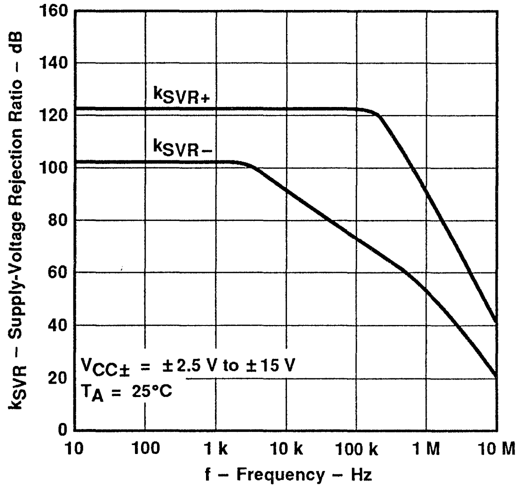


Figure 19

SUPPLY-VOLTAGE REJECTION RATIO vs FREE-AIR TEMPERATURE

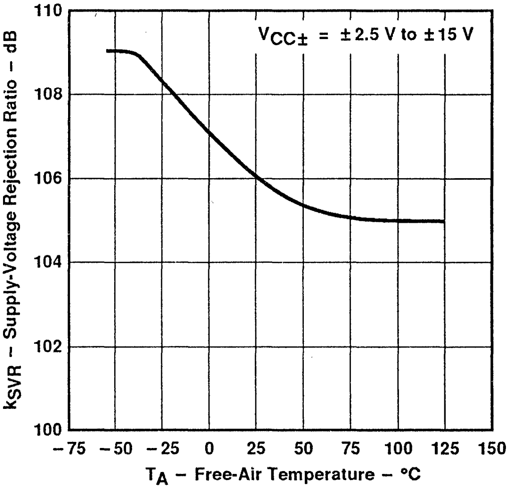


Figure 20

[†] Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

SUPPLY CURRENT
vs
FREE-AIR TEMPERATURE

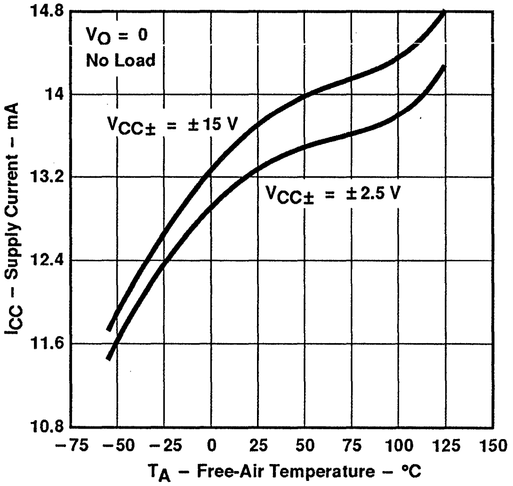


Figure 21

SUPPLY CURRENT
vs
SUPPLY VOLTAGE

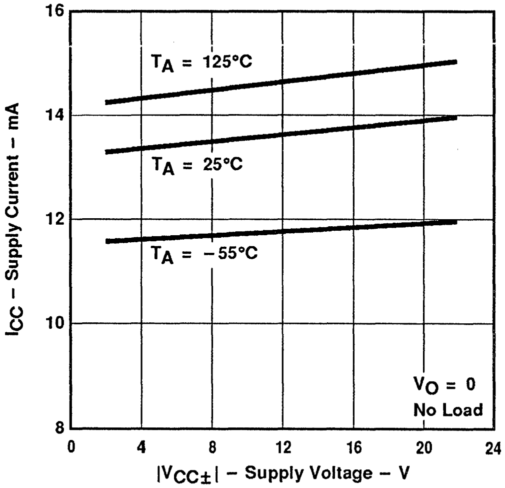


Figure 22

EQUIVALENT INPUT NOISE VOLTAGE
vs
FREQUENCY

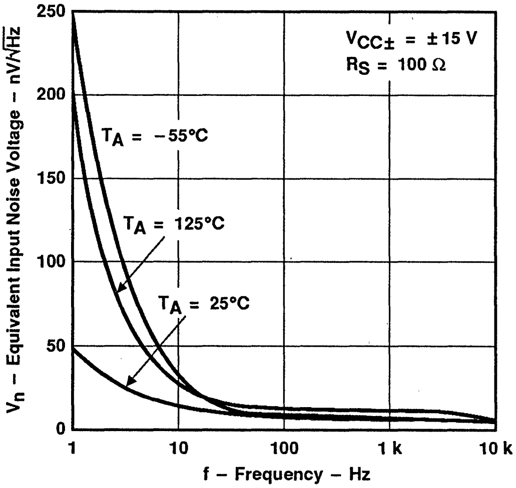


Figure 23

INPUT NOISE VOLTAGE
OVER A 10-SECOND PERIOD

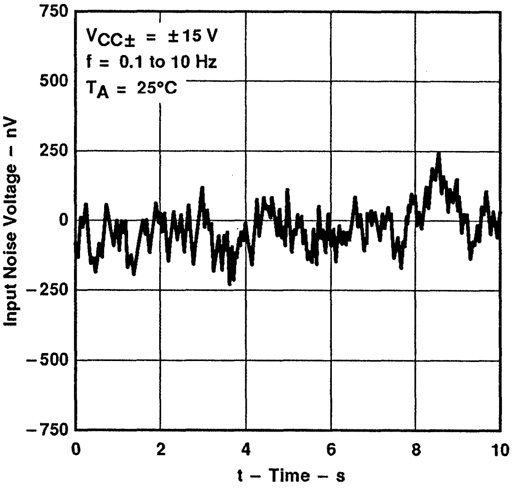


Figure 24

---

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

NOISE CURRENT
vs
FREQUENCY

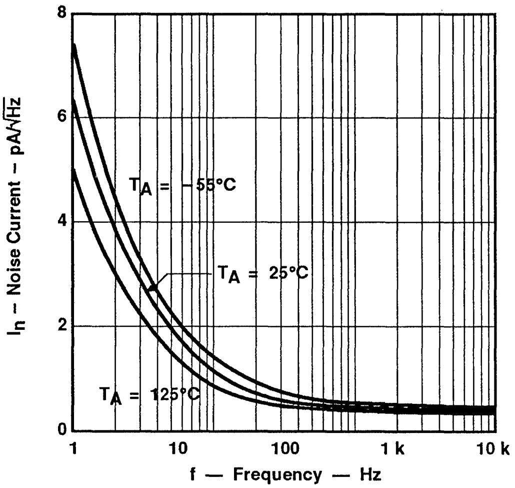


Figure 25

TOTAL HARMONIC DISTORTION
PLUS NOISE vs
FREQUENCY

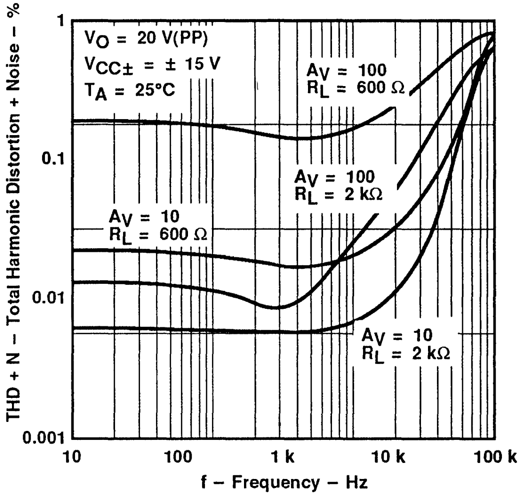


Figure 26

SLEW RATE
vs
FREE-AIR TEMPERATURE

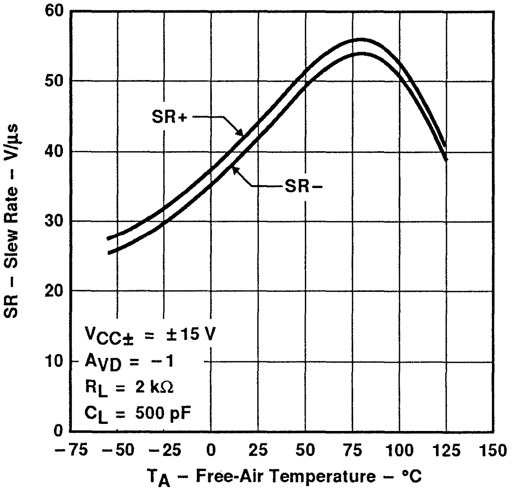


Figure 27

INPUT NOISE VOLTAGE
OVER A 10-SECOND PERIOD

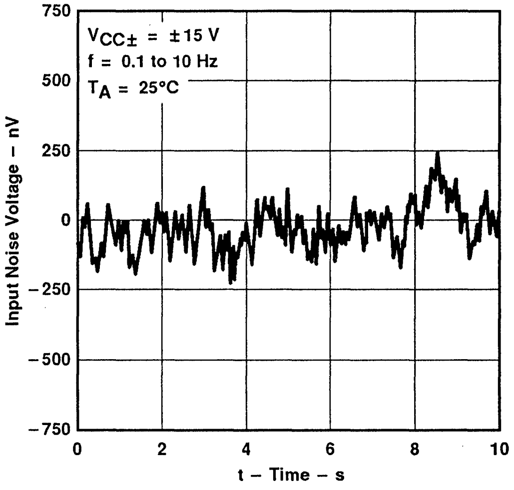


Figure 28

---

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

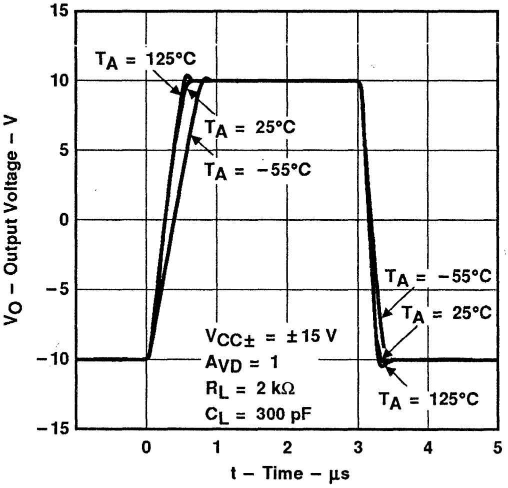

NONINVERTING LARGE-SIGNAL PULSE RESPONSE

Figure 29

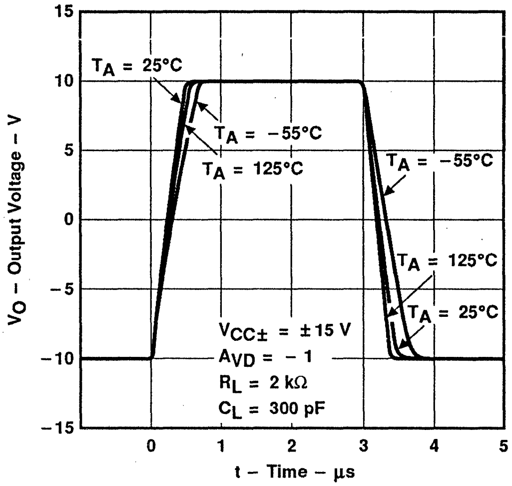

INVERTING LARGE-SIGNAL PULSE RESPONSE

Figure 30

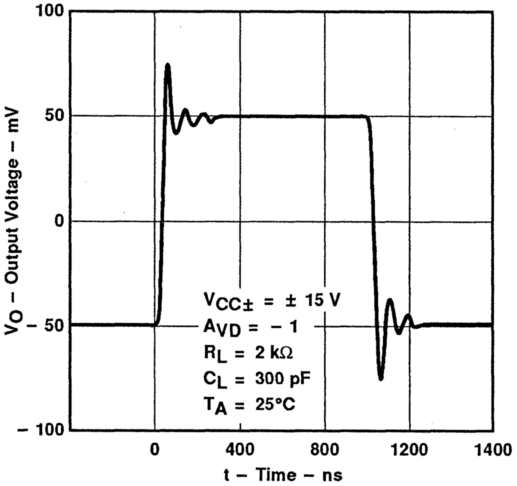

SMALL-SIGNAL PULSE RESPONSE

Figure 31

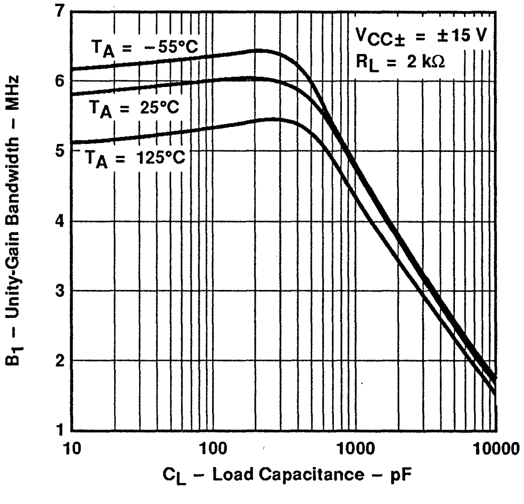

UNITY-GAIN BANDWIDTH vs LOAD CAPACITANCE

Figure 32

---

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

GAIN MARGIN
vs
LOAD CAPACITANCE

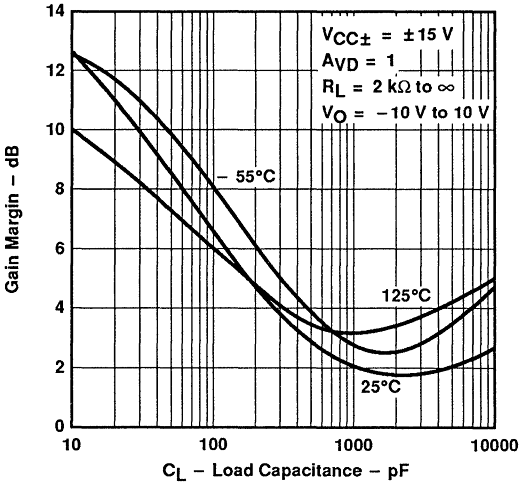


Figure 33

PHASE MARGIN
vs
LOAD CAPACITANCE

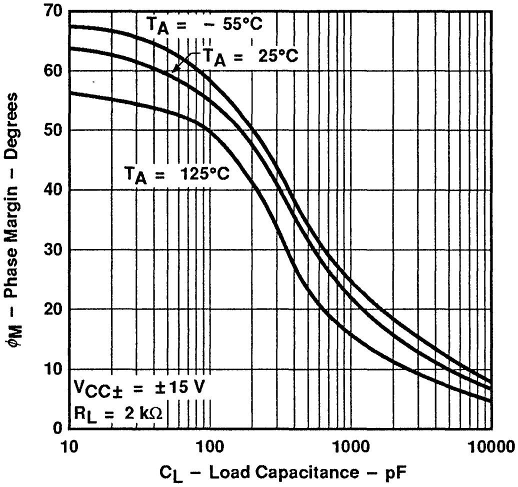


Figure 34

---

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TLE2161, TLE2161A, TLE2161B
EXCALIBUR JFET-INPUT HIGH-OUTPUT-DRIVE µPOWER OPERATIONAL AMPLIFIERS

D3371, NOVEMBER 1989 – REVISED FEBRUARY 1991

available features

- **Excellent Output Drive Capability**
  V_O = ± 2.5 V Min at R_L = 100 Ω, $V_{CC\pm}$ = ± 5 V
  V_O = ± 12.5 V Min at R_L = 600 Ω, $V_{CC\pm}$ = ± 15 V
- **Low Supply Current . . . 280 µA Typ**
- **Decompensated for High Slew Rate and Gain-Bandwidth Product**
  A_{VD} = 5 Min
  Slew Rate = 10 V/µs Typ
  Gain-Bandwidth Product = 6.5 MHz Typ
- **Macromodel Included**
- **Wide Operating Supply Voltage Range $V_{CC\pm}$ = ± 3.5 V to ± 20 V**
- **High Open-Loop Gain . . . 280 V/mV Typ**
- **Low Offset Voltage . . . 500 µV Max**
- **Low Offset Voltage Drift With Time 0.04 µV/month Typ**
- **Low Input Bias Current . . . 5 pA Typ**

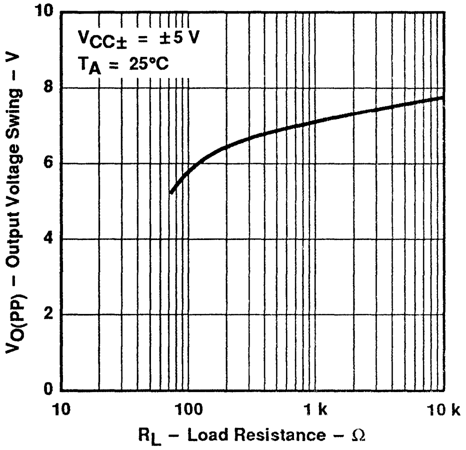
description

The TLE2161, TLE2161A, and TLE2161B are JFET-input, low-power, precision operational amplifiers manufactured using the Texas Instruments Excalibur process. Decompensated for stability with a minimum closed-loop gain of 5, these devices combine outstanding output drive capability with low power consumption, excellent dc precision, and high gain-bandwidth product.

In addition to maintaining the traditional JFET advantages of fast slew rates and low input bias and offset currents, the Excalibur process offers outstanding parametric stability over time and temperature. This results in a device that remains precise even with changes in temperature and over years of use.

A variety of available options includes small-outline packages and chip-carrier versions for high-density system applications.

MAXIMUM PEAK-TO-PEAK
OUTPUT VOLTAGE SWING
vs
LOAD RESISTANCE



AVAILABLE OPTIONS

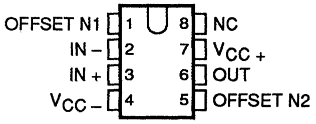
T_A	V_{IO} max AT 25°C	PACKAGE				
		SMALL-OUTLINE (D)	CHIP CARRIER (FK)	CERAMIC DIP (JG)	METAL CAN (L)	PLASTIC DIP (P)
0°C	500 µV	——	——	——	——	TLE2161BCP
to	1.5 mV	TLE2161ACD	——	——	——	TLE2161ACP
70°C	3 mV	TLE2161CD	——	——	——	TLE2161CP
– 40°C	500 µV	——	——	——	——	TLE2161BIP
to	1.5 mV	TLE2161AID	——	——	——	TLE2161AIP
85°C	3 mV	TLE2161ID	——	——	——	TLE2161IP
– 55°C	500 µV	——	——	TLE2161BMJG	TLE2161BML	TLE2161BMP
to	1.5 mV	TLE2161AMD	TLE2161AMFK	TLE2161AMJG	TLE2161AML	TLE2161AMP
125°C	3 mV	TLE2161MD	TLE2161MFK	TLE2161MJG	TLE2161ML	TLE2161MP

D packages are available taped and reeled. Add "R" suffix to device type, (e.g., TLE2161ACDR).

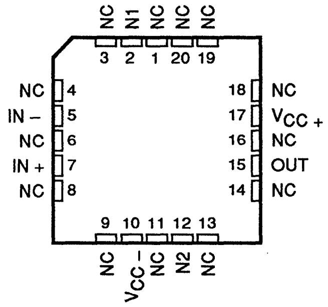
description (continued)

The C-suffix devices are characterized for operation from 0°C to 70°C . The I-suffix devices are characterized for operation from −40°C to 85°C. The M-suffix devices are characterized for operation over the full military temperature range of −55°C to 125°C.

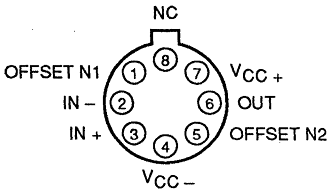
D, JG, OR P PACKAGE
(TOP VIEW)



FK PACKAGE
(TOP VIEW)



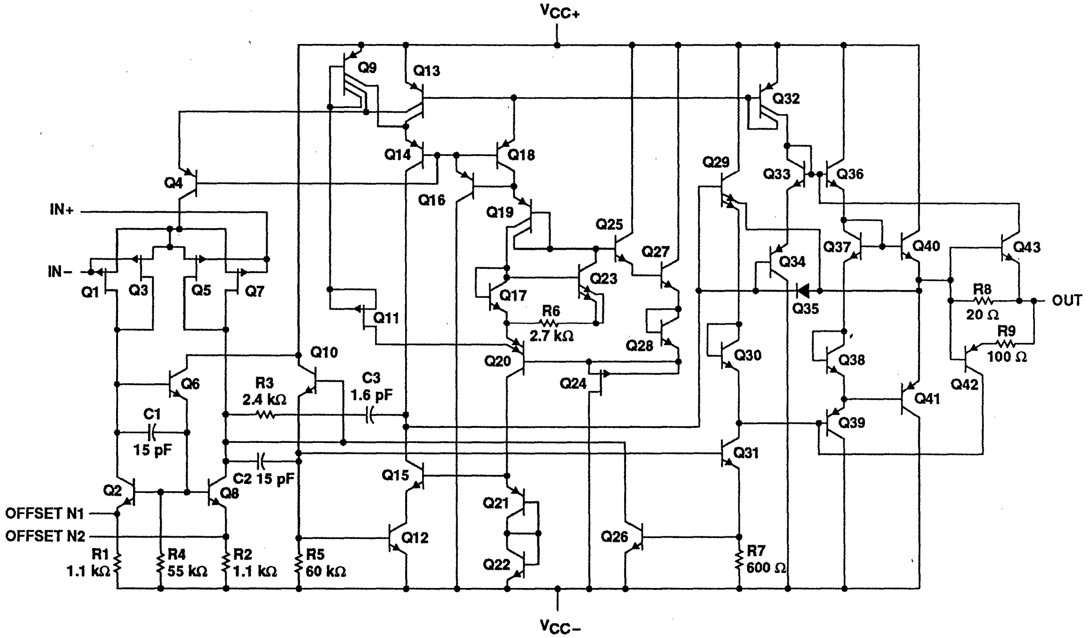
L PACKAGE
(TOP VIEW)



Pin 4 of the L package is in electrical contact with the case.

NC – No internal connection

equivalent schematic



All component values are nominal.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC+} (see Note 1) . . . . 22 V
Supply voltage, V_{CC-} . . . . −22 V
Differential input voltage (see Note 2) . . . . ±44 V
Input voltage range, V_I (any input) . . . . $V_{CC\pm}$
Input current, I_I (each input) . . . . ±1 mA
Output current, I_O . . . . ±80 mA
Total current into V_{CC+} terminal . . . . 80 mA
Total current out of V_{CC-} terminal . . . . 80 mA
Duration of short-circuit current at (or below) 25°C (see Note 3) . . . . unlimited
Continuous total dissipation . . . . See Dissipation Rating Table
Operating free-air temperature range, T_A: C-suffix . . . . 0°C to 70°C
I-suffix . . . . −40°C to 85°C
M-suffix . . . . −55°C to 125°C
Storage temperature range . . . . −65°C to 150°C
Case temperature for 60 seconds: FK package . . . . 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D or P package . . . . 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: JG or L package . . . . 300°C

NOTES: 1. All voltage values, except differential voltages, are with respect to the midpoint between V_{CC+} and V_{CC-}.
2. Differential voltages are at the noninverting input with respect to the inverting input.
3. The output may be shorted to either supply. Temperature and/or supply voltages must be limited to ensure that the maximum dissipation rating is not exceeded.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE T_A = 25°C	T_A = 70°C POWER RATING	T_A = 85°C POWER RATING	T_A = 125°C POWER RATING
D	725 mW	5.8 mW/°C	464 mW	377 mW	145 mW
FK	1375 mW	11.0 mW/°C	880 mW	715 mW	275 mW
JG	1050 mW	8.4 mW/°C	672 mW	546 mW	210 mW
L	650 mW	5.2 mW/°C	416 mW	338 mW	130 mW
P	1000 mW	8.0 mW/°C	640 mW	520 mW	200 mW

recommended operating conditions

		C-SUFFIX		I-SUFFIX		M-SUFFIX		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
Supply voltage, $V_{CC\pm}$		± 3.5	± 20	± 3.5	± 20	± 3.5	± 20	V
Common-mode input voltage, V_{IC}	$V_{CC\pm}$ = ± 5 V	− 1.6	4	− 1.6	4	− 1.6	4	V
	$V_{CC\pm}$ = ± 15 V	− 11	13	− 11	13	− 11	13	
	$V_{CC\pm}$ = ± 20 V	− 15	16.5	− 15	16.5	− 15	16.5	
Operating free-air temperature, T_A		0	70	− 40	85	− 55	125	°C

electrical characteristics at specified free-air temperature, $V_{CC\pm} = \pm 5$ V (unless otherwise noted)

PARAMETER			TEST CONDITIONS	T_A†	MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	TLE2161C	$V_{IC} = 0$, $R_S = 50\ \Omega$	25°C		0.8	3.1	mV
				Full range			4	
		TLE2161AC		25°C		0.6	2.6	
				Full range			3.5	
		TLE2161BC		25°C		0.5	1.9	
				Full range			2.4	
α_{VIO}	Temperature coefficient of input offset voltage			Full range		6		µV/°C
	Input offset voltage long-term drift (see Note 4)			25°C		0.04		µV/mo
I_{IO}	Input offset current			25°C		1		pA
				Full range			0.8	nA
I_{IB}	Input bias current			25°C		3		pA
				Full range			2	nA
V_{ICR}	Common-mode input voltage range			25°C	− 1.6 to 4	− 2 to 6		V
				Full range	− 1.6 to 4			V
V_{OM+}	Maximum positive peak output voltage swing		$R_L = 10$ kΩ	25°C	3.5	3.7		V
				Full range	3.3			
			$R_L = 100\ \Omega$	25°C	2.5	3.1		
				Full range	2			
V_{OM-}	Maximum negative peak output voltage swing		$R_L = 10$ kΩ	25°C	− 3.7	− 3.9		V
				Full range	− 3.3			
			$R_L = 100\ \Omega$	25°C	− 2.5	− 2.7		
				Full range	− 2			
A_{VD}	Large-signal differential voltage amplification		$V_O = \pm 2.8$ V, $R_L = 10$ kΩ	25°C	15	80		V/mV
				Full range	2			
			$V_O = 0$ to 2 V, $R_L = 100\ \Omega$	25°C	0.75	45		
				Full range	0.5			
			$V_O = 0$ to − 2 V, $R_L = 100\ \Omega$	25°C	0.5	3		
				Full range	0.25			
r_i	Input resistance			25°C		10^{12}		Ω
c_i	Input capacitance			25°C		4		pF
z_o	Open-loop output impedance		$I_O = 0$	25°C		280		Ω
CMRR	Common-mode rejection ratio		$V_{IC} = V_{ICR}$ min, $R_S = 50\ \Omega$	25°C	65	82		dB
				Full range	65			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm} / \Delta V_{IO}$)		$V_{CC\pm} = \pm 5$ V to ± 20 V, $R_S = 50\ \Omega$	25°C	75	93		dB
				Full range	75			
I_{CC}	Supply current		$V_O = 0$, No load	25°C		280	325	µA
				Full range			350	
ΔI_{CC}	Supply current change over operating temperature range			Full range		29		µA

†Full range is 0°C to 70°C.

NOTE 4: Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at $T_A = 150$°C extrapolated to $T_A = 25$°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

operating characteristics at specified free-air temperature, $V_{CC\pm}$ = ±5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A†	MIN	TYP	MAX	UNIT
SR	Slew rate (see Figure 1)	A_{VD} = 5, R_L = 10 kΩ, C_L = 100 pF	25°C	7	10		V/μs
			Full range	5			
V_n	Equivalent input noise voltage (see Figure 2)	R_S = 100 Ω, f = 10 Hz	25°C		59	100	nV/√Hz
		R_S = 100 Ω, f = 1 kHz			43	60	
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 10 Hz	25°C		1.1		μV
I_n	Equivalent input noise current	f = 1 kHz	25°C		1		fA/√Hz
THD	Total harmonic distortion	A_{VD} = 5, $V_{O(PP)}$ = 2 V, f = 10 kHz, R_L = 10 kΩ	25°C		0.025%		
	Gain-bandwidth product (see Figure 3)	f = 100 kHz, R_L = 10 kΩ, C_L = 100 pF	25°C		5.8		MHz
		f = 100 kHz, R_L = 100 Ω, C_L = 100 pF			4.3		
	Settling time	ε = 0.1%	25°C		5		μs
		ε = 0.01%			10		
B_{OM}	Maximum output-swing bandwidth	A_{VD} = 5, R_L = 10 kΩ	25°C		420		kHz
ϕ_m	Phase margin (see Figure 3)	A_{VD} = 5, R_L = 10 kΩ, C_L = 100 pF	25°C		70°		
		A_{VD} = 5, R_L = 100 Ω, C_L = 100 pF			84°		

†Full range is 0°C to 70°C.

electrical characteristics at specified free-air temperature, $V_{CC\pm}$ = ±15 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS	T_A†	MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	TLE2161C	V_{IC} = 0, R_S = 50 Ω	25°C		0.6	3	mV
				Full range			3.9	
		TLE2161AC		25°C		0.5	1.5	
				Full range			2.5	
		TLE2161BC		25°C		0.3	0.5	
				Full range			1	
α_{VIO}	Temperature coefficient of input offset voltage			Full range		6		µV/°C
	Input offset voltage long-term drift (see Note 4)			25°C		0.04		µV/mo
I_{IO}	Input offset current			25°C		2		pA
				Full range			1	nA
I_{IB}	Input bias current			25°C		4		pA
				Full range			3	nA
V_{ICR}	Common-mode input voltage range			25°C	− 11 to 13	− 12 to 16		V
				Full range	− 11 to 13			V
V_{OM+}	Maximum positive peak output voltage swing		R_L = 10 kΩ	25°C	13.2	13.7		V
				Full range	13			
			R_L = 600 Ω	25°C	12.5	13.2		
				Full range	12			
V_{OM-}	Maximum negative peak output voltage swing		R_L = 10 kΩ	25°C	− 13.2	− 13.7		V
				Full range	− 13			
			R_L = 600 Ω	25°C	− 12.5	− 13		
				Full range	− 12			
A_{VD}	Large-signal differential voltage amplification		V_O = ± 10 V, R_L = 10 kΩ	25°C	30	230		V/mV
				Full range	20			
			V_O = 0 to 8 V, R_L = 600 Ω	25°C	25	100		
				Full range	10			
			V_O = 0 to − 8 V, R_L = 600 Ω	25°C	3	25		
				Full range	1			
r_i	Input resistance			25°C		10^{12}		Ω
c_i	Input capacitance			25°C		4		pF
z_o	Open-loop output impedance		I_O = 0	25°C		280		Ω
CMRR	Common-mode rejection ratio		V_{IC} = V_{ICR}min, R_S = 50 Ω	25°C	72	90		dB
				Full range	70			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm} / \Delta V_{IO}$)		$V_{CC\pm}$ = ±5 V to ± 15 V, R_S = 50 Ω	25°C	75	93		dB
				Full range	75			
I_{CC}	Supply current		V_O = 0, No load	25°C		290	350	µA
				Full range			375	
ΔI_{CC}	Supply current change over operating temperature range			Full range		34		µA

†Full range is 0°C to 70°C.

NOTE 4: Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at T_A = 150°C extrapolated to T_A = 25°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

operating characteristics at specified free-air temperature, $V_{CC\pm}$ = ±15 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A†	MIN	TYP	MAX	UNIT
SR	Slew rate (see Figure 1)	A_{VD} = 5, R_L = 10 kΩ, C_L = 100 pF	25°C	7	10		V/μs
			Full range	5			
V_n	Equivalent input noise voltage (see Figure 2)	R_S = 100 Ω, f = 10 Hz	25°C		70	100	nV/√Hz
		R_S = 100 Ω, f = 1 kHz			40	60	
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 10 Hz	25°C		1.1		μV
I_n	Equivalent input noise current	f = 1 kHz	25°C		1.1		fA/√Hz
THD	Total harmonic distortion	A_{VD} = 5, $V_{O(PP)}$ = 2 V, f = 10 kHz, R_L = 10 kΩ	25°C		0.025%		
	Gain-bandwidth product (see Figure 3)	f = 100 kHz, R_L = 10 kΩ, C_L = 100 pF	25°C		6.4		MHz
		f = 100 kHz, R_L = 600 Ω, C_L = 100 pF			5.6		
	Settling time	ε = 0.1%	25°C		5		μs
		ε = 0.01%			10		
B_{OM}	Maximum output-swing bandwidth	A_{VD} = 5, R_L = 10 kΩ	25°C		116		kHz
ϕ_m	Phase margin (see Figure 3)	A_{VD} = 5, R_L = 10 kΩ, C_L = 100 pF	25°C		72°		
		A_{VD} = 5, R_L = 600 Ω, C_L = 100 pF			78°		

† Full range is 0°C to 70°C.

electrical characteristics at specified free-air temperature, $V_{CC\pm}$ = ±20 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS	T_A†	MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	TLE2161C	V_{IC} = 0, R_S = 50 Ω	25°C		0.6	3	mV
				Full range			3.9	
		TLE2161AC		25°C		0.6	1.6	
				Full range			2.5	
		TLE2161BC		25°C		0.3	0.5	
				Full range			1	
α_{VIO}	Temperature coefficient of input offset voltage			Full range		6		μV/°C
	Input offset voltage long-term drift (see Note 4)			25°C		0.04		μV/mo
I_{IO}	Input offset current			25°C		3		pA
				Full range			1	nA
I_{IB}	Input bias current			25°C		5		pA
				Full range			3	nA
V_{ICR}	Common-mode input voltage range			25°C	−15 to 16.5	−17 to 21		V
				Full range	−15 to 16.5			V
V_{OM+}	Maximum positive peak output voltage swing		R_L = 10 kΩ	25°C	18.2	18.7		V
				Full range	18			
			R_L = 600 Ω	25°C	15	18.1		
				Full range	12			
V_{OM-}	Maximum negative peak output voltage swing		R_L = 10 kΩ	25°C	−18.2	−18.7		V
				Full range	−18			
			R_L = 600 Ω	25°C	−15	−18		
				Full range	−12			
A_{VD}	Large-signal differential voltage amplification		V_O = ±15 V, R_L = 10 kΩ	25°C	30	280		V/mV
				Full range	20			
			V_O = 0 to 10 V, R_L = 600 Ω	25°C	25	80		
				Full range	10			
			V_O = 0 to −10 V, R_L = 600 Ω	25°C	3	20		
				Full range	1			
r_i	Input resistance			25°C		10^{12}		Ω
c_i	Input capacitance			25°C		4		pF
z_o	Open-loop output impedance		I_O = 0	25°C		280		Ω
CMRR	Common-mode rejection ratio		V_{IC} = V_{ICR} min, R_S = 50 Ω	25°C	75	91		dB
				Full range	70			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm} / \Delta V_{IO}$)		$V_{CC\pm}$ = ±5 V to ±20 V, R_S = 50 Ω	25°C	75	93		dB
				Full range	70			
I_{CC}	Supply current		V_O = 0, No load	25°C		300	375	μA
				Full range			400	
ΔI_{CC}	Supply current change over operating temperature range			Full range		18		μA

†Full range is 0°C to 70°C.

NOTE 4: Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at T_A = 150°C extrapolated to T_A = 25°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

operating characteristics at specified free-air temperature, $V_{CC\pm}$ = ±20 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A†	MIN	TYP	MAX	UNIT
SR	Slew rate (see Figure 1)	A_{VD} = 5, R_L = 10 kΩ, C_L = 100 pF	25°C	7	10		V/μs
			Full range	5			
V_n	Equivalent input noise voltage (see Figure 2)	R_S = 100 Ω, f = 10 Hz	25°C		75	100	nV/√Hz
		R_S = 100 Ω, f = 1 kHz			40	60	
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 10 Hz	25°C		1.1		μV
I_n	Equivalent input noise current	f = 1 kHz	25°C		1.3		fA/√Hz
THD	Total harmonic distortion	A_{VD} = 5, $V_{O(PP)}$ = 2 V, f = 10 kHz, R_L = 10 kΩ	25°C		0.025%		
	Gain-bandwidth product (see Figure 3)	f = 100 kHz, R_L = 10 kΩ, C_L = 100 pF	25°C		6.5		MHz
		f = 100 kHz, R_L = 600 Ω, C_L = 100 pF			5.7		
	Settling time	ε = 0.1%	25°C		5		μs
		ε = 0.01%			10		
B_{OM}	Maximum output-swing bandwidth	A_{VD} = 5, R_L = 10 kΩ	25°C		85		kHz
ϕ_m	Phase margin (see Figure 3)	A_{VD} = 5, R_L = 10 kΩ, C_L = 100 pF	25°C		72°		
		A_{VD} = 5, R_L = 600 Ω, C_L = 100 pF			78°		

†Full range is 0°C to 70°C.

electrical characteristics at specified free-air temperature, $V_{CC\pm} = \pm 5$ V (unless otherwise noted)

PARAMETER			TEST CONDITIONS	T_A†	MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	TLE2161I	$V_{IC} = 0$, $R_S = 50\ \Omega$	25°C		0.8	3.1	mV
				Full range			4.4	
		TLE2161AI		25°C		0.6	2.6	
				Full range			3.9	
		TLE2161BI		25°C		0.5	1.9	
				Full range			2.7	
α_{VIO}	Temperature coefficient of input offset voltage			Full range		6		µV/°C
	Input offset voltage long-term drift (see Note 4)			25°C		0.04		µV/mo
I_{IO}	Input offset current			25°C		1		pA
				Full range			2	nA
I_{IB}	Input bias current			25°C		3		pA
				Full range			4	nA
V_{ICR}	Common-mode input voltage range			25°C	−1.6 to 4	−2 to 6		V
				Full range	−1.6 to 4			V
V_{OM+}	Maximum positive peak output voltage swing		$R_L = 10\ k\Omega$	25°C	3.5	3.7		V
				Full range	3.1			
			$R_L = 100\ \Omega$	25°C	2.5	3.1		
				Full range	2			
V_{OM-}	Maximum negative peak output voltage swing		$R_L = 10\ k\Omega$	25°C	−3.7	−3.9		V
				Full range	−3.1			
			$R_L = 100\ \Omega$	25°C	−2.5	−2.7		
				Full range	−2			
A_{VD}	Large-signal differential voltage amplification		$V_O = \pm 2.8$ V, $R_L = 10\ k\Omega$	25°C	15	80		V/mV
				Full range	2			
			$V_O = 0$ to 2 V, $R_L = 100\ \Omega$	25°C	0.75	45		
				Full range	0.5			
			$V_O = 0$ to −2 V, $R_L = 100\ \Omega$	25°C	0.5	3		
				Full range	0.25			
r_i	Input resistance			25°C		10^{12}		Ω
c_i	Input capacitance			25°C		4		pF
z_o	Open-loop output impedance		$I_O = 0$	25°C		280		Ω
CMRR	Common-mode rejection ratio		$V_{IC} = V_{ICR}$ min, $R_S = 50\ \Omega$	25°C	65	82		dB
				Full range	65			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm} / \Delta V_{IO}$)		$V_{CC\pm} = \pm 5$ V to ±20 V, $R_S = 50\ \Omega$	25°C	75	93		dB
				Full range	65			
I_{CC}	Supply current		$V_O = 0$, No load	25°C		280	325	µA
				Full range			350	
ΔI_{CC}	Supply current change over operating temperature range			Full range		29		µA

†Full range is − 40°C to 85°C.

NOTE 4: Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at $T_A = 150$°C extrapolated to $T_A = 25$°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

operating characteristics at specified free-air temperature, $V_{CC\pm}$ = ±5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A†	MIN	TYP	MAX	UNIT
SR	Slew rate (see Figure 1)	A_{VD} = 5, R_L = 10 kΩ, C_L = 100 pF	25°C	7	10		V/μs
			Full range	5			
V_n	Equivalent input noise voltage (see Figure 2)	R_S = 100 Ω, f = 10 Hz	25°C		59	100	nV/√Hz
		R_S = 100 Ω, f = 1 kHz			43	60	
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 10 Hz	25°C		1.1		μV
I_n	Equivalent input noise current	f = 1 kHz	25°C		1		fA/√Hz
THD	Total harmonic distortion	A_{VD} = 5, $V_{O(PP)}$ = 2 V, f = 10 kHz, R_L = 10 kΩ	25°C		0.025%		
	Gain-bandwidth product (see Figure 3)	f = 100 kHz, R_L = 10 kΩ, C_L = 100 pF	25°C		5.8		MHz
		f = 100 kHz, R_L = 100 Ω, C_L = 100 pF			4.3		
	Settling time	ε = 0.1%	25°C		5		μs
		ε = 0.01%			10		
B_{OM}	Maximum output-swing bandwidth	A_{VD} = 5, R_L = 10 kΩ	25°C		420		kHz
ϕ_m	Phase margin (see Figure 3)	A_{VD} = 5, R_L = 10 kΩ, C_L = 100 pF	25°C		70°		
		A_{VD} = 5, R_L = 100 Ω, C_L = 100 pF			84°		

†Full range is – 40°C to 85°C.

electrical characteristics at specified free-air temperature, $V_{CC\pm}$ = ±15 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS	T_A†	MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	TLE2161I	V_{IC} = 0, R_S = 50 Ω	25°C		0.6	3	mV
				Full range			4.3	
		TLE2161AI		25°C		0.5	1.5	
				Full range			2.9	
		TLE2161BI		25°C		0.3	0.5	
				Full range			1.3	
α_{VIO}	Temperature coefficient of input offset voltage			Full range		6		µV/°C
	Input offset voltage long-term drift (see Note 4)			25°C		0.04		µV/mo
I_{IO}	Input offset current			25°C		2		pA
				Full range			3	nA
I_{IB}	Input bias current			25°C		4		pA
				Full range			5	nA
V_{ICR}	Common-mode input voltage range			25°C	−11 to 13	−12 to 16		V
				Full range	−11 to 13			V
V_{OM+}	Maximum positive peak output voltage swing		R_L = 10 kΩ	25°C	13.2	13.7		V
				Full range	13			
			R_L = 600 Ω	25°C	12.5	13.2		
				Full range	12			
V_{OM-}	Maximum negative peak output voltage swing		R_L = 10 kΩ	25°C	−13.2	−13.7		V
				Full range	−13			
			R_L = 600 Ω	25°C	−12.5	−13		
				Full range	−12			
A_{VD}	Large-signal differential voltage amplification		V_O = ±10 V, R_L = 10 kΩ	25°C	30	230		V/mV
				Full range	20			
			V_O = 0 to 8 V, R_L = 600 Ω	25°C	25	100		
				Full range	10			
			V_O = 0 to −8 V, R_L = 600 Ω	25°C	3	25		
				Full range	1			
r_i	Input resistance			25°C		10^{12}		Ω
c_i	Input capacitance			25°C		4		pF
z_o	Open-loop output impedance		I_O = 0	25°C		280		Ω
CMRR	Common-mode rejection ratio		V_{IC} = V_{ICR}min, R_S = 50 Ω	25°C	72	90		dB
				Full range	65			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm}/\Delta V_{IO}$)		$V_{CC\pm}$ = ±5 V to ±15 V, R_S = 50 Ω	25°C	75	93		dB
				Full range	65			
I_{CC}	Supply current		V_O = 0, No load	25°C		290	350	µA
				Full range			375	
ΔI_{CC}	Supply current change over operating temperature range			Full range		34		µA

†Full range is −40°C to 85°C.

NOTE 4: Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at T_A = 150°C extrapolated to T_A = 25°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

operating characteristics at specified free-air temperature, $V_{CC\pm} = \pm 15$ V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A†	MIN	TYP	MAX	UNIT
SR	Slew rate (see Figure 1)	$A_{VD} = 5$, $R_L = 10$ kΩ, $C_L = 100$ pF	25°C	7	10		V/μs
			Full range	5			
V_n	Equivalent input noise voltage (see Figure 2)	$R_S = 100\ \Omega$, f = 10 Hz	25°C		70	100	nV/√Hz
		$R_S = 100\ \Omega$, f = 1 kHz			40	60	
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 10 Hz	25°C		1.1		μV
I_n	Equivalent input noise current	f = 1 kHz	25°C		1.1		fA/√Hz
THD	Total harmonic distortion	$A_{VD} = 5$, $V_{O(PP)} = 2$ V, f = 10 kHz, $R_L = 10$ kΩ	25°C		0.025%		
	Gain-bandwidth product (see Figure 3)	f = 100 kHz, $R_L = 10$ kΩ, $C_L = 100$ pF	25°C		6.4		MHz
		f = 100 kHz, $R_L = 600\ \Omega$, $C_L = 100$ pF			5.6		
	Settling time	ε = 0.1%	25°C		5		μs
		ε = 0.01%			10		
B_{OM}	Maximum output-swing bandwidth	$A_{VD} = 5$, $R_L = 10$ kΩ	25°C		116		kHz
ϕ_m	Phase margin (see Figure 3)	$A_{VD} = 5$, $R_L = 10$ kΩ, $C_L = 100$ pF	25°C		72°		
		$A_{VD} = 5$, $R_L = 600\ \Omega$, $C_L = 100$ pF			78°		

† Full range is – 40°C to 85°C.

electrical characteristics at specified free-air temperature, $V_{CC\pm} = \pm 20$ V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A†	MIN	TYP	MAX	UNIT
V_{IO} Input offset voltage	TLE2161I	$V_{IC} = 0$, $R_S = 50\ \Omega$	25°C		0.6	3	mV
			Full range			4.3	
	TLE2161AI		25°C		0.6	1.6	
			Full range			2.9	
	TLE2161BI		25°C		0.3	0.5	
			Full range			1.3	
α_{VIO} Temperature coefficient of input offset voltage			Full range		6		μV/°C
Input offset voltage long-term drift (see Note 4)			25°C		0.04		μV/mo
I_{IO} Input offset current			25°C		3		pA
			Full range			3	nA
I_{IB} Input bias current			25°C		5		pA
			Full range			5	nA
V_{ICR} Common-mode input voltage range			25°C	−15 to 16.5	−17 to 21		V
			Full range	−15 to 16.5			V
V_{OM+} Maximum positive peak output voltage swing		$R_L = 10\ k\Omega$	25°C	18.2	18.7		V
			Full range	18			
		$R_L = 600\ \Omega$	25°C	15	18.1		
			Full range	12			
V_{OM-} Maximum negative peak output voltage swing		$R_L = 10\ k\Omega$	25°C	−18.2	−18.7		V
			Full range	−18			
		$R_L = 600\ \Omega$	25°C	−15	−18		
			Full range	−12			
A_{VD} Large-signal differential voltage amplification		$V_O = \pm 15$ V, $R_L = 10\ k\Omega$	25°C	30	280		V/mV
			Full range	20			
		$V_O = 0$ to 10 V, $R_L = 600\ \Omega$	25°C	25	80		
			Full range	10			
		$V_O = 0$ to −10 V, $R_L = 600\ \Omega$	25°C	3	20		
			Full range	1			
r_i Input resistance			25°C		10^{12}		Ω
c_i Input capacitance			25°C		4		pF
z_o Open-loop output impedance		$I_O = 0$	25°C		280		Ω
CMRR Common-mode rejection ratio		$V_{IC} = V_{ICR}$ min, $R_S = 50\ \Omega$	25°C	75	91		dB
			Full range	65			
k_{SVR} Supply-voltage rejection ratio ($\Delta V_{CC\pm} / \Delta V_{IO}$)		$V_{CC\pm} = \pm 5$ V to ±20 V, $R_S = 50\ \Omega$	25°C	75	93		dB
			Full range	65			
I_{CC} Supply current		$V_O = 0$, No load	25°C		300	375	μA
			Full range			400	
ΔI_{CC} Supply current change over operating temperature range			Full range		36		μA

†Full range is − 40°C to 85°C.

NOTE 4: Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at $T_A = 150°C$ extrapolated to $T_A = 25°C$ using the Arrhenius equation and assuming an activation energy of 0.96 eV.

operating characteristics at specified free-air temperature, $V_{CC\pm}$ = ±20 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A†	MIN	TYP	MAX	UNIT
SR	Slew rate (see Figure 1)	A_{VD} = 5, R_L = 10 kΩ, C_L = 100 pF	25°C	7	10		V/μs
			Full range	5			
V_n	Equivalent input noise voltage (see Figure 2)	R_S = 100 Ω, f = 10 Hz	25°C		75	100	nV/√Hz
		R_S = 100 Ω, f = 1 kHz			40	60	
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 10 Hz	25°C		1.1		μV
I_n	Equivalent input noise current	f = 1 kHz	25°C		1.3		fA/√Hz
THD	Total harmonic distortion	A_{VD} = 5, $V_{O(PP)}$ = 2 V, f = 10 kHz, R_L = 10 kΩ	25°C		0.025%		
	Gain-bandwidth product (see Figure 3)	f = 100 kHz, R_L = 10 kΩ, C_L = 100 pF	25°C		6.5		MHz
		f = 100 kHz, R_L = 600 Ω, C_L = 100 pF			5.7		
	Settling time	ε = 0.1%	25°C		5		μs
		ε = 0.01%			10		
B_{OM}	Maximum output-swing bandwidth	A_{VD} = 5, R_L = 10 kΩ	25°C		85		kHz
ϕ_m	Phase margin (see Figure 3)	A_{VD} = 5, R_L = 10 kΩ, C_L = 100 pF	25°C		72°		
		A_{VD} = 5, R_L = 600 Ω, C_L = 100 pF			78°		

† Full range is – 40°C to 85°C.

electrical characteristics at specified free-air temperature, $V_{CC\pm} = \pm 5$ V (unless otherwise noted)

PARAMETER			TEST CONDITIONS	T_A†	MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	TLE2161M	$V_{IC} = 0$, $R_S = 50\ \Omega$	25°C		0.8	3.1	mV
				Full range			6	
		TLE2161AM		25°C		0.6	2.6	
				Full range			4.6	
		TLE2161BM		25°C		0.5	1.9	
				Full range			3.1	
α_{VIO}	Temperature coefficient of input offset voltage			Full range		6		µV/°C
	Input offset voltage long-term drift (see Note 4)			25°C		0.04		µV/mo
I_{IO}	Input offset current			25°C		1		pA
				Full range			15	nA
I_{IB}	Input bias current			25°C		3		pA
				Full range			30	nA
V_{ICR}	Common-mode input voltage range			25°C	−1.6 to 4	−2 to 6		V
				Full range	−1.6 to 4			V
V_{OM+}	Maximum positive peak output voltage swing		$R_L = 10\ k\Omega$	25°C	3.5	3.7		V
				Full range	3			
		FK, JG, and L packages	$R_L = 600\ \Omega$	25°C	2.5	3.6		
				Full range	2			
		D and P packages	$R_L = 100\ \Omega$	25°C	2.5	3.1		
				Full range	2			
V_{OM-}	Maximum negative peak output voltage swing		$R_L = 10\ k\Omega$	25°C	−3.7	−3.9		V
				Full range	−3			
		FK, JG, and L packages	$R_L = 600\ \Omega$	25°C	−2.5	−3.5		
				Full range	−2			
		D and P packages	$R_L = 100\ \Omega$	25°C	−2.5	−2.7		
				Full range	−2			
A_{VD}	Large-signal differential voltage amplification		$V_O = \pm 2.8$ V, $R_L = 10\ k\Omega$	25°C	15	80		V/mV
				Full range	2			
		FK, JG, and L packages	$V_O = 0$ to 2.5 V, $R_L = 600\ \Omega$	25°C	1	65		
				Full range	0.5			
			$V_O = 0$ to −2.5 V, $R_L = 600\ \Omega$	25°C	1	16		
				Full range	0.5			
		D and P packages	$V_O = 0$ to 2 V, $R_L = 100\ \Omega$	25°C	0.75	45		
				Full range	0.5			
			$V_O = 0$ to −2 V, $R_L = 100\ \Omega$	25°C	0.5	3		
				Full range	0.25			

†Full range is −55°C to 125°C.

NOTE 4: Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at T_A = 150°C extrapolated to T_A = 25°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

electrical characteristics at specified free-air temperature, $V_{CC\pm}$ = ±5 V (unless otherwise noted) (continued)

PARAMETER		TEST CONDITIONS	T_A†	MIN	TYP	MAX	UNIT
r_i	Input resistance		25°C		10^{12}		Ω
c_i	Input capacitance		25°C		4		pF
z_o	Open-loop output impedance	$I_O = 0$	25°C		280		Ω
CMRR	Common-mode rejection ratio	$V_{IC} = V_{ICR}$ min, $R_S = 50\ \Omega$	25°C	65	82		dB
			Full range	60			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm} / \Delta V_{IO}$)	$V_{CC\pm} = \pm5$ V to ±20 V, $R_S = 50\ \Omega$	25°C	75	93		dB
			Full range	65			
I_{CC}	Supply current	$V_O = 0$, No load	25°C		280	325	μA
			Full range			350	
ΔI_{CC}	Supply current change over operating temperature range		Full range		39		μA

†Full range is – 55°C to 125°C.

operating characteristics, $V_{CC\pm}$ = ±5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SR	Slew rate (see Figure 1)	$A_{VD} = 5$, $R_L = 10\ k\Omega$, $C_L = 100$ pF		10		V/μs
V_n	Equivalent input noise voltage (see Figure 2)	$R_S = 100\ \Omega$, f = 10 Hz		59		nV/√Hz
		$R_S = 100\ \Omega$, f = 1 kHz		43		
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 10 Hz		1.1		μV
I_n	Equivalent input noise current	f = 1 kHz		1		fA/√Hz
THD	Total harmonic distortion	$A_{VD} = 5$, $V_{O(PP)} = 2$ V, f = 10 kHz, $R_L = 10\ k\Omega$		0.025%		
	Gain-bandwidth product (see Figure 3)	f = 100 kHz, $R_L = 10\ k\Omega$, $C_L = 100$ pF		5.8		MHz
		f = 100 kHz, $R_L = 600\ \Omega$, $C_L = 100$ pF		4.3		
	Settling time	ε = 0.1%		5		μs
		ε = 0.01%		10		
B_{OM}	Maximum output-swing bandwidth	$A_{VD} = 5$, $R_L = 10\ k\Omega$		420		kHz
ϕ_m	Phase margin (see Figure 3)	$A_{VD} = 5$, $R_L = 10\ k\Omega$, $C_L = 100$ pF		70°		
		$A_{VD} = 5$, $R_L = 600\ \Omega$, $C_L = 100$ pF		84°		

electrical characteristics at specified free-air temperature, $V_{CC\pm} = \pm 15$ V (unless otherwise noted)

PARAMETER			TEST CONDITIONS	T_A†	MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	TLE2161M	$V_{IC} = 0$, $R_S = 50\ \Omega$	25°C		0.6	3	mV
				Full range			6	
		TLE2161AM		25°C		0.5	1.5	
				Full range			3.6	
		TLE2161BM		25°C		0.3	0.5	
				Full range			1.7	
α_{VIO}	Temperature coefficient of input offset voltage			Full range		6		µV/°C
	Input offset voltage long-term drift (see Note 4)			25°C		0.04		µV/mo
I_{IO}	Input offset current			25°C		2		pA
				Full range			20	nA
I_{IB}	Input bias current			25°C		4		pA
				Full range			40	nA
V_{ICR}	Common-mode input voltage range			25°C	−11 to 13	−12 to 16		V
				Full range	−11 to 13			V
V_{OM+}	Maximum positive peak output voltage swing		$R_L = 10\ k\Omega$	25°C	13.2	13.7		V
				Full range	12.5			
			$R_L = 600\ \Omega$	25°C	12.5	13.2		
				Full range	12			
V_{OM-}	Maximum negative peak output voltage swing		$R_L = 10\ k\Omega$	25°C	−13.2	−13.7		V
				Full range	−12.5			
			$R_L = 600\ \Omega$	25°C	−12.5	−13		
				Full range	−12			
A_{VD}	Large-signal differential voltage amplification		$V_O = \pm 10$ V, $R_L = 10\ k\Omega$	25°C	30	230		V/mV
				Full range	20			
			$V_O = 0$ to 8 V, $R_L = 600\ \Omega$	25°C	25	100		
				Full range	7			
			$V_O = 0$ to −8 V, $R_L = 600\ \Omega$	25°C	3	25		
				Full range	1			
r_i	Input resistance			25°C		10^{12}		Ω
c_i	Input capacitance			25°C		4		pF
z_o	Open-loop output impedance		$I_O = 0$	25°C		280		Ω
CMRR	Common-mode rejection ratio		$V_{IC} = V_{ICR}$ min, $R_S = 50\ \Omega$	25°C	72	90		dB
				Full range	65			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm} / \Delta V_{IO}$)		$V_{CC\pm} = \pm 5$ V to ± 15 V, $R_S = 50\ \Omega$	25°C	75	93		dB
				Full range	65			
I_{CC}	Supply current		$V_O = 0$, No load	25°C		290	350	µA
				Full range			375	
ΔI_{CC}	Supply current change over operating temperature range			Full range		46		µA

†Full range is −55°C to 125°C.

NOTE 4: Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at $T_A = 150°C$ extrapolated to $T_A = 25°C$ using the Arrhenius equation and assuming an activation energy of 0.96 eV.

operating characteristics at specified free-air temperature, $V_{CC\pm}$ = ±15 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A†	MIN	TYP	MAX	UNIT
SR	Slew rate (see Figure 1)	A_{VD} = 5, R_L = 10 kΩ, C_L = 100 pF	25°C	7	10		V/μs
			Full range	5			
V_n	Equivalent input noise voltage (see Figure 2)	R_S = 100 Ω, f = 10 Hz	25°C		70		nV/√Hz
		R_S = 100 Ω, f = 1 kHz			40		
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 10 Hz	25°C		1.1		μV
I_n	Equivalent input noise current	f = 1 kHz	25°C		1.1		fA/√Hz
THD	Total harmonic distortion	A_{VD} = 5, $V_{O(PP)}$ = 2 V, f = 10 kHz, R_L = 10 kΩ	25°C		0.025%		
	Gain-bandwidth product (see Figure 3)	f = 100 kHz, R_L = 10 kΩ, C_L = 100 pF	25°C		6.4		MHz
		f = 100 kHz, R_L = 600 Ω, C_L = 100 pF			5.6		
	Settling time	ε = 0.1%	25°C		5		μs
		ε = 0.01%			10		
B_{OM}	Maximum output-swing bandwidth	A_{VD} = 5, R_L = 10 kΩ	25°C		116		kHz
ϕ_m	Phase margin (see Figure 3)	A_{VD} = 5, R_L = 10 kΩ, C_L = 100 pF	25°C		72°		
		A_{VD} = 5, R_L = 600 Ω, C_L = 100 pF			78°		

†Full range is – 55°C to 125°C.

electrical characteristics at specified free-air temperature, $V_{CC\pm} = \pm 20$ V (unless otherwise noted)

PARAMETER			TEST CONDITIONS	T_A†	MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	TLE2161M	$V_{IC} = 0$, $R_S = 50\ \Omega$	25°C		0.6	3	mV
				Full range			6	
		TLE2161AM		25°C		0.6	1.6	
				Full range			3.6	
		TLE2161BM		25°C		0.3	0.5	
				Full range			1.7	
α_{VIO}	Temperature coefficient of input offset voltage			Full range		6		µV/°C
	Input offset voltage long-term drift (see Note 4)			25°C		0.04		µV/mo
I_{IO}	Input offset current			25°C		3		pA
				Full range			20	nA
I_{IB}	Input bias current			25°C		5		pA
				Full range			40	nA
V_{ICR}	Common-mode input voltage range			25°C	− 15 to 16.5	− 17 to 21		V
				Full range	− 15 to 16.5			V
V_{OM+}	Maximum positive peak output voltage swing		$R_L = 10\ k\Omega$	25°C	18.2	18.7		V
				Full range	17.5			
			$R_L = 600\ \Omega$	25°C	15	18.1		
				Full range	12			
V_{OM-}	Maximum negative peak output voltage swing		$R_L = 10\ k\Omega$	25°C	− 18.2	− 18.7		V
				Full range	− 17.5			
			$R_L = 600\ \Omega$	25°C	− 15	− 18		
				Full range	− 12			
A_{VD}	Large-signal differential voltage amplification		$V_O = \pm 15$ V, $R_L = 10\ k\Omega$	25°C	30	280		V/mV
				Full range	20			
			$V_O = 0$ to 10 V, $R_L = 600\ \Omega$	25°C	25	80		
				Full range	10			
			$V_O = 0$ to − 10 V, $R_L = 600\ \Omega$	25°C	3	20		
				Full range	1			
r_i	Input resistance			25°C		10^{12}		Ω
c_i	Input capacitance			25°C		4		pF
z_o	Open-loop output impedance		$I_O = 0$	25°C		280		Ω
CMRR	Common-mode rejection ratio		$V_{IC} = V_{ICR}$ min, $R_S = 50\ \Omega$	25°C	75	91		dB
				Full range	65			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm} / \Delta V_{IO}$)		$V_{CC\pm} = \pm 5$ V to ± 20 V, $R_S = 50\ \Omega$	25°C	75	93		dB
				Full range	65			
I_{CC}	Supply current		$V_O = 0$, No load	25°C		300	375	µA
				Full range			400	
ΔI_{CC}	Supply current change over operating temperature range			Full range		50		µA

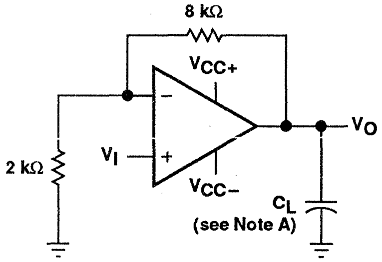
†Full range is − 55°C to 125°C.

NOTE 4: Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at $T_A = 150°C$ extrapolated to $T_A = 25°C$ using the Arrhenius equation and assuming an activation energy of 0.96 eV.

operating characteristics, $V_{CC\pm}$ = ±20 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SR	Slew rate (see Figure 1)	A_{VD} = 5, R_L = 10 kΩ, C_L = 100 pF		10		V/μs
V_n	Equivalent input noise voltage (see Figure 2)	R_S = 100 Ω, f = 10 Hz		75		nV/√Hz
		R_S = 100 Ω, f = 1 kHz		40		
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 10 Hz		1.1		μV
I_n	Equivalent input noise current	f = 1 kHz		1.3		fA/√Hz
THD	Total harmonic distortion	A_{VD} = 5, $V_{O(PP)}$ = 2 V, f = 10 kHz, R_L = 10 kΩ		0.025%		
	Gain-bandwidth product (see Figure 3)	f = 100 kHz, R_L = 10 kΩ, C_L = 100 pF		6.5		MHz
		f = 100 kHz, R_L = 600 Ω, C_L = 100 pF		5.7		
	Settling time	ε = 0.1%		5		μs
		ε = 0.01%		10		
B_{OM}	Maximum output-swing bandwidth	A_{VD} = 5, R_L = 10 kΩ		85		kHz
ϕ_m	Phase margin (see Figure 3)	A_{VD} = 5, R_L = 10 kΩ, C_L = 100 pF		72°		
		A_{VD} = 5, R_L = 600 Ω, C_L = 100 pF		78°		

PARAMETER MEASUREMENT INFORMATION



NOTE A: C_L includes fixture capacitance.

Figure 1. Slew Rate Test Circuit

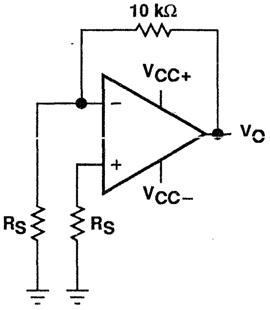
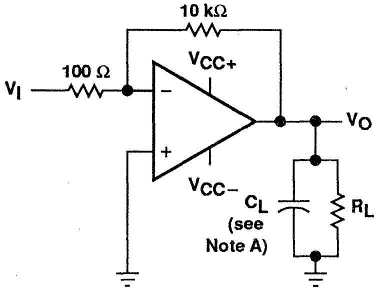


Figure 2. Noise Voltage Test Circuit



NOTE A: C_L includes fixture capacitance.

Figure 3. Gain-Bandwidth Product and Phase Margin Test Circuit

typical values

Typical values as presented in this data sheet represent the median (50% point) of device parametric performance.

input bias and offset current

At the picoampere bias-current level typical of the TLE2161, TLE2161A, and TLE2161B, accurate measurement of the bias current becomes difficult. Not only does this measurement require a picoammeter, but test socket leakages can easily exceed the actual device bias currents. To accurately measure these small currents, Texas Instruments uses a two-step process. The socket leakage is measured using picoammeters with bias voltages applied but with no device in the socket. The device is then inserted into the socket and a second test that measures both the socket leakage and the device input bias current is performed. The two measurements are then subtracted algebraically to determine the bias current of the device.

TYPICAL CHARACTERISTICS

table of graphs

			FIGURE
V_{IO}	Input offset voltage	Distribution	4
I_{IB}	Input bias current	vs Common-mode voltage	5
		vs Temperature	6
I_{IO}	Input offset current	vs Temperature	6
V_{ICR}	Common-mode input voltage range limits	vs Temperature	7
V_{OM}	Maximum peak output voltage swing	vs Output current	8, 9
		vs Supply voltage	10, 11, 12
$V_{O(PP)}$	Maximum peak-to-peak output voltage	vs Frequency	13, 14, 15
A_{VD}	Differential voltage amplification	vs Frequency	16
		vs Temperature	17
I_{OS}	Short-circuit output current	vs Time	18
		vs Temperature	19
z_o	Output impedance	vs Frequency	20
CMRR	Common-mode rejection ratio	vs Frequency	21
I_{CC}	Supply current	vs Supply voltage	22
		vs Temperature	23
	Pulse response	Small-signal	24, 25
		Large-signal	26, 27
	Noise voltage (referred to input)	0.1 to 10 Hz	28
V_n	Equivalent input noise voltage	vs Frequency	29
THD	Total harmonic distortion	vs Frequency	30, 31
	Gain-bandwidth product	vs Supply voltage	32
		vs Temperature	33
ϕ_m	Phase margin	vs Supply voltage	34
		vs Temperature	35
ϕ	Phase shift	vs Frequency	16

TYPICAL CHARACTERISTICS†

TLE2161 DISTRIBUTION OF INPUT OFFSET VOLTAGE

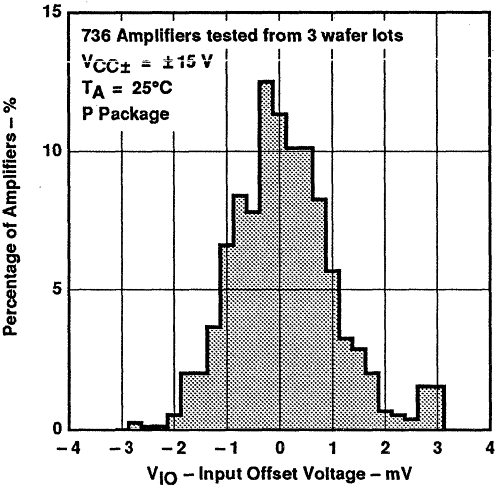


Figure 4

INPUT BIAS CURRENT vs COMMON-MODE INPUT VOLTAGE

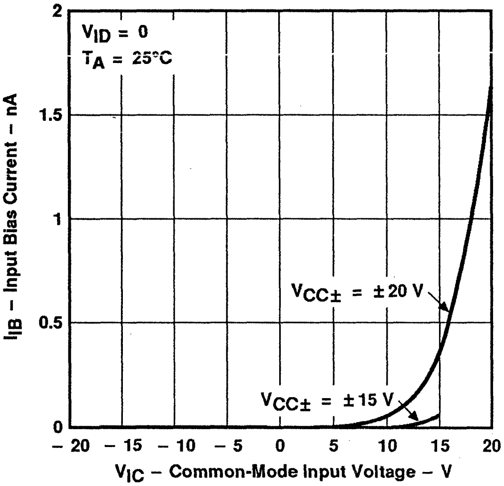


Figure 5

INPUT BIAS CURRENT and INPUT OFFSET CURRENT vs FREE-AIR TEMPERATURE

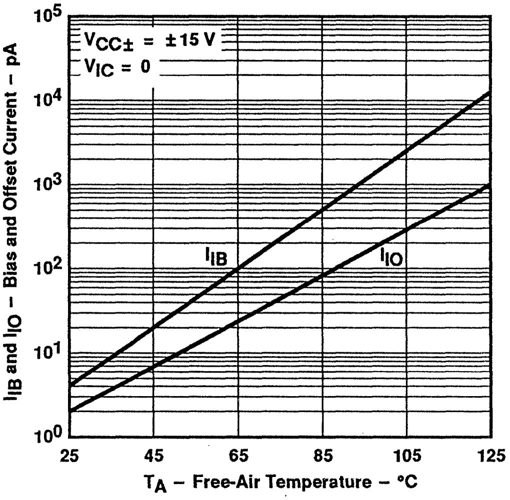


Figure 6

COMMON-MODE INPUT VOLTAGE RANGE LIMITS vs FREE-AIR TEMPERATURE

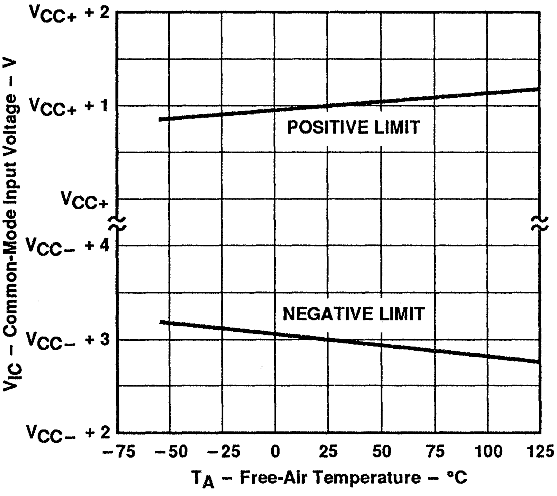


Figure 7

---

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS

MAXIMUM POSITIVE PEAK OUTPUT VOLTAGE vs OUTPUT CURRENT

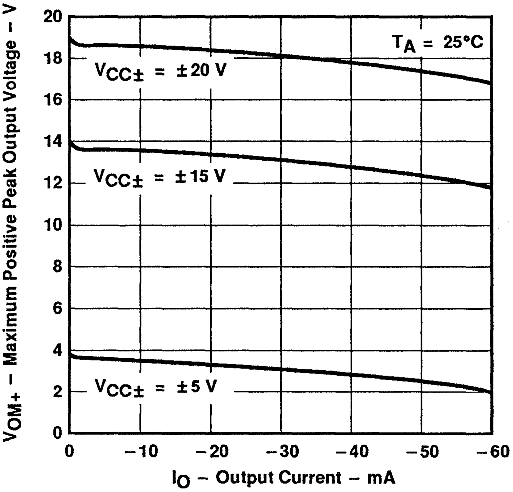


Figure 8

MAXIMUM NEGATIVE PEAK OUTPUT VOLTAGE vs OUTPUT CURRENT

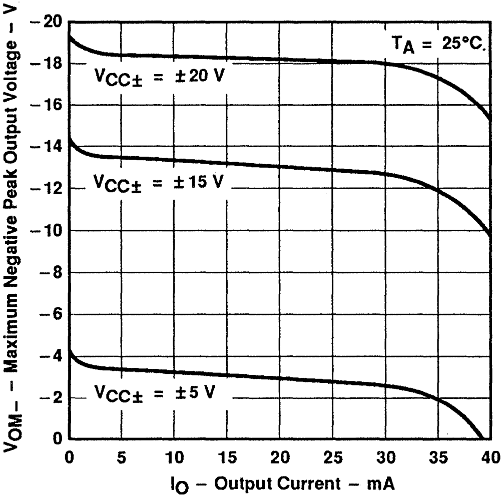


Figure 9

MAXIMUM PEAK OUTPUT VOLTAGE vs SUPPLY VOLTAGE

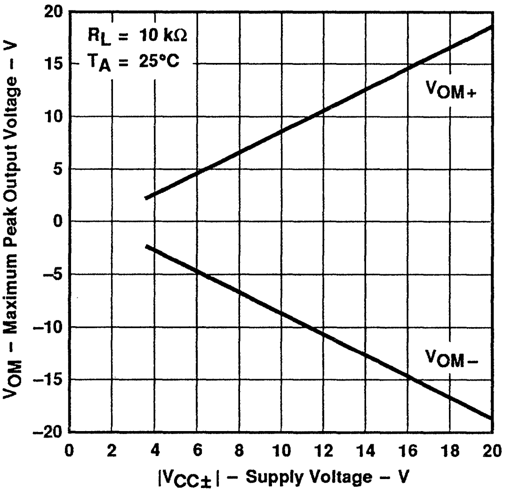


Figure 10

MAXIMUM PEAK OUTPUT VOLTAGE vs SUPPLY VOLTAGE

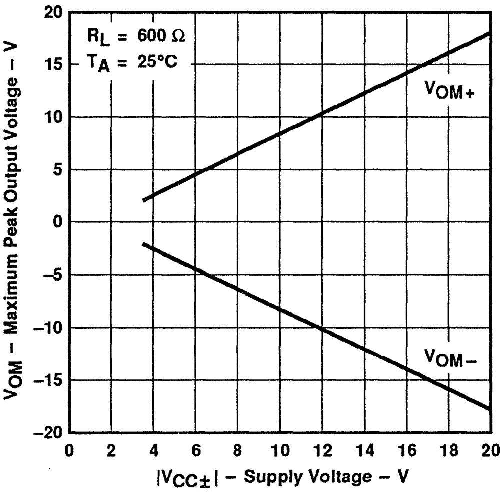


Figure 11

TYPICAL CHARACTERISTICS

MAXIMUM PEAK OUTPUT VOLTAGE
vs
SUPPLY VOLTAGE

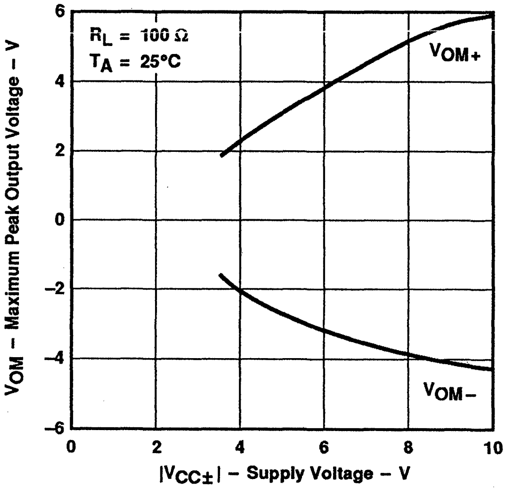


Figure 12

MAXIMUM PEAK-TO-PEAK
OUTPUT VOLTAGE
vs
FREQUENCY

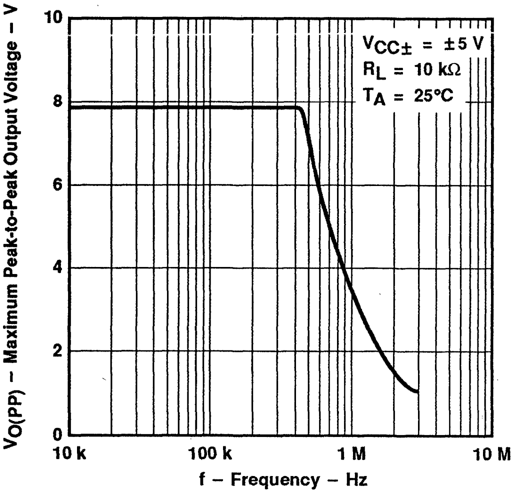


Figure 13

MAXIMUM PEAK-TO-PEAK
OUTPUT VOLTAGE
vs
FREQUENCY

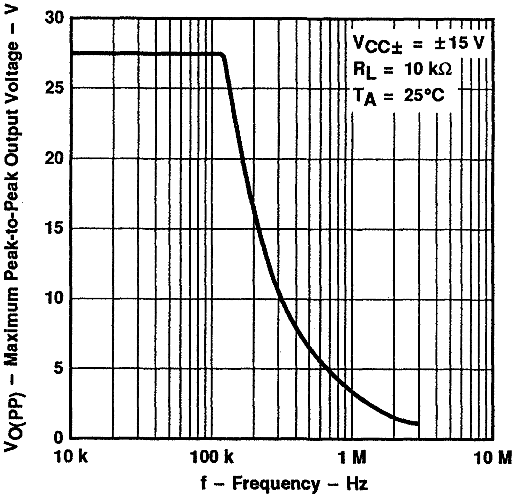


Figure 14

MAXIMUM PEAK-TO-PEAK
OUTPUT VOLTAGE
vs
FREQUENCY

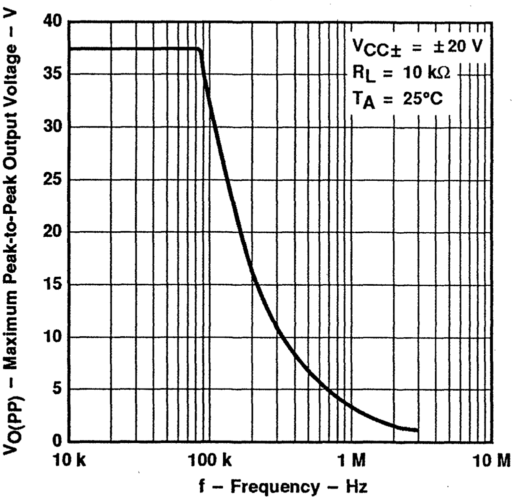


Figure 15

TYPICAL CHARACTERISTICS[†]

LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION and PHASE SHIFT
vs
FREQUENCY

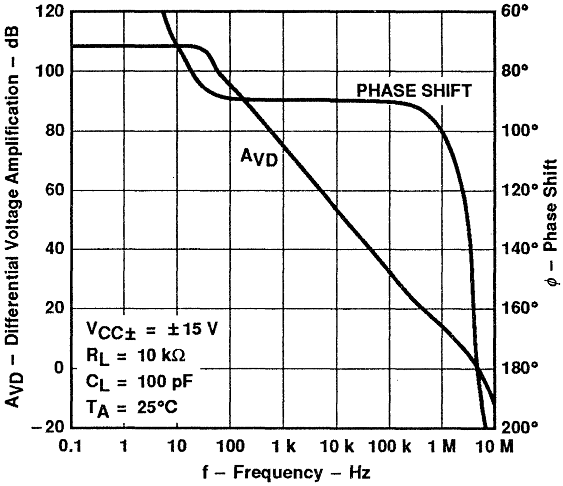


Figure 16

LARGE-SIGNAL VOLTAGE AMPLIFICATION
vs
FREQUENCY FREE-AIR TEMPERATURE

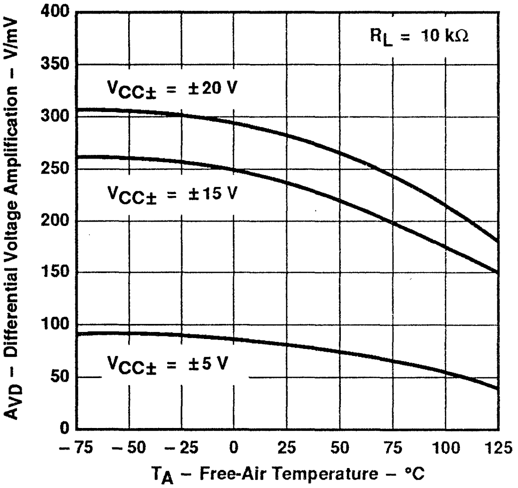


Figure 17

SHORT-CIRCUIT OUTPUT CURRENT
vs
ELAPSED TIME

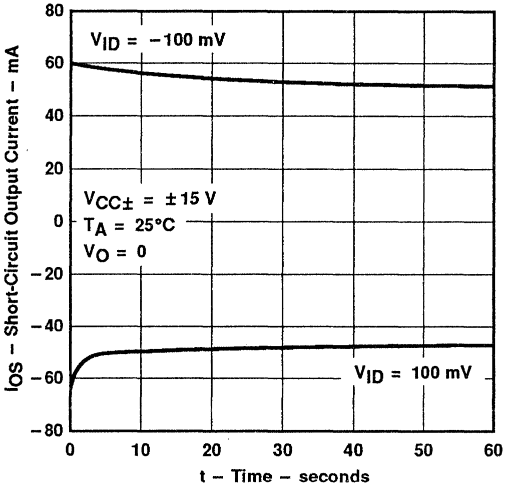


Figure 18

SHORT-CIRCUIT OUTPUT CURRENT
vs
FREE-AIR TEMPERATURE

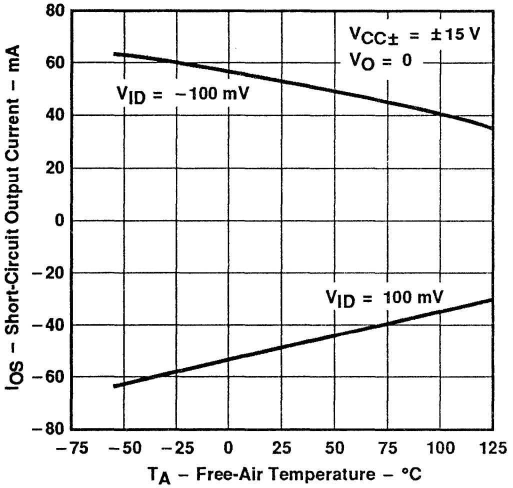


Figure 19

[†] Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

OUTPUT IMPEDANCE
vs
FREQUENCY

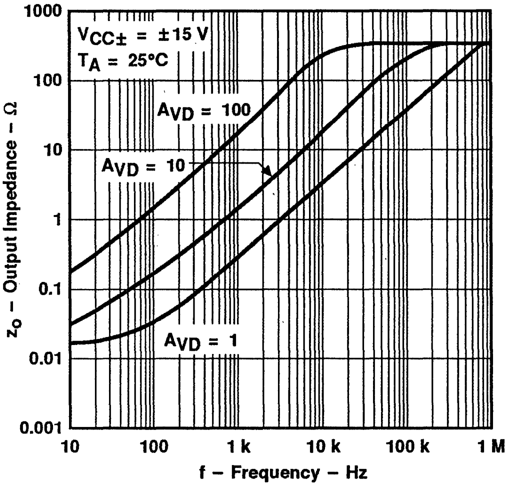


Figure 20

COMMON-MODE REJECTION RATIO
vs
FREQUENCY

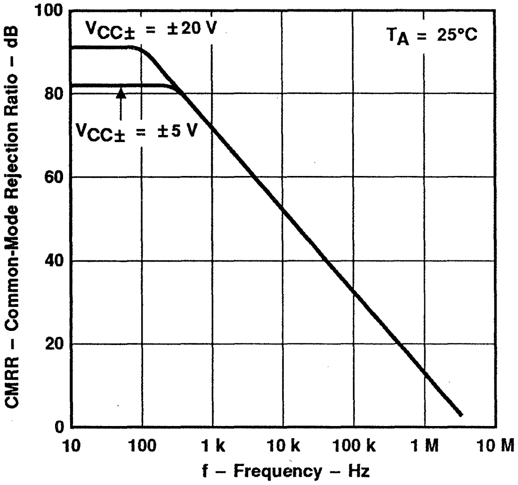


Figure 21

SUPPLY CURRENT
vs
SUPPLY VOLTAGE

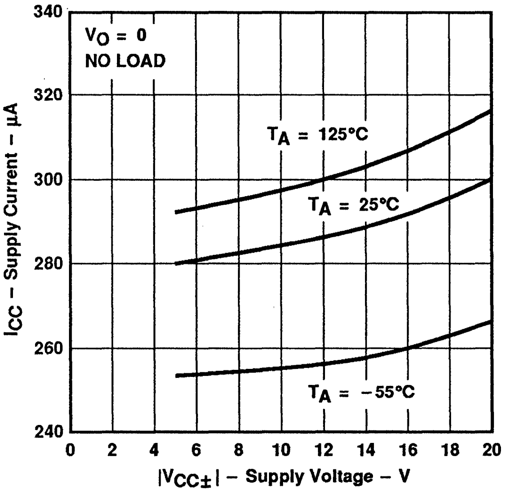


Figure 22

SUPPLY CURRENT
vs
FREE-AIR TEMPERATURE

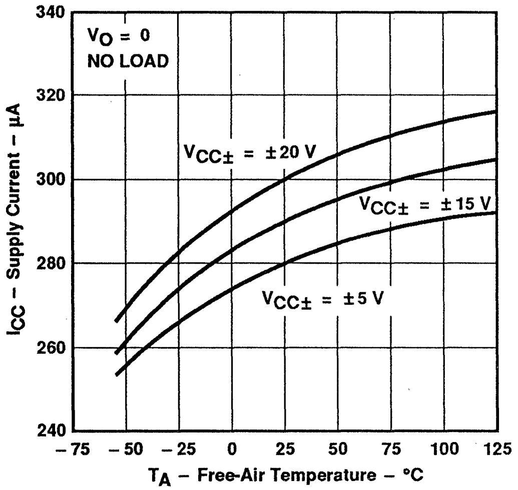


Figure 23

---

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS

SMALL-SIGNAL
PULSE RESPONSE

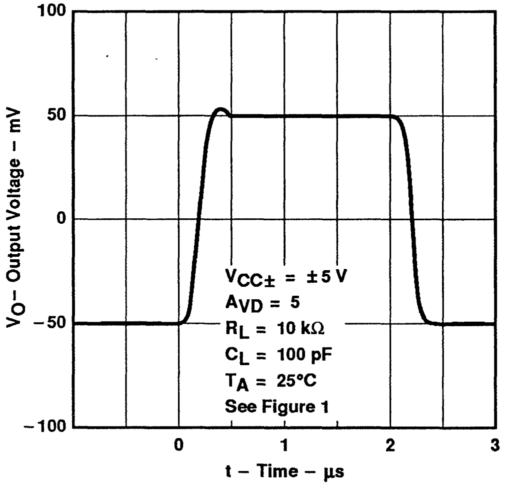


Figure 24

SMALL-SIGNAL
PULSE RESPONSE

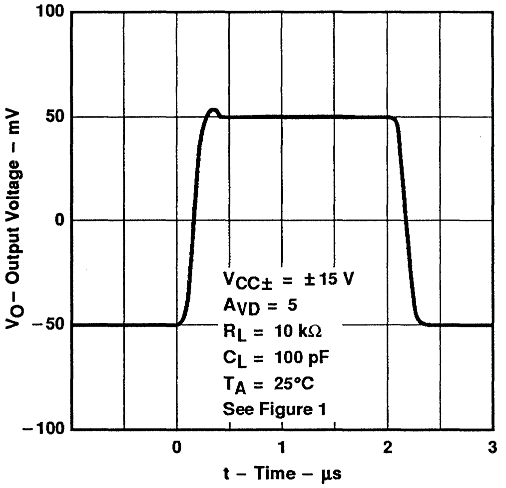


Figure 25

LARGE-SIGNAL
PULSE RESPONSE

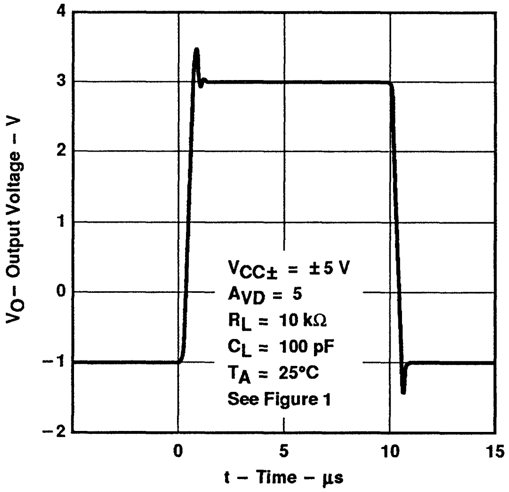


Figure 26

LARGE-SIGNAL
PULSE RESPONSE

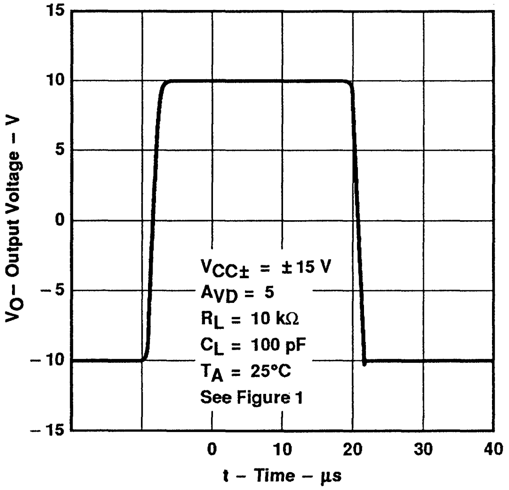


Figure 27

TYPICAL CHARACTERISTICS

NOISE VOLTAGE (REFERRED TO INPUT) OVER A 10-SECOND INTERVAL

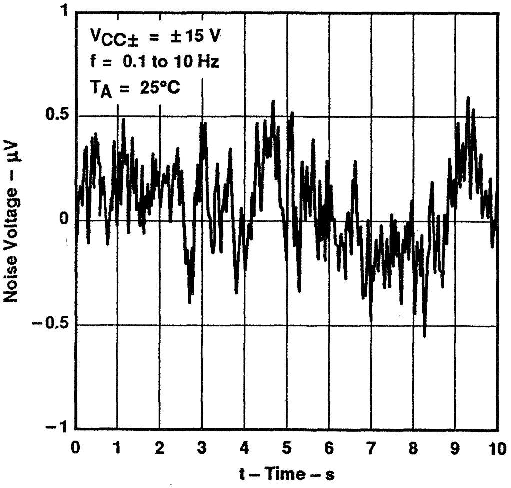


Figure 28

EQUIVALENT INPUT NOISE VOLTAGE vs FREQUENCY

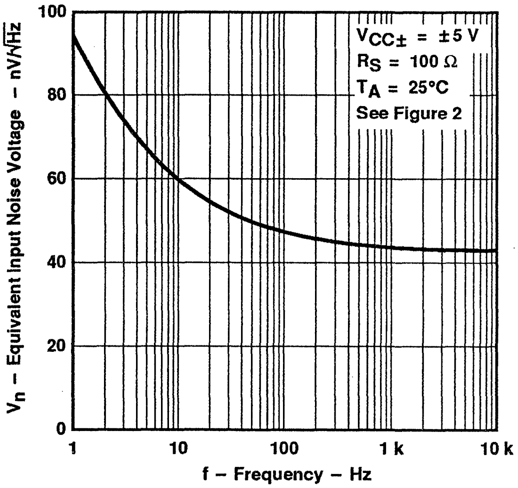


Figure 29

TOTAL HARMONIC DISTORTION vs FREQUENCY

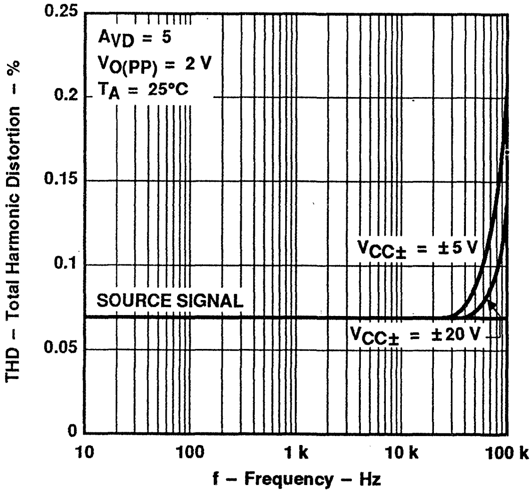


Figure 30

TOTAL HARMONIC DISTORTION vs FREQUENCY

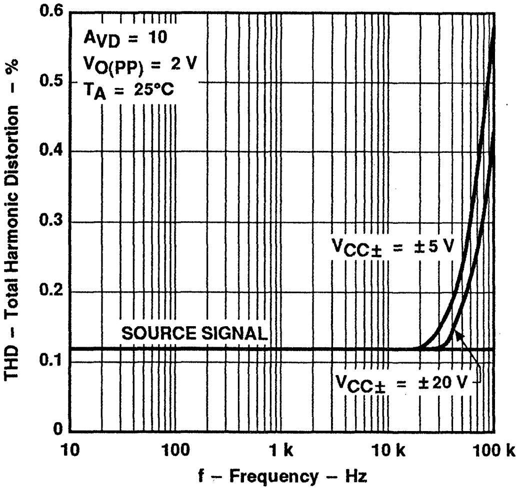


Figure 31

TYPICAL CHARACTERISTICS†

GAIN-BANDWIDTH PRODUCT
vs
SUPPLY VOLTAGE

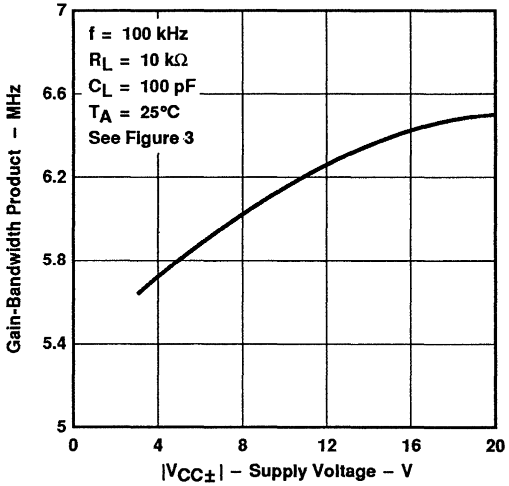


Figure 32

GAIN-BANDWIDTH PRODUCT
vs
FREE-AIR TEMPERATURE

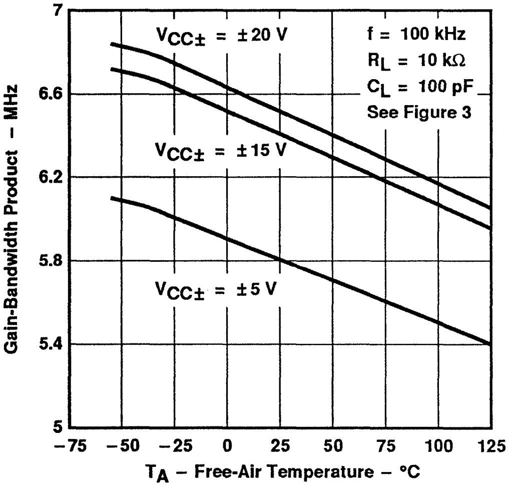


Figure 33

PHASE MARGIN
vs
SUPPLY VOLTAGE

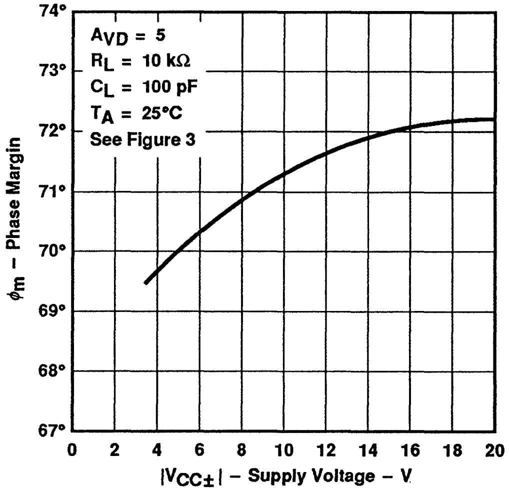


Figure 34

PHASE MARGIN
vs
FREE-AIR TEMPERATURE

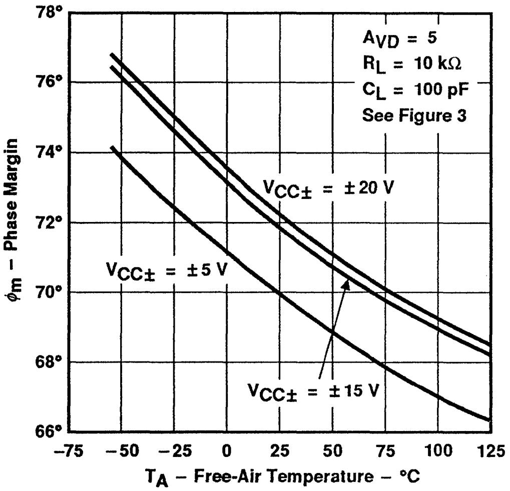


Figure 35

---

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

APPLICATION INFORMATION

macromodel information

Macromodel information provided was derived using *PSpice® Parts*™ model generation software. The Boyle macromodel (see Note 5) and subcircuit in Figures 36 and 37 were generated using the TLE2161 typical electrical and operating characteristics at 25°C. Using this information, output simulations of the following key parameters can be generated to a tolerance of 20% (in most cases):

- Maximum positive output voltage swing
- Maximum negative output voltage swing
- Slew rate
- Quiescent power dissipation
- Input bias current
- Open-loop voltage amplification
- Gain-bandwidth product
- Common-mode rejection ratio
- Phase margin
- DC output resistance
- AC output resistance
- Short-circuit output current limit

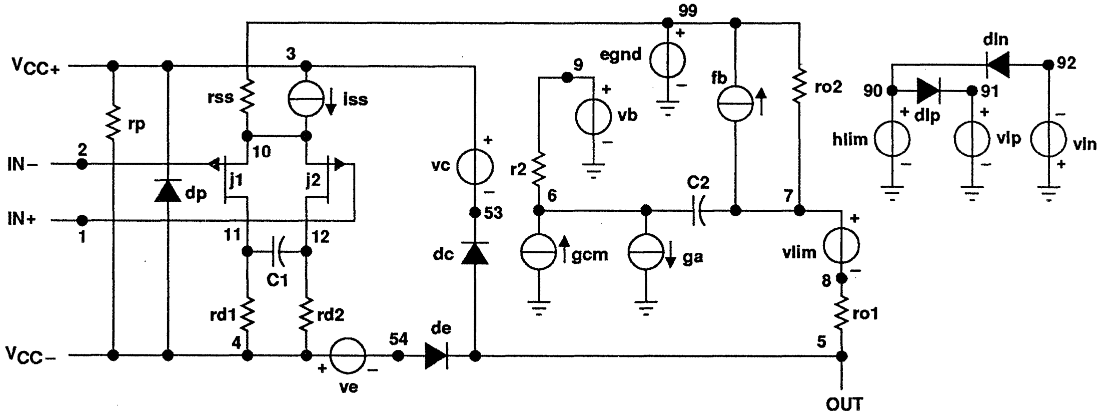


Figure 36. Boyle Macromodel

NOTE 5: G. R. Boyle, B. M. Cohn, D. O. Pederson, and J. E. Solomon, "Macromodeling of Integrated Circuit Operational Amplifiers", IEEE Journal of Solid-State Circuits, SC-9, 353 (1974).

PSpice is a registered trademark of MicroSim Corporation.
Parts is a trademark of MicroSim Corporation.

APPLICATION INFORMATION

macromodel information (continued)

```
.subckt TLE2161  1 2 3 4 5
  c1   11 12 125.4E-14
  c2    6  7 5.000E-12
  dc    5 53 dx
  de   54  5 dx
  dlp  90 91 dx
  dln  92 90 dx
  dp    4  3 dx
  egnd 99  0 poly(2) (3,0) (4,0) 0 .5 .5
  fb    7 99 poly(5) vb vc ve vlp vln 0 4.085E6 -4E6 4E6 4E6 -4E6
  ga    6  0 11 12 201.1E-6
  gcm   0  6 10 99 3.576E-9
  iss   3 10 dc 45.00E-6
  hlim 90  0 vlim 1K
  j1   11  2 10 jx
  j2   12  1 10 jx
  r2    6  9 100.0E3
  rd1   4 11 4.973E3
  rd2   4 12 4.973E3
  ro1   8  5 280
  ro2   7 99 280
  rp    3  4 113.2E3
  rss  10 99 4.444E6
  vb    9  0 dc 0
  vc    3 53 dc 2
  ve   54  4 dc 2
  vlim  7  8 dc 0
  vlp  91  0 dc 50
  vln   0 92 dc 50
.model dx D(Is=800.0E-18)
.model jx PJF(Is=1.000E-12 Beta=480E-6 Vto=-1)
.ends
```

Figure 37. Marcomodel Subcircuit

APPLICATION INFORMATION

input characteristics

The TLE2161, TLE2161A and TLE2161B are specified with a minimum and a maximum input voltage that, if exceeded at either input, could cause the device to malfunction.

Because of the extremely high input impedance and resulting low bias-current requirements, the TLE2161, TLE2161A, and TLE2161B are well-suited for low-level signal processing; however, leakage currents on printed circuit boards and sockets can easily exceed bias-current requirements and cause degradation in system performance. It is a good practice to include guard rings around inputs (see Figure 38). These guards should be driven from a low-impedance source at the same voltage level as the common-mode input.

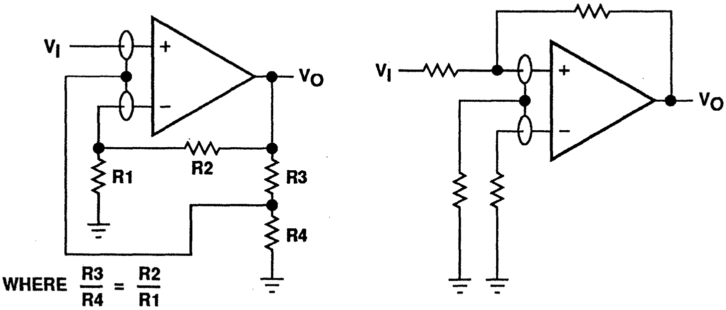


Figure 38. Use of Guard Rings

input offset voltage nulling

The TLE2161 series offers external null pins that can be used to further reduce the input offset voltage. The circuit of Figure 39 can be connected as shown if the feature is desired. If external nulling is not needed, the null pins may be left disconnected.

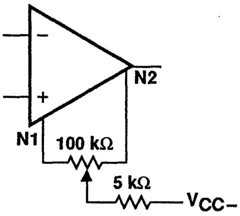


Figure 39. Input Offset Voltage Nulling

TLE2227, TLE2227A
EXCALIBUR LOW-NOISE HIGH-SPEED PRECISION DUAL OPERATIONAL AMPLIFIERS

D3959, SEPTEMBER 1991 – REVISED DECEMBER 1991

available features

- **Outstanding Combination of DC Precision and AC Performance:**
  Unity-Gain Bandwidth . . . 15 MHz Typ
  V_n. . . . 3.3 nV/$\sqrt{\text{Hz}}$ at f = 10 Hz Typ,
  2.5 nV/$\sqrt{\text{Hz}}$ at f = 1 kHz Typ
  V_{IO} . . . 25 µV Typ
  A_{VD}. . . 45 V/µV Typ With R_L = 2 kΩ,
  38 V/µV Typ With R_L = 1 kΩ
- **Available in 16-Pin Small-Outline Wide-Body Package**
- **Output Features Saturation Recovery Circuitry**
- **Macromodels and Statistical Information Included**

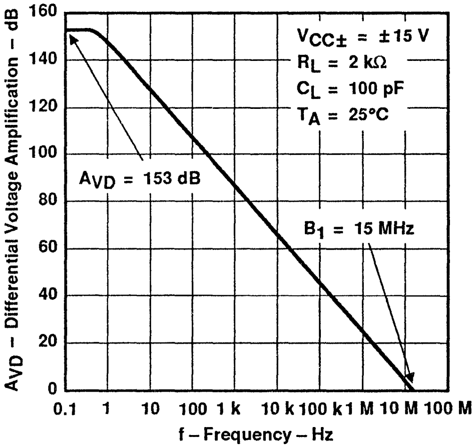
description

The TLE2227 and TLE2227A combine innovative circuit design expertise and high-quality process control techniques to produce a level of ac performance and dc precision previously unavailable in dual operational amplifiers. These devices allow upgrades to systems that use lower-precision devices and are manufactured using Texas Instruments state-of-the-art Excalibur process.

In the area of dc precision, the TLE2227 and TLE2227A offer a typical offset voltage of 25 µV, a common-mode rejection ratio of 131 dB (typ), a supply voltage rejection ratio of 144 dB (typ), and a dc gain of 45 V/µV (typ).

Ac performance is highlighted by a typical unity-gain bandwidth specification of 15 MHz, 55° of phase margin, and noise voltage specifications of 3.3 nV/$\sqrt{\text{Hz}}$ and 2.5 nV/$\sqrt{\text{Hz}}$ at frequencies of 10 Hz and 1 kHz, respectively.

LARGE-SIGNAL
DIFFERENTIAL VOLTAGE AMPLIFICATION
vs
FREQUENCY



The TLE2227 and TLE2227A are available in a wide variety of packages, including the industry standard 16-pin small-outline wide-body version for high-density system applications. The TLE2227 amd TLE2227A are characterized for operation from 0°C to 70°C.

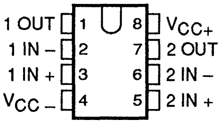
AVAILABLE OPTIONS

T_A	V_{IO} typ AT 25°C	PACKAGE	
		SMALL-OUTLINE (DW)	PLASTIC DIP (P)
0 °C to 70°C	25 µV	TLE2227CDW	TLE2227CP TLE2227ACP

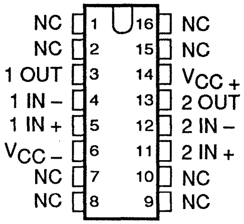
D packages are available taped and reeled. Add "R" suffix to device type (e.g., TLE2227CDWR).

TEXAS INSTRUMENTS

P PACKAGE
(TOP VIEW)

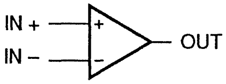


DW PACKAGE
(TOP VIEW)

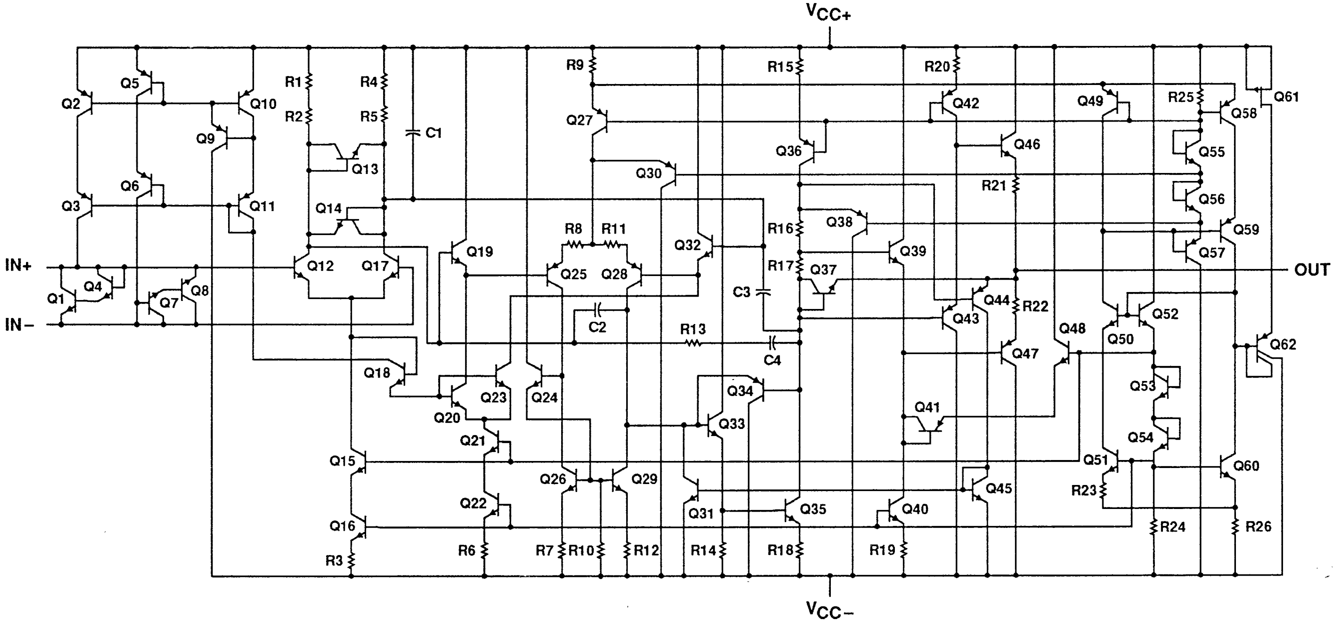


NC – No internal connection

symbol (each amplifier)



equivalent schematic for 1 channel



Component Count: Transistors — 62   Capacitors — 4
Resistors — 24   Diodes — 0

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC+} (see Note 1)	22 V
Supply voltage, V_{CC-}	−22 V
Differential input voltage (see Note 2)	±1.2 V
Input voltage range, V_I (any input)	$V_{CC\pm}$
Input current, I_I (each input)	±1 mA
Output current, I_O	±50 mA
Total current into V_{CC+} terminal	50 mA
Total current out of V_{CC-} terminal	50 mA
Duration of short-circuit current at (or below) 25°C (see Note 3)	unlimited
Continuous total dissipation	See Dissipation Rating Table
Operating free-air temperature range, T_A	0°C to 70°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: DW or P package	260°C

NOTES: 1. All voltage values, except differential voltages, are with respect to the midpoint between V_{CC+} and V_{CC-}.
2. Differential voltages are at the noninverting input with respect to the inverting input. Excessive current will flow if a differential input voltage in excess of approximately ±1.2 V is applied between the inputs unless some limiting resistance is used.
3. The output may be shorted to either supply. Temperature and/or supply voltages must be limited to ensure that the maximum dissipation rating is not exceeded.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING
DW	1025 mW	8.2 mW/°C	656 mW
P	1000 mW	8.0 mW/°C	640 mW

recommended operating conditions

		MIN	MAX	UNIT
Supply voltage, $V_{CC\pm}$		±4	±22	V
Common-mode input voltage, V_{IC}	T_A = 25°C	−11	11	V
	T_A = Full range	−10.5	10.5	
Operating free-air temperature, T_A		0	70	°C

electrical characteristics at specified free-air temperature, $V_{CC\pm} = \pm 15$ V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A†	TLE2227C			TLE2227AC			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	$V_{IC} = 0$, $R_S = 50\ \Omega$	25°C		25			25		µV
α_{VIO}	Temperature coefficient of input offset voltage		Full range		0.4	1		0.2	1	µV/°C
	Input offset voltage long-term drift (see Note 4)		25°C		0.006	1		0.006	1	µV/mo
I_{IO}	Input offset current		25°C		6	90		6	90	nA
			Full range			150			150	
I_{IB}	Input bias current		25°C		15	90		15	90	nA
			Full range			150			150	
V_{ICR}	Common-mode input voltage range	$R_S = 50\ \Omega$	25°C	−11 to 11	−13 to 13		−11 to 11	−13 to 13		V
			Full range	−10.5 to 10.5			−10.5 to 10.5			
V_{OM+}	Maximum positive peak output voltage swing	$R_L = 1\ k\Omega$	25°C	10.5			10.5			V
			Full range	10			10			
		$R_L = 2\ k\Omega$	25°C	12			12			
			Full range	11			11			
V_{OM-}	Maximum negative peak output voltage swing	$R_L = 1\ k\Omega$	25°C	−10.5	−13		−10.5	−13		V
			Full range	−10			−10			
		$R_L = 2\ k\Omega$	25°C	−12	−13.5		−12	−13.5		
			Full range	−11			−11			
A_{VD}	Large-signal differential voltage amplification	$V_O = \pm 11$ V, $R_L = 2\ k\Omega$	25°C	5	45		5	45		V/µV
		$V_O = \pm 10$ V, $R_L = 2\ k\Omega$	Full range	2			2			
		$V_O = \pm 10$ V, $R_L = 1\ k\Omega$	25°C	3.5	38		3.5	38		
			Full range	1			1			
c_i	Input capacitance		25°C		8			8		pF
z_o	Open-loop output impedance	$I_O = 0$	25°C		50			50		Ω
CMRR	Common-mode rejection ratio	$V_{IC} = V_{ICR}$ min, $R_S = 50\ \Omega$	25°C	100	131		100	131		dB
			Full range	98			98			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm} / \Delta V_{IO}$)	$V_{CC\pm} = \pm 4$ V to ± 18 V, $R_S = 50\ \Omega$	25°C	94	144		94	144		dB
		$V_{CC\pm} = \pm 4$ V to ± 18 V, $R_S = 50\ \Omega$	Full range	92			92			
I_{CC}	Supply current	$V_O = 0$, No load	25°C		7.6	10.6		7.6	10.6	mA
			Full range			11.2			11.2	

†Full range is 0°C to 70°C.

NOTE 4: Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at $T_A = 150$°C extrapolated to $T_A = 25$°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

operating characteristics at specified free-air temperature, $V_{CC\pm}$ = ±15 V

PARAMETER		TEST CONDITIONS	T_A†	TLE2227C			TLE2227AC			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
SR	Slew rate	R_L = 2 kΩ, C_L = 100 pF	25°C	1.7	2.8		1.7	2.8		V/µs
			Full range	1.2			1.2			
V_n	Equivalent input noise voltage	R_S = 100 Ω, f = 10 Hz	25°C		3.3	8		3.3	8	nV/√Hz
		R_S = 100 Ω, f = 1 kHz			2.5	4.5		2.5	4.5	
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 10 Hz	25°C		50	250		50	250	nV
I_n	Equivalent input noise current	f = 10 Hz	25°C		1.5	4		1.5	4	pA/√Hz
		f = 1 kHz			0.4	0.6		0.4	0.6	
THD	Total harmonic distortion	VO = ± 10 V, AVD = 1, See Note 5	25°C		< 0.002%			< 0.002%		
B_1	Unity-gain bandwidth	R_L = 2 kΩ, C_L = 100 pF	25°C	7	13		7	13		MHz
B_{OM}	Maximum output-swing bandwidth	R_L = 2 kΩ	25°C		30			30		kHz
ϕ_m	Phase margin	R_L = 2 kΩ, C_L = 100 pF	25°C		55°			55°		

†Full range is 0°C to 70°C.

NOTE 5: Measured distortion of the source used in the analysis was 0.002%.

TLE2237, TLE2237A
EXCALIBUR LOW-NOISE HIGH-SPEED PRECISION NONCOMPENSATED DUAL OPERATIONAL AMPLIFIERS

D3957, SEPTEMBER 1991 – REVISED DECEMBER 1991

available features

- Outstanding Combination of DC Precision and AC Performance:
  Gain-Bandwidth Product . . . 80 MHz Typ
  V_n . . . 3.3 nV/$\sqrt{Hz}$ at f = 10 Hz Typ,
  2.5 nV/$\sqrt{Hz}$ at f = 1 kHz Typ
  V_{IO} . . . 25 μV Max
  A_{VD} . . . 45 V/μV Typ With R_L = 2 kΩ,
  38 V/μV Typ With R_L = 1 kΩ
- Available in 16-Pin Small-Outline Wide-Body Package
- Output Features Saturation Recovery Circuitry
- Macromodels and Statistical Information Included

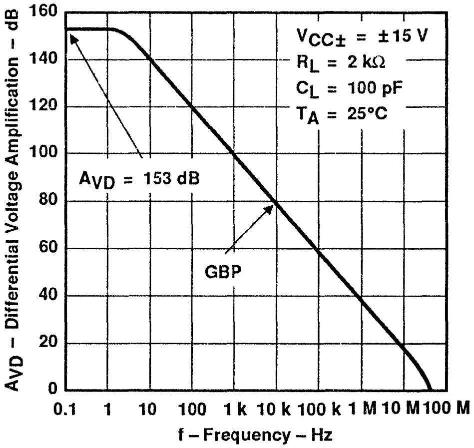
description

The TLE2237 and TLE2237A combine innovative circuit design expertise and high-quality process control techniques to produce a level of ac performance and dc precision previously unavailable in dual operational amplifiers. Using the Texas Instruments state-of-the-art Excalibur process, these devices allow upgrades to systems that use lower-precision devices.

The TLE2237 and TLE2237A are noncompensated versions of the TLE2027 and TLE2027A. The devices are stable to a closed-loop gain of 5. In the area of dc precision, both devices offer an input offset voltage of 25 μV (typ), a common-mode rejection ratio of 131 dB (typ), a supply voltage rejection ratio of 144 dB (typ), and a dc gain of 45 V/μV (typ).

The ac performance is highlighted by a typical gain-bandwidth product specification of 80 MHz, 50° of phase margin, and noise voltage specifications of 3.3 nV/$\sqrt{Hz}$ and 2.5 nV/$\sqrt{Hz}$ at frequencies of 10 Hz and 1 kHz, respectively.

LARGE-SIGNAL
DIFFERENTIAL VOLTAGE AMPLIFICATION
vs
FREQUENCY



The TLE2237 and TLE2237A are available in a wide variety of packages, including the industry standard 16-pin small-outline wide-body version for high-density system applications. The TLE2237 and TLE2237A are characterized for operation from 0°C to 70°C.

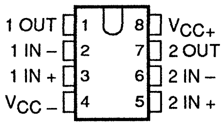
AVAILABLE OPTIONS

T_A	V_{IO} typ AT 25°C	PACKAGE	
		SMALL-OUTLINE (DW)	PLASTIC DIP (P)
0 °C to 70°C	25 μV	TLE2237CDW	TLE2237CP TLE2237ACP

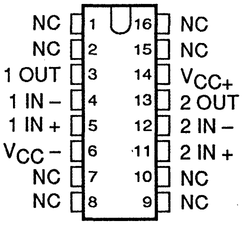
D packages are available taped and reeled. Add "R" suffix to device type (e.g., TLE2237CDWR).

TEXAS INSTRUMENTS
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

P PACKAGE
(TOP VIEW)

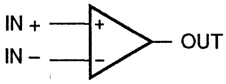


DW PACKAGE
(TOP VIEW)

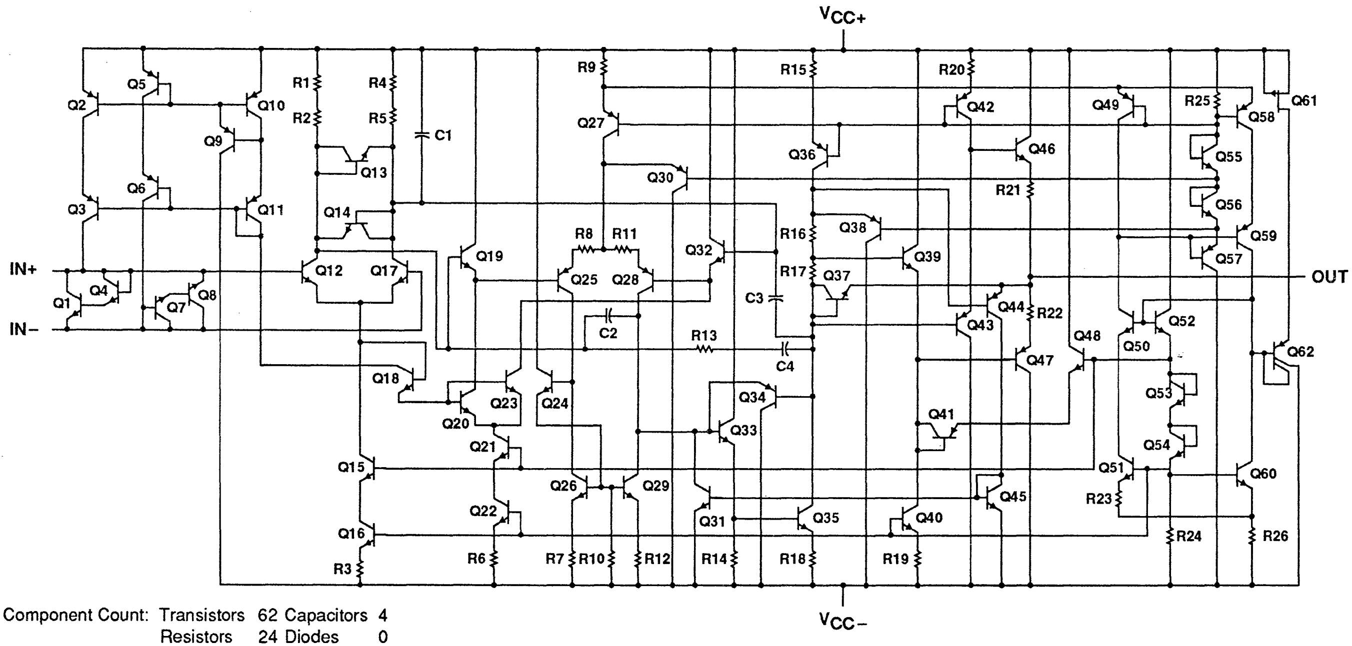


NC – No internal connection

symbol (each amplifier)



equivalent schematic (for 1 channel)



Component Count: Transistors 62 Capacitors 4
Resistors 24 Diodes 0

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC+} (see Note 1)	22 V
Supply voltage, V_{CC-}	−22 V
Differential input voltage (see Note 2)	±1.2 V
Input voltage range, V_I (any input)	$V_{CC\pm}$
Input current, I_I (each input)	±1 mA
Output current, I_O	±50 mA
Total current into V_{CC+} terminal	50 mA
Total current out of V_{CC-} terminal	50 mA
Duration of short-circuit current at (or below) 25°C (see Note 3)	unlimited
Continuous total dissipation	See Dissipation Rating Table
Operating free-air temperature range, T_A	0°C to 70°C
Storage temperature range	−65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: DW or P package	260°C

NOTES: 1. All voltage values, except differential voltages, are with respect to the midpoint between V_{CC+} and V_{CC-}.

2. Differential voltages are at the noninverting input with respect to the inverting input. Excessive current will flow if a differential input voltage in excess of approximately ±1.2 V is applied between the inputs unless some limiting resistance is used.

3. The output may be shorted to either supply. Temperature and/or supply voltages must be limited to ensure that the maximum dissipation rating is not exceeded.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING
DW	1025 mW	8.2 mW/°C	656 mW
P	1000 mW	8.0 mW/°C	640 mW

recommended operating conditions

		MIN	MAX	UNIT
Supply voltage, $V_{CC\pm}$		±4	±22	V
Common-mode input voltage, V_{IC}	T_A = 25°C	−11	11	V
	T_A = Full range	−10.5	10.5	
Operating free-air temperature, T_A		0	70	°C

electrical characteristics at specified free-air temperature, $V_{CC\pm}$ = ± 15 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A†	TLE2237C			TLE2237AC			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_{IC} = 0, R_S = 50 Ω	25°C		25			25		µV
α_{VIO}	Temperature coefficient of input offset voltage		Full range		0.4	1		0.2	1	µV/°C
	Input offset voltage long-term drift (see Note 4)		25°C		0.006	1		0.006	1	µV/mo
I_{IO}	Input offset current		25°C		6	90		6	90	nA
			Full range			150			150	
I_{IB}	Input bias current		25°C		15	90		15	90	nA
			Full range			150			150	
V_{ICR}	Common-mode input voltage range	R_S = 50 Ω	25°C	– 11 to 11	– 13 to 13		– 11 to 11	– 13 to 13		V
			Full range	– 10.5 to 10.5			– 10.5 to 10.5			
V_{OM+}	Maximum positive peak output voltage swing	R_L = 1 kΩ	25°C	10.5			10.5			V
			Full range	10			10			
		R_L = 2 kΩ	25°C	12			12			
			Full range	11			11			
V_{OM-}	Maximum negative peak output voltage swing	R_L = 1 kΩ	25°C	– 10.5	– 13		– 10.5	– 13		V
			Full range	– 10			– 10			
		R_L = 2 kΩ	25°C	– 12	– 13.5		– 12	– 13.5		
			Full range	– 11			– 11			
A_{VD}	Large-signal differential voltage amplification	V_O = ± 11 V, R_L = 2 kΩ	25°C	5	45		5	45		V/µV
		V_O = ± 10 V, R_L = 2 kΩ	Full range	2			2			
		V_O = ± 10 V, R_L = 1 kΩ	25°C	3.5	38		3.5	38		
			Full range	1			1			
c_i	Input capacitance		25°C		8			8		pF
z_o	Open-loop output impedance	I_O = 0	25°C		50			50		Ω
CMRR	Common-mode rejection ratio	V_{IC} = V_{ICR} min, R_S = 50 Ω	25°C	100	131		100	131		dB
			Full range	98			98			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm} / \Delta V_{IO}$)	$V_{CC\pm}$ = ± 4 V to ± 18 V, R_S = 50 Ω	25°C	94	144		94	144		dB
		$V_{CC\pm}$ = ± 4 V to ± 18 V, R_S = 50 Ω	Full range	92			92			
I_{CC}	Supply current	V_O = 0, No load	25*C		7.6	10.6		7.6	10.6	mA
			Full range			11.2			11.2	

†Full range is 0°C to 70°C.

NOTE 4: Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at T_A = 150°C extrapolated to T_A = 25°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

operating characteristics at specified free-air temperature, $V_{CC\pm} = \pm 15$ V

PARAMETER		TEST CONDITIONS	T_A†	TLE2237C			TLE2237AC			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
SR	Slew rate	$A_{VD} = 5$, $R_L = 2\ k\Omega$, $C_L = 100$ pF	25°C	6	7.5		6	7.5		V/μs
			Full range	5			5			
V_n	Equivalent input noise voltage	$R_S = 100\ \Omega$, f = 10 Hz	25°C		3.3	8		3.3	8	nV/√Hz
		$R_S = 100\ \Omega$, f = 1 kHz			2.5	4.5		2.5	4.5	
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 10 Hz	25°C		50	250		50	250	nV
I_n	Equivalent input noise current	f = 10 Hz	25°C		1.5	4		1.5	4	pA/√Hz
		f = 1 kHz			0.4	0.6		0.4	0.6	
THD	Total harmonic distortion	$V_O = \pm 10$ V, $A_{VD} = 5$, See Note 5	25°C		< 0.002%			< 0.002%		
GBP	Gain-bandwidth product	f = 100 kHz, $R_L = 2\ k\Omega$, $C_L = 100$ pF	25°C	50	76		50	76		MHz
B_{OM}	Maximum output-swing bandwidth	$R_L = 2\ k\Omega$	25°C		80			80		kHz
ϕ_m	Phase margin	$R_L = 2\ k\Omega$, $C_L = 100$ pF	25°C		50°			50°		

†Full range is 0°C to 70°C.

NOTE 5: Measured distortion of the source used in the analysis was 0.002%.

uA709AM, uA709M, uA709C
GENERAL-PURPOSE OPERATIONAL AMPLIFIERS

D942, FEBRUARY 1971 – REVISED MAY 1988

- **Common-Mode Input Range . . . ±10 V Typical**
- **Designed to be Interchangeable with Fairchild µA709A, µA709, and µA709C**
- **Maximum Peak-to-Peak Output Voltage Swing . . . 28-V Typical with 15-V Supplies**

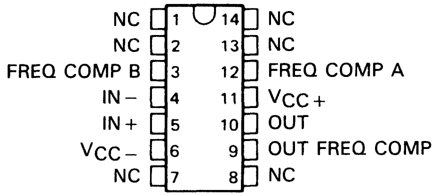
description

These circuits are general-purpose operational amplifiers, each having high-impedance differential inputs and a low-impedance output. Component matching, inherent with silicon monolithic circuit-fabrication techniques, produces an amplifier with low-drift and low-offset characteristics. Provisions are incorporated within the circuit whereby external components may be used to compensate the amplifier for stable operation under various feedback or load conditions. These amplifiers are particularly useful for applications requiring transfer or generation of linear or nonlinear functions.

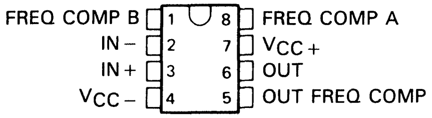
The uA709A circuit features improved offset characteristics, reduced input-current requirements, and lower power dissipation when compared to the uA709 circuit. In addition, maximum values of the average temperature coefficients of offset voltage and current are specified for the uA709A.

The uA709AM and uA709M are characterized for operation over the full military temperature range of −55°C to 125°C. The uA709C is characterized for operation from 0°C to 70°C.

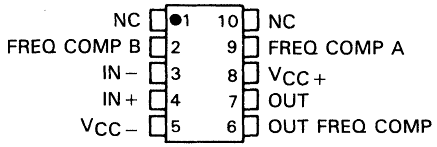
uA709AM, uA709M . . . J OR W PACKAGE
(TOP VIEW)



uA709AM, uA709M . . . JG PACKAGE
uA709C . . . D, JG, OR P PACKAGE
(TOP VIEW)

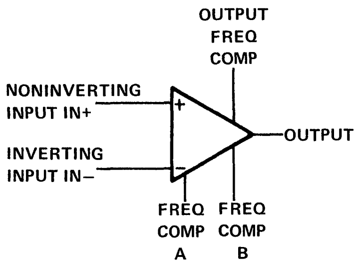


uA709AM, uA709M . . . U FLAT PACKAGE
(TOP VIEW)



NC—No internal connection

symbol



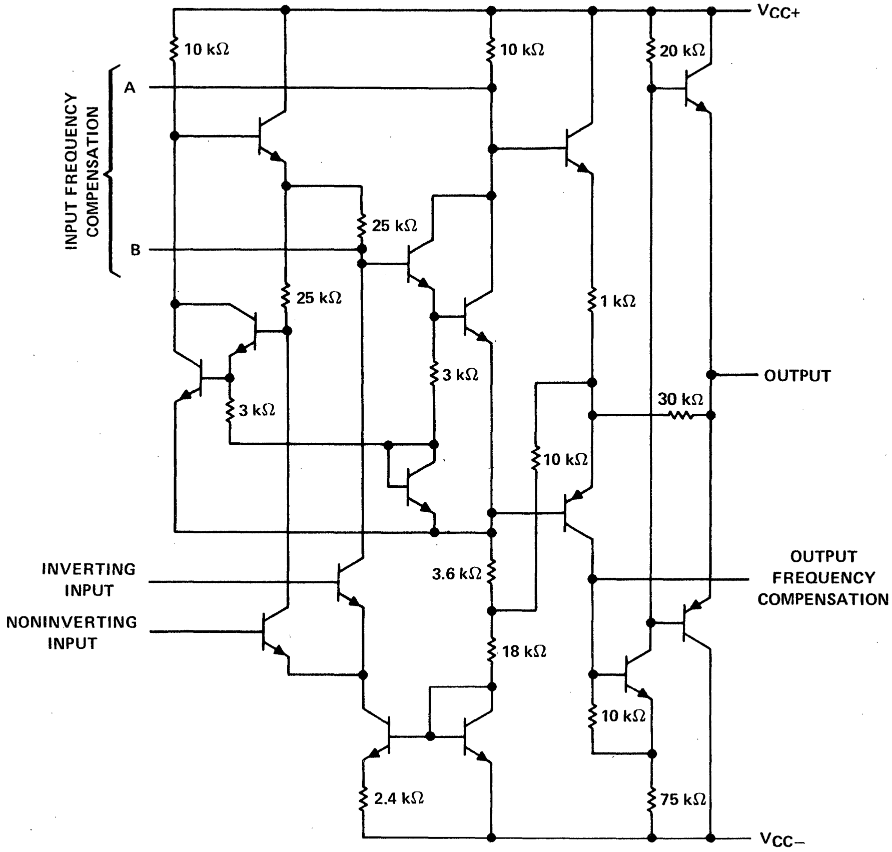
AVAILABLE OPTIONS

T_A	V_{IO} MAX AT 25°C	PACKAGE SMALL OUTLINE (D)	CERAMIC (J)	CERAMIC DIP (JG)	PLASTIC DIP (P)	FLAT PACK (U)	FLAT PACK (W)
0°C to 70°C	7.5 mV	uA709CD	—	uA709CJG	uA709CP	—	—
−55°C to 125°C	5 mV	—	uA709MJ	uA709MJG	—	uA709MU	uA709MW
	2 mV		uA709AMJ	uA709AMJG		uA709AMU	uA709AMW

The D package is available taped and reeled. Add the suffix R to the device type when ordering, (e.g., uA709CDR)

TEXAS INSTRUMENTS
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

schematic



Component values shown are nominal.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

		uA709AM uA709M	uA709C	UNIT
Supply voltage V_{CC+} (see Note 1)		18	18	V
Supply voltage V_{CC-} (see Note 1)		−18	−18	V
Differential input voltage (see Note 2)		±5	±5	V
Input voltage (either input, see Notes 1 and 3)		±10	±10	V
Duration of output short-circuit (see Note 4)		5	5	s
Continuous total dissipation		See Dissipation Rating Table		
Operating free-air temperature range		−55 to 125	0 to 70	°C
Storage temperature range		−65 to 150	−65 to 150	°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds	J, JG, U, or W package	300	300	°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	D or P package		260	°C

NOTES: 1. All voltage values, unless otherwise noted, are with respect to the midpoint between V_{CC+} and V_{CC-}.
2. Differential voltages are at the noninverting input terminal with respect to the inverting input terminal.
3. The magnitude of the input voltage must never exceed the magnitude of the supply voltage or 10 V, whichever is less.
4. The output may be shorted to ground or either power supply.

DISSIPATION RATING TABLE

PACKAGE	T_A ≤ 25°C POWER RATING	DERATING FACTOR	DERATE ABOVE T_A	T_A = 70°C POWER RATING	T_A = 125°C POWER RATING
D	300 mW	N/A	N/A	300 mW	N/A
J (uA709__M)	300 mW	11.0 mW/°C	123°C	300 mW	275 mW
JG (uA709__M)	300 mW	8.4 mW/°C	114°C	300 mW	210 mW
JG (uA709C)	300 mW	N/A	N/A	300 mW	N/A
P	300 mW	N/A	N/A	300 mW	N/A
U	300 mW	5.4 mW/°C	94°C	300 mW	135 mW
W	300 mW	8.0 mW/°C	113°C	300 mW	200 mW

electrical characteristics at specified free-air temperature, $V_{CC\pm}$ = ±9 V to ±15 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		uA709AM			uA709M			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IO}	Input offset voltage	V_O = 0 R_S ≤ 10 kΩ	25°C		0.6	2		1	5	mV
			Full range			3			6	
α_{VIO}	Average temperature coefficient of input offset voltage	V_O = 0, R_S = 50 Ω	Full range		1.8	10		3		μV/°C
		V_O = 0, R_S = 10 kΩ	Full range		4.8	25		6		
I_{IO}	Input offset current	V_O = 0	25°C		10	50		50	200	nA
			−55°C		40	250		100	500	
			125°C		3.5	50		20	200	
α_{IIO}	Average temperature coefficient of input offset current	V_O = 0	−55°C to 25°C		0.45	2.8				nA/°C
			25°C to 125°C		0.08	0.5				
I_{IB}	Input bias current	V_O = 0	25°C		0.1	0.2		0.2	0.5	μA
			−55°C		0.3	0.6		0.5	1.5	
V_{ICR}	Common-mode input voltage range	$V_{CC\pm}$ = ±15 V	25°C	±8	±10		±8	±10		V
			Full range	±8			±8			
V_{OPP}	Maximum peak-to-peak output voltage swing	$V_{CC\pm}$ = ±15 V, R_L ≥ 10 kΩ	25°C	24	28		24	28		V
			Full range	24			24			
		$V_{CC\pm}$ = ±15 V, R_L = 2 kΩ	25°C	20	26		20	26		
		$V_{CC\pm}$ = ±15 V, R_L ≥ 2 kΩ	Full range	20			20			
A_{VD}	Large-signal differential voltage amplification	$V_{CC\pm}$ = ±15 V, R_L ≥ 2 kΩ, V_O = ±10 V	25°C		45			45		V/mV
			Full range	25		70	25		70	
r_i	Input resistance		25°C	350	750		150	400		kΩ
			−55°C	85	185		40	100		
r_o	Output resistance	V_O = 0, See Note 5	25°C		150			150		Ω
CMRR	Common-mode rejection ratio	V_{IC} = V_{ICR} min	25°C	80	110		70	90		dB
			Full range	80			70			
k_{SVS}	Power supply sensitivity ($\Delta V_{IO}/\Delta V_{CC}$)	V_{CC} = ±9 V to ±15 V	25°C		40	100		25	150	μV/V
			Full range			100			150	
I_{CC}	Supply current	$V_{CC\pm}$ = ±15 V, No load, V_O = 0	25°C		2.5	3.6		2.6	5.5	mA
			−55°C		2.7	4.5				
			125°C		2.1	3				
P_D	Total power dissipation	$V_{CC\pm}$ = ±15 V, No load, V_O = 0	25°C		75	108		78	165	mW
			−55°C		81	135				
			125°C		63	90				

† All characteristics are specified under open-loop with zero common-mode input voltage unless otherwise specified. Full range for uA709AM and uA709M is −55°C to 125°C.

‡ All typical values are at $V_{CC\pm}$ = ±15 V.

NOTE 5: This typical value applies only at frequencies above a few hundred hertz because of the effects of drift and thermal feedback.

electrical characteristics at specified free-air temperature (unless otherwise noted $V_{CC\pm} = \pm 15$ V)

PARAMETER		TEST CONDITIONS†		uA709C MIN	uA709C TYP	uA709C MAX	UNIT
V_{IO}	Input offset voltage	$V_{CC\pm} = \pm 9$ V to ± 15 V, $V_O = 0$	25°C		2	7.5	mV
			Full range			10	
I_{IO}	Input offset current	$V_{CC\pm} = \pm 9$ V to ± 15 V, $V_O = 0$	25°C		100	500	nA
			Full range			750	
I_{IB}	Input bias current	$V_{CC\pm} = \pm 9$ V to ± 15 V, $V_O = 0$	25°C		0.3	1.5	μA
			Full range			2	
V_{ICR}	Common-mode input voltage range		25°C	±8	±10		V
V_{OPP}	Maximum peak-to-peak output voltage swing	$R_L \geq 10$ kΩ	25°C	24	28		V
			Full range	24			
		$R_L = 2$ kΩ	25°C	20	26		
		$R_L \geq 2$ kΩ	Full range	20			
A_{VD}	Large-signal differential voltage amplification	$R_L \leq 2$ kΩ, $V_O = \pm 10$ V	25°C	15	45		V/mV
			Full range	12			
r_i	Input resistance		25°C	50	250		kΩ
			Full range	35			
r_o	Output resistance	$V_O = 0$, See Note 5	25°C		150		Ω
CMRR	Common-mode rejection ratio	$V_{IC} = V_{ICR}$ min	25°C	65	90		dB
k_{SVS}	Supply voltage sensitivity	$V_{CC} = \pm 9$ V to ± 15 V	25°C		25	200	μV/V
P_D	Total power dissipation	$V_O = 0$, No load	25°C		80	200	mW

† All characteristics are specified under open-loop operation with zero volts common-mode voltage unless otherwise specified. Full range for uA709C is 0°C to 70°C.

NOTE 5: This typical value applies only at frequencies above a few hundred hertz because of the effects of drift and thermal feedback.

operating characteristics $V_{CC\pm} = \pm 9$ V to ± 15 V, $T_A = 25$°C

PARAMETER		TEST CONDITIONS		uA709AM uA709M uA709C MIN	TYP	MAX	UNIT
t_r	Rise time	$V_I = 20$ mV, $R_L = 2$ kΩ, See Figure 1	$C_L = 0$		0.3	1	μs
	Overshoot factor		$C_L = 100$ pF		6%	30%	

PARAMETER MEASUREMENT INFORMATION

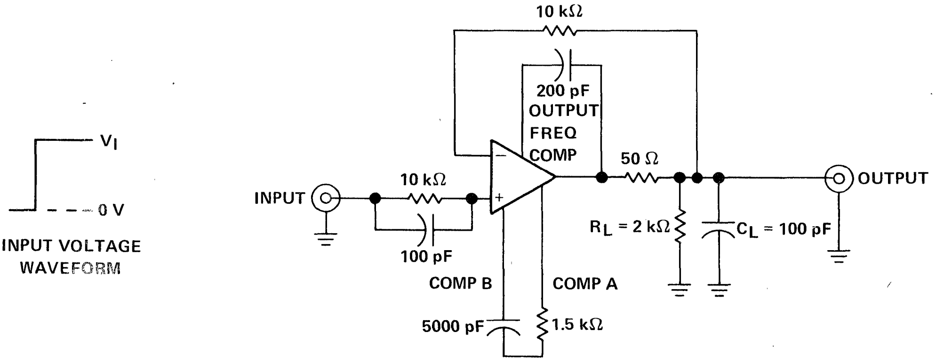


FIGURE 1. RISE TIME AND SLEW RATE

uA741C, uA741I, uA741M
GENERAL-PURPOSE OPERATIONAL AMPLIFIERS

D920, NOVEMBER 1970 — REVISED JANUARY 1992

- **Short-Circuit Protection**
- **Offset-Voltage Null Capability**
- **Large Common-Mode and Differential Voltage Ranges**
- **No Frequency Compensation Required**
- **Low Power Consumption**
- **No Latch-Up**
- **Designed to Be Interchangeable With Fairchild μA741**

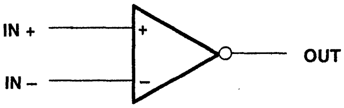
description

The uA741 is a general-purpose operational amplifier featuring offset-voltage null capability.

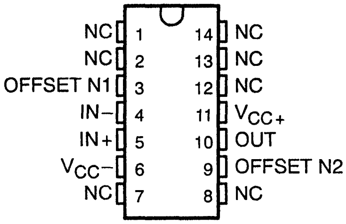
The high common-mode input voltage range and the absence of latch-up make the amplifier ideal for voltage-follower applications. The device is short-circuit protected and the internal frequency compensation ensures stability without external components. A low potentiometer may be connected between the offset null inputs to null out the offset voltage as shown in Figure 2.

The uA741C is characterized for operation from 0°C to 70°C. The uA741I is characterized for operation from −40°C to 85°C.The uA741M is characterized for operation over the full military temperature range of −55°C to 125°C.

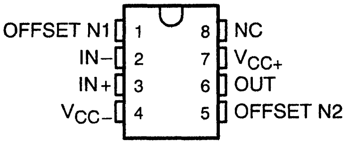
symbol



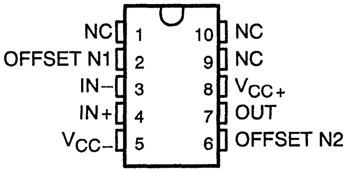
uA741M . . . J PACKAGE
(TOP VIEW)



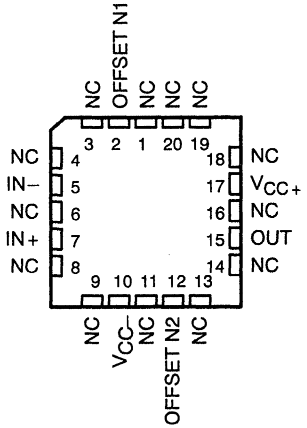
uA741M . . . JG PACKAGE
uA741C, uA741I . . . D OR P PACKAGE
(TOP VIEW)



uA741M . . . U FLAT PACKAGE
(TOP VIEW)



uA741M . . . FK PACKAGE
(TOP VIEW)



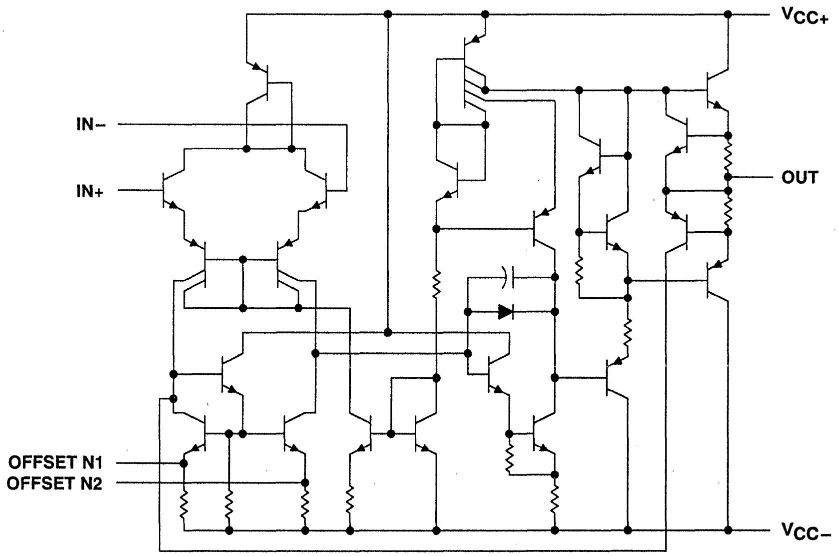
NC–No internal connection

AVAILABLE OPTIONS

T_A	PACKAGE					
	SMALL OUTLINE (D)	CHIP CARRIER (FK)	CERAMIC DIP (J)	CERAMIC DIP (JG)	PLASTIC DIP (P)	FLAT PACK (U)
0°C to 70°C	uA741CD				uA741CP	
−40°C to 85°C	uA741ID				uA741IP	
−55°C to 125°C		uA741MFK	uA741MJ	uA741MJG		uA741MU

The D package is available taped and reeled. Add the suffix R (e.g., uA741CDR).

schematic



Component Count

Transistors	**22**
Resistors	**11**
Diode	**1**
Capacitor	**1**

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

		uA741C	uA741I	uA741M	UNIT
Supply voltage V_{CC+} (see Note 1)		18	22	22	V
Supply voltage V_{CC-} (see Note 1)		−18	−22	−22	V
Differential input voltage (see Note 2)		±15	±30	±30	V
Input voltage any input (see Notes 1 and 3)		±15	±15	±15	V
Voltage between either offset null terminal (N1/N2) and V_{CC-}		±15	±0.5	±0.5	V
Duration of output short circuit (see Note 4)		unlimited	unlimited	unlimited	
Continuous total power dissipation		See Dissipation Rating Table			
Operating free-air temperature range		0 to 70	−40 to 85	-55 to 125	°C
Storage temperature range		−65 to 150	−65 to 150	−65 to 150	°C
Case temperature for 60 seconds	FK package			260	°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds	J, JG, or U package			300	°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	D or P package	260	260		°C

NOTES: 1. All voltage values, unless otherwise noted, are with respect to the midpoint between V_{CC+} and V_{CC-}.
2. Differential voltages are at the noninverting input terminal with respect to the inverting input terminal.
3. The magnitude of the input voltage must never exceed the magnitude of the supply voltage or 15 V, whichever is less.
4. The output may be shorted to ground or either power supply. For the uA741M only, the unlimited duration of the short circuit applies at (or below) 125°C case temperature or 75°C free-air temperature.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR	DERATE ABOVE T_A	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING	$T_A = 125°C$ POWER RATING
D	500 mW	5.8 mW/°C	64°C	464 mW	377 mW	N/A
FK	500 mW	11.0 mW/°C	105°C	500 mW	500 mW	275 mW
J	500 mW	11.0 mW/°C	105°C	500 mW	500 mW	275 mW
JG	500 mW	8.4 mW/°C	90°C	500 mW	500 mW	210 mW
P	500 mW	N/A	N/A	500 mW	500 mW	N/A
U	500 mW	5.4 mW/°C	57°C	432 mW	351 mW	135 mW

electrical characteristics at specified free-air temperature, $V_{CC}\pm = \pm 15$ V

PARAMETER		TEST CONDITIONS	T_A†	UA741C			UA741I, UA741M			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	$V_O = 0$	25°C		1	6		1	5	mV
			Full range			7.5			6	
$\Delta V_{IO(adj)}$	Offset voltage adjust range	$V_O = 0$	25°C		±15			±15		mV
I_{IO}	Input offset curent	$V_O = 0$	25°C		20	200		20	200	nA
			Full range			300			500	
I_{IB}	Input bias current	$V_O = 0$	25°C		80	500		80	500	nA
			Full range			800			1500	
V_{ICR}	Common-mode input voltage range		25°C	±12	±13		±12	±13		V
			Full range	±12			±12			
V_{OM}	Maximum peak output voltage swing	$R_L = 10$ kΩ	25°C	±12	±14		±12	±14		V
		$R_L \geq 10$ kΩ	Full range	±12			±12			
		$R_L = 2$ kΩ	25°C	±10	±13		±10	±13		
		$R_L \geq 2$ kΩ	Full range	±10			±10			
A_{VD}	Large-signal differential voltage amplification	$R_L \geq 2$ kΩ	25°C	20	200		50	200		V/mV
		$V_O = \pm 10$ V	Full range	15			25			
r_i	Input resistance		25°C	0.3	2		0.3	2		MΩ
r_o	Output resistance	$V_O = 0$, See Note 5	25°C		75			75		Ω
C_i	Input capacitance		25°C		1.4			1.4		pF
CMRR	Common-mode rejection ratio	$V_{IC} = V_{ICR}$ min	25°C	70	90		70	90		dB
			Full range	70			70			
k_{SVS}	Supply voltage sensitivity ($\Delta V_{IO}/\Delta V_{CC}$)	$V_{CC} = \pm 9$ V to ±15 V	25°C		30	150		30	150	µV/V
			Full range			150			150	
I_{OS}	Short-circuit output current		25°C		±25	±40		±25	±40	mA
I_{CC}	Supply current	No load, $V_O = 0$	25°C		1.7	2.8		1.7	2.8	mA
			Full range			3.3			3.3	
P_D	Total power dissipation	No load, $V_O = 0$	25°C		50	85		50	85	mW
			Full range			100			100	

† All characteristics are measured under open-loop conditions with zero common-mode input voltage unless otherwise specified. Full range for the uA741C is 0°C to 70°C, the uA741I is –40°C to 85°C, and the uA741M is –55°C to 125°C.

NOTE 5: This typical value applies only at frequencies above a few hundred hertz because of the effects of drift and thermal feedback.

operating characteristics, $V_{CC}\pm = \pm 15$ V, $T_A = 25°C$

PARAMETER		TEST CONDITIONS	uA741C			uA741I, uA741M			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
t_r	Rise time	V_I = 20 mV, R_L = 2 kΩ, C_L = 100 pF, See Figure 1		0.3			0.3		μs
	Overshoot factor			5%			5%		
SR	Slew rate at unity gain	V_I = 10 V, R_L = 2 kΩ, C_L = 100 pF, See Figure 1		0.5			0.5		V/μs

PARAMETER MEASUREMENT INFORMATION

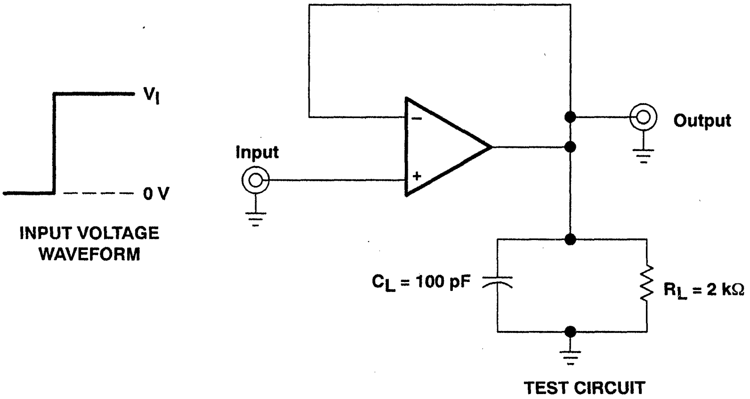


Figure 1. Rise Time, Overshoot, and Slew Rate

APPLICATION INFORMATION

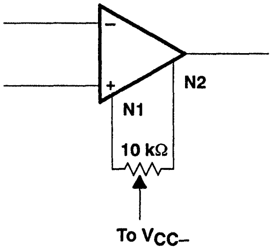


Figure 2. Input Offset Voltage Null Circuit

TYPICAL CHARACTERISTICS†

INPUT OFFSET CURRENT
vs
FREE-AIR TEMPERATURE

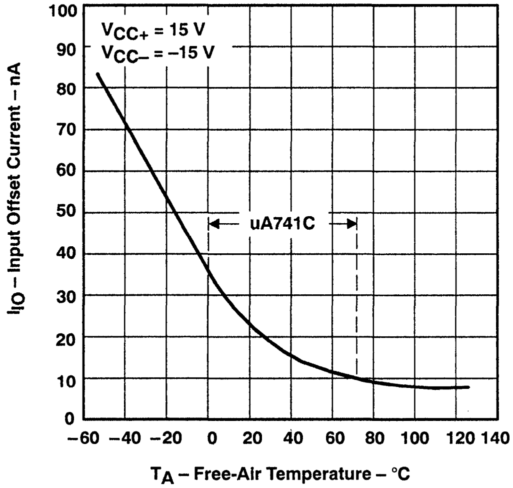


Figure 3

INPUT BIAS CURRENT
vs
FREE-AIR TEMPERATURE

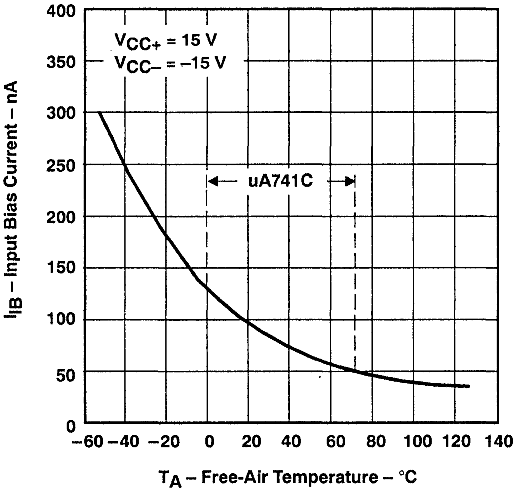


Figure 4

MAXIMUM PEAK OUTPUT VOLTAGE
vs
LOAD RESISTANCE

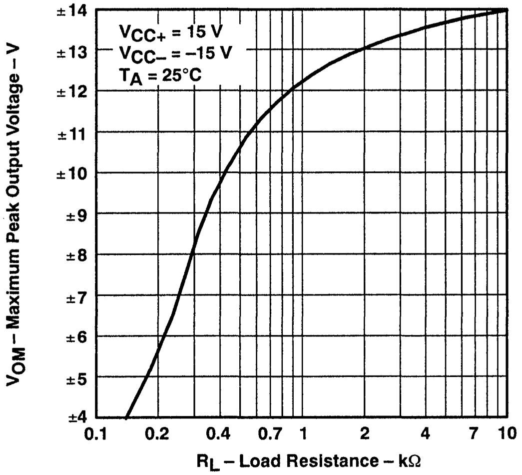


Figure 5

---

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS

MAXIMUM PEAK OUTPUT VOLTAGE
vs
FREQUENCY

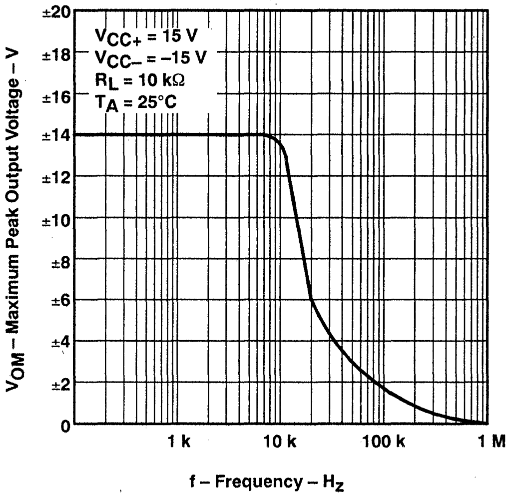


Figure 6

OPEN-LOOP SIGNAL DIFFERENTIAL
VOLTAGE AMPLIFICATION
vs
SUPPLY VOLTAGE

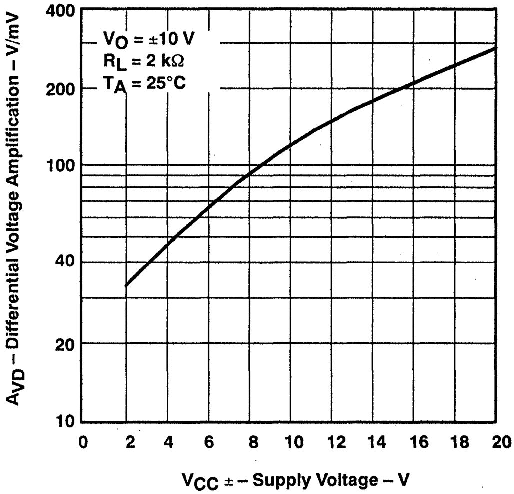


Figure 7

OPEN-LOOP LARGE-SIGNAL DIFFERENTIAL
VOLTAGE AMPLIFICATION
vs
FREQUENCY

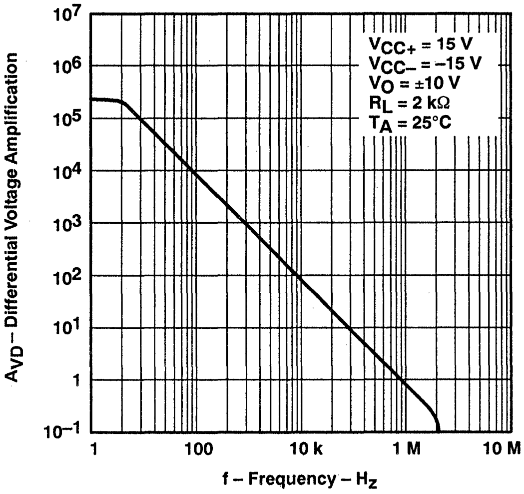


Figure 8

TYPICAL CHARACTERISTICS

COMMON-MODE REJECTION RATIO vs FREQUENCY

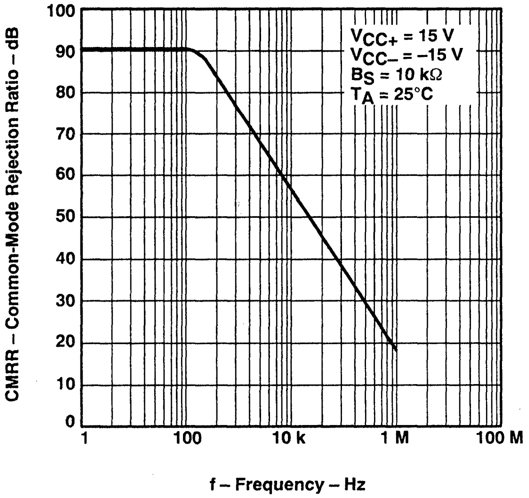


Figure 9

OUTPUT VOLTAGE vs ELAPSED TIME

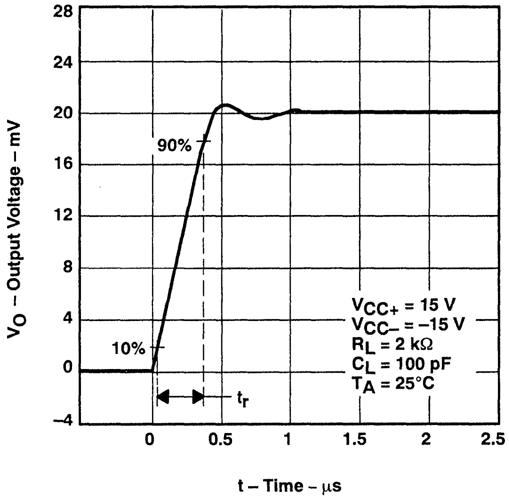


Figure 10

VOLTAGE-FOLLOWER LARGE-SIGNAL PUBLIC RESPONSE

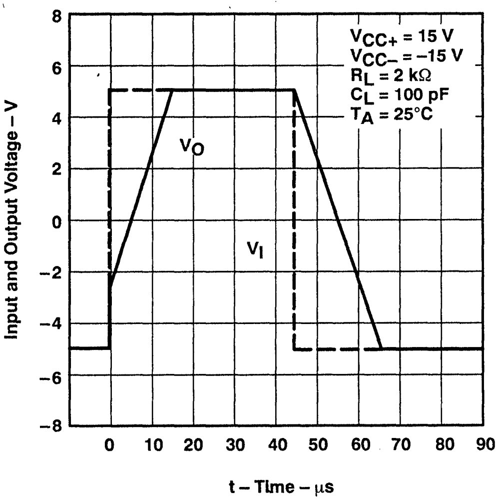


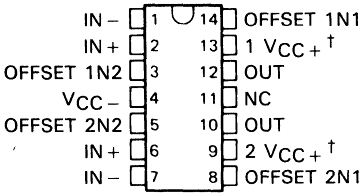
Figure 11

uA747C, uA747M
DUAL GENERAL-PURPOSE OPERATIONAL AMPLIFIERS

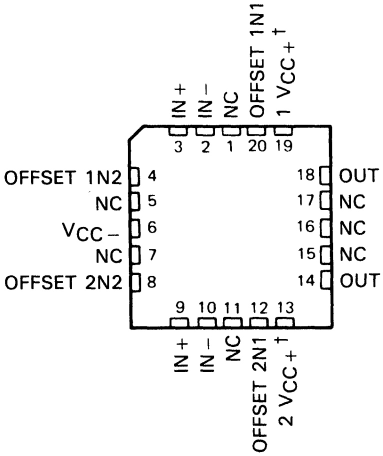
D971, FEBRUARY 1971—REVISED OCTOBER 1990

- No Frequency Compensation Required
- Low Power Consumption
- Short-Circuit Protection
- Offset-Voltage Null Capability
- Wide Common-Mode and Differential Voltage Ranges
- No Latch-Up
- Designed to be Interchangeable with Fairchild μA747M and μA747C

D, J, N, OR W PACKAGE
(TOP VIEW)



uA747M . . . FK PACKAGE
(TOP VIEW)



NC—No internal connection

† The two positive supply terminals (1 V_{CC+} and 2 V_{CC+}) are connected together internally.

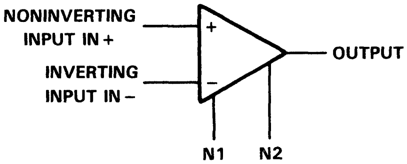
description

The uA747 is a dual general-purpose operational amplifier featuring offset-voltage null capability. Each half is electrically similar to uA741.

The high common-mode input voltage range and the absence of latch-up make this amplifier ideal for voltage-follower applications. The device is short-circuit protected and the internal frequency compensation ensures stability without external components. A low-value potentiometer may be connected between the offset null inputs to null out the offset voltage as shown in Figure 2.

The uA747C is characterized for operation from 0°C to 70°C; the uA747M is characterized for operation over the full military temperature range of −55°C to 125°C.

symbol (each amplifier)



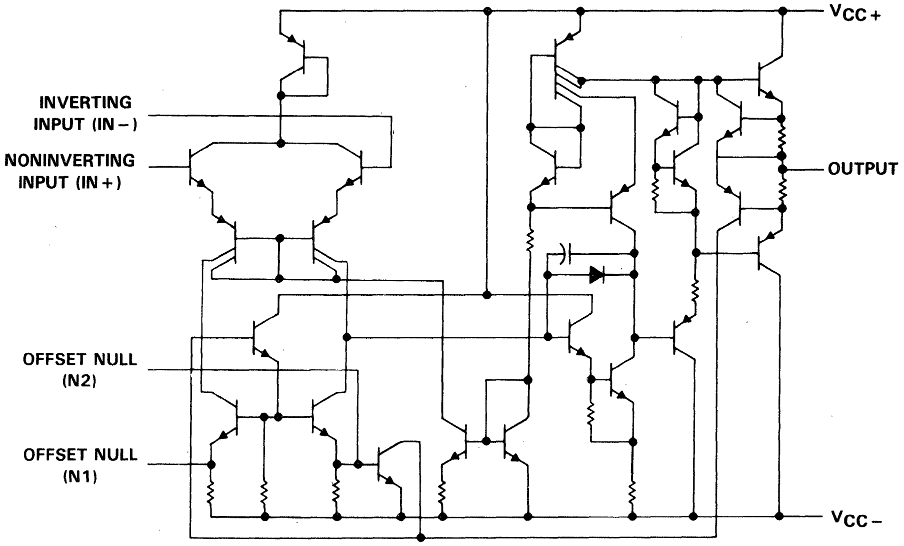
AVAILABLE OPTIONS

T_A	V_{IO} MAX AT 25°C	PACKAGE				
		14-PIN				20-PIN
		SMALL OUTLINE (D)	CERAMIC DIP (J)	PLASTIC DIP (N)	FLAT PACK (W)	CHIP CARRIER (FK)
0°C to 70°C	6 mV	uA747CD	—	uA747CN	—	—
−55°C to 125°C	5 mV	—	uA747MJ	—	uA747MW	uA747MFK

The D package is available taped and reeled. Add the suffix R to the device type, (i.e., uA747CDR).

TEXAS INSTRUMENTS
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

schematic (each amplifier)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

		uA747C	uA747M	UNIT
Supply voltage, V_{CC+} (see Note 1)		18	22	V
Supply voltage, V_{CC-} (see Note 1)		−18	−22	V
Differential input voltage (see Note 2)		±30	±30	V
Input voltage any input (see Notes 1 and 3)		±15	±15	V
Voltage between any offset null terminal (N1/N2) and V_{CC-}		±0.5	±0.5	V
Duration of output short-circuit (see Note 4)		unlimited	unlimited	
Continuous total dissipation		See Dissipation Rating Table		
Operating free-air temperature range		0 to 70	−55 to 125	°C
Storage temperature range		−65 to 150	−65 to 150	°C
Case temperature for 60 seconds	FK package		260	°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds	J or W package		300	°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	D or N package	260		°C

NOTES: 1. All voltage values, unless otherwise noted, are with respect to the midpoint between V_{CC+} and V_{CC-}.
2. Differential voltages are at the noninverting input terminal with respect to the inverting input terminal.
3. The magnitude of the input voltage must never exceed the magnitude of the supply voltage or 15 V, whichever is less.
4. The output may be shorted to ground or either power supply. For the uA747M only, the unlimited duration of the short-circuit applies at (or below) 125°C case temperature or 75°C free-air temperature.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR	DERATE ABOVE T_A	$T_A = 70°C$ POWER RATING	$T_A = 125°C$ POWER RATING
D	800 mW	7.6 mW/°C	45°C	608 mW	—
FK	800 mW	11.0 mW/°C	77°C	800 mW	275 mW
J	800 mW	11.0 mW/°C	77°C	800 mW	275 mW
N	800 mW	9.2 mW/°C	63°C	736 mW	—
W	800 mW	8.0 mW/°C	50°C	640 mW	200 mW

electrical characteristics at specified free-air temperature, V_{CC+} = 15 V, V_{CC-} = −15 V

PARAMETER		TEST CONDITIONS†		uA747C			uA747M			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	$V_O = 0$	25°C		1	6		1	5	mV
			Full range			7.5			6	
$\Delta V_{IO(adj)}$	Offset voltage adjust range		25°C		±15			±15		mV
I_{IO}	Input offset current		25°C		20	200		20	200	nA
			Full range			300			500	
I_{IB}	Input bias current		25°C		80	500		80	500	nA
			Full range			800			1500	
V_{ICR}	Common-mode input voltage range		25°C	±12	±13		±12	±13		V
			Full range	±12			±12			
V_{OPP}	Maximum peak-to-peak output voltage swing	$R_L = 10\ k\Omega$	25°C	24	28		24	28		V
		$R_L \geq 10\ k\Omega$	Full range	24			24			
		$R_L = 2\ k\Omega$	25°C	20	26		20	26		
		$R_L \geq 2\ k\Omega$	Full range	20			20			
A_{VD}	Large-signal differential voltage amplification	$R_L \geq 2\ k\Omega$, $V_O = \pm 10$ V	25°C	25	200		50	200		V/mV
			Full range	15			25			
r_i	Input resistance		25°C	0.3*	2		0.3	2		MΩ
r_o	Output resistance	See Note 6	25°C		75			75		Ω
C_i	Input capacitance		25°C		1.4			1.4		pF
CMRR	Common-mode rejection ratio	$V_{IC} = V_{ICR}$	25°C	70	90		70	90		dB
			Full range	70			70			
k_{SVS}	Supply voltage sensitivity ($\Delta V_{IO}/\Delta V_{CC}$)	$V_{CC} = \pm 9$ V to ±15 V	25°C		30	150		30	150	μV/V
			Full range			150			150	
I_{OS}	Short-circuit output current		25°C		±25	±40		±25	±40	mA
I_{CC}	Supply current (each amplifier)	No load	25°C		1.7	2.8		1.7	2.8	mA
			Full range			3.3			3.3	
P_D	Power dissipation (each amplifier)	No load, $V_O = 0$	25°C		50	85		50	85	mW
			Full range			100			100	
V_{o1}/V_{o2}	Channel separation		25°C		120			120	0	dB

†All characteristics are measured under open-loop conditions with zero common-mode input voltage unless otherwise specified. Full range for uA747C is 0°C to 70°C and for uA747M is −55°C to 125°C.

*On products compliant to MIL-STD-883, Class B, this parameter is not production tested.

NOTE 6: This typical value applies only at frequencies above a few hundred hertz because of the effects of drift and thermal feedback.

operating characteristics, V_{CC+} = 15 V, V_{CC-} = −15 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_r	Rise time	$V_I = 20$ mV, $R_L = 2\ k\Omega$, $C_L = 100$ pF, See Figure 1		0.3		μs
	Overshoot factor			5%		
SR	Slew rate at unity gain	$V_I = 10$ V, $R_L = 2\ k\Omega$, $C_L = 100$ pF, See Figure 1		0.5		V/μs

PARAMETER MEASUREMENT INFORMATION

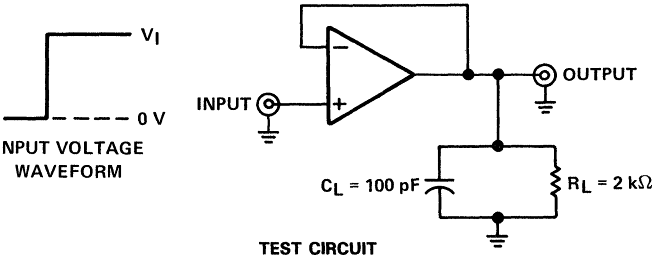


FIGURE 1. RISE TIME, OVERSHOOT, AND SLEW RATE

TYPICAL APPLICATION DATA

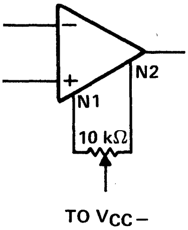


FIGURE 2. INPUT OFFSET VOLTAGE NULL CIRCUIT

TYPICAL CHARACTERISTICS

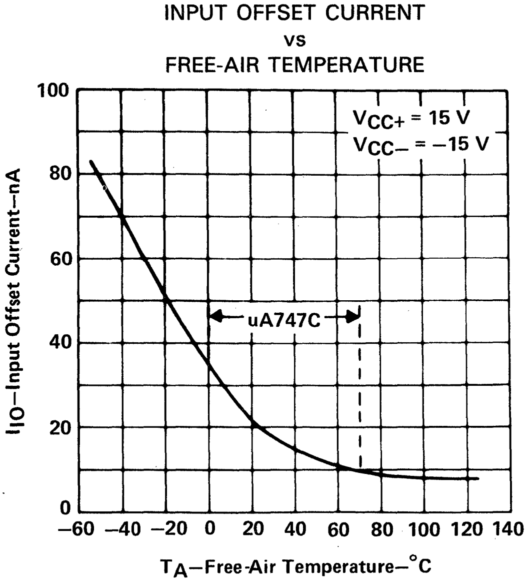


FIGURE 3

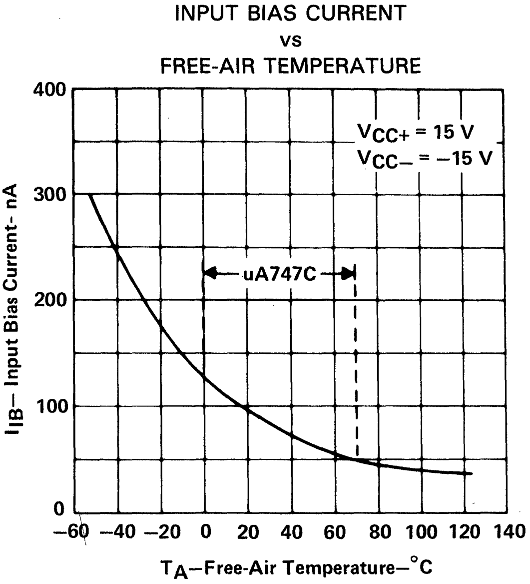


FIGURE 4

TYPICAL CHARACTERISTICS

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE vs LOAD RESISTANCE

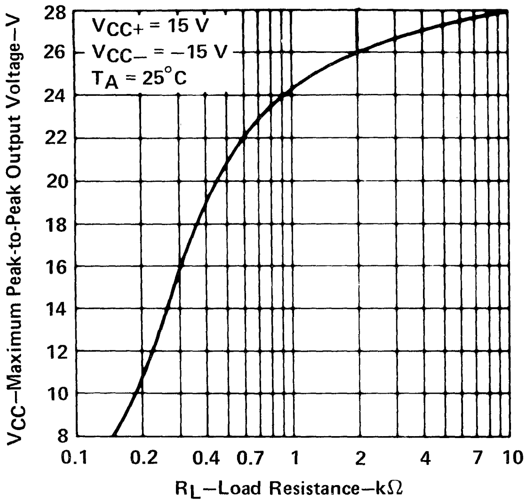


FIGURE 5

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE vs FREQUENCY

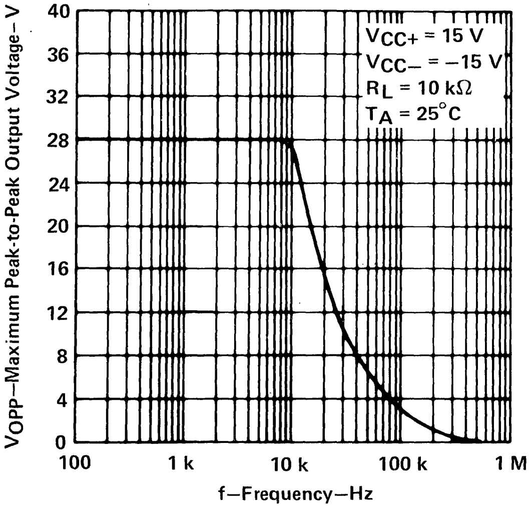


FIGURE 6

OPEN-LOOP LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION vs SUPPLY VOLTAGE

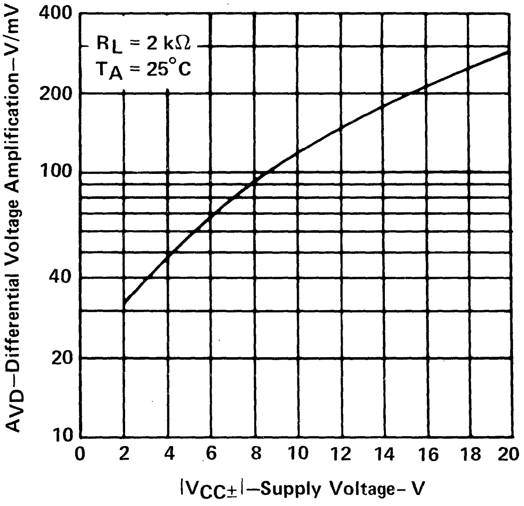


FIGURE 7

OPEN-LOOP LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION vs FREQUENCY

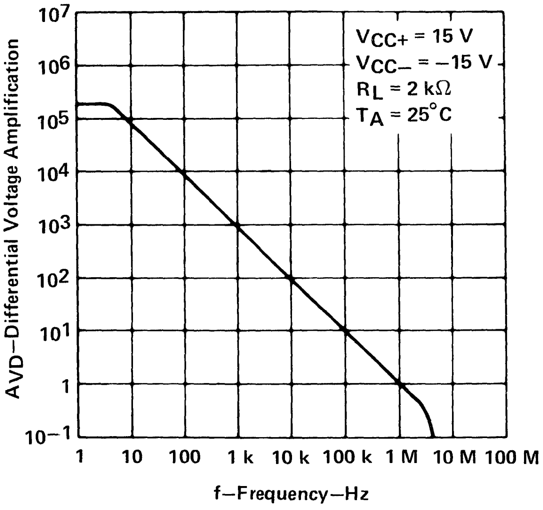


FIGURE 8

TYPICAL CHARACTERISTICS

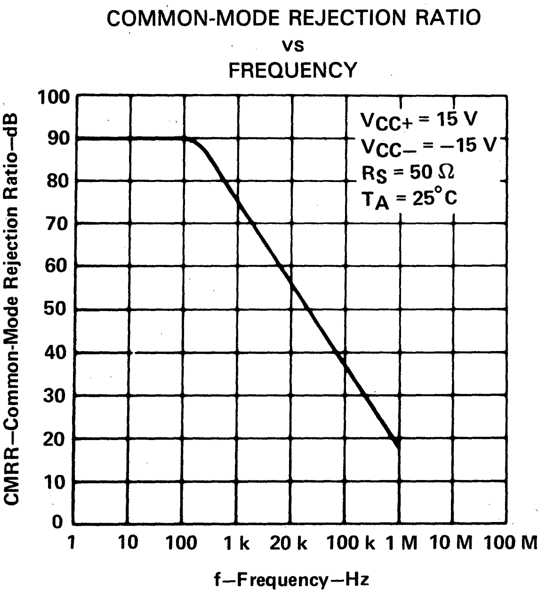


FIGURE 9

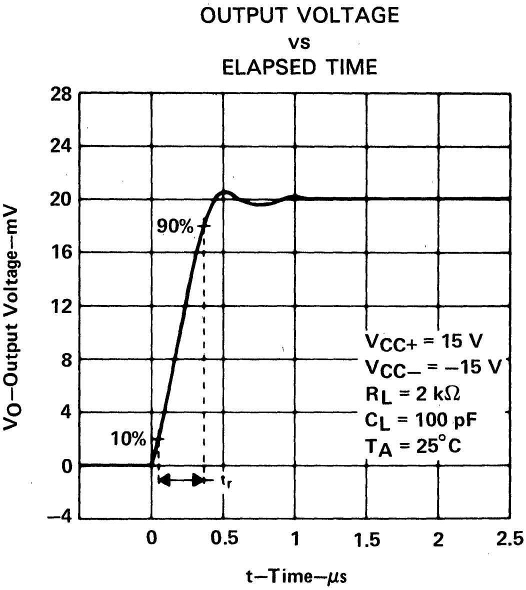


FIGURE 10

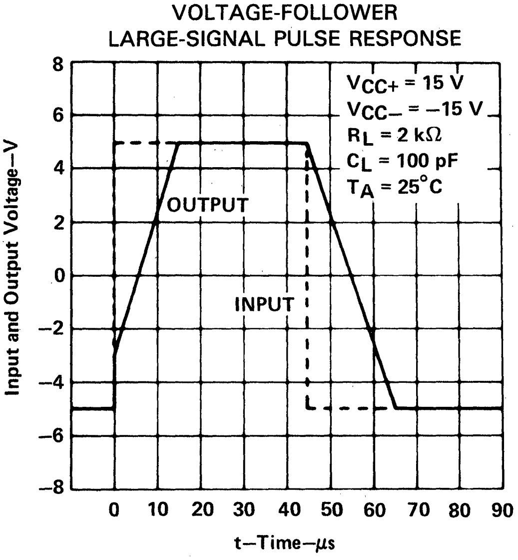


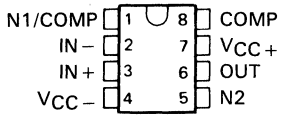
FIGURE 11

uA748C, uA748M
GENERAL-PURPOSE OPERATIONAL AMPLIFIERS

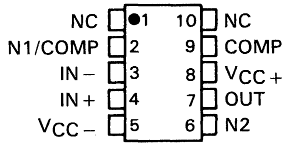
D921, DECEMBER 1970—REVISED OCTOBER 1990

- **Frequency and Transient Response Characteristics Adjustable**
- **Short-Circuit Protection**
- **Offset-Voltage Null Capability**
- **Wide Common-Mode and Differential Voltage Ranges**
- **Low Power Consumption**
- **No Latch-Up**
- **Same Pin Assignments as uA709**

uA748C . . . D OR P PACKAGE
uA748M . . . JG PACKAGE
(TOP VIEW)



uA748M . . . U FLAT PACKAGE
(TOP VIEW)



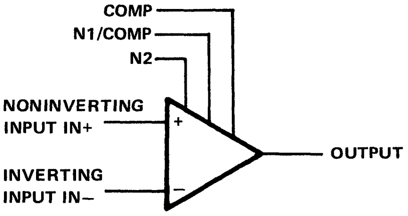
NC—No internal connection

description

The uA748 is a general-purpose operational amplifier that offers the same advantages and attractive features as the uA741 except for internal compensation. External compensation can be as simple as a 30-pF capacitor for unity-gain conditions and, when the closed-loop gain is greater than one, can be changed to obtain wider bandwidth or higher slew rate. This circuit features high gain, large differential and common-mode input voltage range, and output short-circuit protection. Input offset voltage adjustment can be provided by connecting a variable resistor between the offset null pins as shown in Figure 12.

The uA748C is characterized for operation from 0°C to 70°C; the uA748M is characterized for operation over the full military temperature range of −55°C to 125°C.

symbol

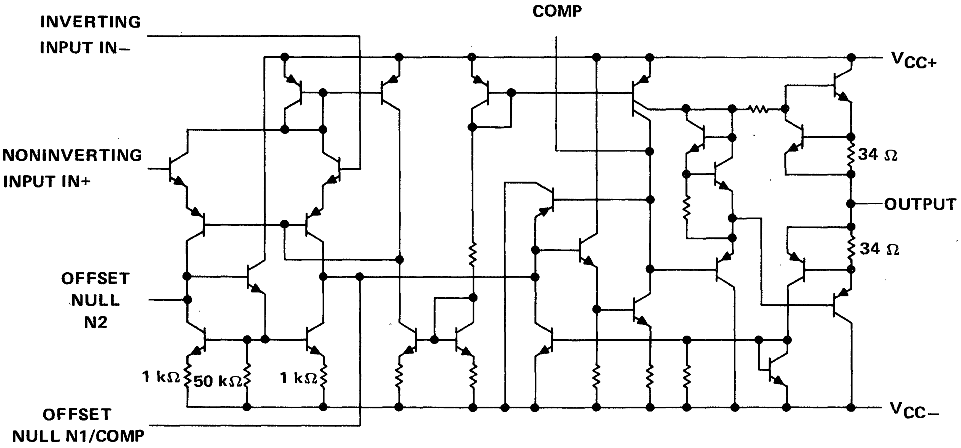


AVAILABLE OPTIONS

T_A	V_{IO} MAX AT 25°C	PACKAGE			
		8-PIN			10-PIN
		SMALL OUTLINE (D)	CERAMIC DIP (JG)	PLASTIC DIP (P)	FLAT PACK (U)
0°C to 70°C	6 mV	uA748CD	—	uA748CP	—
−55°C to 125°C	5 mV	—	uA748MJG	—	uA748MU

The D package is available taped and reeled. Add the suffix R to the device type, (e.g., uA748CDR).

schematic



Resistor values shown are nominal.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

		uA748C	uA748M	UNIT
Supply voltage V_{CC+} (see Note 1)		18	22	V
Supply voltage V_{CC-} (see Note 1)		−18	−22	V
Differential input voltage (see Note 2)		±30	±30	V
Input voltage (either input, see Notes 1 and 3)		±15	±15	V
Voltage range between either offset null terminal (N1/N2) and V_{CC-}		−0.5 to 2	−0.5 to 2	V
Duration of output short-circuit (see Note 4)		unlimited	unlimited	
Continuous total power dissipation		See Dissipation Rating Table		
Operating free-air temperature range		0 to 70	−55 to 125	°C
Storage temperature range		−65 to 150	−65 to 150	°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds	JG or U package		300	°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	D or P package	260		°C

NOTES:
1. All voltage values, unless otherwise noted, are with respect to the midpoint between V_{CC+} and V_{CC-}.
2. Differential voltages are at the noninverting input terminal with respect to the inverting input terminal.
3. The magnitude of the input voltage must never exceed the magnitude of the supply voltage or 15 V, whichever is less.
4. The output may be shorted to ground or either power supply. For the uA748M only, the unlimited duration of the short-circuit applies at (or below) 125°C case temperature or 75°C free-air temperature.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR	DERATE ABOVE T_A	$T_A = 70°C$ POWER RATING	$T_A = 125°C$ POWER RATING
D	500 mW	5.8 mW/°C	64°C	464 mW	N/A
JG	500 mW	8.4 mW/°C	90°C	500 mW	210 mW
P	500 mW	N/A	N/A	500 mW	N/A
U	500 mW	5.4 mW/°C	57°C	432 mW	135 mW

electrical characteristics at specified free-air temperature, V_{CC+} = 15 V, V_{CC-} = −15 V, C_C = 30 pF

PARAMETER		TEST CONDITIONS†		uA748C			uA748M			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	$V_O = 0$	25°C		1	6		1	5	mV
			Full range			7.5			6	
I_{IO}	Input offset current	$V_O = 0$	25°C		20	200		20	200	nA
			Full range			300			500	
I_{IB}	Input bias current	$V_O = 0$	25°C		80	500		80	500	nA
			Full range			800			1500	
V_{ICR}	Common-mode input voltage range		25°C	±12	±13		±12	±13		V
			Full range	±12			±12			
V_{OM}	Maximum peak output voltage swing	R_L = 10 kΩ	25°C	±12	±14		±12	±14		V
		$R_L \geq$ 10 kΩ	Full range	±12			±12			
		R_L = 2 kΩ	25°C	±10	±13		±10	±13		
		$R_L \geq$ 2 kΩ	Full range	±10			±10			
A_{VD}	Large-signal differential voltage amplification	$R_L \geq$ 2 kΩ,	25°C	20	200		50	200		V/mV
		V_O = ±10 V	Full range	15			25			
r_i	Input resistance		25°C	0.3	2		0.3	2		MΩ
r_o	Output resistance	$V_O = 0$, See Note 5	25°C		75			75		Ω
C_i	Input capacitance		25°C		1.4			1.4		pF
CMRR	Common-mode rejection ratio	$V_{IC} = V_{ICR}$ min,	25°C	70	90		70	90		dB
		$V_O = 0$	Full range	70			70			
k_{SVS}	Supply voltage sensitivity ($\Delta V_{IO}/\Delta V_{CC}$)	V_{CC} = ±9 V to ±15 V,	25°C		30	150		30	150	µV/V
		$V_O = 0$	Full range			150			150	
I_{OS}	Short-circuit output current		25°C		±25	±40		±25	±40	mA
I_{CC}	Supply current	No load,	25°C		1.7	2.8		1.7	2.8	mA
		$V_O = 0$	Full range			3.3			3.3	
P_D	Total power dissipation	No load,	25°C		50	85		50	85	mW
		$V_O = 0$	Full range			100			100	

† All characteristics are measured under open-loop conditions with zero common-mode input voltage unless otherwise specified. Full range for uA748C is 0°C to 70°C and for uA748M is −55°C to 125°C.

NOTE 5: This typical value applies only at frequencies above a few hundred hertz because of the effects of drift and thermal feedback.

operating characteristics, V_{CC+} = 15 V, V_{CC-} = −15 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_r	Rise time	V_I = 20 mV, R_L = 2 kΩ, C_L = 100 pF, C_C = 30 pF, See Figure 1		0.3		µs
	Overshoot factor			5%		
SR	Slew rate at unity gain	V_I = 10 V, R_L = 2 kΩ, C_L = 100 pF, C_C = 30 pF, See Figure 1		0.5		V/µs

PARAMETER MEASUREMENT INFORMATION

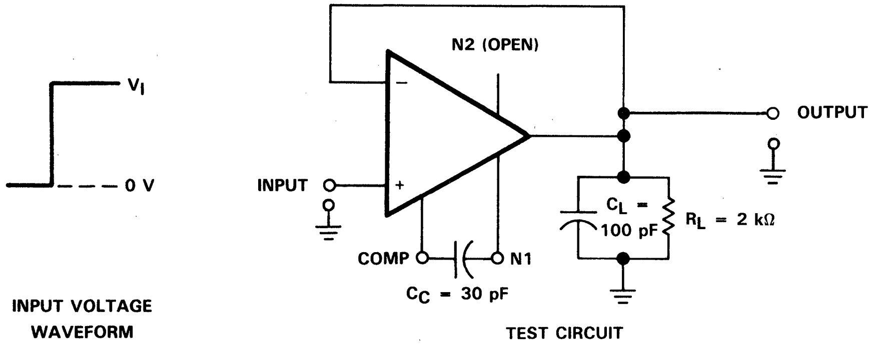


FIGURE 1. RISE TIME, OVERSHOOT, AND SLEW RATE

TYPICAL CHARACTERISTICS

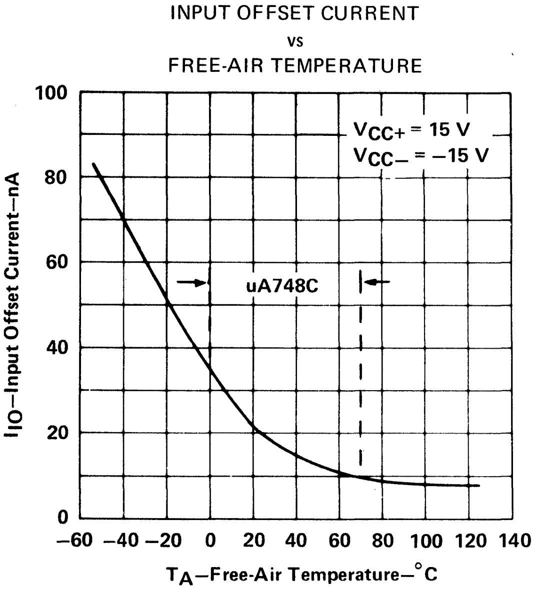


FIGURE 2

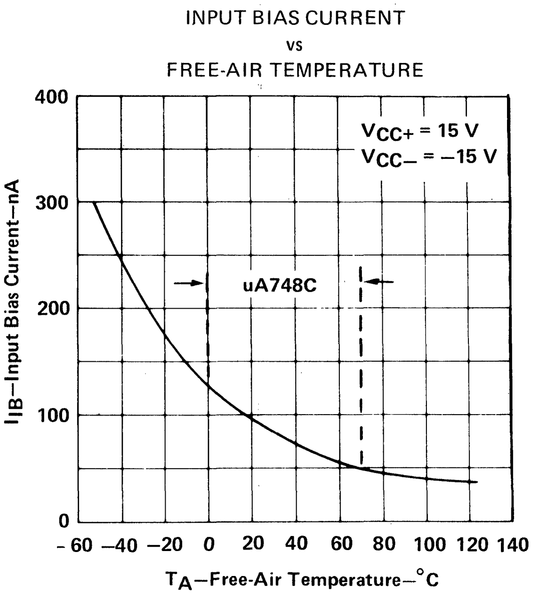


FIGURE 3

TYPICAL CHARACTERISTICS

MAXIMUM PEAK OUTPUT VOLTAGE
vs
LOAD RESISTANCE

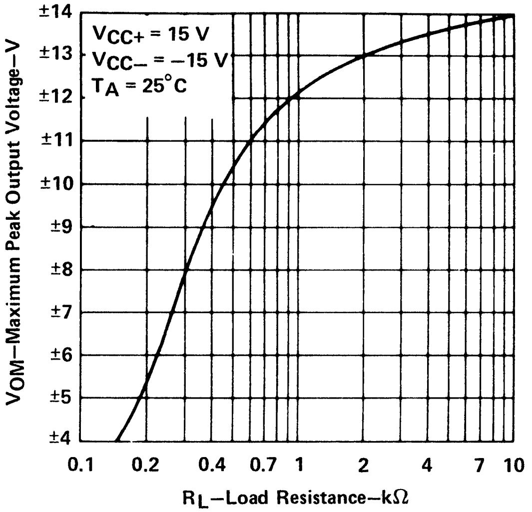


FIGURE 4

MAXIMUM PEAK OUTPUT VOLTAGE
vs
FREQUENCY

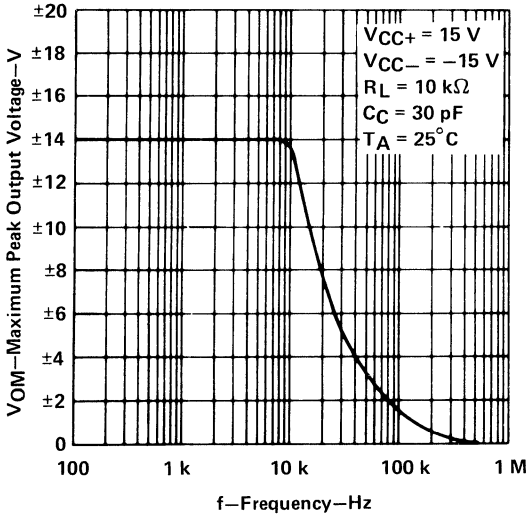


FIGURE 5

OPEN-LOOP LARGE-SIGNAL DIFFERENTIAL
VOLTAGE AMPLIFICATION
vs
SUPPLY VOLTAGE

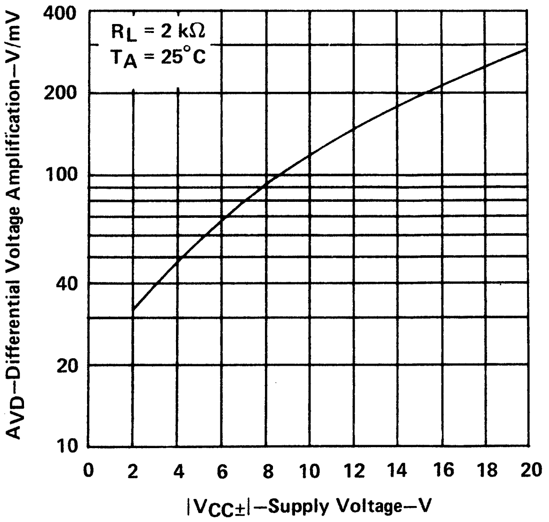


FIGURE 6

OPEN-LOOP LARGE-SIGNAL DIFFERENTIAL
VOLTAGE AMPLIFICATION
vs
FREQUENCY

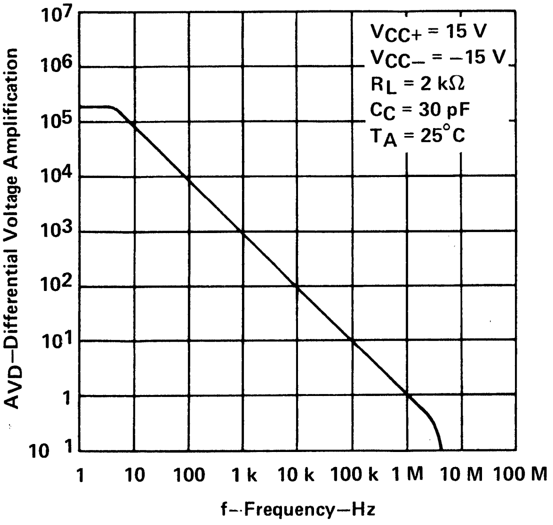


FIGURE 7

TYPICAL CHARACTERISTICS

COMMON-MODE REJECTION RATIO
vs
FREQUENCY

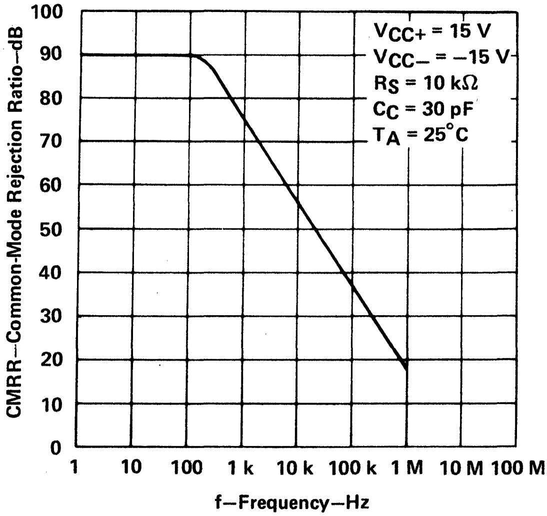


FIGURE 8

OUTPUT VOLTAGE
vs
ELAPSED TIME

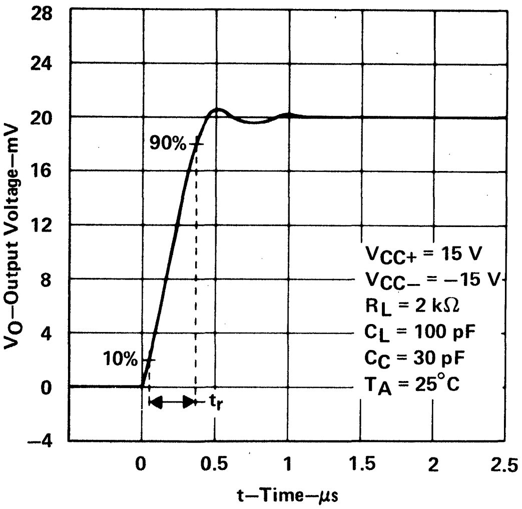


FIGURE 9

VOLTAGE-FOLLOWER
LARGE-SIGNAL PULSE RESPONSE

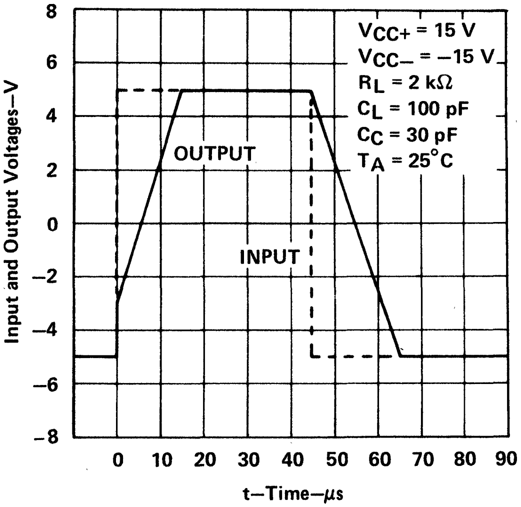


FIGURE 10

TYPICAL APPLICATION DATA

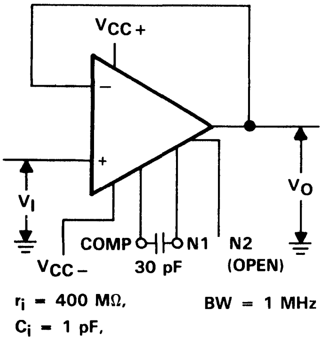
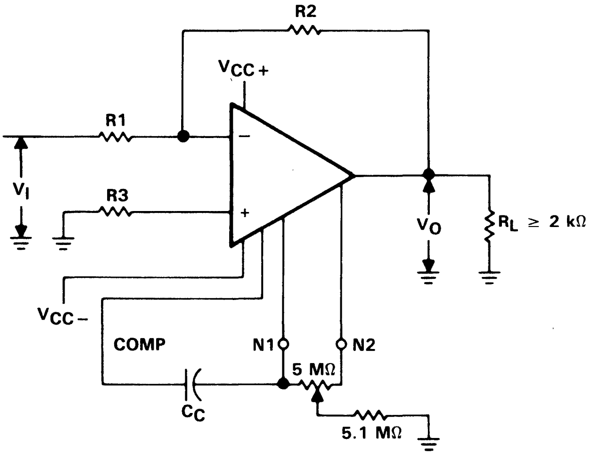


FIGURE 11. UNITY-GAIN VOLTAGE FOLLOWER



$$\frac{V_O}{V_I} = -\frac{R2}{R1}$$

$$C_C \geq \frac{R1 \cdot 30\ \text{pF}}{R1 + R2}$$

$$R3 = \frac{R1 \cdot R2}{R1 + R2}$$

FIGURE 12. INVERTING CIRCUIT WITH ADJUSTABLE GAIN COMPENSATION, AND OFFSET ADJUSTMENT

Mechanical Data 3

Contents

ORDERING INSTRUCTIONS

Electrical characteristics presented in this data book, unless otherwise noted, apply for the circuit type(s) listed in the page heading regardless of package. The availability of a circuit function in a particular package is denoted by an alphabetical reference above the pin-connection diagram(s). These alphabetical references refer to mechanical outline drawings shown in this section.

Factory orders for circuits described in this data book should include a four-part type number as shown in the following example.

Example: **TL** **598M** **J** **/883B**

Prefix

MUST CONTAIN TWO OR THREE LETTERS

SN	TI Special Functions or Interface Products
TL, TLE	TI Linear Products
TLC	TI Linear Silicon-Gate CMOS Products

STANDARD SECOND-SOURCE PREFIXES

AD	Analog Devices
ADC, LF, LM, LP, or MP	National
LT or LTC	Linear Technology
MC	Motorola
NE, SA, or SE	Signetics
OP	PMI
RC, RM, or RV	Raytheon
uA	Fairchild/National
UC	Unitrode

Unique Circuit Description Including Temperature Range

MUST CONTAIN TWO OR MORE CHARACTERS
(From Individual Data Sheets)

Examples:	10	34070
	592	1451AC
	7757	2217-285

Package

MUST CONTAIN ONE OR TWO LETTERS

D, DB, DW, FK, FN, J, JD, JG, KC, KK, KV, LP, N, NS, NT, NW, P, PK, PW, U
(From Pin-Connection Diagrams on Individual Data Sheet)

MIL-STD-883B, Method 5004, Class B

Omit /883B When Not Applicable

ORDERING INSTRUCTIONS

Circuits are shipped in one of the carriers below. Unless a specific method of shipment is specified by the customer (with possible additional costs), circuits will be shipped via the most practical carrier.

Dual-In-Line (J, JD, JG, N, NT, NS, NW, P)
- A-Channel Antistatic or Conductive Plastic Tubing

Small Outline (D, DW)
- Tape and Reel
- Antistatic or Conductive Plastic Tubing

Shrink Small Outline (DB)
- Tape and Reel

Thin Shrink Small Outline (PW)
- Tape and Reel

Chip Carriers (FK, FN)
- Antistatic or Conductive Plastic Tubing

Flat (U)
- Milton Ross Carriers

Plug-In (LP)
- Plastic Bag
- Tape and Reel

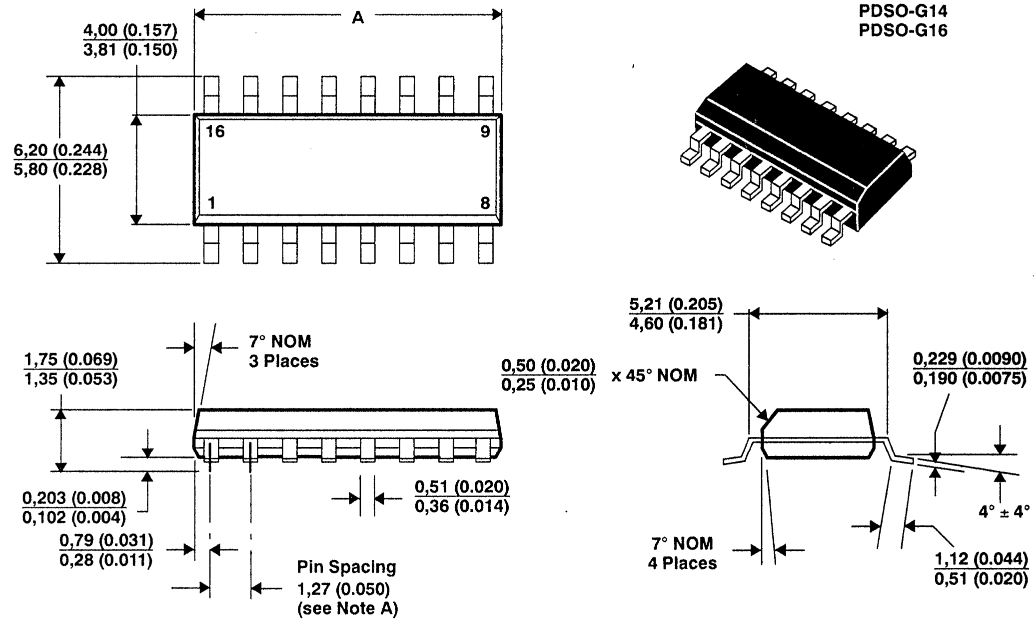
Power Tab (KC, KK, KV)
- A-Channel Antistatic or Conductive Plastic Tubing

D008, D014, and D016 plastic small-outline packages

Each of these small-outline packages consists of a circuit mounted on a lead frame and encapsulated within a plastic compound. The compound will withstand soldering temperature with no deformation, and circuit performance characteristics will remain stable when operated in high-humidity conditions. Leads require no additional cleaning or processing when used in soldered assembly.

D008, D014, and D016
(16-pin package used for Illustration)

Designation per JEDEC Std 30:
PDSO-G8
PDSO-G14
PDSO-G16



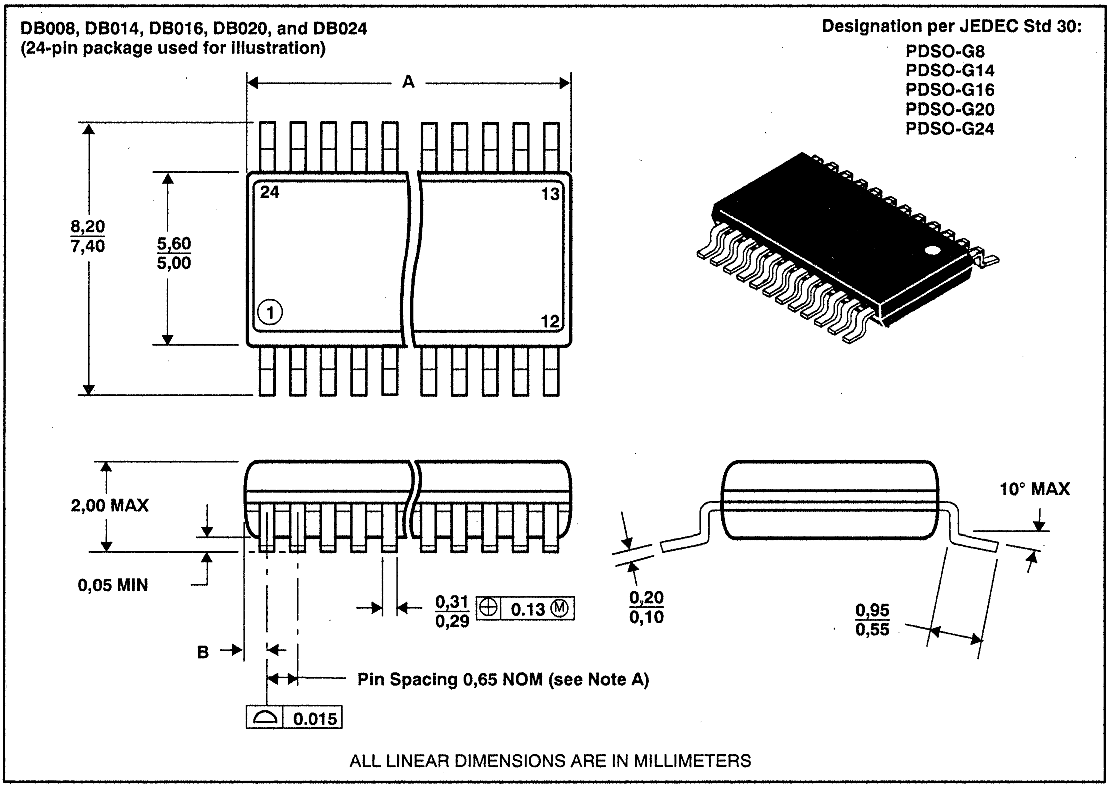
PINS / DIM	8	14	16
A MIN	4,80 (0.189)	8,55 (0.337)	9,80 (0.386)
A MAX	5,00 (0.197)	8,74 (0.344)	10,00 (0.394)

ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

NOTES:
- A. Leads are within 0,25 (0.010) radius of true position at maximum material condition.
- B. Body dimensions do not include mold flash or protrusion.
- C. Mold flash or protrusion shall not exceed 0,15 (0.006).
- D. Lead tips to be planar within ±0,051 (0.002) exclusive of solder.

DB008, DB014, DB016, DB020, and DB024 shrink small-outline packages

These shrink small-outline packages consist of a circuit mounted on a lead frame and encapsulated within a plastic compound. The compound will withstand soldering temperature with no deformation, and circuit performance characteristics will remain stable when operated in high-humidity conditions. Leads require no additional cleaning or processing when used in soldered assembly.



NOTES: A. Leads are within 0,25 mm radius of true position at maximum material condition.
B. Body dimensions do not include mold flash or protrusion.
C. Mold or flash end protrusion shall not exceed 0,15 mm.
D. Interlead flash shall be controlled by TI statistical process control (additional information available through TI field office).
E. Lead tips to be planar within ±0,05 mm exclusive of solder.

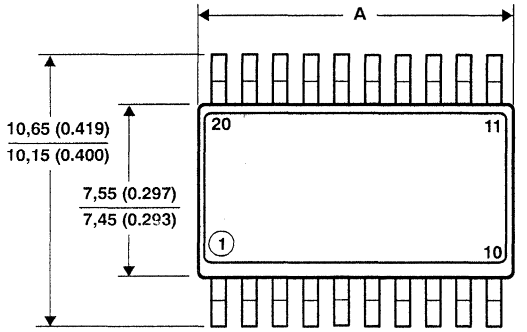
PINS DIM	8	14	16	20	24
A MIN	2,70	5,90	5,90	6,90	7,90
A MAX	3,30	6,50	6,50	7,50	8;50
B MAX	0,68	1,30	0,98	0,83	0,68

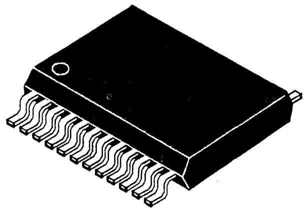
DW016, DW020, DW024, and DW028 plastic small-outline packages

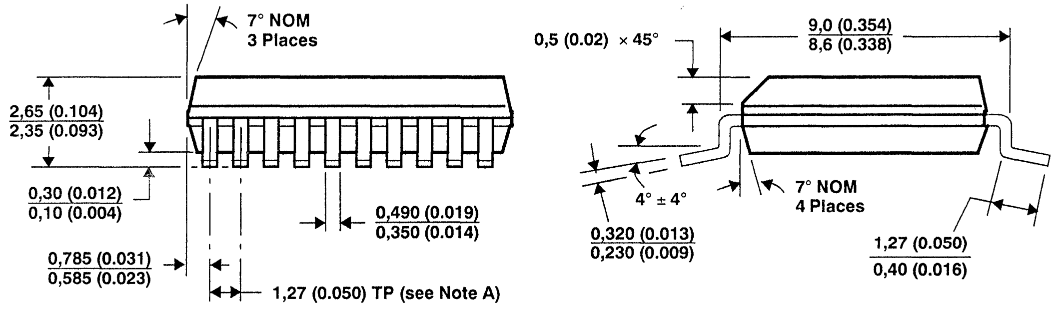
Each of these small-outline packages consists of a circuit mounted on a lead frame and encapsulated within a plastic compound. The compound will withstand soldering temperature with no deformation, and circuit performance characteristics will remain stable when operated in high-humidity conditions. Leads require no additional cleaning or processing when used in soldered assembly.

DW016, DW020, DW024, and DW028
(20-pin package used for illustration)

Designation per JEDEC Std 30:
PDSO-G16
PDSO-G20
PDSO-G24
PDSO-G28







DIM \ PINS	16	20	24	28
A MIN	10,16 (0.400)	12,70 (0.500)	15,29 (0.602)	17,68 (0.696)
A MAX	10,36 (0.408)	12,90 (0.508)	15,49 (0.610)	17,88 (0.704)

ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

NOTES: A. Leads are within 0,25 (0.010) radius of true position at maximum material condition.
B. Body dimensions do not include mold flash or protrusion.
C. Mold flash or protrusion shall not exceed, 0,15 (0.006).
D. Lead tips to be planar within ±0,051 (0.002) exclusive of solder.

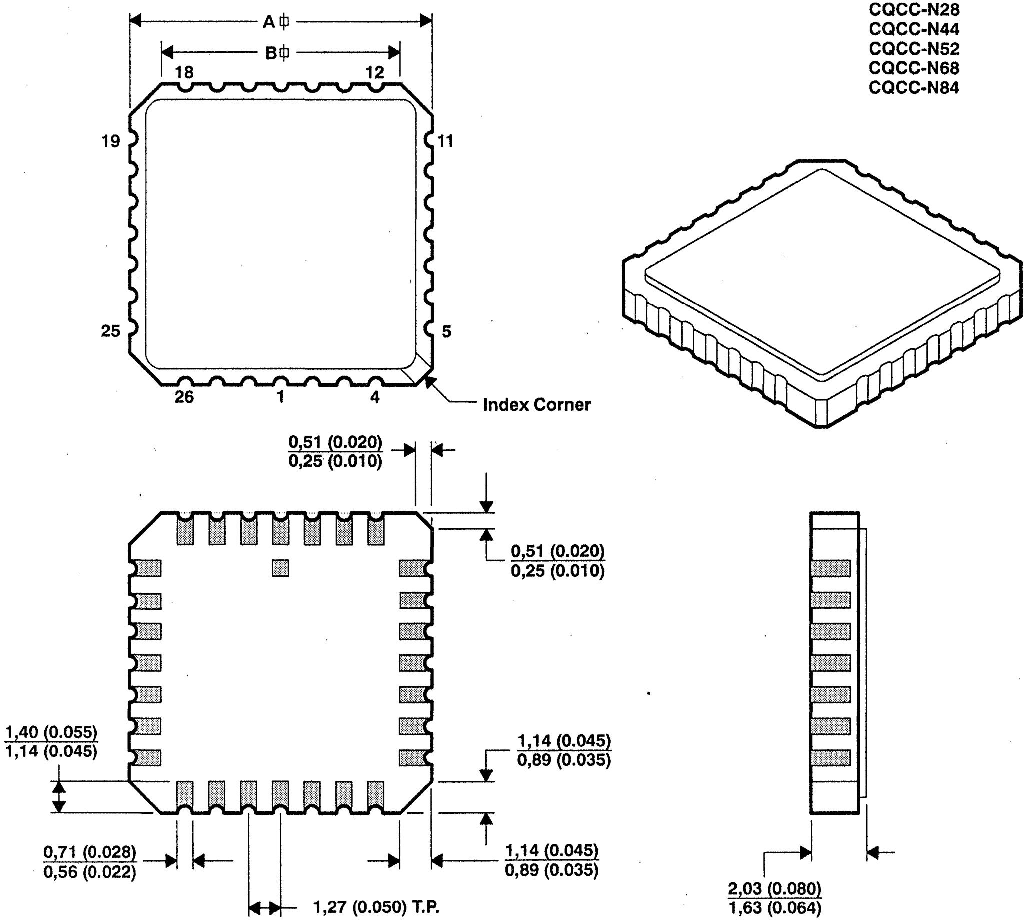
FK020, FK028, FK044, FK052, FK068, and FK084 ceramic chip carrier

Each of these hermetically sealed chip carrier packages has a three-layer ceramic base with a metal lid and braze seal. These packages are intended for surface mounting on solder leads on 1,27 (0.050) centers. Terminals require no additional cleaning or processing when used in soldered assembly.

FK package terminal assignments conform to JEDEC Standards 1 and 2.

FK020, FK028, FK044, FK052, FK068, AND FK084
(28-pin used for illustration)

Designation per JEDEC Std 30:
CQCC-N20
CQCC-N28
CQCC-N44
CQCC-N52
CQCC-N68
CQCC-N84



ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

NOTES: A. See next page for A and B dimensions.

FK020, FK028, FK044, FK052, FK068, and FK084 ceramic chip carrier (continued)

JEDEC OUTLINE DESIGNATION†	NUMBER OF TERMINALS	A		B	
		MIN	MAX	MIN	MAX
MS-004-CB	20	8,69 (0.342)	9,09 (0.358)	7,80 (0.307)	9,09 (0.358)
MS-004-CC	28	11,23 (0.442)	11,63 (0.458)	10,31 (0.406)	11,63 (0.458)
MS-004-CD	44	16,26 (0.640)	16,76 (0.660)	12,58 (0.495)	14,22 (0.560)
MS-004-CE	52	18,78 (0.740)	19,32 (0.760)	12,58 (0.495)	14,22 (0.560)
MS-004-CF	68	23,83 (0.938)	24,43 (0.962)	21,60 (0.850)	21,80 (0.858)
MS-004-CG	84	28,99 (1,141)	29,59 (1,164)	26,60 (1.047)	27,00 (1,063)

† All dimensions and notes for the specified JEDEC outline apply.

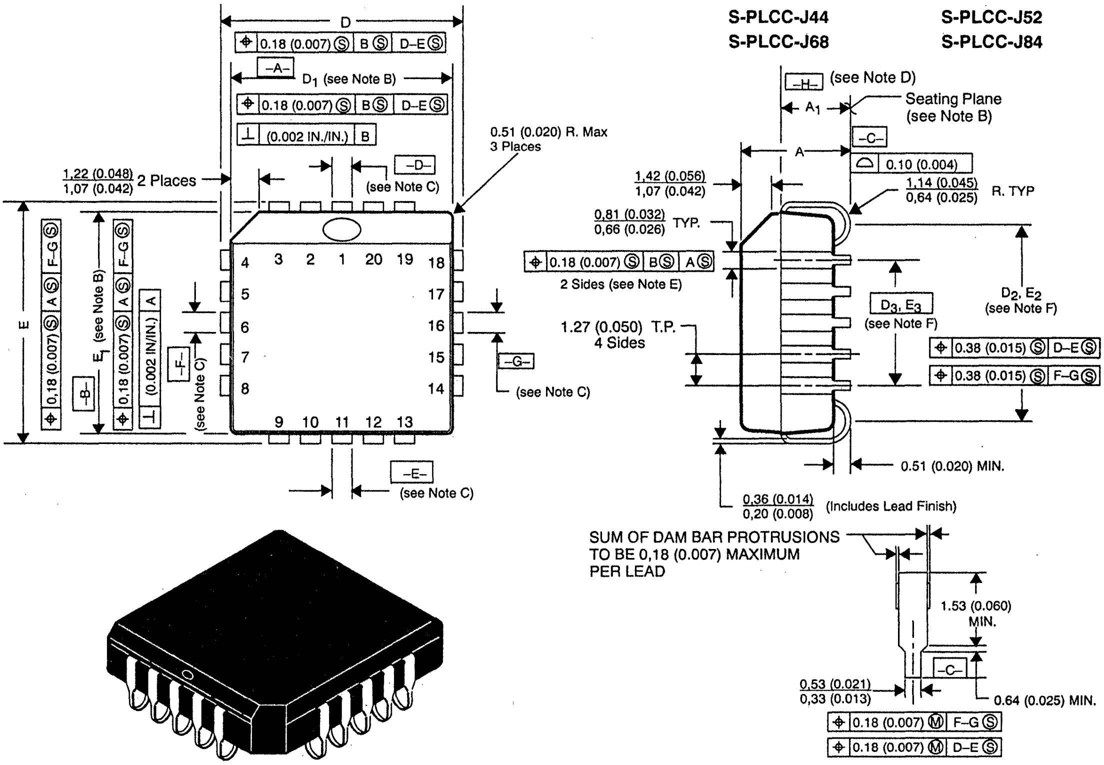
FN020, FN028, FN044, FN052, FN068, and FN084 plastic J-leaded chip carrier

Each of these chip carrier packages consists of a circuit mounted on a lead frame and encapsulated within an electrically nonconductive plastic compound. The compound withstands soldering temperatures with no deformation, and circuit performance characteristics remain stable when the devices are operated in high-humidity conditions. The package is intended for surface mounting on 1,27 (0.050) centers. Leads require no additional cleaning or processing when used in soldered assembly.

FN020, FN028, FN044, FN052, FN068, and FN084
(20-PIN package used for illustration)

Designation per JEDEC Std 30:

S-PLCC-J20	S-PLCC-J28
S-PLCC-J44	S-PLCC-J52
S-PLCC-J68	S-PLCC-J84



(see table on following page for additional dimensions)

ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

NOTES: B. All dimensions conform to JEDEC Specification MO-047AA/AF. Dimensions and tolerancing are per ANSI Y14.5M – 1982.

C. Dimensions D_1 and E_1 do not include mold flash protrusion. Protrusion shall not exceed 0,25 (0.010) on any side. Centerline of center pin each side is within 0,10 (0.004) of package centerline by dimension B. The lead contact points are planar within 0,10 (0.004).

D. Datums D – E and F – G for center leads are determined at datum – H –.

E. Datum – H – is located at top of leads where they exit plastic body.

F. Location of datums – A – and – B – to be determined at datum – H –.

G. Determined at seating plane – C –.

FN020, FN028, FN044, FN052, FN068, and FN084 plastic J-leaded chip carrier (continued)

JEDEC OUTLINE	NO.OF PINS	A		A_1		D, E		D_1, E_1		D_2, E_2		D_3, E_3
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	BASIC
MO-047AA	20	4,19 (0.165)	4,57 (0.180)	2,29 (0.090)	3,05 (0.120)	9,78 (0.385)	10,03 (0.395)	8,89 (0.350)	9,04 (0.356)	7,37 (0.290)	8,38 90.330)	5,08 (0.200)
MO-047AB	28	4,19 (0.165)	4,57 (0.180)	2,29 (0.090)	3,05 (0.120)	12,32 (0.485)	12,57 (0.495)	11,43 (0.450)	11,58 (0.456)	9,91 (0.390)	10,92 (0.430)	7,62 (0.300)
MO-047AC	44	4,19 (0.165)	4,57 (0.180)	2,29 (0.090)	3,05 (0.120)	17,40 (0.685)	17,65 (0.695)	16,51 (0.650)	16,66 (0.656)	14,99 (0.590)	16,00 (0.630)	12,70 (0.500)
MO-047AD	52	4,19 (0.165)	5,08 (0.200)	2,29 (0.090)	3,30 (0.130)	19,94 (0.785)	20,19 (0.795)	19,05 (0.750)	19,20 (0.756)	17,53 (0.690)	18,54 (0.730)	15,24 (0.600)
MO-047AE	68	4,19 (0.165)	5,08 (0.200)	2,29 (0.090)	3,30 (0.130)	25,02 (0.985)	25,27 (0.995)	24,13 (0.950)	24,33 (0.958)	22,61 (0.890)	23,62 (0.930)	20,32 (0.800)
MO-047AF	84	4,19 (0.165)	5,08 (0.200)	2,29 (0.090)	3,30 (0.130)	30,10 (1.185)	30,35 (1.195)	29,21 (1.150)	29,41 (1.141)	27,69 (1.090)	28,70 (1.130)	25,40 (1.000)

NOTES A: All dimensions conform to JEDEC Specification MO-047AA/AF. Dimensions and tolerancing are per ANSI Y14.5M – 1982.

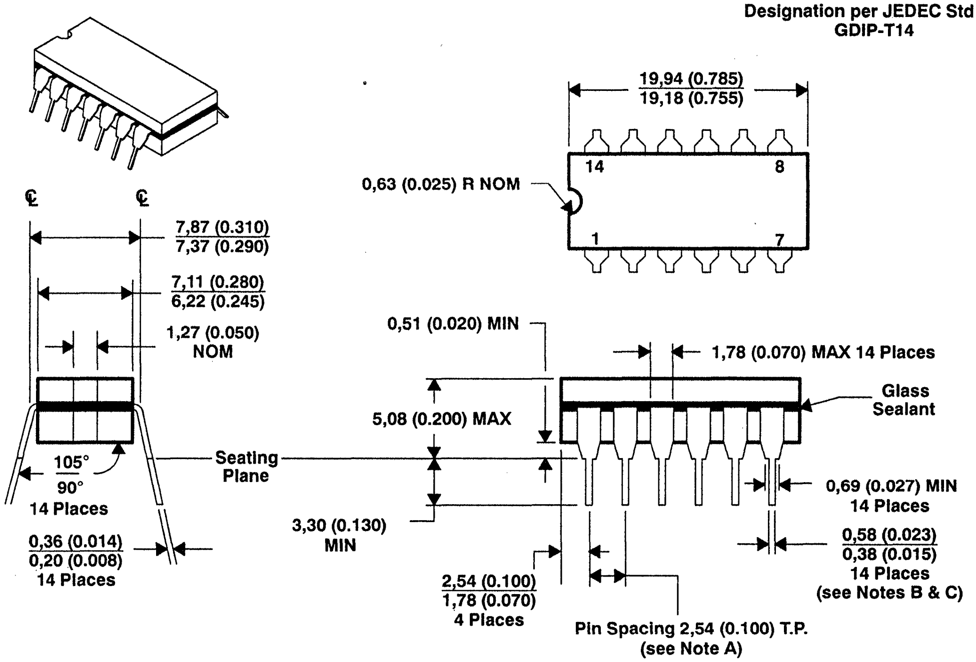
F: Determined at seating plane $\boxed{-C-}$.

J014
ceramic dual-in-line package

This hermetically sealed dual-in-line package consists of a ceramic base, ceramic cap, and lead frame. Hermetic sealing is accomplished with glass. The package is intended for insertion in mounting hole rows on 7,62 (0.300) centers. Once the leads are compressed and inserted, sufficient tension is provided to secure the package in the board during soldering. Tin-plated ("bright-dipped") leads require no additional cleaning or processing when used in soldered assembly.

J014

Designation per JEDEC Std 30:
GDIP-T14



Falls within JEDEC TO–116 and EIA MO–001AA dimensions

ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

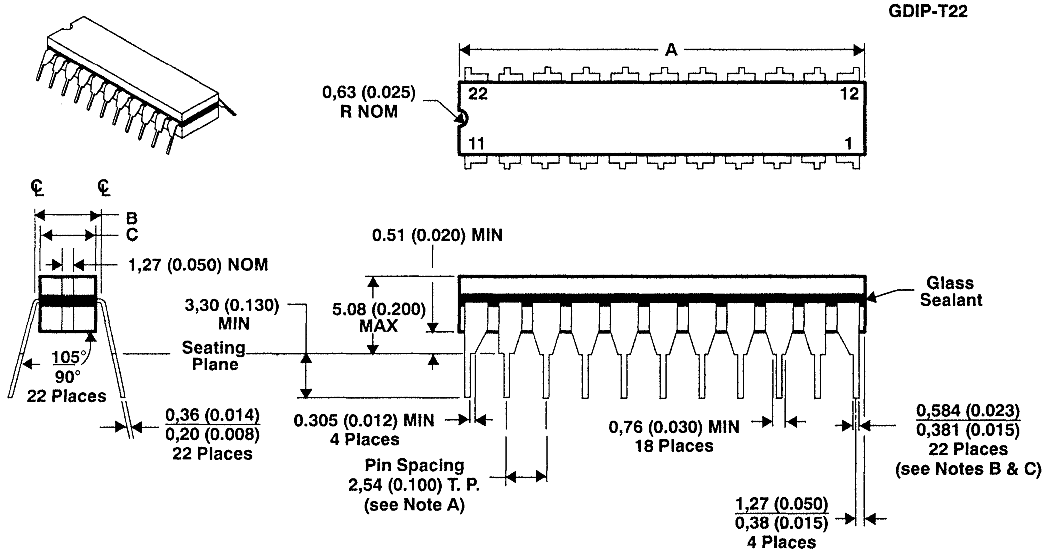
NOTES: A. Each pin centerline is located within 0,25 (0.010) of its true longitudinal position.
B. This dimension does not apply for solder-dipped leads.
C. When solder-dipped leads are specified, dipped area of the lead extends from the lead tip to at least 0,51 (0.020) above seating plane.

J016, J018, J020, and J022 ceramic dual-in-line

These hermetically sealed dual-in-line packages consist of a ceramic base, ceramic cap, and a lead frame. Hermetic sealing is accomplished with glass. These packages are intended for insertion in mounting-hole rows of 7,62 (0.300) centers for the J016, J018, J020, and 10,16 (0.400) centers for the J022, respectively. Once the leads are compressed and inserted, sufficient tension is provided to secure the package in the board during soldering. Tin-plated (bright-dipped) leads require no additional cleaning or processing when used in solder assembly.

J016, J018, J020, and J022
(22-pin package used for illustration)

Designation per JEDEC Std 30:
GDIP-T16
GDIP-T18
GDIP-T20
GDIP-T22



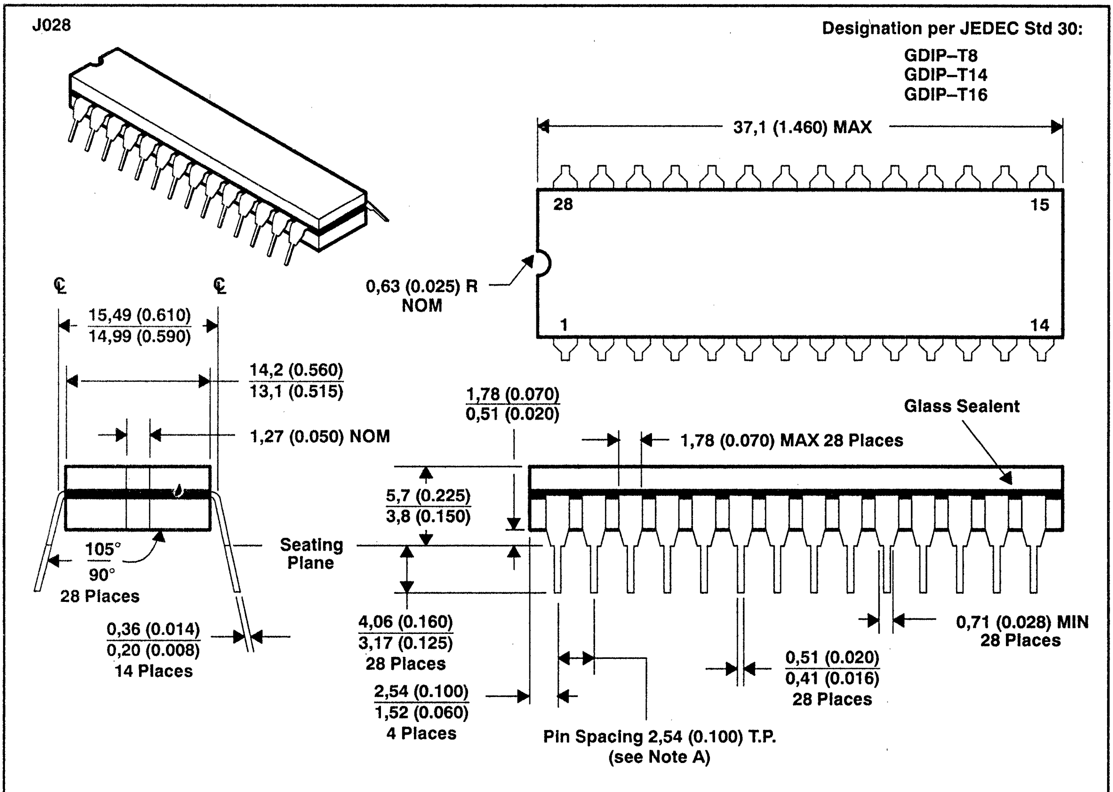
ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

DIM / PINS	A		B		C	
	MIN	MAX	MIN	MAX	MIN	MAX
16	19,18 (0.755)	19,94 (0.785)	7,37 (0.290)	7,87 (0.310)	6,22 (0.245)	7,62 (0.300)
18		23,1 (0.910)	7,37 (0.290)	7,87 (0.310)	6,22 (0.245)	7,62 (0.300)
20	23,62 (0.930)	24,76 (0.975)	7,37 (0.290)	7,87 (0.310)	6,22 (0.245)	7,62 (0.300)
22		28,0 (1.100)	9,91 (0.390)	10,41 (0.410)		9,65 (0.388)

NOTES: A. Each pin centerline is located within 0,25 (0.010) of its true longitudinal position.
B. This dimension does not apply for solder-dipped leads.
C. When solder-dipped leads are specified, dipped area of the lead extends from the lead tip to at least 0,51 (0.020) above the seating plane.

J028
ceramic dual-in-line package

This hermetically sealed dual-in-line package consists of a ceramic base, ceramic cap, and lead frame. Hermetic sealing is accomplished with glass. The package is intended for insertion in mounting hole rows on 15,24 (0.600) centers. Once the leads are compressed and inserted, sufficient tension is provided to secure the package in the board during soldering. Tin-plated ("bright-dipped") leads require no additional cleaning or processing when used in soldered assembly.



ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

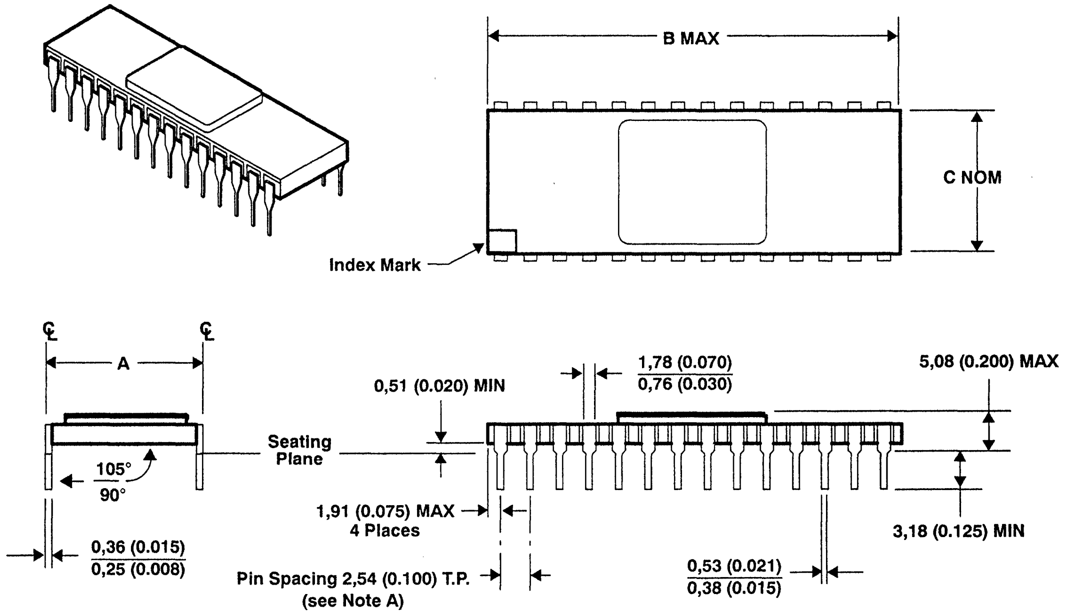
NOTES: D. Each pin centerline is located within 0,25 (0.010) of its true longitudinal position.
E. This dimension does not apply for solder-dipped leads.
F. When solder-dipped leads are specified, dipped area of the lead extends from the lead tip to at least 0,51 (0.020) above seating plane.

JD024 and JD028
ceramic side-braze dual-in-line packages

These hermetically sealed dual-in-line packages consist of a ceramic base, metal cap, and side-brazed tin-plated leads. These packages are intended for insertion in mounting-hole rows of 15,24 (0.600) centers. Leads require no additional cleaning or processing when used in solder assembly.

JD024 and JD028
(28-pin package used for illustration)

Designation per JEDEC Std 30:
GDIP–T24
GDIP–T28



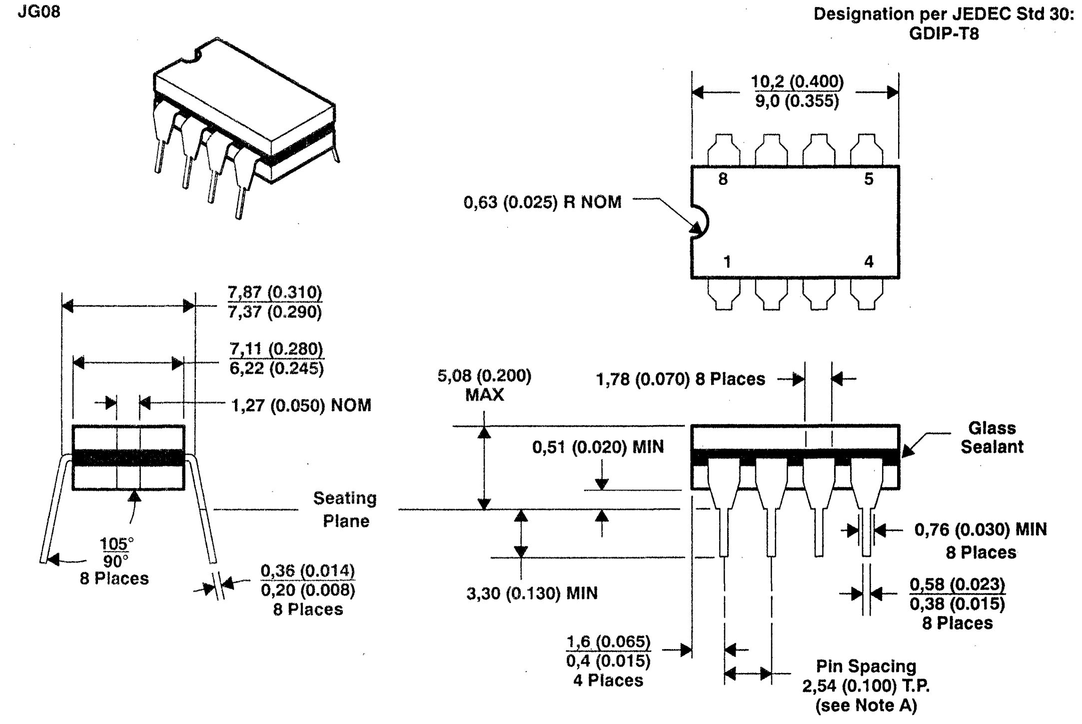
PINS / DIM	24	28
A +0,51 (+0.020) −0,25 (−0.010)	15,24 (0.600)	15,24 (0.600)
B (MAX)	31,8 (1.250)	36,8 (1.450)
C (NOM)	15,0 (0.590)	15,0 (0.590)

ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

NOTE A: Each pin centerline is located within 0,25 (0.010) of its true longitudinal position.

JG008
ceramic dual-in-line package

This hermetically sealed dual-in-line package consists of a ceramic base, ceramic cap, and lead frame. Hermetic sealing is accomplished with glass. The package is intended for insertion in mounting hole rows on 7,62 (0.300) centers. Once the leads are compressed and inserted, sufficient tension is provided to secure the package in the board during soldering. Tin-plated ("bright-dipped") leads require no additional cleaning or processing when used in soldered assembly.



ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

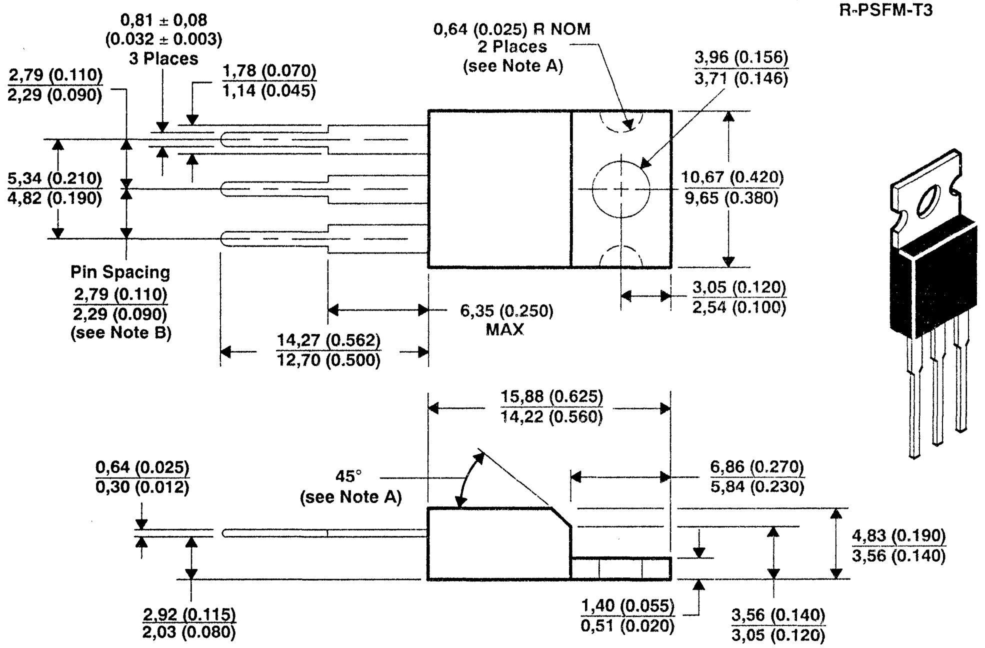
NOTE A: Each pin centerline is located within 0,25 (0.010) of its true longitudinal position.

KC003
plastic flange-mount package

This package consists of a circuit mounted on a lead frame and encapsulated within a plastic compound. The compound will withstand soldering temperature with no deformation, and circuit performance characteristics will remain stable when the package is operated under high-humidity conditions.

KC003

Designation per JEDEC Std 30:
R-PSFM-T3



The center terminal is in electrical contact with the mounting tab.
Falls within JEDEC TO-220AB dimensions

ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

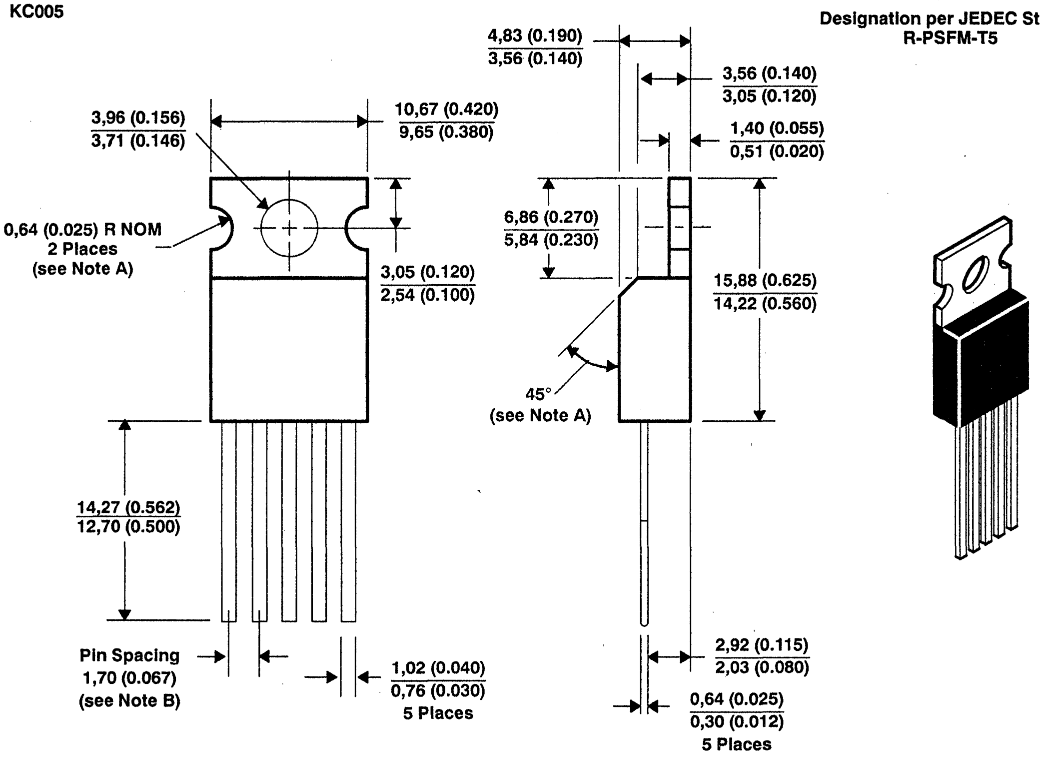
NOTES: A. Notches and/or mold chamfer may or may not be present.
B. Leads are within 0,13 (0.005) radius of true position (T.P.) at maximum material conditions.

KC005
plastic flange-mount package

This package consists of a circuit mounted on a lead frame and encapsulated within a plastic compound. The compound will withstand soldering temperature with no deformation, and circuit performance characteristics will remain stable when the package is operated under high-humidity conditions.

KC005

Designation per JEDEC Std 30:
R-PSFM-T5



ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

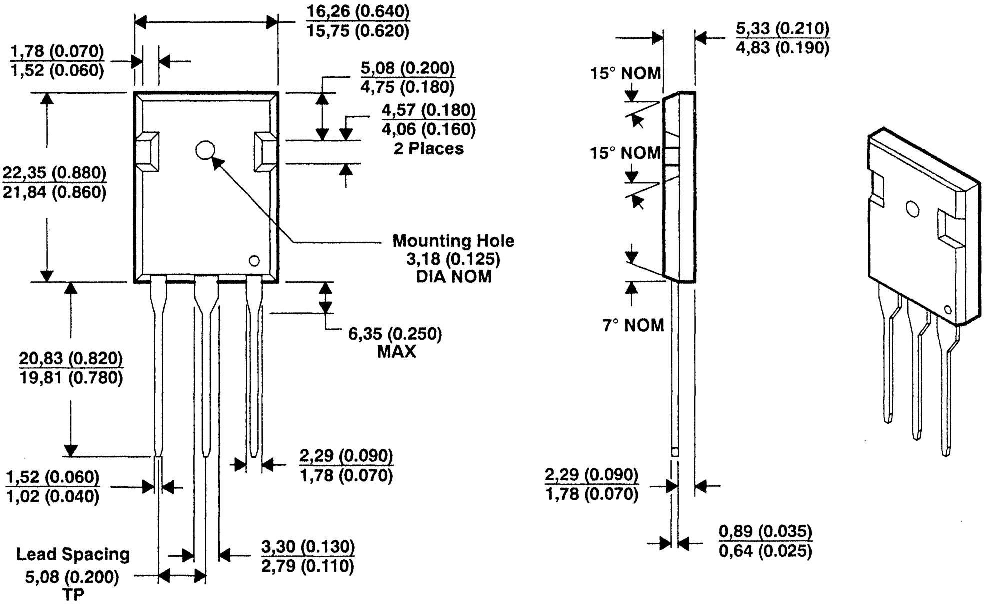
NOTES: A. Notches and chamfer may or may not be present.
B. Leads are with 0,13 (0.005) radius of true position (T.P.) at maximum material conditions.

KK003
plastic flange-mount package

This package consists of a circuit mounted on a lead frame and encapsulated within a plastic compound. The compound will withstand soldering temperature with no deformation, and circuit performance characteristics will remain stable when the package is operated under high-humidity conditions.

KK003

Designation per JEDEC Std 30:
X-PSFM-T3



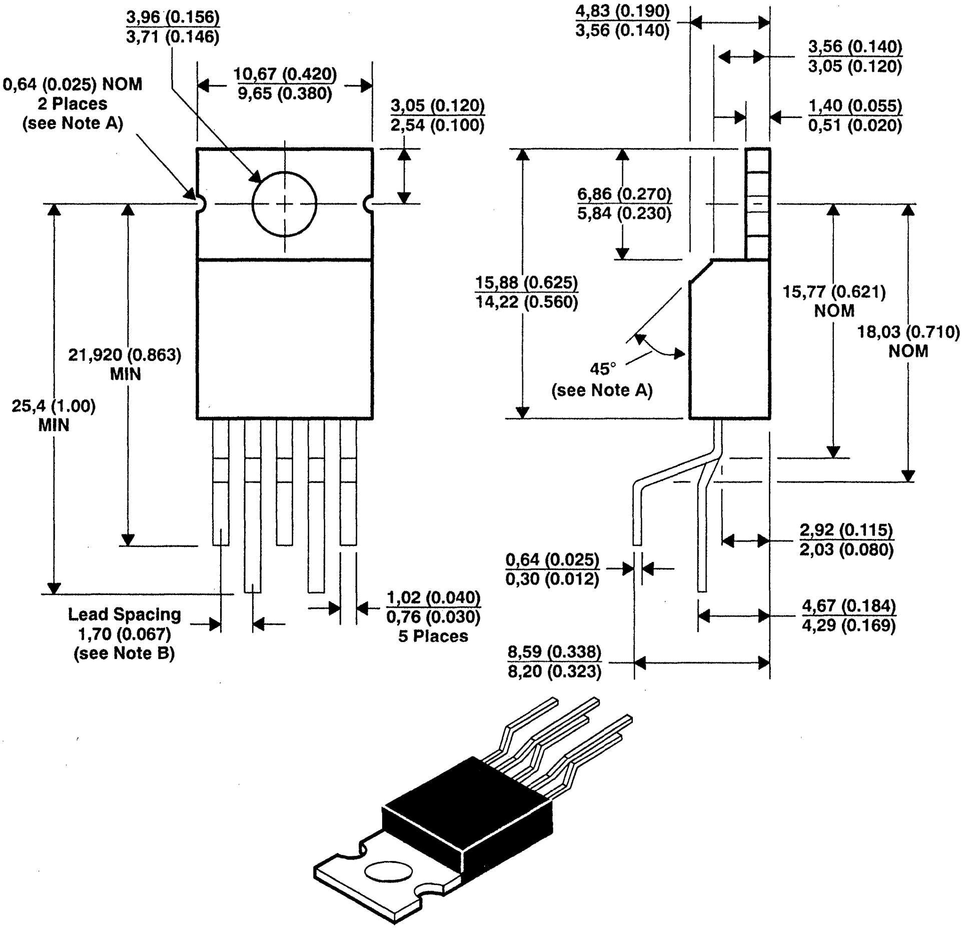
ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

KV005
plastic flange-mount package

This package consists of a circuit mounted on a lead frame and encapsulated within a plastic compound. The compound will withstand soldering temperature with no deformation, and circuit performance characteristics will remain stable when the package is operated under high-humidity conditions.

KV005

Designation per JEDEC Std 30:
R-PSFM-T5



ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

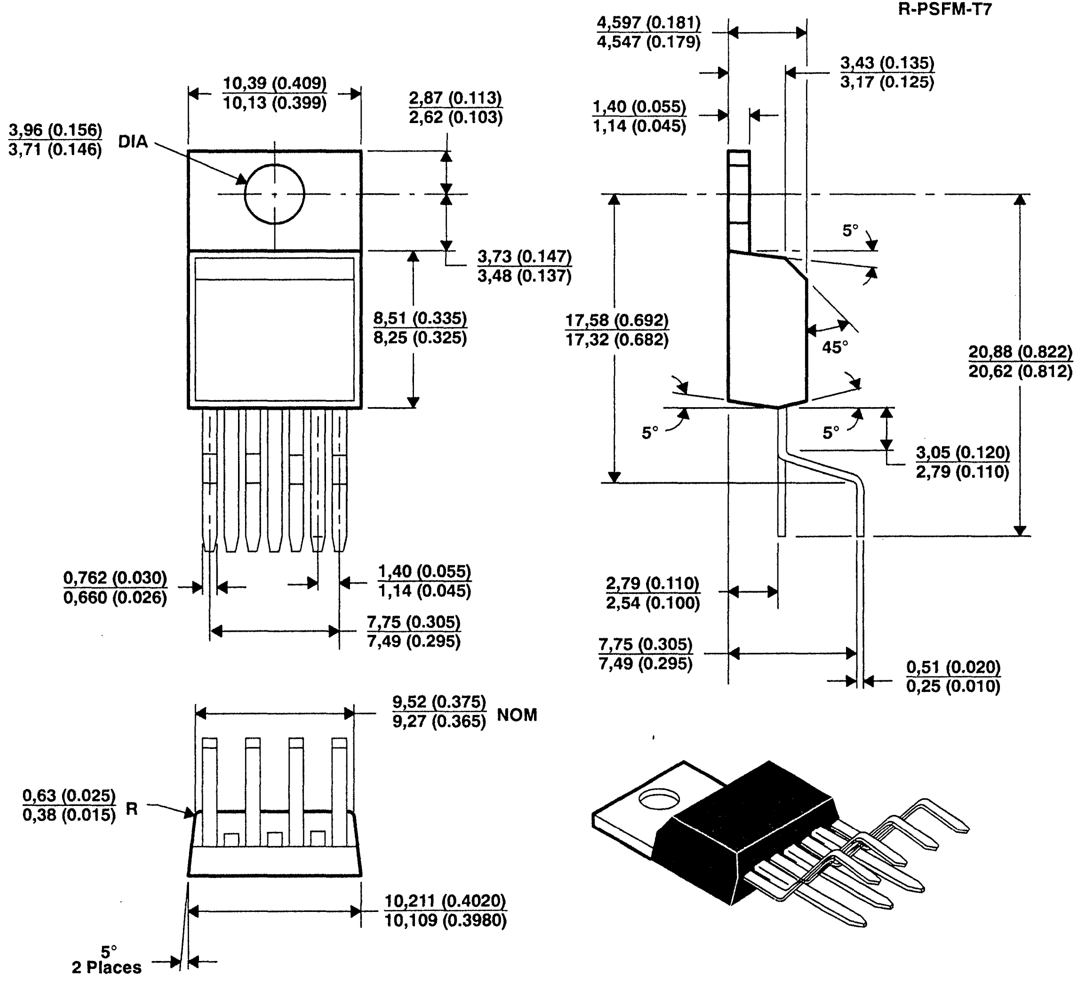
NOTES: A. Notches and chamfer may or may not be present.
B. Leads are with 0,13 (0.005) radius of true position (T.P.) at maximum material conditions.

KV007 plastic flange-mount package

This package consists of a circuit mounted on a lead frame and encapsulated within a plastic compound. The compound will withstand soldering temperature with no deformation, and circuit performance characteristics will remain stable when the package is operated under high-humidity conditions.

KV007

Designation per JEDEC Std 30:
R-PSFM-T7



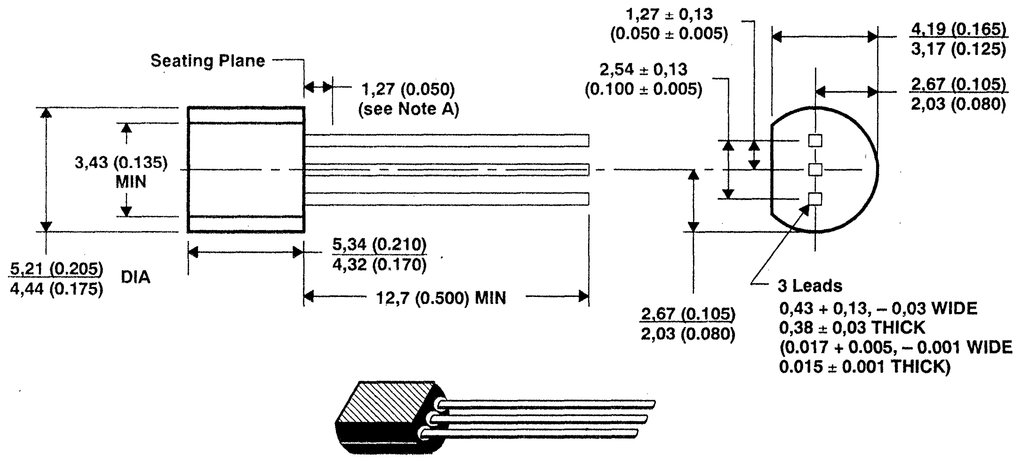
ALL LINEAR DIMENSIONS ARE IN MILLILMETERS AND PARENTHETICALLY IN INCHES.

LP003
plastic cylindrical package

This package consists of a circuit mounted on a lead frame and encapsulated within a plastic compound. The compound will withstand soldering temperature with no deformation and circuit performance characteristics remain stable when operated in high-humidity conditions. Leads require no additional cleaning or processing when used in soldered assembly.

LP003

Designation per JEDEC Std 30:
PBCY-W3



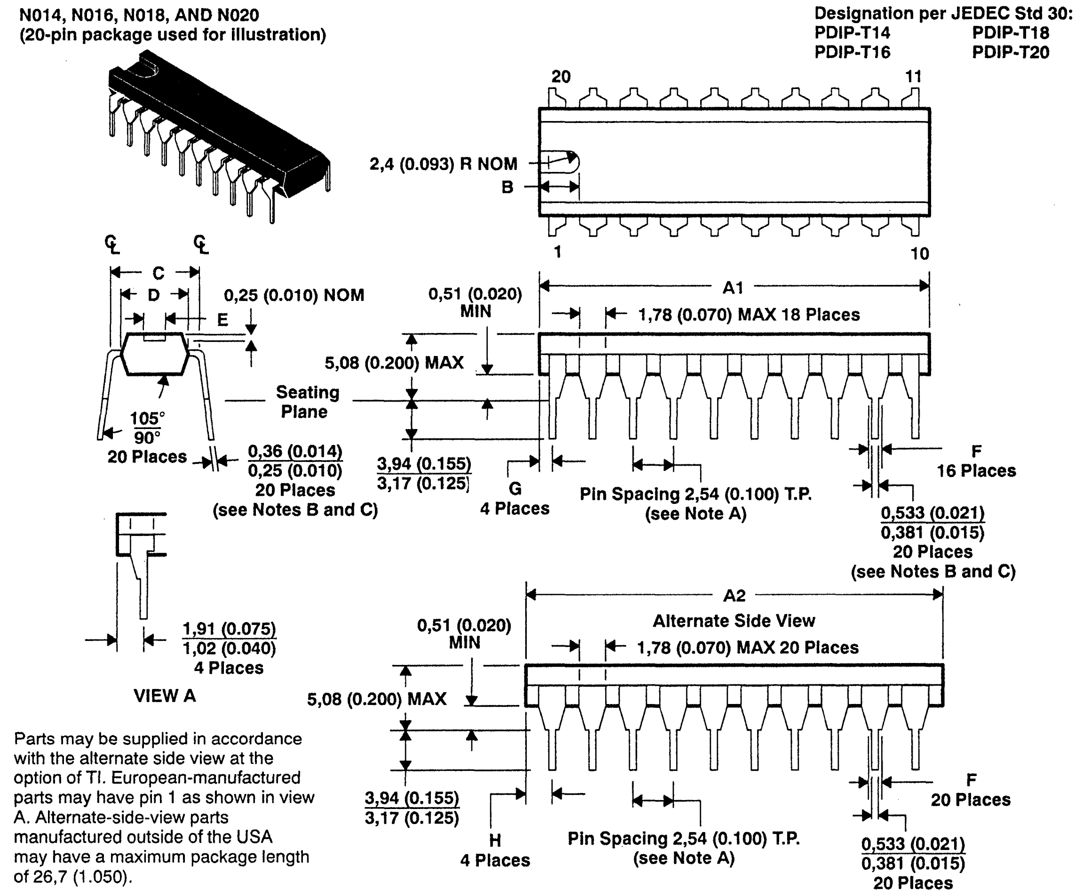
Falls within JEDEC TO-226AA dimensions
(TO-226AA replaces TO-92)

ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

NOTE A: Lead dimensions are not controlled within this area.

N014, N016, N018, and N020
300-mil plastic dual-in-line packages

These dual-in-line packages consist of a circuit mounted on a lead frame and encapsulated within a plastic compound. The compound will withstand soldering temperature with no deformation and circuit performance characteristics will remain stable when operated in high-humidity conditions. These packages are intended for insertion in mounting-hole rows on 7,62 (0.300) centers. Once the leads are compressed and inserted, sufficient tension is provided to secure the package in the board during soldering. Leads require no additional cleaning or processing when used in soldered assembly.



Parts may be supplied in accordance with the alternate side view at the option of TI. European-manufactured parts may have pin 1 as shown in view A. Alternate-side-view parts manufactured outside of the USA may have a maximum package length of 26,7 (1.050).

ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

NOTES: A. Each pin centerline is located within 0,25 (0.010) of its true longitudinal position.
B. This dimension does not apply for solder-dipped leads.
C. When solder-dipped leads are specified, dipped area of the lead extends from the lead tip to at least 0,51 (0.020) above seating plane.

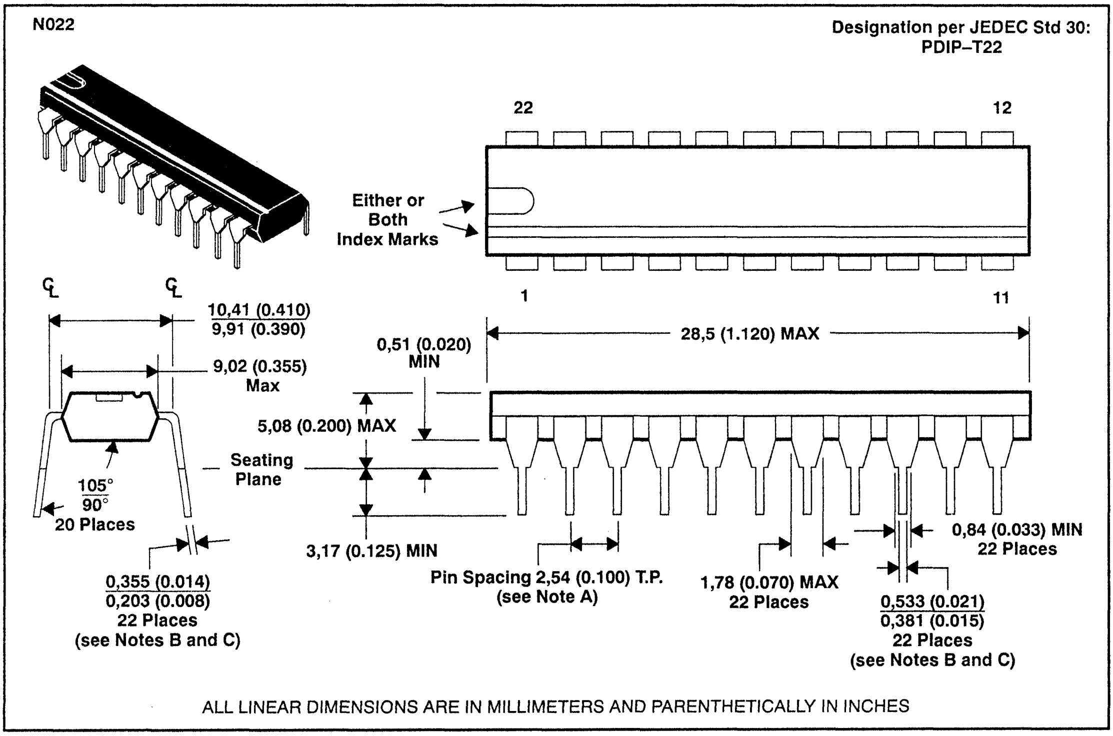
N014, N016, N018, and N020
300-mil plastic dual-in-line package (continued)

PIN DIM		14	16	18	20
A1	MIN	18,0 (0.710)			23,22 (0.914)
	MAX	19,8 (0.780)	19,8 (0.780)	23,4 (0.920)	24,77 (0.975)
A2	MIN	18,0 (0.710)			23,62 (0.930)
	MAX	19,8 (0.780)			25,4 (1.000)
B	NOM	2,8 (0.110)	2,8 (0.110)	4,06 (0.160)	2,80 (0.110)
C	MIN	7,37 (0.290)	7,37 (0.290)	7,37 (0.290)	7,37 (0.290)
	MAX	7,87 (0.310)	7,87 (0.310)	7,87 (0.310)	7,87 (0.310)
D	MIN	6,10 (0.240)	6,10 (0.240)		6,60 (0.240)
	MAX	6,60 (0.260)	6,60 (0.260)	6,99 (0.275)	7,11 (0.280)
E	NOM	2,0 (0.080)	2,0 (0.080)	2,03 (0.080)	2,0 (0.080)
F	MIN	0,84 (0.033)	0,84 (0.033)	0,89 (0.035)	0,84 (0.033)
G	MIN	(see Note A)	0,38 (0.015)	(See Note A)	1,68 (0.066)
	MAX	(see Note A)	1,65 (0.065)	(see Note A)	0,22 (0.009)
H	MIN	2,54 (0.100)	1,02 (0.040)	0,23 (0.009)	0,38 (0.015)
	MAX	1,52 (0.060)	2,41 (0.095)	1,91 (0.075)	1,27 (0.050)

NOTES: A. The 14-pin and 18-pin plastic dual-in-line package is only offered with the external pins shaped in their entirety, and do not have alternate side view dimensions.

N022
400-mil plastic dual-in-line package

This dual-in-line package consist of a circuit mounted on a lead frame and encapsulated within a plastic compound. The compound will withstand soldering temperature with no deformation and circuit performance characteristics will remain stable when operated in high-humidity conditions. This package is intended for insertion in mounting-hole rows on 10,16 (0.400) centers . Once the leads are compressed and inserted, sufficient tension is provided to secure the package in the board during soldering. Leads require no additional cleaning or processing when used in soldered assembly.



NOTES: B. Each pin centerline is located within 0,25 (0.010) of its true longitudinal position.

C. This dimension does not apply for solder-dipped leads.

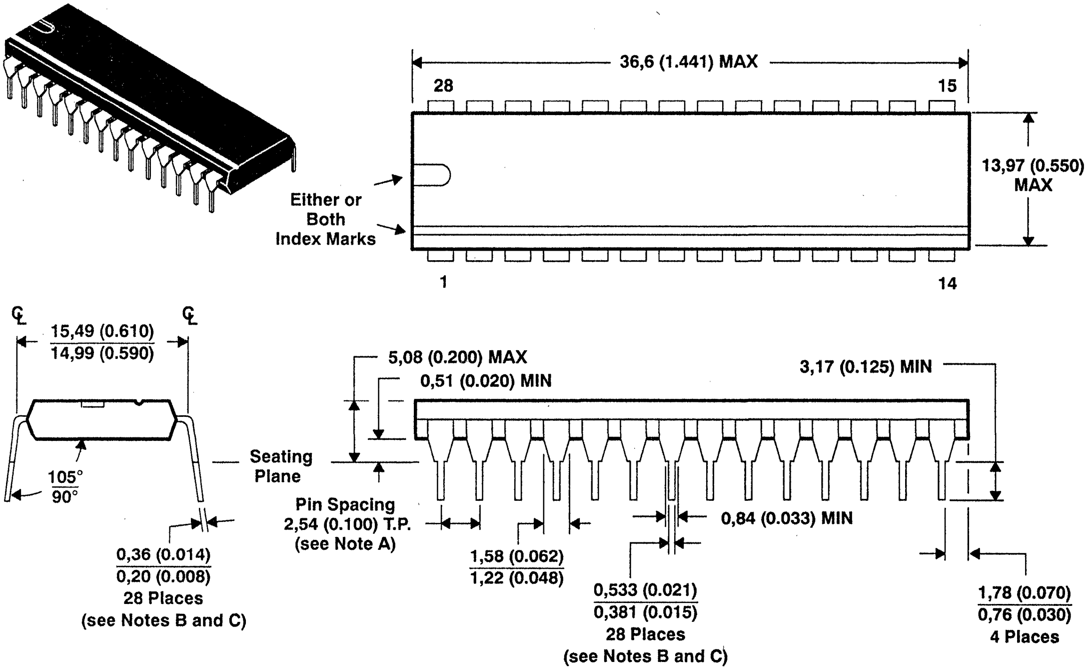
D. When solder-dipped leads are specified, dipped area of the lead extends from the lead tip to at least 0,51 (0.020) above seating plane.

N028
600-mil plastic dual-in-line package

This dual-in-line package consists of a circuit mounted on a lead frame and encapsulated within a plastic compound. The compound will withstand soldering temperature with no deformation and circuit performance characteristics will remain stable when operated in high-humidity conditions. This package is intended for insertion in mounting-hole rows on 15,24 (0.600) centers (see Note A). Once the leads are compressed and inserted, sufficient tension is provided to secure the package in the board during soldering. Leads require no additional cleaning or processing when used in soldered assembly.

N028

Designation per JEDEC Std 30:
PDIP-T28



ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

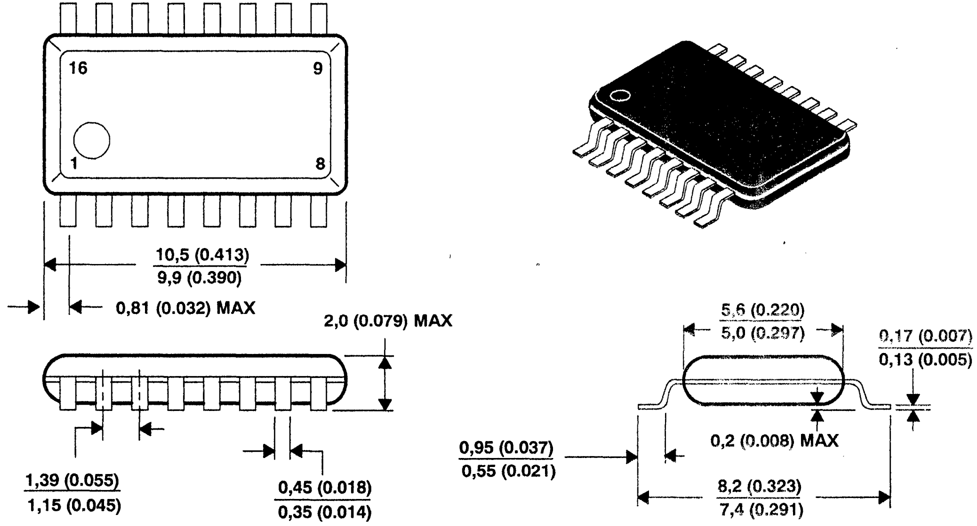
NOTES: A. Each pin centerline is located within 0,25 (0.010) of its true longitudinal position.
B. This dimension does not apply for solder-dipped leads.
C. When solder-dipped leads are specified, dipped area of the lead extends from the lead tip to at least 0,51 (0.020) above seating plane.

NS016
plastic package

This package consists of a circuit mounted on a lead frame and encapsulated within a plastic compound. The compound withstands soldering temperature with no deformation, and circuit performance characteristics remain stable when operated in high-humidity conditions. Leads require no additional cleaning or processing when used in soldered assembly.

NS016

Designation per JEDEC Std 30:
PDSO-G16



ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

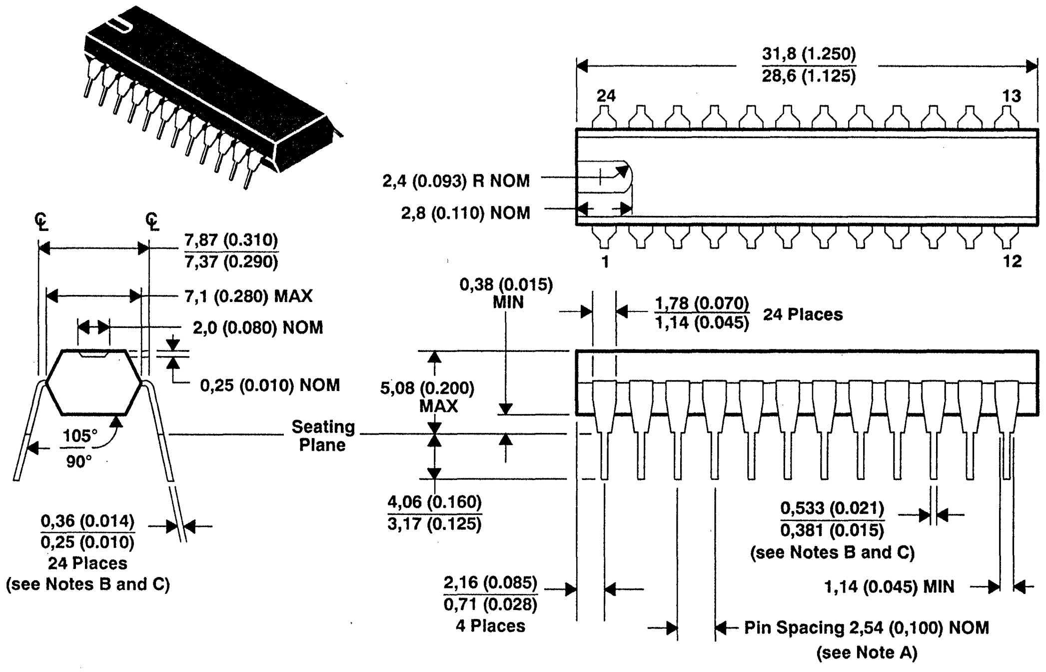
NT024
300-mil plastic dual-in-line packages

This package consists of a circuit mounted on a lead frame and encapsulated within a plastic compound. The compound will withstand soldering temperature with no deformation and circuit performance characteristics will remain stable when operated in high-humidity conditions. This package is intended for insertion in mounting-hole rows on 7,62 (0.300) centers . Once the leads are compressed and inserted, sufficient tension is provided to secure the package in the board during soldering. Leads require no additional cleaning or processing when used in soldered assembly.

NOTE: For all except 24-pin package, the letter N is used by itself since the 24-pin package may be available in more than one row-spacing. For the 24-pin package, the 7,62 (0.300) version is designated NT; the 15,24 (0.600) version is designated NW. If no second letter or row-spacing is specified, the package is assumed to have 15,24 (0.600) row-spacing.

NT024

Designation per JEDEC Std 30:
PDIP-T24



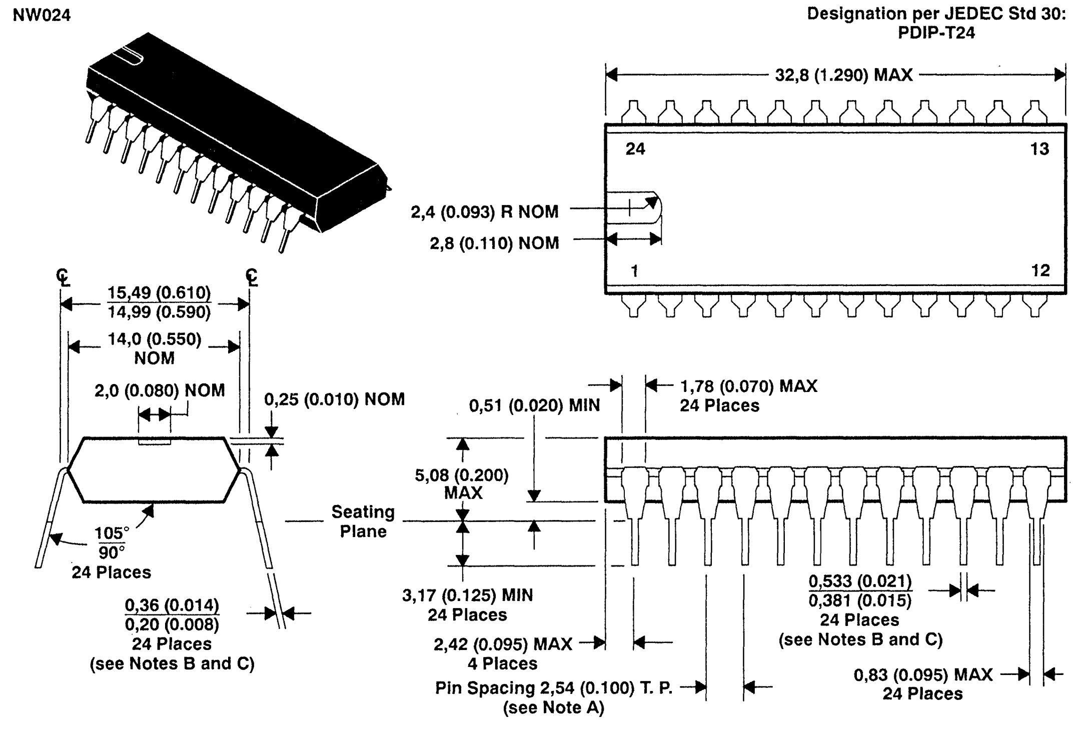
ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

NOTES: A. Each pin centerline is located within 0,25 (0.010) of its true longitudinal position.
B. This dimension does not apply for solder-dipped leads.
C. When solder-dipped leads are specified, dipped area of the lead extends from the lead tip to at least 0,51 (0.020) above seating plane.

NW024
600-mil plastic dual-in-line package

This dual-in-line package consist of a circuit mounted on a lead frame and encapsulated within a plastic compound. The compound will withstand soldering temperature with no deformation and circuit performance characteristics will remain stable when operated in high-humidity conditions. This package is intended for insertion in mounting-hole rows on 15,24 (0.600) centers. Once the leads are compressed and inserted, sufficient tension is provided to secure the package in the board during soldering. Leads require no additional cleaning or processing when used in soldered assembly.

NOTE: For all except 24-pin packages, the letter N is used by itself since only the 24-pin package is available in more than one row-spacing. For the 24-pin package, the 7,62 (0.300) version is designated NT; the 15,24 (0.600) version is designated NW. If no second letter or row-spacing is specified, the package is assumed to have 15,24 (0.600) row-spacing.

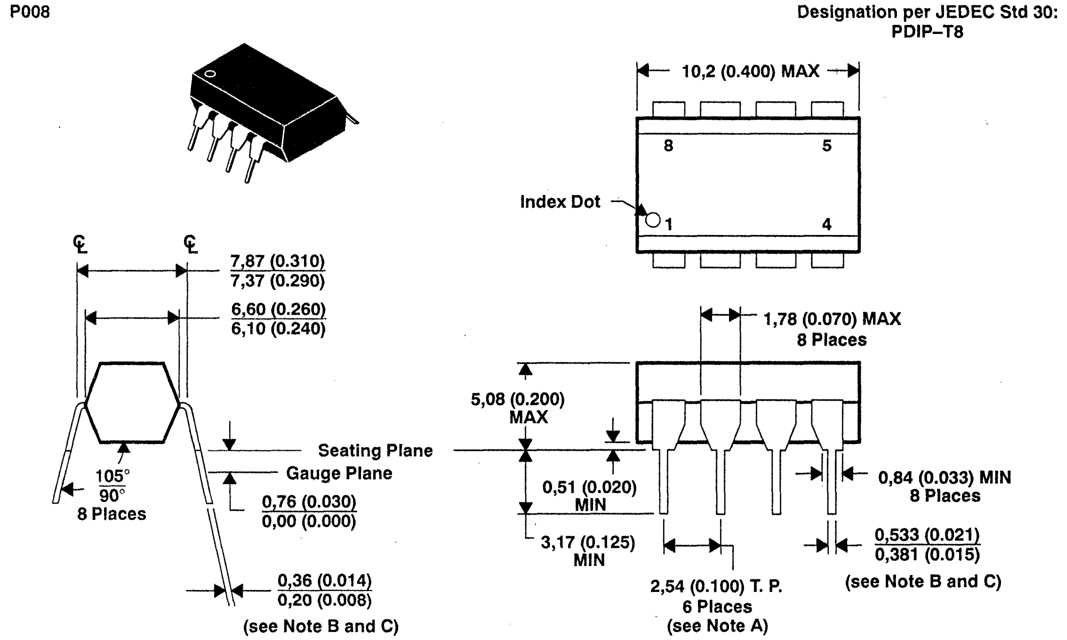


ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

NOTES: A. Each pin centerline is located within 0,25 (0.010) of its true longitudinal position.
B. This dimension does not apply for solder-dipped leads.
C. When solder-dipped leads are specified, dipped area of the lead extends from the lead tip to at least 0,51 (0.020) above seating plane.

P008
plastic dual-in-line package

This package consists of a circuit mounted on an 8-pin lead frame and encapsulated within a plastic compound.The compound will withstand soldering temperature with no deformation, and circuit performance characteristics will remain stable when operated in high-humidity conditions. The package is intended for insertion in mounting-hole rows on 7,62 (0.300) centers. Once the leads are compressed and inserted, sufficient tension is provided to secure the package in the board during soldering. Solder-plated lead require no additional cleaning or processing when used in soldered assembly.



ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

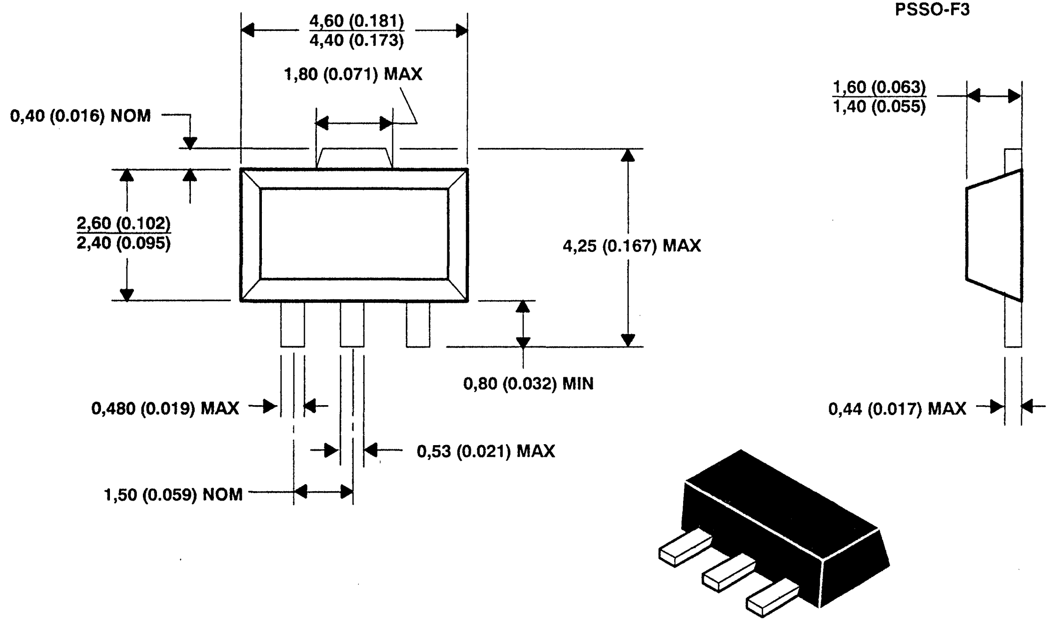
NOTES: A. Each pin centerline is located within 0,25 (0.010) of its true longitudinal position.
B. This dimension does not apply for solder-dipped leads.
C. When solder-dipped leads are specified, dipped area of the lead extends from the lead tip to at least 0,51 (0.020) above seating plane.

PK003
plastic lead-mount package

This package consists of a circuit mounted on a lead frame and encapsulated within a plastic compound. The compound will withstand soldering temperature with no deformation, and circuit performance characteristics will remain stable when operated in high-humidity conditions.

PK003

Designation per JEDEC Std 30:
PSSO-F3

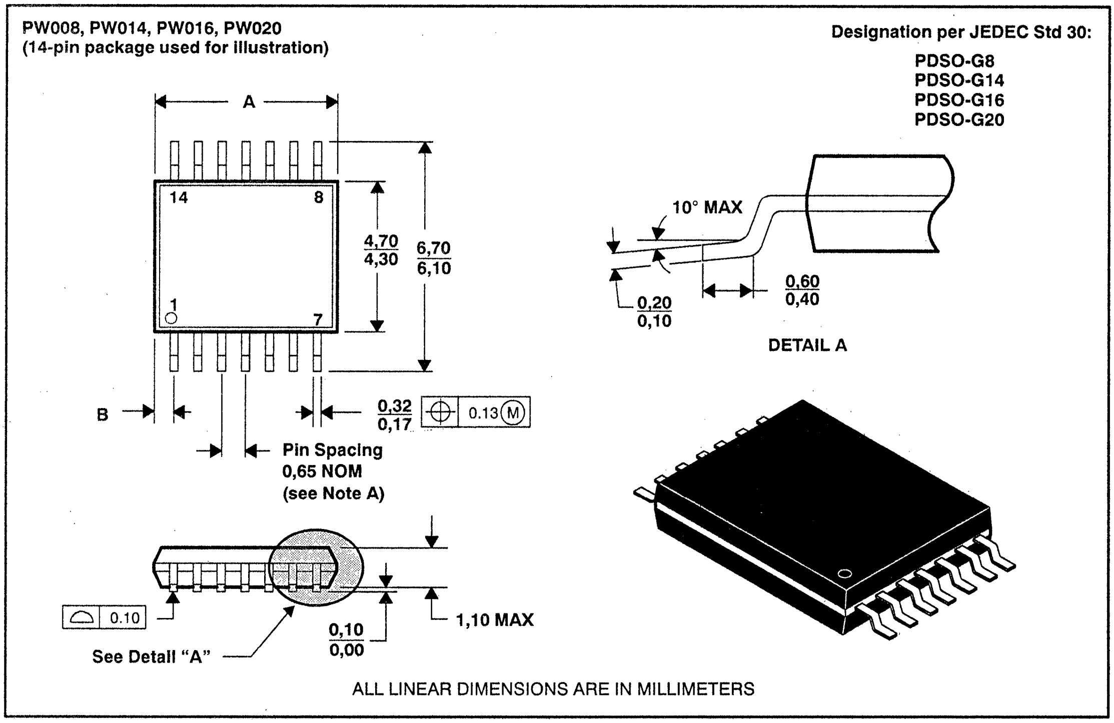


The center lead is in electrical contact with the tab

ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

PW008, PW014, PW016, PW020
shrink small-outline packages

These shrink small-outline packages consist of a circuit mounted on a lead frame and encapsulated within a plastic compound. The compound will withstand soldering temperature with no deformation, and circuit performance characteristics will remain stable when operated in high-humidity conditions. Leads require no additional cleaning or processing when used in soldered assembly.



NOTES: A. Leads are within 0,25 mm radius of true position at maximum material condition.
B. Body dimensions include mold flash or protrusion.
C. Mold flash or protrusion shall not exceed 0,15 mm.
D. Lead tips to be planar within ±0,051 mm exclusive of solder.

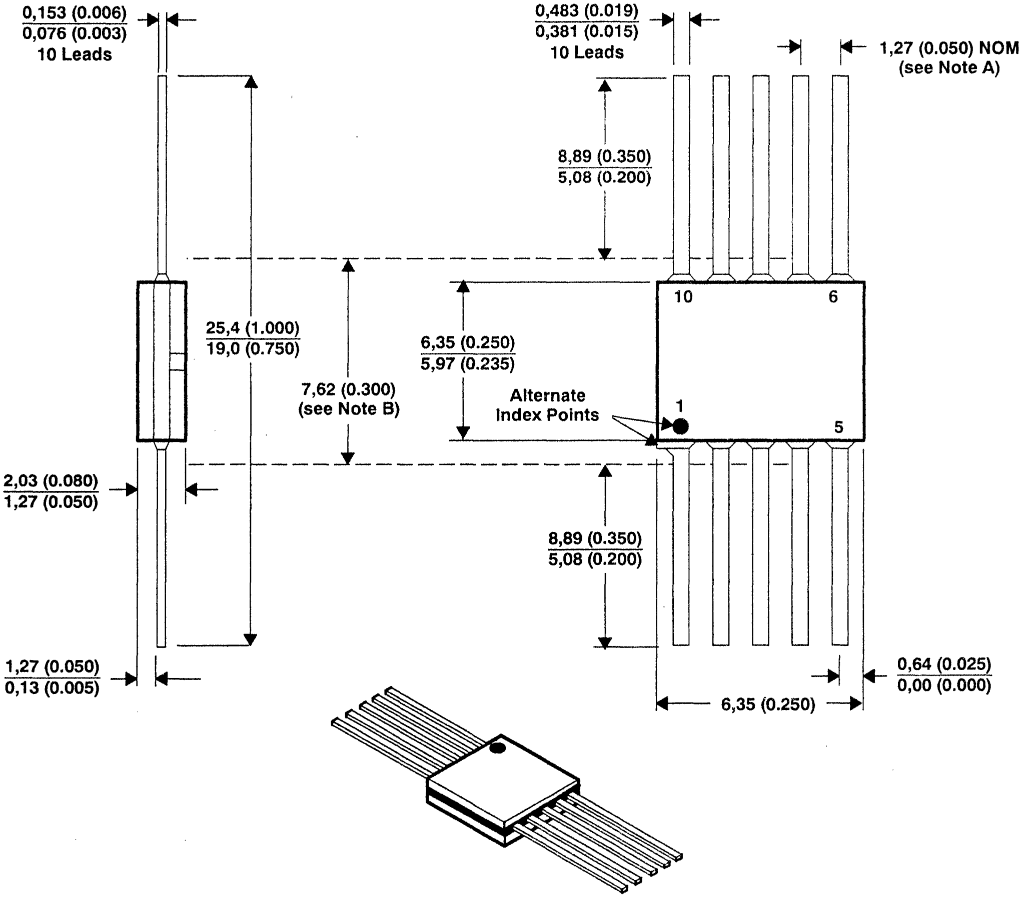
DIM \ PINS	8	14	16	20
A MIN	2,99	4,99	4,99	6,40
A MAX	3,03	5,30	5,30	6,80
B MAX	0,65	0,70	0,38	0,48

U010
ceramic flat package

This flat package consists of a ceramic base, ceramic cap, and lead frame. Circuit bars are alloy mounted. Hermetic sealing is accomplished with glass. Leads require no additional cleaning or processing when used in soldered assembly.

U010

Designation per JEDEC Std 30:
GDFP-F10



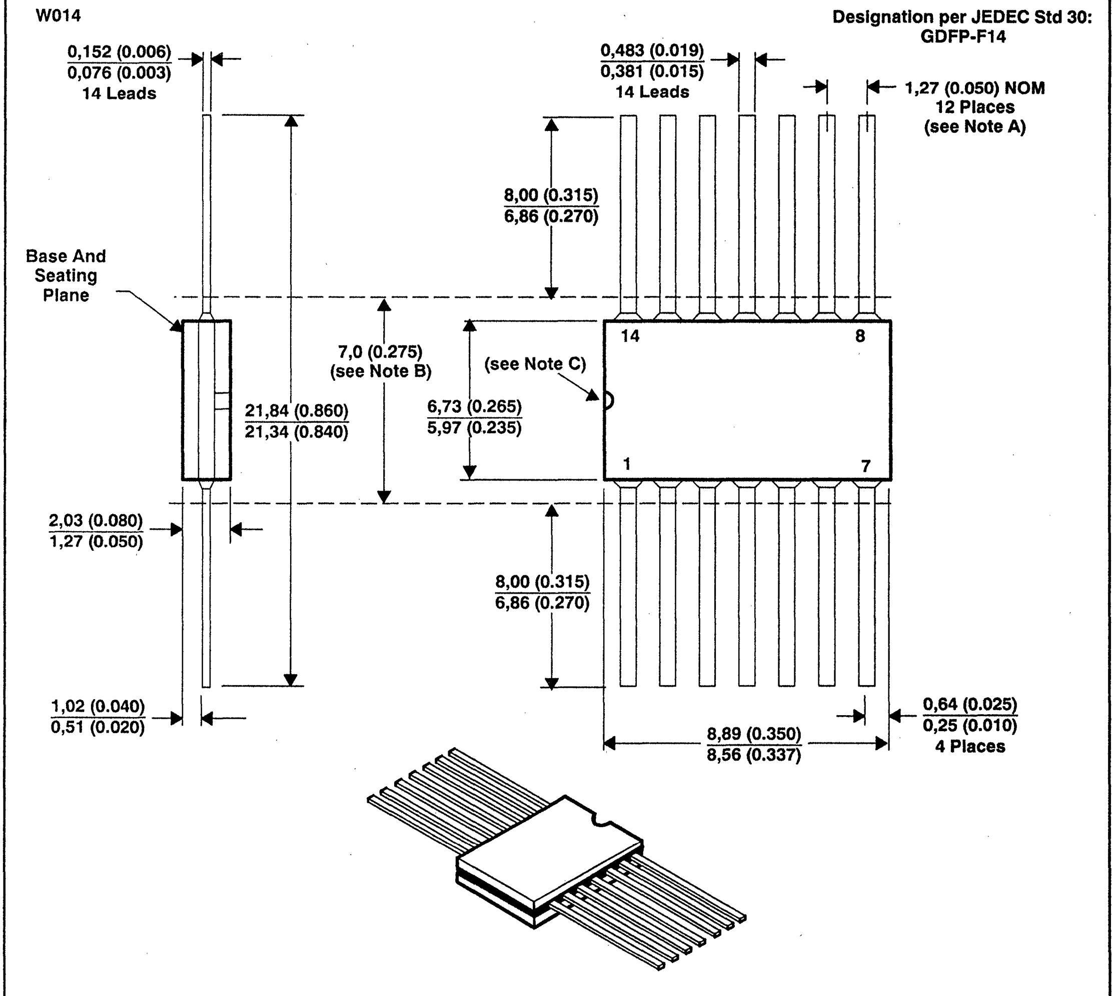
Falls within JEDEC MO-004AA dimensions

ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

NOTES: A. Leads are within 0,13 (0.005) radius of true position (T.P.) at maximum material conditions.
B. This dimension determines a zone within which all body and lead irregularities lie.

W014
ceramic flat package

This hermetically sealed flat package consists of an electrically nonconductive ceramic base and cap and a lead frame. Hermetic sealing is accomplished with glass. Leads require no additional cleaning or processing when used in soldered assembly.



Fall within JEDEC MO-004AA dimensions

ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

NOTES: A. Leads are within 0,13 (0.005) radius of true position (T.P.) at maximum material condition.
B. This dimension determines a zone within which all body and lead irregularities lie.
C. Index point is provided on cap for terminal identification only.

NOTES

NOTES

NOTES

NOTES

TI North American Sales Offices

ALABAMA: Huntsville: (205) 837-7530

ARIZONA: Phoenix: (602) 995-1007

CALIFORNIA: Irvine: (714) 660-1200
Roseville: (916) 786-9206
San Diego: (619) 278-9600
Santa Clara: (408) 980-9000
Woodland Hills: (818) 704-8100

COLORADO: Aurora: (303) 368-8000

CONNECTICUT: Wallingford: (203) 269-0074

FLORIDA: Altamonte Springs: (407) 260-2116
Fort Lauderdale: (305) 973-8502
Tampa: (813) 882-0017

GEORGIA: Norcross: (404) 662-7900

ILLINOIS: Arlington Heights: (708) 640-3000

INDIANA: Carmel: (317) 573-6400
Fort Wayne: (219) 482-3311

IOWA: Cedar Rapids: (319) 395-9550

KANSAS: Overland Park: (913) 451-4511

MARYLAND: Columbia: (301) 964-2003

MASSACHUSETTS: Waltham: (617) 895-9100

MICHIGAN: Farmington Hills: (313) 553-1500

MINNESOTA: Eden Prairie: (612) 828-9300

MISSOURI: St. Louis: (314) 821-8400

NEW JERSEY: Iselin: (908) 750-1050

NEW MEXICO: Albuquerque: (505) 345-2555

NEW YORK: East Syracuse: (315) 463-9291
Fishkill: (914) 897-2900
Melville: (516) 454-6600
Pittsford: (716) 385-6770

NORTH CAROLINA: Charlotte: (704) 527-0930
Raleigh: (919) 876-2725

OHIO: Beachwood: (216) 464-6100
Beavercreek: (513) 427-6200

OREGON: Beaverton: (503) 643-6758

PENNSYLVANIA: Blue Bell: (215) 825-9500

PUERTO RICO: Hato Rey: (809) 753-8700

TEXAS: Austin: (512) 250-6769
Dallas: (214) 917-1264
Houston: (713) 778-6592

UTAH: Salt Lake City: (801) 466-8973

WASHINGTON: Redmond: (206) 881-3080

WISCONSIN: Waukesha: (414) 798-1001

CANADA: Nepean: (613) 726-1970
Richmond Hill: (416) 884-9181
St. Laurent: (514) 335-8392

TI Regional Technology Centers

CALIFORNIA: Irvine: (714) 660-8140
Santa Clara: (408) 748-2220

GEORGIA: Norcross: (404) 662-7950

ILLINOIS: Arlington Heights: (708) 640-2909

INDIANA: Indianapolis: (317) 573-6400

MASSACHUSETTS: Waltham: (617) 895-9196

MEXICO: Mexico City: 491-70834

MINNESOTA: Minneapolis: (612) 828-9300

TEXAS: Dallas: (214) 917-3881

CANADA: Nepean: (613) 726-1970

Customer Response Center

TOLL-FREE: (800) 336-5236

OUTSIDE UNITED STATES:
(214) 995-6611
(8:00 a.m.-5:00 p.m. CST)

TI Authorized North American Distributors

- Alliance Electronics, Inc. (military product only)
- Almac Electronics
- Anthem Electronics
- Arrow (Canada)
- Arrow/Kierulff Electronics Group
- Future Electronics (Canada)
- GRS Electronics Co., Inc.
- Hall-Mark Electronics
- Lex Electronics
- Marshall Industries
- Newark Electronics
- Rochester Electronics, Inc. (obsolete product only (508) 462-9332)
- Wyle Laboratories
- Zeus Components

TI Distributors

ALABAMA: Arrow/Kierulff (205) 837-6955; Hall-Mark (205) 837-8700; Marshall (205) 881-9235; Lex (205) 895-0480.

ARIZONA: Anthem (602) 966-6600; Arrow/Kierulff (602) 437-0750; Hall-Mark (602) 437-1200; Marshall (602) 496-0290; Lex (602) 431-0030; Wyle (602) 437-2088.

CALIFORNIA: Los Angeles/Orange County: Anthem (818) 775-1333, (714) 768-4444; Arrow/Kierulff (818) 701-7500, (714) 838-5422; Hall-Mark (818) 773-4500, (714) 727-6000; Marshall (818) 878-7000, (714) 458-5301; Lex (818) 880-9686, (714) 587-0404; Wyle (818) 880-9000, (714) 863-9953; Zeus (714) 921-9000, (818) 889-3838;

Rucklin: (916) 624-9744;

Sacramento: Hall-Mark (916) 624-9781; Marshall (916) 635-9700; Lex (916) 364-0230; Wyle (916) 638-5282;

San Diego: Anthem (619) 453-9005; Arrow/Kierulff (619) 565-4800; Hall-Mark (619) 268-1201; Marshall (619) 578-9600; Lex (619) 495-0015; Wyle (619) 565-9171; Zeus (619) 277-9681;

San Francisco Bay Area: Anthem (408) 453-1200; Arrow/Kierulff (408) 441-9700; Hall-Mark (408) 432-4000; Marshall (408) 942-4600; Lex (408) 432-7171; Wyle (408) 727-2500; Zeus (408) 629-4789.

COLORADO: Anthem (303) 790-4500; Arrow/Kierulff (303) 373-5616; Hall-Mark (303) 790-1662; Marshall (303) 451-8383; Lex (303) 799-0258; Wyle (303) 457-9953.

CONNECTICUT: Anthem (203) 575-1575; Arrow/Kierulff (203) 265-7741; Hall-Mark (203) 271-2844; Marshall (203) 265-3822; Lex (203) 264-4700.

FLORIDA: Fort Lauderdale: Arrow/Kierulff (305) 429-8200; Hall-Mark (305) 971-9280; Marshall (305) 977-4880; Lex (305) 421-6633;

Orlando: Arrow/Kierulff (407) 333-9300; Hall-Mark (407) 830-5855; Marshall (407) 767-8585; Lex (407) 331-7555; Zeus (407) 365-3000;

Tampa: Hall-Mark (813) 541-7440; Marshall (813) 573-1399; Lex (813) 541-5100.

GEORGIA: Arrow/Kierulff (404) 497-1300; Hall-Mark (404) 623-4400; Marshall (404) 923-5750; Lex (404) 449-9170.

ILLINOIS: Anthem (708) 884-0200; Arrow/Kierulff (708) 250-0500; Hall-Mark (708) 860-3800; Marshall (708) 490-0155; Newark (312)784-5100; Lex (708) 330-2888.

INDIANA: Arrow/Kierulff (317) 299-2071; Hall-Mark (317) 872-8875; Marshall (317) 297-0483; Lex (317) 843-1050.

IOWA: Arrow/Kierulff (319) 395-7230; Lex (319) 373-1417.

KANSAS: Arrow/Kierulff (913) 541-9542; Hall-Mark (913) 888-4747; Marshall (913) 492-3121; Lex (913) 492-2922.

MARYLAND: Anthem (301) 995-6640; Arrow/Kierulff (301) 995-6002; Hall-Mark (301) 988-9800; Marshall (301) 622-1118; Lex (301) 596-7800; Zeus (301) 997-1118.

MASSACHUSETTS: Anthem (508) 657-5170; Arrow/Kierulff (508) 658-0900; Hall-Mark (508) 667-0902; Marshall (508) 658-0810; Lex (508) 694-9100; Wyle (617) 272-7300; Zeus (617) 246-8200.

MICHIGAN: Detroit: Arrow/Kierulff (313) 462-2290; Hall-Mark (313) 462-1205; Marshall (313) 525-5850; Newark (313) 967-0600; Lex (313) 525-8100;

Grand Rapids: Arrow/Kierulff (616) 243-0912.

MINNESOTA: Anthem (612) 944-5454; Arrow/Kierulff (612) 829-5588; Hall-Mark (612) 941-2600; Marshall (612) 559-2211; Lex (612) 941-5280.

MISSOURI: Arrow/Kierulff (314) 567-6888; Hall-Mark (314) 291-5350; Marshall (314) 291-4650; Lex (314) 739-0526.

NEW JERSEY: Anthem (201) 227-7960; Arrow/Kierulff (201) 538-0900, (609) 596-8000; GRS (609) 964-8560; Hall-Mark (201) 515-3000, (609) 235-1900; Marshall (201) 882-0320, (609) 234-9100; Lex (201) 227-7880, (609) 273-7900.

NEW MEXICO: Alliance (505) 292-3360.

NEW YORK: Long Island: Anthem (516) 864-6600; Arrow/Kierulff (516) 231-1000; Hall-Mark (516) 737-0600; Marshall (516) 273-2424; Lex (516) 231-2500; Zeus (914) 937-7400;

Rochester: Arrow/Kierulff (716) 427-0300; Hall-Mark (716) 425-3300; Marshall (716) 235-7620; Lex (716) 383-8020;

Syracuse: Marshall (607) 785-2345.

NORTH CAROLINA: Arrow/Kierulff (919) 876-3132; Hall-Mark (919) 872-0712; Marshall (919) 878-9882; Lex (919) 876-0000.

OHIO: Cleveland: Arrow/Kierulff (216) 248-3990; Hall-Mark (216) 349-4632; Marshall (216) 248-1788; Lex (216) 464-2970;

Columbus: Hall-Mark (614) 888-3313;

Dayton: Arrow/Kierulff (513) 435-5563; Marshall (513) 898-4480; Lex (513) 439-1800; Zeus (513) 293-6162.

OKLAHOMA: Hall-Mark (918) 254-6110; Lex (918) 622-8000.

OREGON: Almac (503) 629-8090; Anthem (503) 643-1114; Arrow/Kierulff (503) 627-7667; Marshall (503) 644-5050; Wyle (503) 643-7900.

PENNSYLVANIA: Anthem (215) 443-5150; Arrow/Kierulff (215) 928-1800; GRS (215) 922-7037; Marshall (412) 788-0441; Lex (412) 963-6804.

TEXAS: Austin: Arrow/Kierulff (512) 835-4180; Hall-Mark (512) 258-8848; Lex (512) 339-0088; Wyle (512) 345-8853;

Dallas: Anthem (214) 238-7100; Arrow/Kierulff (214) 380-6464; Hall-Mark (214) 553-4300; Marshall (214) 233-5200; Lex (214) 247-6300; Wyle (214) 235-9953; Zeus (214) 783-7010;

Houston: Arrow/Kierulff (713) 530-4700; Hall-Mark (713) 781-6100; Marshall (713) 895-9200; Lex (713) 784-3600; Wyle (713) 879-9953.

UTAH: Anthem (801) 973-8555; Arrow/Kierulff (801) 973-6913; Marshall (801) 485-1551; Wyle (801) 974-9953.

WASHINGTON: Almac (206) 643-9992, (509) 924-9500; Anthem (206) 483-1700; Arrow/Kierulff (206) 643-4800; Marshall (206) 486-5747; Wyle (206) 881-1150.

WISCONSIN: Arrow/Kierulff (414) 792-0150; Hall-Mark (414) 797-7844; Marshall (414) 797-8400; Lex (414) 784-9451.

CANADA: Calgary: Future (403) 235-5325;

Edmonton: Future (403) 438-2858;

Montreal: Arrow Canada (514) 421-7411; Future (514) 694-7710; Marshall (514) 694-8142;

Ottawa: Arrow Canada (613) 226-6903; Future (613) 820-8313; **Quebec City:** Arrow Canada (418) 871-7500;

Toronto: Arrow Canada (416) 670-7769; Future (416) 612-9200; Marshall (416) 458-8046;

Vancouver: Arrow Canada (604) 421-2333; Future (604) 294-1166.

TI Die Processors

Chip Supply	(407) 298-7100
Elmo Semiconductor	(818) 768-7400
Minco Technology Labs	(512) 834-2022

TEXAS
INSTRUMENTS

D0691

TI Worldwide Sales Offices

ALABAMA: Huntsville: 4960 Corporate Drive, Suite N-150, Huntsville, AL 35805-6202, (205) 837-7530.

ARIZONA: Phoenix: 8825 N. 23rd Avenue, Suite 100, Phoenix, AZ 85021, (602) 995-1007.

CALIFORNIA: Irvine: 1920 Main Street, Suite 900, Irvine, CA 92714, (714) 660-1200; **Roseville:** 1 Sierra Gate Plaza, Suite 255B, Roseville, CA 95678, (916) 786-9206; **San Diego:** 5625 Ruffin Road, Suite 100, San Diego, CA 92123, (619) 278-9600; **Santa Clara:** 5353 Betsy Ross Drive, Santa Clara, CA 95054, (408) 980-9000; **Woodland Hills:** 21550 Oxnard Street, Suite 700, Woodland Hills, CA 91367, (818) 704-8100.

COLORADO: Aurora: 1400 S. Potomac Street, Suite 101, Aurora, CO 80012, (303) 368-8000.

CONNECTICUT: Wallingford: 9 Barnes Industrial Park So., Wallingford, CT 06492, (203) 269-0074.

FLORIDA: Altamonte Springs: 370 S. North Lake Boulevard, Suite 1008, Altamonte Springs, FL 32701, (407) 260-2116; **Fort Lauderdale:** 2950 N.W. 62nd Street, Suite 100, Fort Lauderdale, FL 33309, (305) 973-8502; **Tampa:** 4803 George Road, Suite 390, Tampa, FL 33634-6234, (813) 882-0017.

GEORGIA: Norcross: 5515 Spalding Drive, Norcross, GA 30092, (404) 662-7900.

ILLINOIS: Arlington Heights: 515 W. Algonquin, Arlington Heights, IL 60005, (708) 640-3000.

INDIANA: Carmel: 550 Congressional Drive, Suite 100, Carmel, IN 46032, (317) 573-6400; **Fort Wayne:** 118 E. Ludwig Road, Suite 102, Fort Wayne, IN 46825, (219) 482-3311.

IOWA: Cedar Rapids: 373 Collins Road N.E., Suite 201, Cedar Rapids, IA 52402, (319) 395-9550.

KANSAS: Overland Park: 7300 College Boulevard, Lighton Plaza, Suite 150, Overland Park, KS 66210, (913) 451-4511.

MARYLAND: Columbia: 8815 Centre Park Drive, Suite 100, Columbia, MD 21045, (301) 964-2003.

MASSACHUSETTS: Waltham: 950 Winter Street, Suite 2800, Waltham, MA 02154, (617) 895-9100.

MICHIGAN: Farmington Hills: 33737 W. 12 Mile Road, Farmington Hills, MI 48331, (313) 553-1500.

MINNESOTA: Eden Prairie: 11000 W. 78th Street, Suite 100, Eden Prairie, MN 55344, (612) 828-9300.

MISSOURI: St. Louis: 12412 Powerscourt Drive, Suite 125, St. Louis, MO 63131, (314) 821-8400.

NEW JERSEY: Iselin: Parkway Towers, 485E. Route 1 South, Iselin, NJ 08830, (908) 750-1050.

NEW MEXICO: Albuquerque: 2709 Pan American Freeway, N.E., Albuquerque, NM 87107, (505) 345-2555.

NEW YORK: East Syracuse: 6365 Collamer Drive, East Syracuse, NY 13057, (315) 463-9291; **Fishkill:** 300 Westage Business Center, Suite 140, Fishkill, NY 12524, (914) 897-2900; **Melville:** 1895 Walt Whitman Road, Melville, NY 11747, (516) 454-6600; **Pittsford:** 2851 Clover Street, Pittsford, NY 14534, (716) 385-6770.

NORTH CAROLINA: Charlotte: 8 Woodlawn Green, Suite 100, Charlotte, NC 28217, (704) 527-0930; **Raleigh:** 2809 Highwoods Boulevard, Suite 100, Raleigh, NC 27625, (919) 876-2725.

OHIO: Beachwood: 23775 Commerce Park Road, Beachwood, OH 44122, (216) 464-6100; **Beavercreek:** 4200 Colonel Glenn Highway, Suite 600, Beavercreek, OH 45431, (513) 427-6200.

OREGON: Beaverton: 6700 S.W. 105th Street, Suite 110, Beaverton, OR 97005, (503) 643-6758.

PENNSYLVANIA: Blue Bell: 670 Sentry Parkway, Blue Bell, PA 19422, (215) 825-9500.

PUERTO RICO: Hato Rey: 615 Mercantile Plaza Building, Suite 505, Hato Rey, PR 00918, (809) 753-8700.

TEXAS: Austin: 12501 Research Boulevard, Austin, TX 78759, (512) 250-6769; **Dallas:** 7839 Churchill Way, Dallas, TX 75251, (214) 917-1264; **Houston:** 9301 Southwest Freeway, Suite 360, Houston, TX 77074, (713) 778-6592.

UTAH: Salt Lake City: 1800 S. West Temple Street, Suite 201, Salt Lake City, UT 84115, (801) 466-8973.

WASHINGTON: Redmond: 5010 148th Avenue N.E., Building B, Suite 107, Redmond, WA 98052, (206) 881-3080.

WISCONSIN: Waukesha: 20825 Swenson Drive, Suite 900, Waukesha WI 53186, (414) 798-1001.

CANADA: Nepean: 301 Moodie Drive, Mallorn Center, Suite 102, Nepean, Ontario, Canada K2H 9C4, (613) 726-1970; **Richmond Hill:** 280 Centre Street East, Richmond Hill, Ontario, Canada L4C 1B1, (416) 884-9181; **St. Laurent:** 9460 Trans Canada Highway, St. Laurent, Quebec, Canada H4S 1R7, (514) 335-8392.

ARGENTINA: Texas Instruments Argentina Viamonte 1119, 1053 Capital Federal, Buenos Aires, Argentina, 1/748-3699.

AUSTRALIA (& NEW ZEALAND): Texas Instruments Australia Ltd., 6-10 Talavera Road, North Ryde (Sydney), New South Wales, Australia 2113, 2-878-9000; 14th Floor, 380 Street, Kilda Road, Melbourne, Victoria, Australia 3004, 3-696-1211; 171 Philip Highway, Elizabeth, South Australia 5112, 8 255-2066.

BELGIUM: S.A. Texas Instruments Belgium N.V., 11, Avenue Jules Bordetlaan 11, 1140 Brussels, Belgium, (02) 242 30 80.

BRAZIL: Texas Instruments Electronicos do Brasil Ltda., Rua Paes Leme, 524-7o andar, 05424 Sao Paulo, Brazil, 11-815-6166.

DENMARK: Texas Instruments A/S, Borupvang 2D, DK-2750 Ballerup, Denmark, (45) 44687400.

FINLAND: Texas Instruments OY, P.O. Box 86, 02321 Espoo, Finland, (0) 802 6517.

FRANCE: Texas Instruments France, 8-10 Avenue Morane Saulnier-B.P. 67, 78141 Velizy Villacoublay cedex, France, (1) 30 70 10 03.

GERMANY: Texas Instruments Deutschland GmbH., Haggertystrasse 1, 8050 Freising, (08161) 80-0 od. Nbst; Kurfürstendamm 195-196, 1000 Berlin 15, (030) 8 82 73 65; Düsseldorfer Strasse 40, 6236 Eschborn 1, (06196) 80 70; Kirchhorster Strasse 2, 3000 Hannover 51, (0511) 64 68-0; Maybachstrasse II, 7302 Ostfildern 2 (Nellingen), (0711) 3403257; Gildehofcenter, Hollestrasse 3, 4300 Essen 1, (0201) 24 25-0.

HOLLAND: Texas Instruments Holland B.V., Hogehilweg 19, Postbus 12995, 1100 AZ Amsterdam-Zuidoost, Holland, (020) 5602911.

HONG KONG: Texas Instruments Hong Kong Ltd., 8th Floor, World Shipping Center, 7 Canton Road, Kowloon, Hong Kong, 7351223.

HUNGARY: Texas Instruments International, Budaorsi u.42, H-1112 Budapest, Hungary, (1) 1 66 66 17.

IRELAND: Texas Instruments Ireland Ltd., 7/8 Harcourt Street, Dublin 2, Ireland, (01) 481677.

ITALY: Texas Instruments Italia S.p.A., Centro Direzionale Colleoni, Palazzo Perseo-Via Paracelso, 12, 20041, Agrate Brianza (Mi), Italy (039) 63221; Via Castello della Magliana, 38, 00148 Roma, Italy (06) 6572651; Via Amendola, 17, 40100 Bologna, Italy, (051) 554004.

JAPAN: Texas Instruments Japan Ltd., Aoyama Fuji Building 3-6-12 Kita-Aoyama Minato-ku, Tokyo, Japan 107, 03-3498-2111; MS Shibaura Building 9F, 4-13-23 Shibaura, Minato-ku, Tokyo, Japan 108, 03-3769-8700; Nissho-Iwai Building 5F, 2-5-8 Imabashi, Chuou-ku, Osaka, Japan 541, 06-204-1881; Dai-ni Toyota Building Nishi-kan 7F, 4-10-27 Meieki, Nakamura-ku, Nagoya, Japan 450, 052-583-8691; Kanazawa Oyama-cho Daiichi Seimei Building 6F, 3-10 Oyama-cho, Kanazawa, Ishikawa, Japan 920, 0762-23-5471; Matsumoto Showa Building 6F, 1-2-11 Fukashi, Matsumoto, Nagano, Japan 390, 0263-33-1060; Daiichi Olympic Tachikawa Building 6F, 1-25-12, Akebono-cho, Tachikawa, Tokyo, Japan 190, 0425-27-6760; Yokohama Business Park East Tower 10F, 134 Gondo-cho, Hodogaya-ku, Yokohama, Kanagawa 240, Japan, 045-338-1220; Nihon Seimei Kyoto Yasaka Building 5F, 843-2, Higashi Shiokohjicho, Higashi-iru, Nishinotoh-in, Shiokohji-dori, Shimogyo-ku, Kyoto, Japan 600, 075-341-7713; Sumitomo Seimei Kumagaya Building 8F, 2-44 Yayoi, Kumagaya, Saitama, Japan 360, 0485-22-2440; 2597-1, Aza Harudai, Oaza Yasaka, Kitsuki, Oita, Japan 873, 09786-3-3211.

KOREA: Texas Instruments Korea Ltd., 28th Floor, Trade Tower, 159-1, Samsung-Dong, Kangnam-ku Seoul, Korea, 2 551 2800.

MALAYSIA: Texas Instruments Malaysia, Sdn. Bhd., Asia Pacific, Lot 36.1 #Box 93, Menara Maybank, 100 Jalan Tun Perak, 50050 Kuala Lumpur, Malaysia, 2306001.

MEXICO: Texas Instruments de Mexico S.A. de C.V., Alfonso Reyes 115, Col. Hipodromo Condesa, Mexico, D.F., 06170, 5-515-6081.

NORWAY: Texas Instruments Norge A/S, PB 106, Refstad (Sinsenveien 53), 0513 Oslo 5, Norway, (02) 155090.

PEOPLE'S REPUBLIC OF CHINA: Texas Instruments China Inc., Beijing Representative Office, 7-05 CITIC Building, 19 Jianguomenwai Dajie, Beijing, China, 500-2255, Ext. 3750.

PHILIPPINES: Texas Instruments Asia Ltd., Philippines Branch, 14th Floor, Ba-Lepanto Building, Paseo de Roxas, Makati, Metro Manila, Philippines, 2 817 6031.

PORTUGAL: Texas Instruments Equipamento Electronico (Portugal) LDA., 2650 Moreira Da Maia, 4470 Maia, Portugal, (2) 948 1003.

SINGAPORE (& INDIA, INDONESIA, THAILAND): Texas Instruments Singapore (PTE) Ltd., Asia Pacific Division, 101 Thomson Road, #23-01, United Square, Singapore 1130, 350 8100.

SPAIN: Texas Instruments España S.A., c/Gobelas 43, Ctra de La Coruna km. 14, La Florida, 28023 Madrid, Spain, (1) 372 8051; c/Diputacion, 279-3-5, 08007 Barcelona, Spain, (3) 317 91 80.

SWEDEN: Texas Instruments International Trade Corporation (Sverigefilialen), Box 30, S-164 93 Kista, Sweden, (08) 752 58 00.

SWITZERLAND: Texas Instruments Switzerland AG, Riedstrafse 6, CH-8953 Dietikon, Switzerland, (01) 74 42 811.

TAIWAN: Texas Instruments Taiwan Limited, Taipei Branch, 10th Floor Bank Tower, No. 205, Tung Hua N. Road, Taipei, Taiwan, Republic of China, 2-7139311.

UNITED KINGDOM: Texas Instruments Ltd., Manton Lane, Bedford, England, MK41 7PA, (0234) 270 111.

TI Authorized North American Distributors

Alliance Electronics, Inc. (military product only)
Almac Electronics
Anthem Electronics
Arrow/Kierulff Electronics Group
Arrow (Canada)
Future Electronics (Canada)
GRS Electronics Co., Inc.
Hall-Mark Electronics
Lex Electronics
Marshall Industries
Newark Electronics
Wyle Laboratories
Zeus Components
Rochester Electronics, Inc. (obsolete product only)

TEXAS INSTRUMENTS

B0691

TEXAS
INSTRUMENTS

Other Linear Product Lines from TI

Operational Amplifiers
Data Acquisition
Voltage Regulators
Data Transmission
Display Drivers
Intelligent Power ICs
Optoelectronics
Telecom
Speech

Thank you for your interest in TI Linear Products. On the last two pages is a list of TI sales offices worldwide and North American authorized distributors. Our sales representatives will be happy to answer your questions about pricing, device availability and technical product information. For information on how to order technical literature, please contact our Literature Center at the following address:

Texas Instruments Incorporated
LITERATURE CENTER
P.O. Box 809066
Dallas, TX 75380-9066
214-995-6611

TEXAS
INSTRUMENTS

Printed in U.S.A.
0192–140